Choose the right f.e.t.

Blind use of any old f.e.t. can result in disastrous circuit performance and possibly catastrophic failure of a device. These notes should help you select an appropriate device for the six applications illustrated.

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Constant current source

In one of the lesser-used applications, the f.e.t. approaches the ideal current source. Operation in the pinch-off (see Fig. 1) region results in virtually-constant I_D for large variations in V_{DS} and constant V_{GS}. This is due to the low output conductance (g_{OSS}) of the f.e.t. defined by $\Delta I_D/\Delta V_{DS}$. It is related to the more commonly used term "dynamic impedance" (Z_D) of a current source by $Z_D = 1/g_{OSS}$. For good regulation g_{OSS} should be as low as possible.

Fig. 2 shows a basic current source. Resistor R_S is used to set the value of V_{GS} and thus the value of constant I_D. For a given I_D, the required value of V_{GS} is

$$V_{GS} \approx V_p\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

which enables R_S to be calculated from $R_S = V_{GS}/I_D$.

If R_S is made variable, a wide range of V_p and I_{DSS} values can be accommodated provided $I_{DSS} \not< I_D$. However, if a nominal I_D is required and trimming of R_S is not practical, choose an f.e.t. with small "data sheet" spreads of V_p and I_{DSS}.

The resultant dynamic impedance of Fig. 2 is

$$Z_D = \frac{1+R_S G_{fs}}{g_{OSS}}$$

and therefore high g_{OSS} devices are desirable.

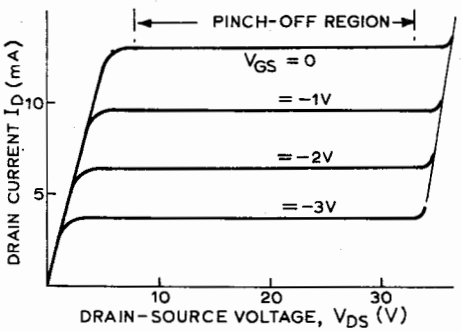

Figure 1

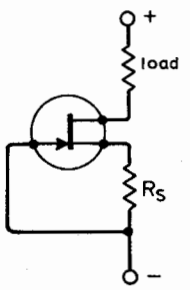

Figure 2

Another requirement for good regulation is that the drain-to-source voltage V_{DS} is maintained above the pinch-off voltage, otherwise g_{OSS} will be greatly increased (and dynamic impedance reduced). Ideally V_{DS} should be at least twice the value of V_p. Therefore, for correct operation the total voltage across the f.e.t. and R_S should be a minimum of $2V_p + V_{GS}$.

In certain circumstances the permitted voltage drop across the current source may be limited. If so, choose an f.e.t. with a low V_p.

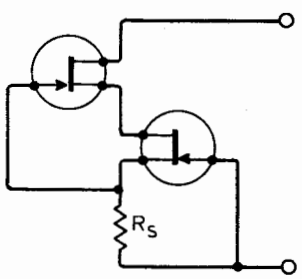

Figure 3

Fig. 3 shows an improved current source using two cascaded f.e.ts. The resulting dynamic impedance is

$$Z_D = \frac{g_{fs}(1+R_S g_{fs})}{g_{OSS1} g_{OSS2}}$$

Analogue switch

Figure shows an n-channel junction f.e.t. in a basic analogue switch configuration. The on-resistance r_{DS} should be as low as possible if a significant error in the sampled voltage is to be avoided. The error due to r_{DS} (at low frequency) is

$$e_{in.}\frac{R_S+r_{DS}}{R_S+R_L+r_{DS}},$$

where R_S is the signal source impedance and R_L the load impedance.

In the off condition, the f.e.t. exhibits a certain amount of drain-to-source leakage current ($I_{D\,off}$) which gives rise to an error voltage developed across R_L. The error due to $I_{D\,off}$ at low frequency is $I_{D\,off} \cdot R_L$. For this reason, $I_{D\,off}$ must be correctly specified.

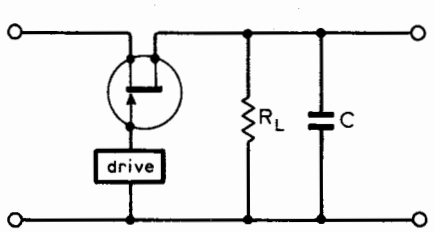

Figure 4

To turn the f.e.t. off, the gate must be driven negative with respect to the source by at least the value of V_p. Thus the required drive voltage is

$$V_{G(min)} = V_p + V_{analogue(pk)}$$

If the available drive voltage is limited, use low V_p devices.

Voltage-controlled resistor

Where operated with very low values of V_{DS}, f.e.ts exhibit predictable changes in R_{DS} for given changes in V_{GS}. Under such conditions, f.e.ts can be considered as a resistor whose value is determined by the value of the applied V_{GS}. Hence the term voltage-controlled resistor.

This characteristic makes the f.e.t. an ideal candidate for potential divider, attenuator and a.g.c. applications. Circuit shows an n-channel junction device used in a basic potential divider. Here, the R_{DS} should be significantly lower than R_L. The R_{DS} can be defined as $R_{DS0}/(1-V_{GS}/V_p)$, where $R_{DS0} = R_{DS}$ at $V_{GS} = 0$.

As can be seen in the graph, the output characteristics are extremely linear in the region $|V_{DS}| \ll |V_p|$. This bilateral characteristic can be used to advantage for the a.g.c. of low-level a.c. signals. If, however, V_{DS} exceeds $0.1\,V_p$, the output characteristics becomes markedly non-linear.

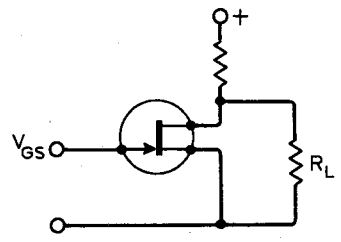

Figure 5

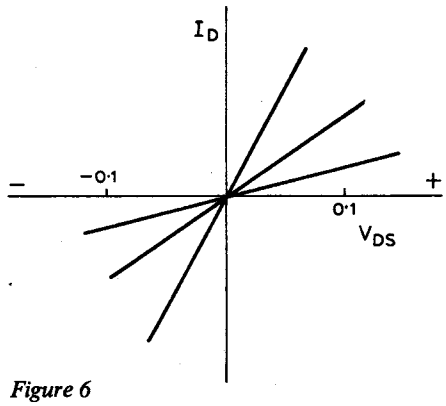

Figure 6

Low frequency amplifier

Under normal amplifier operation, the gate/source junction is a reverse-biased diode which presents a high impedance to the input signal. It is this high input impedance which makes the f.e.t. superior to its bipolar counterpart if loading of the input signal is to be avoided. The input impedance can be characterized by the gate current I_G which should be specified at the V_{DG} and I_D required for normal operation.

Circuit shows the basic common-source amplifier. The gain is

$$\frac{g_{fs}.R_L}{1+g_{fs}.R_S}$$

and if R_S is decoupled at the frequencies in question by a suitable capacitor, it becomes $\approx g_{fs}R_L$.

Graph shows a typical transfer characteristic. As g_{fs} is the slope of the characteristic at any given point, g_{fs} is a maximum when $V_{GS} = 0$. The g_{fs} at any other point on the curve can be found from $g_{fs} = g_{fs0}(1-V_{gs}/V_p)$ or $g_{fs0}/\sqrt{I_{DSS}/I_D}$, where $g_{fs0} = g_{fs}$ at $V_{gs} = 0$ and $I_{DSS} = I_D$ at $V_{gs} = 0$.

Drain current decreases with increasing temperature by approximately 0.7% degC. This phenomenon can result in undesirable variations in stage gain. Fortunately, this drift can be minimized by another effect which causes the effective V_{GS} to decrease by approximately 2.2mV/degC. This latter phenomenon causes I_D to increase with increasing temperature. Minimal d.c. drift will occur at the point where the two effects cancel each other. This point can be defined as $I_{DZ} = I_{DSS}(0.63/V_p)^2$, where $I_{DZ} = I_D$ for zero d.c. drift. High-V_p devices must be biased to low values of I_D, with a resultant drop in g_{fs}.

For low-noise applications, care should be taken in specifying the noise performance of the device. The major contribution of noise is from $1/f$ noise. This is normally characterized by manufacturers as "en" (short-circuit equivalent noise voltage in $nV/\sqrt{Hz}$) at various spot frequencies. However, for high signal-source impedances, the effect of noise current (i_n) becomes significant; since, at low frequencies, i_n is a function of gate leakage current, low I_G is desirable. Both i_n and I_G should be specified at the operating values of $V_{DS}+I_D$.

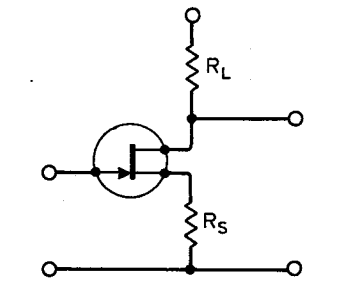

Figure 7

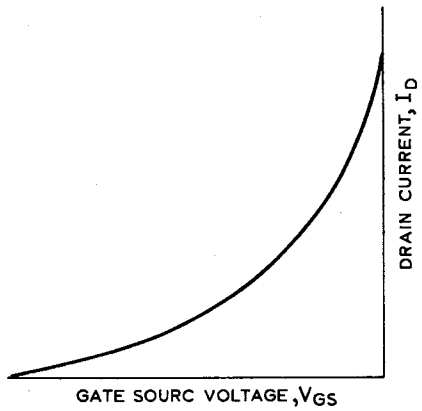

Figure 8

Electrometer circuit

The high input impedance of the f.e.t. makes it the ideal choice for electrometer applications. The basic electrometer circuit shown uses two and an inexpensive operational amplifier. Transistor Tr_1 is a source follower with Tr_2 acting as a dynamic source impedance. Resistor R_f sets the measuring range and R_1 through R_3 provide intermediate scaling. Choose Tr_1 to have low I_{GSS}, and the I_{DSS} of Tr_1 and Tr_2 to be matched as closely as possible; although R_4 will null some mismatch in addition to nulling the offset of the op-amp. Typically, Tr_1 and Tr_2 would be a dual f.e.t.

The value of the feedback resistor (R_f) is the reciprocal of the measuring range, with a scaling factor of unity.

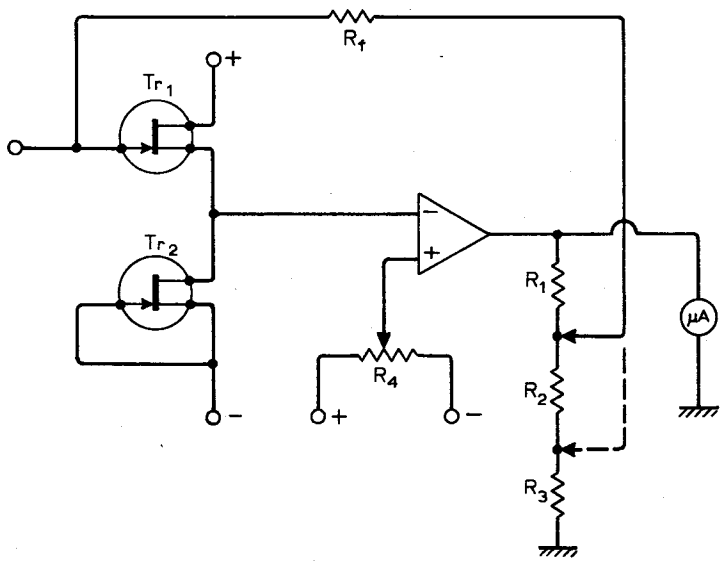

Figure 9

Differential amplifier

The circuit below uses three junction devices in a differential amplifier configuration. The I_{DSS}, g_{fs} and V_{GS} of Tr_1 and Tr_2 should be matched as closely as possible; the V_{GS} match should be specified at the operating value of I_D. If good matching is ensured, the gain is

$$\frac{g_{fs}R_L}{1+g_{os}R_L}.$$

Using low g_{os} devices, this approximates to $g_{fs}R_L$.

In practice, Tr_1 and Tr_2 may be either a matched pair of discrete devices or a dual f.e.t. Dual f.e.ts tend to be cheaper than their matched-pair equivalent and, with the increasing use of monolithic duals, are inherently more reliable. Also, with the two semiconductor elements in close proximity in the same package, either two-chip or monolithic, thermal behaviour is more predictable.

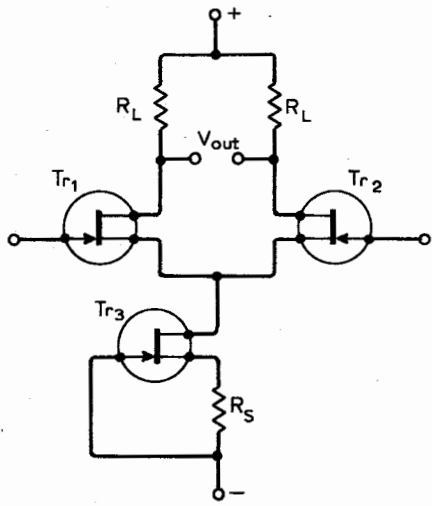

Figure 10

The common-mode gain of the differential stage is approximately

$$\frac{g_{fs}R_L}{1+2Z_Sg_{fs}}$$

assuming perfect matching of the f.e.ts and load resistors, and where Z_s is the source impedance.

Therefore inclusion of Tr_3 as a current source presenting a high dynamic source impedance greatly reduces the common-mode gain. The minimum I_{DSS} of Tr_3 must be the sum of Tr_1 and Tr_2 bias currents.

Further reading

Siliconix application notes Field Effect Transistor Current Source, by J. S. Sherwin
FETs As Analogue Switches, by Shelby Givens
Biasing FETs For Zero D.C. Drift, by Lee L. Evans