Choosing and Using N-Channel Dual J-Fets

Monolithic dual FET's have made parameter matching obsolete—eliminating laborious sorting and grading. Their improved performance (e.g. 5μV/°C offset drift) and reduced cost make them a natural choice for many applications. But there are important differences in construction among dual J-FETs, which determine temperature coefficients, performance, reliability, and consequently, choice for a given application.

INTRODUCTION

The field-effect transistor is now a widely-accepted circuit component because of its high input impedance, low noise, and great versatility. It is used in amplifying, switching, modulating, and generating signals. FET's are used in pairs as differential input stages for dc amplifiers, because of their great advantages of picoampere-level input leakage currents and teraohm input impedances. However, these advantages have been to some extent counterbalanced by the difficulty of obtaining and using matched units to obtain high common-mode rejection and low offset voltage and drift.

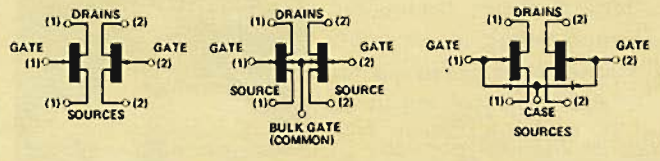
Recently, three types of high-performance matched pairs of junction FET's in single cans have become available. They are:

1. *Hybrids:* two chips that have been graded, selected, and mounted on a single header. (Example: Siliconix U235)
2. *Common-gate interdigitated:* single monolithic chips consisting of two FET's in intimate proximity with a common back side (bulk) gate. (Example: National FM1111)
3. *Monolithic isolated:* single monolithic chips containing two FET's electrically separated by diffused isolation diodes. (Example: Analog Devices AD3954)

In this article, we shall compare the differences in construction techniques, key specifications, and application philosophy among the three types, and show details of several applications employing monolithic isolated dual FET's. In addition, we shall tabulate the salient specs of two contrasting families of monolithic diffusion-isolated dual FET's: the AD3954A–8 general purpose duals and AD5902–9 ultra-low leakage small-geometry duals.

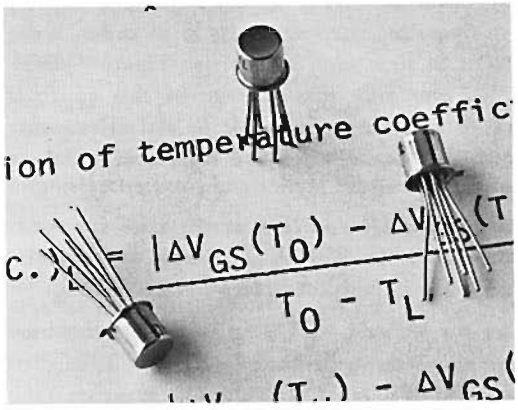
WHY A DUAL FET?

Dual FET's are used primarily in applications calling for two identical FET's. However, if they can be produced cheaply enough, (and they can—the monolithic AD3958, in the hermetic package, is cheaper than a pair of discrete FET's in plastic packages) they may also be considered in applications for a pair of independent (but similar) FET's, where space and cost can be saved by using two devices in the same can—if interaction of the elements of the dual device does not raise new problems.



(a) Hybrid Types *(b) Monolithic Common-Gate Types* *(c) Monolithic Junction-Isolated Types*

Figure 1. Dual-FET Schematic Diagrams



The bulk of applications for identical FET's are in the input stages of high-impedance operational amplifiers and comparators, where stability with temperature and common mode rejection depend greatly on parameter match. Applications for more-than-one FET include squarers, adjustable-frequency filters, switches, series-shunt voltage-variable attenuators, current sources, etc. Specific examples of some of these applications will be discussed at length in this article.

HOW ARE DUAL FETS MADE? WHAT ARE THE ADVANTAGES AND DISADVANTAGES?

Hybrids are made by collecting relevant data on a large number of individual FET chips, then, with the aid of a computer, selecting pairs that match to a specified degree. These are then mounted on a header that has two insulated mounting pads. To maintain the expense and yields within reason, the matching is usually performed at only one operating point (the nominal zero-drift drain current, I_{DZ}. As will be shown below, this may ensure excellent (though often nonlinear) temperature characteristics under one set of operating conditions; but detailed differences in linearity between one device and another may make the matching fruitless if the device is to be operated at a different value of drain current.

In addition, the dual-chip assembly is sensitive to thermal gradients, and will thus have greater than desired drift, due to the following: overloads; ambient temperature transients; static thermal gradients developed by adjacent circuitry.

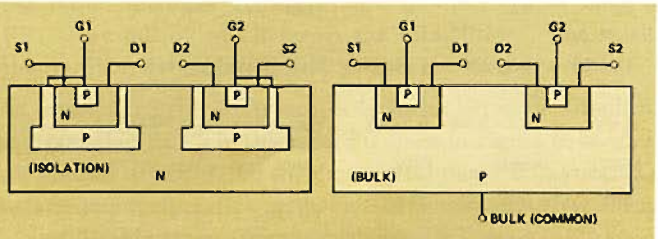
Furthermore, the handling that is inherent in measuring, storing, finding, and assembling pairs of chips has three disadvantages: it is more costly than handling single chips, it inevitably results in some loss of yield between measurement and assembly (causing a further increase in cost); and it tends to reduce ultimate reliability. The dual-chip FET does have the advantage of virtually complete *electrical* independence of the two FET's.

Monolithic duals are built in two ways, as shown in Figure 2. In both cases, the drain-source channel runs between an upper

gate terminal and a lower "bulk" gate. In some *interdigitated* duals, the bulk gate is common to both FET's and brought out to a separate terminal; in the *isolated* duals, two series-opposing diodes separate the bulk gates of the two FET's, and the bulk gates are internally connected to the top gates. Both types overcome the disadvantages of hybrid duals. Identification of chips containing matched pairs occurs at the wafer stage, and no extra handling of chips is required. Not only do the units that match have excellent temperature tracking at the specified value of drain current, but because they are even more alike than "two peas in a pod," they track well at other current levels as well. (See Figures 4 and 5) In addition, the gate-source difference voltage vs. temperature is quite linear, which allows further improvement of temperature coefficient by external manipulations in some circuit applications, as will be discussed in the Applications section.

Isolated vs. Common-gate duals. Isolated dual FET's, such as Analog's AD3954, are grown side-by-side with bulk N material separating the two P back gates. This produces isolation by two diodes in series opposing, with better than ±40V gate-to-gate breakdown voltage. Thus, the two FET's can be operated independently, the same as the two-chip duals, at any levels within the 40V BV_{GSS} rating, with negligible interaction.

In the case of the interdigitated duals (e.g., FM3954), with a common back gate, when pinchoff voltage (1.0 to 4.5V) is exceeded, the depletion layer reaches the bulk, and a "reach-through" or "punch-through" phenomenon occurs, characterized by a sharp reduction in input impedance (analogous to zener breakdown). For some applications, the common bulk is not a serious weakness; there are even a few applications in which it is a positive advantage. For most applications, however, the prospect of interaction is at best a nuisance that the engineer must consider—and perhaps expend extra components to avoid or mitigate; at worst, it is a potential source of component failure, if the "punch-through" current rating (typically 100μA) is exceeded. Nevertheless, because of the "interdigitated" construction, in which both FET's share the chip area more intimately, these types are likely more closely to approach identity between the twins, particularly in room temperature match of V_{GS}.



(a) Isolated dual FET AD3954 (b) Common-Gate dual FET

Figure 2. Monolithic Dual FET Construction

MONOLITHIC VS. HYBRID DUALS:
Offset Voltage and Drift Considerations

Matched pairs are used primarily to minimize drift in op amps and comparators. Let us therefore consider the relative ability of monolithic and hybrid duals to cancel drift. Typical op amp circuits in which they are used will be found on pages 7 and 8.

With a given value of drain-source voltage applied to a single FET, the gate-to-source voltage is a function of drain current and temperature. If I_D is varied, the temperature coefficient of V_{GS} variation will also be found to vary in nonlinear fashion. In the example shown in Figure 3, it is 2.7mV/°C at I_D = 1mA, and very nearly zero at I_D = 200μA. FET's having this geometry

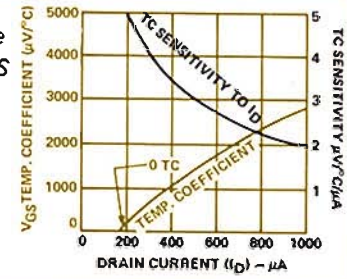


Figure 3. V_{GS} Temperature Coefficient (color) and V_{GS} TC Sensitivity (black) vs. Drain Current for single device (½ AD3954). (V_{DS} = 20V, I_{DSS} = 2mA)

are usually operated at currents near 200μA to take advantage of the small TC in that region. If the TC is low for single units, then matched pairs should have excellent performance. However, it is important to consider the rate of variation of TC with drain current, also plotted in Figure 3. For the example shown, it is about 4.5μV/°C per μA of I_D at I_D = 200μA. This means that for a 1% variation in I_D (viz., 2μA) the TC will change by about 9μV/°C.

If the FET's in a matched pair are not exactly alike, small local differences in shape of the V_{GS} TC curves will cause the offset vs. temperature to be nonlinear. In Figure 4, differential V_{GS} offsets are plotted vs. temperature for a monolithic dual FET and for a hybrid two-chip pair. It can be seen that the close identity of the FET's on the monolithic chip produces quite linear offset, which—because of its linearity—can be trimmed to "a gnat's eyebrow" by adjusting one of the drain currents. In the case of the two-chip device, while it meets the 10μV/°C specification on a gross basis, the nonlinearity precludes the possibility of further minimization of TC, except over a narrow range of temperatures.

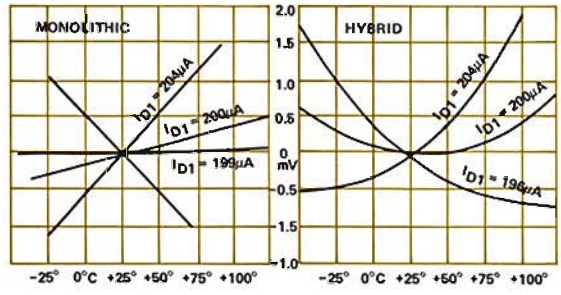


Figure 4. V_{GS1-2} differential offset voltage as a function of temperature for typical monolithic and two-chip hybrid dual FET's, under identical conditions. (Both are "10μV/°C" units.) V_{DG} = 20V, I_{D2} is initially set to 200μA, and the vertical scale represents departure from 25°C initial offset (millivolts)

The differences are further accentuated when the FET's are operated at values of drain current that differ greatly from the nominal match point. In Figure 5, the drain current is 500μA. For the monolithic pair, a 1% change in one of the currents is sufficient to restore a quite low TC. In the case of the hybrid, it is evident that matching is quite lost.

COMPARABLE SMALL GEOMETRY DUAL FETS, Condensed Specifications

Parameter	Symbol	Isolated Dual Monolithics (Analog Devices) AD5909	Hybrids 2N5909	Conditions T_A = +25°C, unless otherwise noted
Drift vs. Temperature	$\left\|\frac{\Delta V_{GS_{1-2}}}{\Delta T}\right\|$ max	40μV/°C	40μV/°C	V_{DG} = 10V, I_D = 30μA, −55°C<T_A<+25°C<T_A<+125°C
Offset Voltage	$V_{GS_{1-2}}$	50mV	15mV	V_{DG} = 10V, I_D = 30μA
Gate Current	$-I_G$ max	1pA	1pA	V_{DG} = 10V, I_D = 30μA
Gate Current	$-I_G$ max @ +125°C	1nA	1nA	V_{DG} = 10V, I_D = 30μA, T_A = +125°C
Transconductance	g_{fs} min–max	50–150μ mhos	50–150μ mhos	V_{DG} = 10V, I_D = 30μA, 1kHz
Transconductance Mismatch	$\left\|\frac{g_{fs_{1-2}}}{g_{fs}}\right\|$ max	5%	5%	V_{DG} = 10V, I_D = 30μA, T_A = +125°C
Saturation Current	I_{DSS} min–max	0.03–0.5mA	0.03–0.5mA	V_{DS} = 10V, V_{GS} = 0
Saturation Mismatch	$\left\|\frac{I_{DSS_{1-2}}}{I_{DSS}}\right\|$	5%	5%	V_{DS} = 10V, V_{GS} = 0
Pinchoff Voltage	$-V_p$ or $-V_{GS}$(off) min–max	0.6–4.5V	0.6–4.5V	V_{DS} = 10V, I_D = 1nA
Source–Gate Voltage	$-V_{GS}$ max	4V	4V	V_{DG} = 10V, I_D = 30μA
Gate Voltage	V_{GSS} Dt max	40V	40V	
Drain Voltage	V_{DSO} Dt max	40V	40V	
Gate-Gate Breakdown	V_{GGO} min	40V	80V	
Price (100+) *		$5.95	$5.95	

COMPARABLE MEDIUM-GEOMETRY DUAL FETS, Condensed Comparative Specifications

		Analog Devices Isolated Dual Monolithic		National Semiconductor Interdigitated Dual Monolithic		Siliconix Hybrids		
PARAMETER	SYMBOL	AD3954A	AD3958	FM3954A	FM3958	2N5196	U235	CONDITIONS
								T_A = +25°C, unless noted
Drift vs. Temperature	$\left\|\frac{\Delta V_{GS_{1-2}}}{\Delta T}\right\|$ max	5μV/°C	100μV/°C	5μV/°C	100μV/°C	5μV/°C	100μV/°C	V_{DG} = 20V, I_D = 200μA, −55°C<T_A<+25°C, +25°C<T_A<+25°C
Offset Voltage	$\|V_{GS_{1-2}}\|$	25mV	50mV	5mV	25mV	5mV	25mV	V_{DG} = 20V, I_D = 200μA
Gate Current	$-I_G$ max	50pA	50pA	50pA	50pA	15pA	50pA	V_{DG} = 20V, I_D = 200μA
Gate Current	$-I_G$, max @ +125°C	250nA	250nA	250nA	250nA	15nA	250nA	V_{DG} = 20V, I_D = 200μA, T_A = +125°C
Transconductance	g_{fs}, min–max	1000–3000μ℧	1000–3000μ℧	1000–4000μ℧	1000–3000μ℧	1000–4000μ℧	1000–3000μ℧	V_{DS} = 20V, V_{GS} = 0, 1kH
Transconductance Mismatch	$\left\|\frac{g_{fs_{1-2}}}{g_{fs}}\right\|$	1%	1%	3%	15%	3%	15%	V_{DG} = 20V, I_D = 200μA
Saturation Current	I_{DSS}, min–max	0.5–5mA	0.5–5mA	0.5–5mA	0.5–5mA	0.7–7mA	0.5–5mA	V_{DG} = 20V, V_{GS} = 0
Saturation Mismatch	$\left\|\frac{I_{DSS_{1-2}}}{I_{DSS}}\right\|$	5%	5%	5%	5%	5%	5%	V_{DG} = 20V, V_{GS} = 0
Pinchoff Voltage	$-V_p$ or $-V_{GS}$ (off) min–max	1–4.5V	1–4.5V	1–4.5V	1–4.5V	0.7–4V	1–4.5V	V_{DS} = 20V, I_D = 1nA
Source-Gate Voltage	$-V_{GS}$ min–max	0.5–4V	0.5–4V	0.5V	4.0V	0.2–3.8V	0.5–4V	V_{DG} = 20V, I_D = 200μA
Gate Voltage	V_{GSS} Dt, max	40V	40V	50V	50V	50V	50V	Either V_{GS} or V_{GD}
Drain Voltage	V_{DSO} Dt, max	40V	40V	50V	50V	50V	50V	
Gate-Gate Breakdown	V_{GGO}, min	40V	40V	<2V_{GS}(off)	See text	>50V	>50V	I_G = 1nA, I_D = 0, I_S = 0
Price (100+)*		$9.70	$2.15	$10.30	$1.80	$17.50	$3.00	

*As of 6 October 1970 †D indicates an absolute maximum limit above which degradation or destruction may occur

NOTES ON TWO FAMILIES: AD3954A, etc., vs. AD5906, etc.

The AD3954A, and its ilk are characterized by moderate drain current, y_{fs}, and gate leakage (typically 200μA, 2,000μ℧, and 20pA, respectively). The corresponding parameters for the AD5906 family are an order of magnitude lower (typically 20μA, 100μ℧, and 0.8pA, respectively). Both families have comparable offset and drift specifications. The AD3954 family is designed for general-purpose FET applications where reasonably good voltage gain and reasonably low offset and bias current are desired. The AD5909, because of its extremely low leakage current, is designed for electrometer and high impedance circuit applications. It should be operated with current-source drain loads (to squeeze the utmost in gain from its low transconductance) and V_{DG} should be maintained at a low constant value, irrespective of common mode level, through "bootstrapping", to minimize bias current variation with common mode swing. Its can should be connected to a common mode "guard" potential, to minimize bias current contributed by leakage to the outside world. Because of its lower g_m, the 5909 family is less suitable for fast applications.

This dependence of TC match on I_D is particularly important when dual FET's are used in the input stages of op amps with simple resistive ancillary circuitry. Drain current can vary widely with common mode voltage (unless constant current sources and/or "bootstrapping" are used), which in turn can produce substantial changes of TC in circuits using paired chips, considerably less with monolithic FET's.

These measured results depict the differences between two *specific* devices, but they are representative of their species. Hybrids often have better +25°C offset specifications than monolithics. However, since these offsets can be adjusted out without significant penalty, the better linearity of monolithics keeps them as the preferred choice. (Figures 7 and 8)

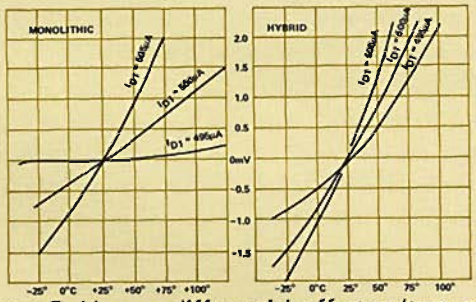


Figure 5. V_{GS1-2} differential offset voltage as a function of temperature for the same two FET's as in Figure 4, but with I_{D2} = 500µA. Same vertical scale as Figure 4.

Temperature Gradient

Another factor of importance when considering drift is the effect of unequal temperature changes in the two members of a matched pair. For the FET characterized in Figure 3, the TC at 200µA I_D is about 150µV/°C. Thus, under electrically balanced conditions, a 1°C thermal unbalance would cause a relative drift of 150µV. Such unbalances might be caused transiently if one of the FET's were momentarily cut off or saturated (as can happen quite easily in comparator applications). They might also be caused by a sudden change in the ambient temperature, with unequal heat flow to the two input transistors. They can even occur in the steady state if the FET's are in close proximity to a source of constant (or variable) heat flow (e.g., a load resistor). Then, the closer, the more identical, and the more intimately heat sunk the FET's are (all of which favors the monolithics), the smaller the transient variations and the shorter the recovery time.

An example of the difference in behavior between monolithic and two-chip FET's in this regard is given in Figure 6, in which are plotted offset vs. tab angle of typical dual FET's rotated in a stationary temperature gradient. The maximum offset change is considerably greater for the two-chip FET.

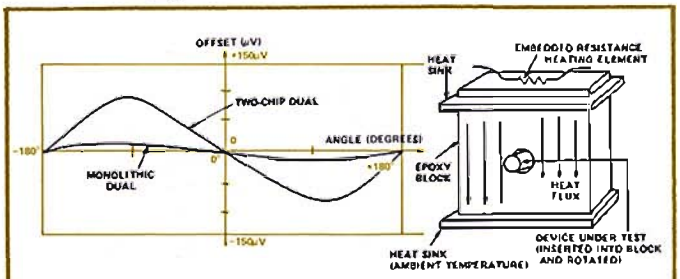


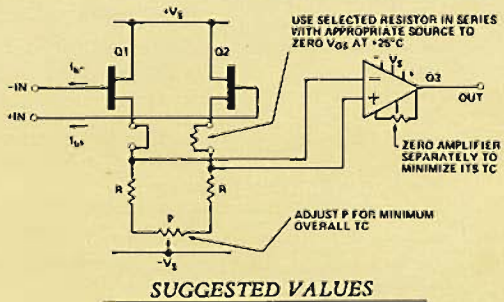
Figure 6. Offset Voltage vs. Angle of Can Tab to 1°C/mm Thermal Field

APPLICATION OF DUAL FETS

Operational Amplifiers (and Comparators)

This discussion will sidestep the controversy over whether to "make or buy" FET-input op amps. Such decisions depend on circuit complexity, budget, equipment/system requirements for performance, reliability, ease of manufacture, special features, and—the propensities of the project engineer and his management.* Suffice it to say that whether the decision is "make" or "buy", Analog Devices is always pleased to supply the active elements, be they complete FET-input op amps, or FET pairs with AD741 main amplifiers. The basic circuit applications discussed here utilize dual FET's, in conjunction with Analog's low-cost op amps, plus passive components.

FET input stage designs offer two basic options: FET's as source followers (essentially unity gain) or FET's as amplifiers. The circuits shown are by no means the most sophisticated designs available, but they are simple circuits that will perform reliably, provided that reasonable skill and care has been employed in laying out and wiring the circuits. All the rules that pertain to low-level high impedance circuitry apply here. For example, if a leakage path of as much as 10^{12} ohms exists between the +15V supply and the FET gates, input current will be increased by 15pA beyond the FET's own leakage current. This is marginal for 50pA applications and unacceptable for 1pA applications. To avoid excessive leakage, the high-impedance input leads should be guarded by (and the metal case connected to) a potential that is close to that of the input (common, in the case of inverters; the output, in the case of unity-gain followers; the feedback return—at low impedance—in the case of followers with gain).



SUGGESTED VALUES

I_B	Q1, Q2†	R*	P†	Q3†
50pA	AD3954A to AD3958	75kΩ	10kΩ AD79PR10k	AD741K
1pA	AD5906 to AD5909	500kΩ	50kΩ AD79PR50k	AD502K

*Resistors are 1% tolerance, low TC (15–100ppm/°C depending on allowable offset drift)
†Available from Analog Devices, Inc.

Figure 7. FET's Connected as Followers

Follower Circuit

Figure 7 shows a FET-input op amp using the dual FET's as followers. Use the table to determine circuit parameters and FET family, depending on the desired input "bias" current level. Choose the specific FET type as a function of desired voltage drift and offset level. Complete tabulations of specifications of available dual FET's, in both the AD3954A and AD5909 series are to be found in the family data sheets, available upon request. See page 6 for condensed specifications.

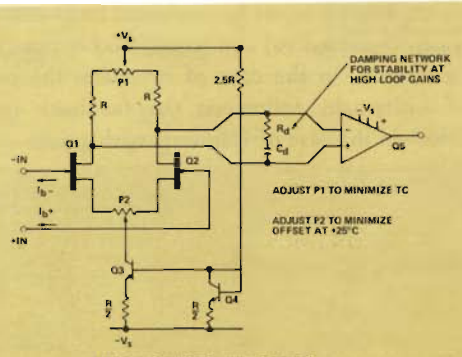
*However, the newly-announced AD503 (see page 1) is itself a compelling argument for "buy"

The resistors, R, can be 1% values, but they should have low temperature coefficients (preferably of the same polarity), from 15ppm/°C to 100ppm/°C, depending on the drift level desired and the FET pair used. Changes in resistor values affect the FET channel currents, and differential changes affect the offset drift temperature coefficient. Feedback maintains the voltages across the two resistors (and pot arms) very nearly equal, within the input error of the main amplifier.

The amplifiers specified for use with the FET's are low-drift types, because their drift adds directly to that of the FET's. The amplifier's own input offset (at the inputs of Q3) is first adjusted to zero, because minimum amplifier TC occurs near zero offset. Then potentiometer P is adjusted to minimize the variation of offset with ambient temperature. Finally a value of resistance empirically selected to minimize offset at +25°C is inserted in series with the appropriate FET source terminal.

Amplifier Circuit

The follower circuit has limitations: it does not reduce the influence of main amplifier offset; it does not reject variations in the negative supply voltage; the overall gain is only that of the main amplifier. On the other hand, it is capable of wide common mode swing, especially for positive values of CMV. The amplifier circuit in Figure 8 overcomes some of the limitations, at the cost of extra components and of reduced positive common mode swing (due to limitations imposed by the rated common mode range of the main amplifier).



SUGGESTED VALUES

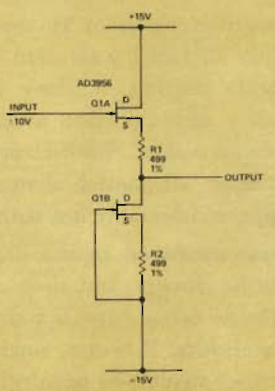
I_b	Q1, Q2†	R*	P1†	P2†	Q3, Q4†	Q5†	R_D	C_D
50pA	AD3954A to AD3958	25kΩ	2kΩ AD79PR2k	500Ω AD79PR1k	2N4880 Dual Transistor	AD741C	2.2kΩ	0.47μF
1pA	AD5906 to AD5909	150kΩ	10kΩ AD79PR10k	2kΩ AD79PR5k	2N4880 Dual Transistor	AD502J	15kΩ	0.05μF

*Resistors are 1% tolerance, low TC (15–100ppm/°C depending on allowable offset drift)
†Available from Analog Devices, Inc.

Figure 8. FET's Connected as Amplifiers

Here, the outputs from the FET preamplifier stage are taken from the drains. Q3 and Q4 and their associated resistors form a current source to maintain the total current drawn by Q1 and Q2 at a constant value little affected by common mode swing. Thus, this circuit will have better common mode rejection than the circuit of Figure 7, from −10V to +5V. It will also have better power supply rejection, and at least 20dB more gain at low frequencies. The additional gain supplied by the FET input stage reduces the effect of main amplifier offset and drift, allowing use of less costly amplifiers. To maintain stability at high values of loop gain, an RC damper between the inputs of Q5 (or feedback capacitance) is recommended. For best results, the resistors referred to R should be metal film types having low TC's, but the especially critical match of TC's (for lowest drift) is between the R's.

LOW DRIFT FOLLOWER

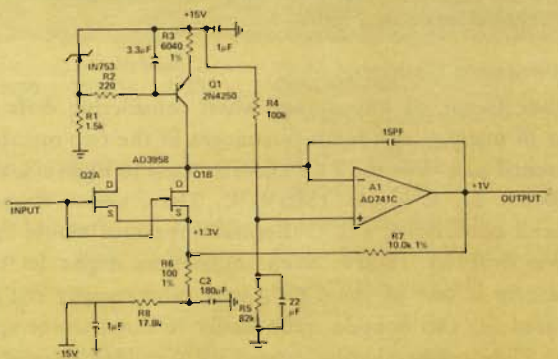


For applications where the FET is needed primarily to unload a very high impedance signal, this circuit may be used to buffer the input of a low cost op amp, such as the AD741C. It is an extremely simple outside-the-loop alternative to Figures 7 and 8.

As shown, it will be foolproof when driving loads of 100kΩ or higher, without any selection. FET's selected to have I_{DSS} of 1.5mA minimum can drive load resistances as low as 20kΩ, while maintaining linearity of 0.01% for a ±10V output range. At no load, the gain is typically 0.998. The output impedance is equal to $R_1 + 1/y_{fs}$.

To get the most out of the design, it is useful to choose the source resistors (R1 and R2) as a function of the load. The gate of Q1A should never be driven more positive than the source at the maximum positive input. R2 can be trimmed to zero the output. At no load (e.g., when driving a high-impedance op amp input—say, AD741C), short circuits may be substituted for R1 and R2.

LOW NOISE AC PREAMPLIFIER



This amplifier will provide a voltage gain of 100 over a bandwidth (−3dB) of 9Hz to 250kHz. It is well suited to such diverse sources as magnetic phonograph pickups (low impedance) and piezoelectric transducers (high impedance).

The AD3958 FET's provide an overall noise voltage of typically 1.1μV in a 50kHz bandwidth, referred to the input. (Noise current is also low, of the order of 1pA in the same bandwidth.) Paralleling the FET's increases the signal to noise ratio by 3dB, because transconductance increases directly with the number of units, while noise increases with the square root. In this circuit, each FET operates at a drain current of 0.5mA. However, if the units are selected for $I_{DSS} \geq 1$mA, voltage noise can be further reduced by about 2dB (25%) by reducing R3 to 3,010Ω and R8 to 9,090Ω, to increase drain current.

To make best use of the input stage's low noise, it must also have high gain, in order to minimize the noise contribution from the AD741C op amp. This is accomplished by using a current source (Q1) as the load in the drain circuit. The input signal should have a dc return path to ground for Q2's gate currents. This path can have an extremely high resistance (limited only by the need to avoid reverse-biasing the electrolytic capacitor C2) because of the AD3958's picoampere-level bias current.

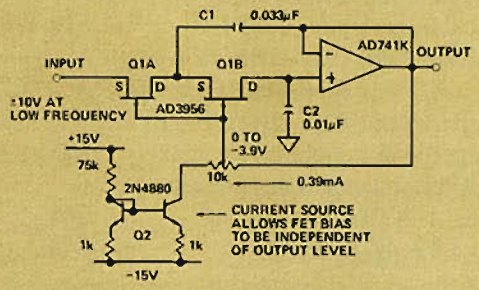
ADJUSTABLE LOW PASS FILTER

This circuit is useful primarily to filter out small ac noise components riding on a relatively slowly-varying signal. Gate voltage variation of matched channel resistances of the AD3956 allows adjustment of cutoff frequency over a 10:1 range (1:10kHz for the capacitance values shown) with 12dB/octave attenuation and 0.6dB peaking.

Signal or noise components in the vicinity of cutoff will suffer 3% harmonic distortion (at worst) just above ±150mV for 10kHz settings and ±15mV for 1kHz settings. Distortion will be proportionately less at lower frequencies, allowing larger signals to be passed. The reason for this is that the voltage drop across the FET resistors increases with frequency, but the drain voltage-drain current characteristic is linear only well below pinchoff. If FET's are selected for pinchoff at the higher end of the specified 1.0 to 4.5V range, linearity can be improved. If large ac signal components are present in the vicinity of cutoff, the input level should be reduced correspondingly.

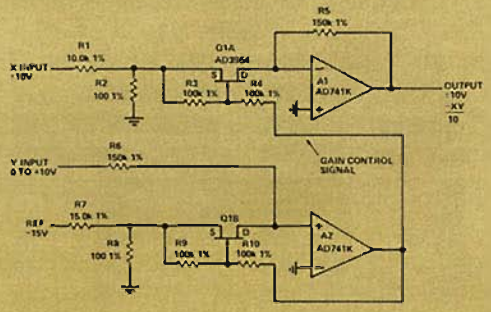
The cutoff frequency has a TC of about 1%/°C. The circuit should be fed from a low-impedance source, such as another operational amplifier.

Cutoff frequency ranges can be scaled directly by scaling the capacitance values. The 3.3:1 capacitance ratio provides 0.6dB corner peaking. Smaller ratios reduce peaking, larger ratios increase it. With 0.6dB peaking response is down about 1.2dB at the asymptotic cutoff frequency.



2 QUADRANT MULTIPLIER

This circuit is useful as a gain controller for ac or dc signals. A 0 to +10V Y input signal will control the gain of an X input signal in the ±10V range.



At Y = +10V, the gain is unity and typical best straight line linearity, when the X input is varied from −10V to +10V, is 0.1%. Nonlinearity increases as Y decreases to lower the gain. At a gain of 0.1, corresponding to Y = +1V, typical linearity is 1% and consists of mostly third harmonic distortion. Y input linearity is 1% from 1V to 10V.

The gain control portion of the system consists of Q1A which feeds an inverting operational amplifier A1. The FET is fed from a low source resistance made up of the divider R1 and R2 which delivers ±100mV to the source of Q1A. Normally, linearity, even at this signal level, is very poor as the bias on Q1A is raised towards the pinchoff voltage. By feeding some of the input signal back to the gate via R3, so as to maintain the gate signal voltage dynamically midway between the source and drain voltages, second harmonics are eliminated, leaving only third harmonics, and total distortion is greatly reduced. Distortion cancellation results from the excellent symmetry of the AD3954 which makes the source and drain essentially interchangeable and allows about a 5X larger input signal to be used for the same distortion, thus improving the signal to noise ratio.

For a gain range of 10 to 1, Q1A is operated as a variable resistance having a range from 1.5k to 15k. Since this varies the feedback ratio around amplifier A1, the −3dB bandwidth, which is typically 45kHz at a gain of 0.1, decreases to 4.5kHz at a gain of 1. The bandwidth can be readily increased by designing the circuit for lower input and output levels, say ±1V instead of ±10V, simply by reducing R1 and R5.

As a gain controller, only the upper portion of the circuit is needed; it is merely necessary to vary the dc input voltage to R4 in the range of −4V to 1. Zero gain occurs, of course, at the pinchoff voltage and the gain is somewhat temperature sensitive. Improved performance is obtained by the addition of the bias control circuit involving Q1B and operational amplifier A2. In this circuit, a dc reference voltage of +100mV derived from the 15V supply voltage is fed to the source of Q1B. Feedback automatically adjusts the resistance of Q1B to balance the current from the Y input through R6 so as to hold the positive input of A2 at virtual ground. This circuit then automatically produces a bias at the gate which varies in accordance with the characteristics of the particular FET and with temperature. This bias is the same as that required to produce the desired gain as a function of the Y input. By feeding the output of A2 to the bias resistor R4 for Q1A, the resistance of Q1A from source to drain can be made equal to the resistance of Q1B to the extent that the FET pair is matched. This circuit thus provides the correct gate bias and transforms the Y input voltage from −4V to 0 to the 0 to +10V range. If the FET's are perfectly matched, the gain of Q1A vs. temperature is compensated and nonlinearity vs. the Y input is also compensated. The circuit can be made to operate at different Y input voltage levels or at different reference voltages by changing R6 and R7. Note that the gain varies inversely with the supply voltage, which is used as a reference supply. Sensitivity can be decreased by using a reference zener diode.

There is a slight amount of feedthrough from the Y input when the X input is 0, which results in a small dc output proportional to the Y input if there is an offset in A1. This can be eliminated by balancing out the voltage offset of A1; in ac circuits it can be eliminated by inserting a large value tantalum coupling capacitor between the drain of Q1A and the negative input of A1.