Power MOSFETS — the technology, the techniques

Brian Dance

IN 1976 Siliconix startled the semiconductor world with a new type of power MOSFET device. Recently other manufacturers have produced many other types of MOSFET products which are challenging power transistors and Darlingtons.

The name MOSFET stands for Metal Oxide Silicon Field Effect Transistor. Field effect transistors (FETs) are essentially voltage controlled devices, unlike conventional transistors in which the small base current controls a larger collector output current. FETs have very high input impedances so that very little input current is required to control their output current.

The input impedance of MOSFETs is especially high because they have an insulating film of silicon dioxide between the input gate electrode and the channel through which the output current flows. The gate electrode is therefore essentially completely insulated and virtually no input current can flow.

Various types of small MOSFET devices have been available for many years. Internally they contain a very small silicon chip on the surface of which the MOSFET device has been fabricated. Any current passes through these devices in a horizontal direction through the very thin surface layers and therefore the maximum current is quite low; maximum power dissipation in such devices is not normally over 1W.

VMOS devices

In the so-called VMOS devices, developed by Siliconix about eight years ago, the current flows vertically through the semiconductor material — hence the name VMOS. This name is also associated with the V-shaped groove formed in the surface of the semiconductor material of such devices. Figure 1 shows a cross-section of a VMOS transistor.

If the gate electrode is connected to the source and the drain contact at the bottom of Figure 1 is made positive relative to the source, no appreciable current will flow from drain to source, since the internal diode formed between the p and n type materials will be reverse biased. If, however, the gate electrode is made positive with respect to the source, the electric field produced by the gate potential creates a channel in the position shown in Figure 1. A current can now flow upwards from the drain through the channel to the source. As the gate becomes more positive, the width of the channel increases and the current from drain to source increases.

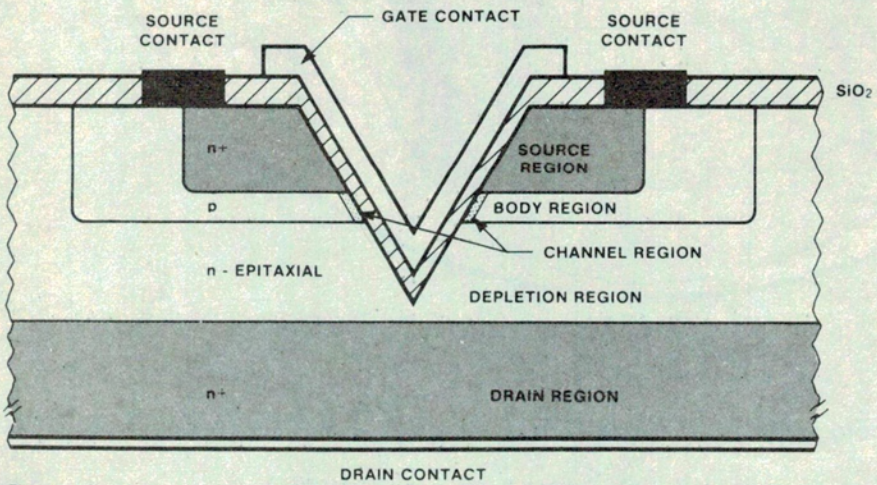


Figure 1. **Structure of the VMOS device developed by Siliconix. With the gate biased positive with respect to the source, current flows from the drain region to the source via the channel region indicated. As the gate is biased more positive, the channel region increases, increasing the drain-source current. VMOS FETs are majority-carrier devices and can switch current in less than 10 ns. Bipolar transistors cannot compete as they suffer from minority carrier storage in the base region.**

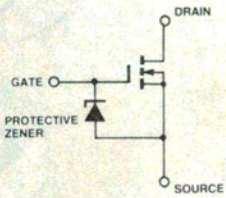


Figure 2. **Zener protection of the gate.**

If small changes in the gate voltage are to produce the required channel depth, the insulating layer must be extremely thin, which results in an appreciable gate input capacitance (typically some 50 pf). The thin layer also imposes a limit to the maximum voltage which can safely be applied to the gate without the risk of breaking down this thin layer and thus destroying the device. As the gate input resistance is so high (often of the order of a million megohms), it is very easy for small stray electrostatic charges to be picked up on the gate and produce voltages which can puncture the insulating film.

In some devices a small zener diode is connected between the gate and the source, as shown in Figure 2. If the gate to source voltage exceeds the zener voltage, the zener conducts and shorts out the voltage, protecting the MOSFET.

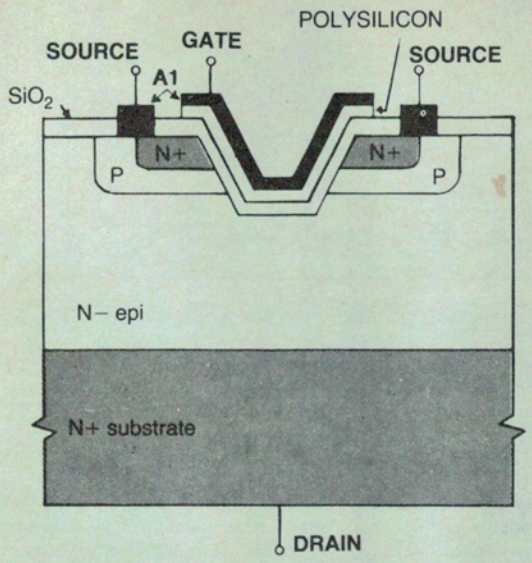


Figure 3. **The U-groove device, introduced by Intersil, reduces problems associated with the intense electric field at the edge of the V-notch in VMOS devices. The polysilicon layer prevents migration of sodium impurity ions through the gate oxide layer, a source of chip failure in VMOS.**

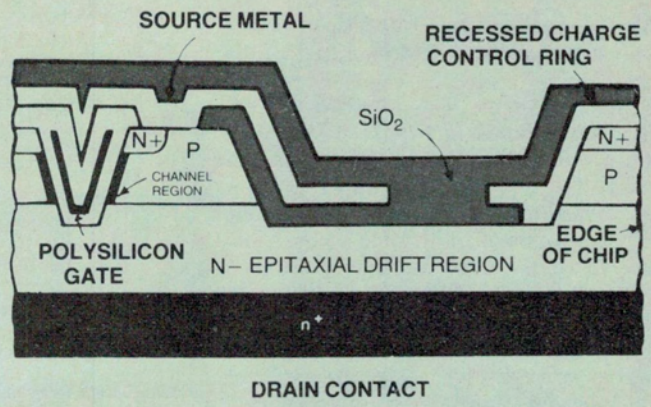


Figure 4. **Having introduced power MOSFET technology, Siliconix have gone on to improve the devices. The tri-planar construction shown here allows much higher packing densities on the chip, the smaller size resulting in lower on state resistance. Polysilicon gates are buried in the oxide layers allowing source metallisation to cover a greater fraction of the chip area.**

However, the maximum zener current is quite small, so the zener can easily be damaged. The maximum input voltage 'in circuit' should not exceed the zener voltage so that the zener is used to provide protection against electrostatic charges only.

If the gate becomes more than a fraction of a volt negative with respect to the source, the zener will conduct in its forward direction. If one wishes to operate a MOSFET with the gate voltage negative with respect to the source at any part of the duty cycle, a device not containing a zener should be selected, but then one must take precautions to avoid electrostatic charge pick up.

The first VMOS devices marketed were n-channel devices, with an n-type channel formed in the p-type material shown in Figure 1.

Comparison with bipolars

As the early VMOS devices could not handle so much current or so much applied voltage as conventional transistors, yet were more expensive than the latter, they obviously had some advantages or their manufacture would not have been a viable proposition.

Ordinary bipolar transistors suffer from the disadvantage of minority carrier storage in the base region. VMOS products are majority carrier devices and can therefore switch a current in less than 10 nanoseconds and operate up to several hundred mega-Hertz. For example, the 2N6657 can switch 1 A on or off in less than 4 ns, this being 10 to 200 times faster than a comparable bipolar device.

'Secondary breakdown' is another problem with bipolar transistors. If the current density increases at one point, the temperature rises in this region, leading to a still greater current density — a positive feedback effect which can lead to the rapid destruction of the device. In VMOS devices, an increase in the current density in the channel produces an increased temperature which results in a *lower* current density in that region, so that the current density automatically equalises itself throughout the chip without the formation of hot spots.

It follows that it is possible to connect two or more VMOS devices in parallel (often without any additional components), since the total current is automatically shared equally between the devices. Any device passing more current than the mean will become hotter and this will reduce the current somewhat in that device.

Apart from their higher cost, one of the disadvantages of VMOS devices is that their saturation voltage (typically 2V, maximum 4V for some devices when passing 1A) is much greater than for bipolar transistors. Although the V-shaped groove utilises the silicon area quite efficiently, the relatively sharp bottom of the groove is a disadvantage, since a strong electric field can be developed at this point between the gate and the drain where the insulating layer tends to be thinner than elsewhere. This results in a limited operating voltage capability owing to the possibility of gate to channel breakdown.

A perfect switching device would have an infinite resistance in the off state, but the drain current of many VMOS devices is in the nA region when in the off state with gate and source voltages equal. The resistance in the conducting state is normally a few ohms instead of the zero resistance of the perfect switch. This on-resistance is greater for devices with higher voltage ratings.

U-groove devices

The problem of the relatively intense electric field at the edge of the V-shaped notch of VMOS devices has already been mentioned. Intersil, followed by some other manufacturers, reduced this problem by producing devices with the structure shown in Figure 3, where the bottom of the groove is flat. Note that there is an additional layer of phosphorus-doped polycrystalline silicon between the gate and the insulating layer of silicon dioxide. This overcomes another problem of the early VMOS devices, namely the migration of sodium impurity ions through the gate oxide layer, which can cause reliability problems.

Other VMOS products

In 1980 Siliconix announced an improved triplanar VMOS process with the device structure shown in Figure 4. The source, the gate and the drain are each fabricated in a different plane. It is stated that this type of structure allows much higher packing densities on the chip and the smaller size will enable lower on state resistances to be obtained. Polysilicon gates are buried under the oxide layers so that the source metallisation can cover a greater fraction of the chip area.

Another major improvement from the triplanar structure arises from the use

of thin low-resistivity doped layers and from a re-arrangement of the V grooves for optimum use of the epitaxial layers.

Vertical DMOS

Although the modified VMOS processes are very good for devices rated up to about 150 V, they are not ideal for higher voltages. The vertical DMOS structure shown in Figure 5 has been found very suitable for high voltage devices. The current flows upwards from the drain into the n-epitaxial layer, but then flows horizontally for a short distance through a channel to the source.

Supertex of California originally used this technique to make devices with ratings of up to about 500 V, but somewhat higher voltage devices of this type have since become available. Figure 5 shows how the main junction region is surrounded by a concentric second junction which is in turn surrounded by a third junction. Apart from high voltage capability, this process can produce devices with a very low on-resistance (down to 0.05 ohm). In addition the devices are very fast, owing to the low gate capacitance. For example, a 1 A device can operate at about 2 GHz and a 10 A device at about 500 MHz.

The Ferranti Company of Oldham, England has co-operated with Supertex to develop vertical DMOS devices, both n-channel and p-channel, with ratings up to 650 V and drain currents up to 16 A continuous.

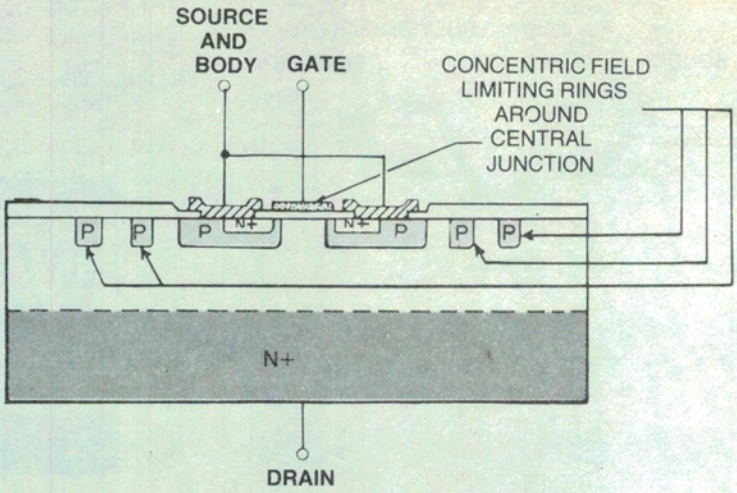


Figure 5. **In the vertical DMOS device, current flows from the drain (N+) into the n-epitaxial layer (N−) then flows horizontally through a channel into the source. The concentric rings of p-type material around the main junction help improve the current capability and reduce the on-resistance. This form of construction achieves significantly higher voltage and current ratings compared to prior power MOSFETs.**

Hitachi devices

Hitachi has developed a MOSFET device with the structure shown in Figure 6. The gate oxide layer is designed to handle only 20 to 30 V, so a field plate is provided to prevent high electric fields from forming near the gate. This type of device is most suitable for audio frequencies and for operation at up to a maximum of a few MHz. Both p-channel and n-channel types are available with ratings of up to 200 V and 8 A.

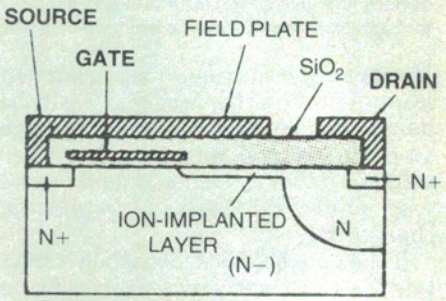


Figure 6. **Hitachi MOSFET construction.**

HEXFET devices

In mid-1980 International Rectifier introduced a range of devices named HEXFET after the hexagonal structure of the source cells which are connected by a common silicon gate (see Figure 7). The density of these source cells is over half a million per square inch.

HEXFET devices are available in both p-channel and n-channel polarities and can handle high power levels. They have voltage ratings of up to 500 V and continuous current ratings of up to 25 A. Values of channel resistance as low as 0.05 ohm can be obtained in the on state.

Some of the main applications for HEXFETS include servo motor control, RF induction heating, welding control equipment, audio amplification and other uses where the control of high power is required.

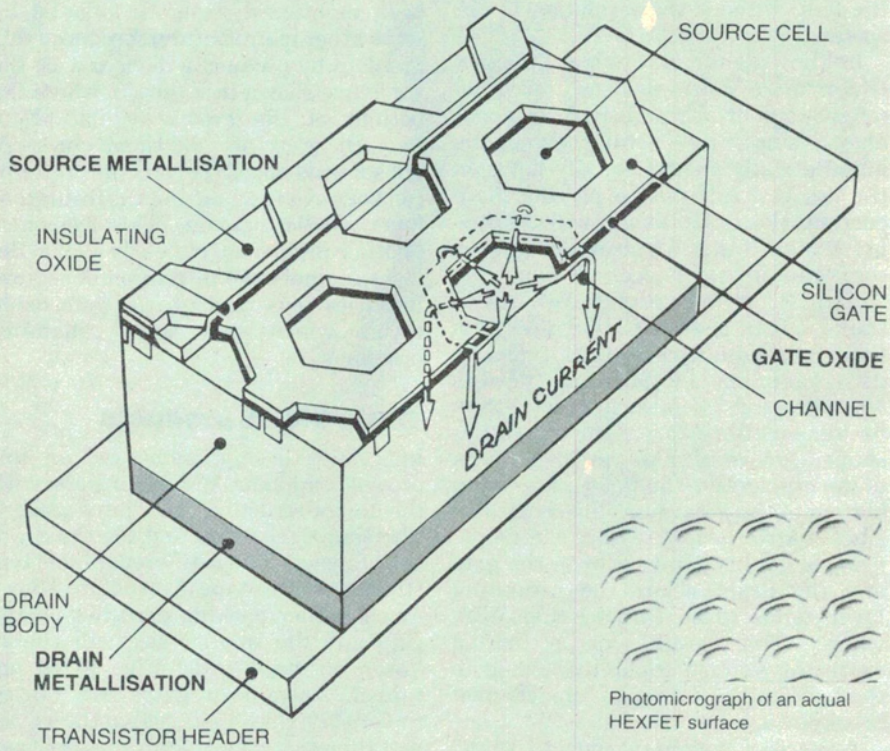
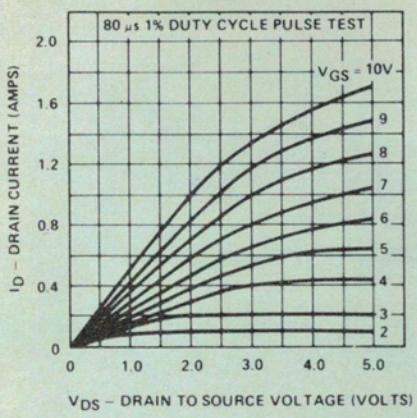
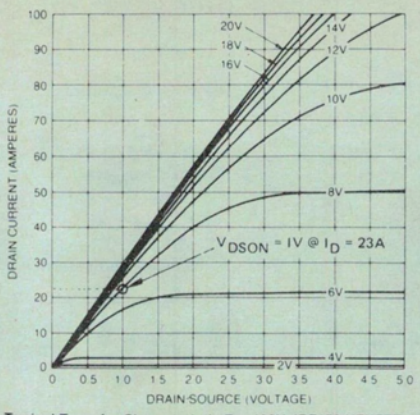


Figure 7. **Construction of the HEXFET device introduced by the International Rectifier company in mid-1980. The hexagonal source cells (hence the name) are connected by a common silicon gate. Claimed advantages include high voltage and current ratings plus very low on-resistance.**

SIPMOS

The latest technology to emerge in the power MOSFET field is SIPMOS from Siemens of West Germany, which is an extension of the vertical DMOS technique. Siemens has used this technique to fabricate the first 1000 V MOSFET device, the BUZ 54, which can handle 5 A. It has found wide uses in switching





Typical Transfer Characteristic For 100V, IRF150 HEXFET.

The saturation characteristics of a VMOS device (left) and a HEXFET (right)

mode power supplies.

Other SIPMOS devices have ratings in the range of 50 V to 500 V, all being n-channel types. SIPMOS transistors can switch loads of up to 5 kW using inputs to the gate of less than 1 mA at 5 V. Maximum drain currents of up to 30 A can be handled, while on-resistance values can be as low as 0.03 ohm.

Applications

Power MOSFET devices can be used as alternatives to power transistors and power Darlington devices in many applications, but they are generally more expensive than the latter and the circuit designer must decide which types of device are most suitable for his own application.

The use of power MOSFET products is particularly attractive when one can take advantage of their high switching speed or their high frequency capability. Although they may be somewhat more expensive than other transistors, the use of these new devices may simplify circuitry and reduce the overall costs. For example, a conventional power transistor requires a considerable current at its input and one or more driver stages may be required to provide this current, whereas the high input impedance of the power MOSFET enables the latter to operate with such small input currents that power driver stages can usually be eliminated.

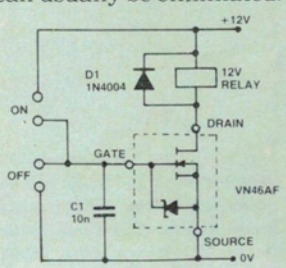


Figure 8. **Simple touch switch.**

Simple touch switch

The circuit of Figure 8 shows how the very high input impedance of a VMOS power MOSFET can be employed in a simple touch switch. When the circuit is first switched on, the capacitor C1 is normally fully discharged, so the VN46AF VMOS device passes negligible drain current.

When the upper pair of contacts is touched, current flows from the +12 V line through the person's skin and charges C1. The VN46AF device is thus biased to conduction and the relay closes. If a finger is now placed across the lower touch contacts, C1 discharges and the VN46AF is turned off, opening the relay. The diode D1 is used to bypass the transient voltages formed when the current ceases to flow through the relay coil — such voltages can destroy MOSFETs.

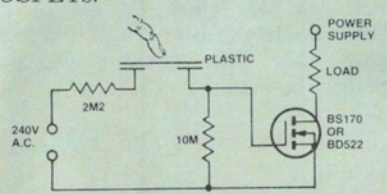


Figure 9. **Capacitive touch switch.**

Capacitive touch switch

The gate circuit impedance of VMOS devices is so high that circuits can be designed as touch switches in which no part of the circuit is actually touched. In Figure 9 (designed by ITT Semiconductors), the presence of a finger just above the plastic material at the point of separation of the electrodes under the plastic is sufficient to cause current to flow in the load.

The capacitance between each of the electrodes and the finger allows a small alternating current to flow through the 2M2 safety resistor to the gate circuit of the small BS170 or the larger BD522 n-channel device.

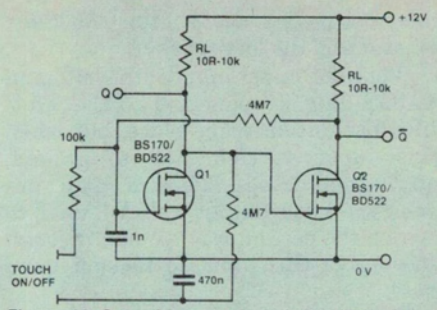


Figure 10. **Capacitive touch switch will cycle on and off if finger is held on the sensor.**

Figure 10 shows another touch switch designed by ITT Semiconductors, only a single touch point being used for on/off operation. When power is first switched on, T1 will conduct and T2 is kept non-conducting. Touching the sensor contacts will cause T2 to conduct and feedback from the drain of this device through the 4M7 resistor to the gate of T1 will keep the latter device in the non-conducting state. The 470n capacitor now becomes charged.

If the sensor is touched again, the positive potential from this capacitor is transferred to the gate of T1 and the latter device is switched to conduction, whilst T2 is turned off. If the sensor is touched for longer than about one second, the circuit will operate as a relaxation oscillator which changes its state about once per second. The load impedances employed in this circuit need not be identical, any values from about 10 ohm to 10k being suitable.

CMOS interfacing

The 4000 series of CMOS logic devices can provide only small output currents, but sometimes one wishes to use the output from such a device to control a relay or other load which requires a relatively large current. A VMOS device can conveniently be employed to match the high output impedance of a CMOS device to a relatively low load

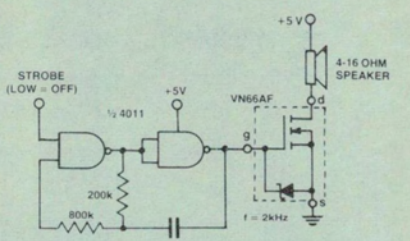


Figure 11. **Audio alarm.**

impedance such as a tungsten filament lamp.

An example is the audio alarm circuit of Figure 11. Two of the four logic gates of a CD4011 device are connected as a standard 2 kHz oscillator. Any appreciable current taken from the output of this oscillator affects the operation of the circuit, but the VN66AF requires negligible current and forms an ideal

interface device between the CMOS oscillator and the loudspeaker.

When the upper input of the left hand CMOS gate is connected to the +5 V line, oscillation takes place, but when this input is connected to ground, oscillation ceases. Thus a high impedance logic output can be used to switch the oscillator on and off through the use of this input to the left hand gate.

Figure 12 is an interesting variation of the circuit of Figure 11 in which the four gates of a 4011 device are used to form two oscillators. The two left hand gates form a sub-audio frequency oscillator which modulates the audio oscillator formed by the two right hand gates of Figure 12. Thus one obtains a much more impressive two-tone alarm sound than with the simpler constant-note circuit of Figure 11.

The timer circuit of Figure 13 is another example of VMOS interfacing between a CMOS device and a relay. In the quiescent state, the upper input to the left hand gate will be low and the output from this gate high. Thus the output from the right hand gate will be low and the relay will remain open.

If the start switch is momentarily closed, the high input applied to one input of the left hand gate will cause the output from this gate to go low, while the output from the right hand gate goes high and switches the VN46AF to conduction. Thus the relay closes.

The capacitor between the two gates charges slowly through the fixed and variable resistor from the positive supply line. When the inputs to the right hand gate become sufficiently high in potential, the output of this gate goes low and by feedback to the left hand gate the circuit switches back rapidly to its quiescent state in which

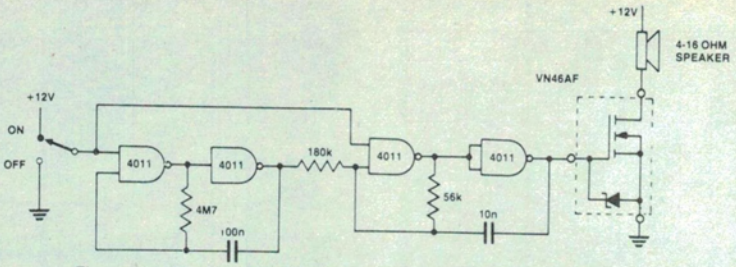


Figure 12. **This two-tone alarm is a variation of the Figure 11 circuit.**

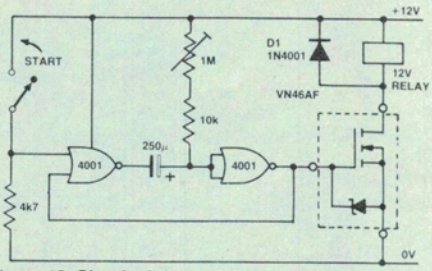


Figure 13. **Simple timer has a variable range from a few seconds to a few minutes. The 1M pot sets the time the relay holds in.**

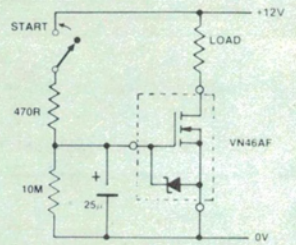


Figure 14. **Simple delay timer. The load could be a lamp, relay or whatever.**

negligible current passes through the relay. The length of time for which the relay remains closed can be set by the 1M pot or by altering the value of the capacitor connected between the two gates. When the values shown are used, times obtained range from a few seconds to a few minutes as the variable resistor is moved.

Delay switch

A simple VMOS delay switch is shown in Figure 14. When the switch is closed for a moment, the capacitor becomes fully charged and the VN46AF passes current through the load. The capacitor slowly discharges through the 10M resistor, so the gate voltage of the VN46AF will eventually fall to a value where very little current can pass through the load.

Auto devices

The fast switching ability of MOSFET devices renders them very suitable for use in vehicle electronic ignition systems. Timing pulses from a magnetic or other contactless pickup may be fed to an IC which provides a voltage output for the control of a MOSFET device. The latter switches the current through an ignition coil to provide the required high voltage.

An automobile circuit using a SIPMOS transistor as a power switch is shown in Figure 15. As in so many applications of MOSFET devices, the high input impedance of the SIPMOS device is utilised here, since it can be voltage driven by a suitable IC. This circuit is for an automobile alternator voltage regulator and has been designed for a SIPMOS device rated at

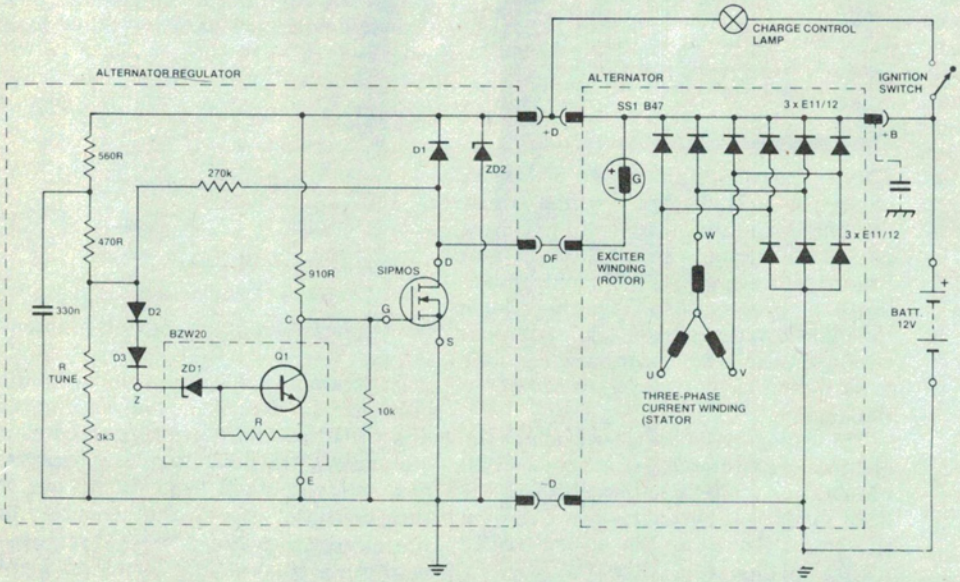


Figure 15. **The latest power MOSFET development, SIPMOS, has already found application in automotive electronics. This circuit is an alternator regulator and employs a SIPMOS device rated at 500 V/8 A and an on-resistance not greater than 0.2 ohm.**

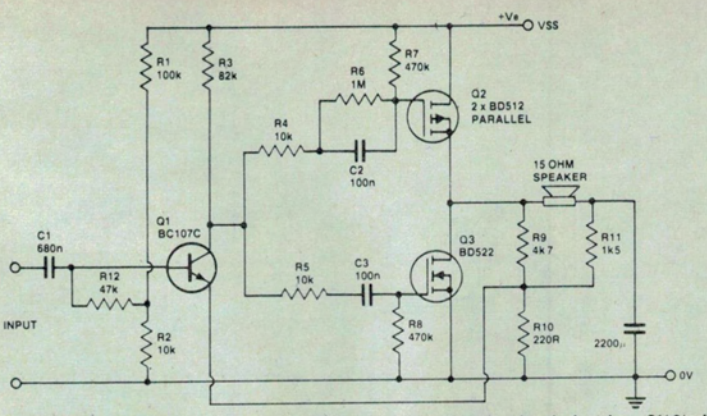


Figure 17. **Class ABC amplifier circuit from ITT Semiconductors is simple but has 3½% distortion at 1.75 W and is only suited to general applications.**

about 500 V maximum drain-to-source voltage, 8 A current and an on-resistance of not more than 0.2 ohm.

Simple audio applications

The excellent linearity of VMOS devices has attracted considerable interest in their possible use in the audio field but the relatively high price of these devices and their previously limited power handling capability retarded their adoption until recently. They may be used in simple, low-power circuits, but moderately high power ultra-low distortion circuits have also been designed using VMOS devices. The very fast switching ability of VMOS devices also makes them very suitable for Class D pulse width modulation circuits.

To operate a VMOS device as a simple class A amplifier, it is only necessary to provide a bias network so that the device operates in its linear region without cutoff. The gate is connected to a tap on a resistive potential divider across the power supply lines and the input signal is capacitively coupled to the gate. The gain will be approximately equal to the mutual conductance of the device multiplied by the load resistance; gain values of over 30 dB are obtainable, and this gain extends well into the MHz region.

A circuit of this general type is shown in Figure 16. The bias level of the VMOS device is stabilised by means of negative voltage feedback from the drain to the gate circuit.

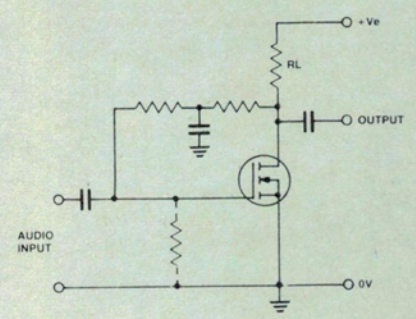


Figure 16. **General circuit of a simple class-A audio amplifier using a power MOSFET.**

Figure 17 shows a particularly interesting circuit from ITT Semiconductors which they call a class ABC amplifier, since it is basically a Class B amplifier, but one of the transistors is more in Class A, while the other is definitely in Class C. It is a simple circuit not designed for particularly low distortion.

The output stage is unusual in that it comprises two BD512 p-channel VMOS devices in one part and a complementary BD522 single device in the other part. This is because hole mobility in the p-channel BD512 is only half that of the electron mobility in the n-channel BD522s so two p-channel devices are required to obtain about the same mutual conductance as that provided by the single n-channel device. As explained earlier, MOSFETs can be connected in parallel without extra circuitry because they automatically share the current.

As the drain electrodes of the VMOS devices in Figure 17 are connected to the device tabs, all of the tabs can be bolted to the same heatsink without the need for insulating washers. The negative feedback circuit compensates for any variations in the biasing requirements of the particular VMOS devices employed. Both ac and dc feedback are employed, but there is heavier dc feedback through R11 and R10 to stabilise the quiescent dc output voltage at half the supply potential so as to ensure a maximum available output voltage swing.

This circuit provides a voltage gain of 30 and a bandwidth extending from 35 Hz to 125 kHz at the −6 dB points. Distortion increases at ultrasonic frequencies above about 25 kHz (as with most audio amplifiers). When a 25 V supply is used, the distortion is a minimum of about 0.4% at about 0.5 W, rising to about 0.8% at 1 W, 2% at 1.5 W and 3½% at 1.75 W.

High fidelity

In 1976 Siliconix published a circuit for a high quality 40 W amplifier using VMOS devices, but each half of the output stage required three VMP12 (now designated 2N6658), 90 V TO-3 devices in parallel. Thus, twelve of the devices were required in a stereo amplifier providing 40 W per channel. Rather cumbersome — and costly. However, distortion at the mid-frequency range was only about 0.04% at the 40 W level and about 0.025% at the 1 W level. Only 22 dB of feedback was needed to obtain a response flat to 4 MHz and the slew rate was 100V/μs!

One of the advantages claimed for VMOS amplifiers is the lack of transient intermodulation (TIM), because the power bandwidth exceeds the small signal bandwidth. For any frequency below 500 kHz, the amplifier simply overloads before TIM appears.

Taking things a step further, the circuit in Figure 18 is a simple power amplifier first published in the Hitachi MOSFET application notes. The 2SK133 and 2SJ48 have an on-resistance of roughly two ohms, so that at 7 A peak output current you can expect a voltage drop of about 14 V across each device. With the power supply voltages shown the circuit is capable of around 50 W.

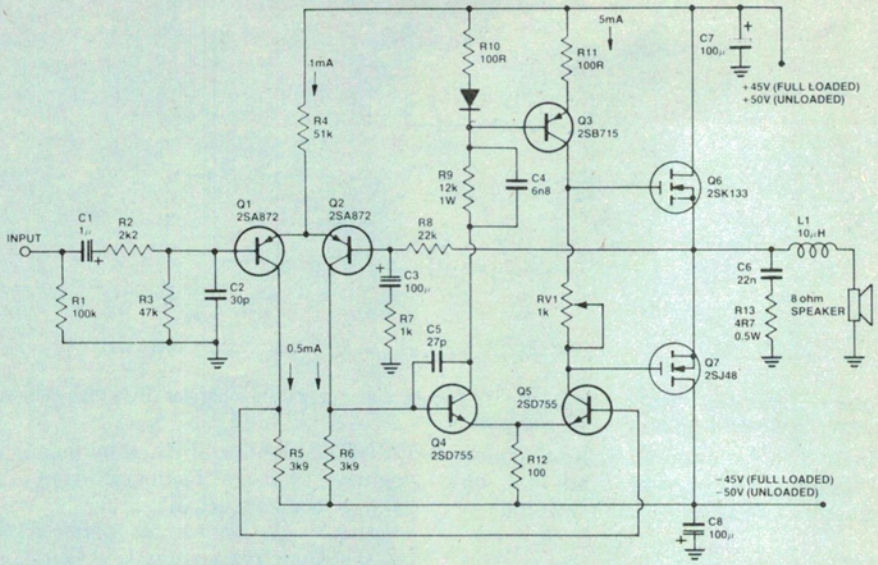


Figure 18. **Circuit of a 50 W hi-fi amplifier from the Hitachi MOSFET application notes. Performance is quite good but dependent on the driver transistors.**

Transistors Q1 and Q2 form an input differential pair that compares the input signal with the output signal of the amplifier. The difference between these two signal voltages is fed to a second differential pair, Q4 and Q5. This ensures that the open-loop voltage gain of the amplifier is high and allows a fairly high feedback factor when negative feedback is applied. A relatively large amount of negative feedback is essential when using MOSFETs like this in audio amplifiers to linearise the MOSFET characteristics which have, on average, *10 times* the distortion of a typical bipolar transistor of similar power capabilities.

The transistors forming the driver stage, Q3 and Q5, have been specially designed by Hitachi to drive MOSFETs. They're superb devices, having a V_{ceo} of 100 V and a typical gain (h_{FE}) of around 500. With these transistors the distortion characteristics shown in Figure 19 can be expected. Unfortunately, these transistors are not available in Australia at the present time and substituting alternative available transistors degrades performance considerably. A BD139/BD140 complementary pair for instance, with typical h_{FE} of around 50, is not capable of providing the necessary open-loop gain, especially at high frequencies. An experimental circuit we built with BC177s and BD139/BD140s gave less than 0.02% at 1 kHz at full power, rising to as much as 0.1% or more at 20 kHz. So, MOSFETs with all of their advantages have disadvantages too — mainly due to the fact that the forward transconductance is only a fraction of that of a good bipolar transistor.

In order to design an extremely high quality amplifier employing MOSFETs, we are really faced with a new set of problems to solve, but with the promise of performance that makes it worthwhile. (This section on Figure 18 inserted by David Tilbrook . . . Ed.).

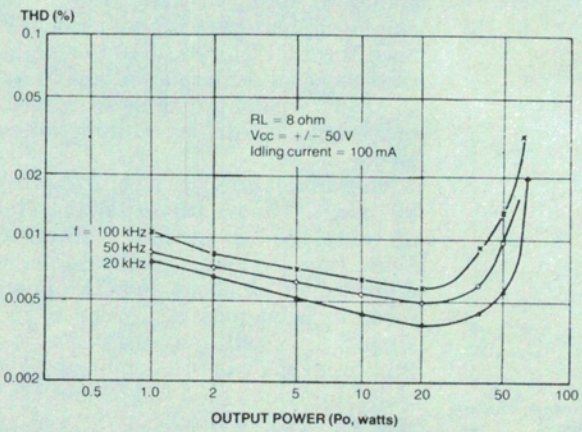


Figure 19. **Distortion characteristics of the circuit in Figure 18.**

VFETS for everyone — Part I

Wally Parsons looks back to valves to explain VFETs.

Wally Parsons

A DIODE VALVE emits electrons from a heated cathode and these are then attracted by an electric field to the positive anode. Since only the cathode is heated, current can flow in only one direction. The diode will thus act as a rectifier, conducting only on alternate half-cycles of an AC voltage (see Fig. 1).

If a grid structure is placed between these electrodes, it can be used to control current flow. A negative potential will repel electrons, opposing their flow to the anode, and by placing the grid close to the cathode, a small change in grid potential will have the same effect on anode current as a much larger change in anode potential. Therefore, the device will amplify. Since the anode current is controlled by the electric field in and around the grid, the triode is, in a sense, a field effect device.

The action is direct, and electron flow responds rapidly to changes in control potential. Moreover, in switching applications it can switch an inductive load rapidly, because the back EMF sees an extremely high impedance and no reverse current flows.

Figure 2 shows the relationship of anode voltage, grid volts, and anode current for a triode. It can be seen that anode current can be controlled by both anode volts and grid volts. If a load is inserted in the anode circuit, current changes will cause voltage changes across the load. These can be plotted in the form of a load line as shown, and also as a transfer curve for the specific load.

The amplification is quite linear, but gain and output are limited – as shown by the semi-vertical slope of the curves.

Inserting a second grid between the control grid and anode and applying a fixed positive voltage somewhat lower than on the anode further accelerates

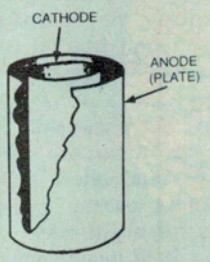
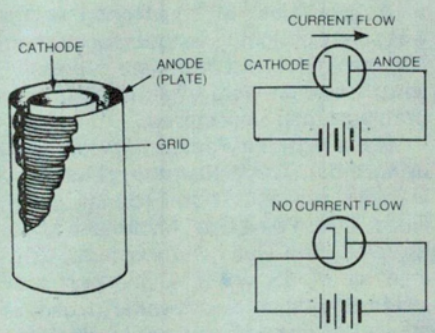


Fig 1. Basic diode tube construction and operation.



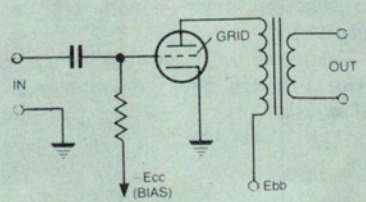
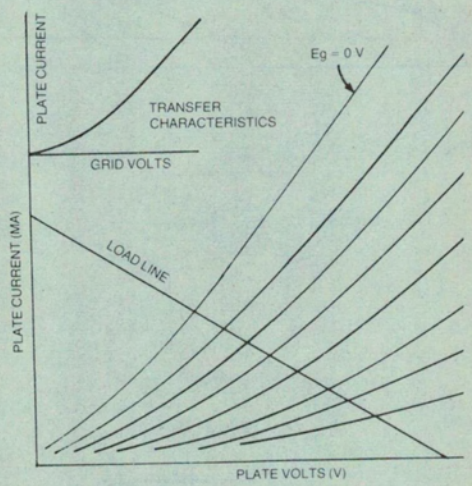


Fig 2. Triode construction, circuit and characteristics.

electrons, but because of the grid's open structure, most of them continue on to the anode. Note the screen voltage takes precedence over the anode in controlling current. And we can swing the anode voltage further for more output, and get higher gain too.

The addition of the second grid with a fixed high potential results in a current flow essentially independent of anode voltage, but still subject to the action of the control grid. (Figure 3). Trouble occurs, however, when we try



to produce an anode voltage swing lower than the screen voltage. Electrons are moving so fast that when they strike the anode they dislodge other electrons, which are attracted to the higher potential screen grid, thus reducing current through the load.

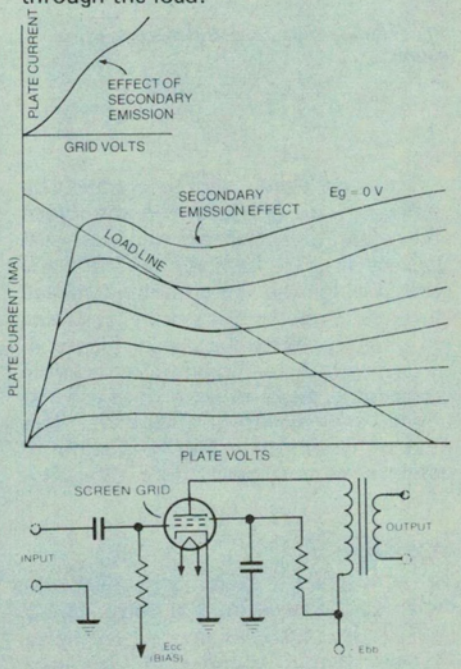
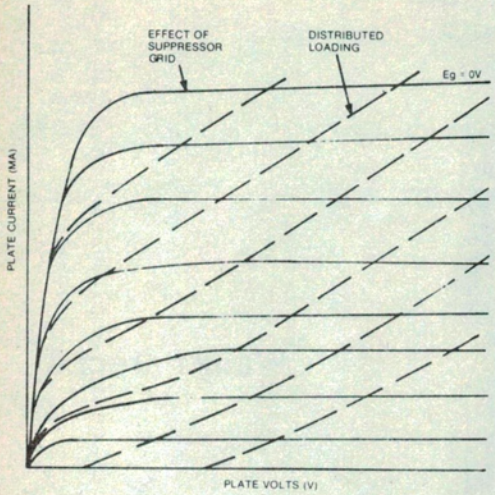
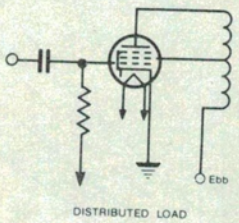


Fig 3. Series output arrangement.





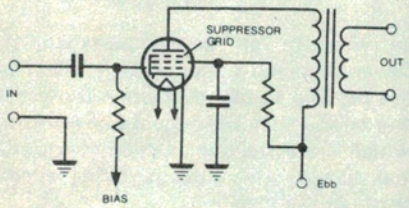


Fig 4. Single ended output with current source.

This problem was overcome by adding a third grid between the screen and plate and tied to the cathode. Because it is at cathode potential the grid pushes the secondarily emitted electrons back to the anode, resulting in a family of curves as in Figure 4.

Distributed loading is also possible by dividing the load between screen and anode, and results in Figure 4a. This kind of flexibility makes it possible to design circuits of exceptional linearity.

Problems

So far so good – except for a few problems. To begin with, the valve, like a light bulb, converts more electricity to heat than to useful work. It's very inefficient – for example the author (who is associated with the Canadian version of ETI) uses two 75 watt output class AB valve amplifiers to keep his studio at 25° C. without any additional heating in a Canadian mid-winter!

Also like a light bulb, a valve's performance deteriorates from the moment power is applied. Thus, direct coupled circuits can give real headaches in maintaining correct operating characteristics.

And then there's the output transformer. In order to match the thousands of ohms impedance to a low impedance load such as a loudspeaker, a transformer is virtually a necessity. With the inefficiencies already involved we can't afford the resultant impedance mismatches if we try to eliminate transformers. And we can't use gobs of feedback to reduce the resulting distortion. It's bad enough that, if we don't opt for a delicately balanced direct coupled circuit we have a low frequency roll-off and 90° phase shift at every R-C coupling point, but we have in any case the additional phase shift and internal resonances of the transformer. In practice, we are limited to between 20 and 26 dB of overall feedback. Obviously, a high level of open loop linearity must be designed into such an amplifier.

A great deal of engineering energy was spent designing output transformerless amplifiers, but few were successful, and those that were often created more problems than they solved.

Some legendary amplifiers *were* built using tubes. The Williamson, (I have one in daily use and it still sounds great), Quad, Leak Point One, MacIntosh Unity Coupled. The Quad, for example, delivered all of 15 watts – and was rock stable driving an electrostatic (Quad, of course) at live performance levels. Mac's drove a lot of disc cutters (at 60 watts) to produce discs which still sound spectacular.

But many were anxious to do something with the new-fangled transistors, and we did.

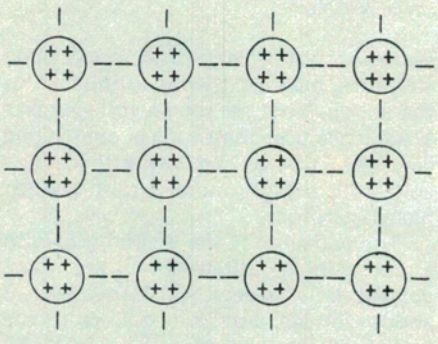


Fig 5a. Basic lattice structure

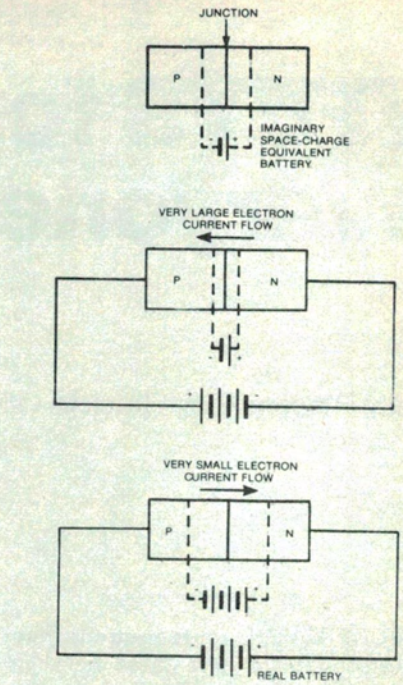


Fig 6. Drain to source resistance against temperature (Siliconix).

Transistors

The bi-polar transistor is composed of three materials, either a p-type semiconductor between two n-types, or an n-type between two p-types, (Figure 7a). A semiconductor such as silicon or germanium has a crystalline structure in the form of a diamond lattice with each atom having four adjacent neigh-

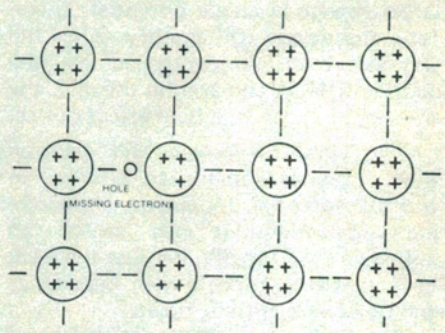


Fig 5b. P-type lattice structure.

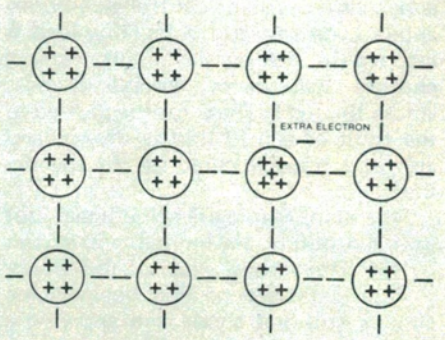


Fig 5c. N-type lattice structure.

bours, held together by co-valent bonds, each bond involving a shared pair of electrons. These electrons are not available for conducting current, so conduction is very semi. Indeed, resistance being around 100 million times that of copper.

However, if we introduce an impurity such as phosphorus or arsenic which has five valency electrons four of which form bonds while the fifth is only lightly held and is available for conduction. This is an n-type material (negative as it has an excess of electrons). If we add an impurity such as aluminium, only three valence electrons are available. Therefore, one of the valence bonds is not completed, resulting in a vacancy or hole in the lattice structure (Fig. 5). An electron from an adjacent electron pair bond may absorb enough energy to break its bond and fill the hold. This is a p-type material. This doesn't look like much of a big deal, but the result is quite dramatic.

Note that the atomic structure is in equilibrium – there is no net charge. However, if a free electron breaks its bond, it leaves behind a positive net charge; if it completes a bond by entering a hole, a negative net charge results. Current flow is produced by bringing about this carrier mobility. What was originally a very high resistance is now, under the right conditions, able to conduct substantial current, just as a small impurity (e.g. sulphuric acid) added to non-conductive pure water, makes electrolytic conduction possible.

When p and n-type materials are joined together, a p-n junction is formed (Fig. 6). Some of the free electrons from the n-type material diffuse across the junction and recombine with holes of the p-type material. The opposite process takes place with holes from the p-type material, producing a space charge or depletion region on either side of the junction, giving the p-type material a slight negative charge, and the n-type a slight positive charge. This process is finally limited by the resulting potential gradient.

If a battery is connected, as shown in Figure 6a, free electrons from the n-type material are attracted to the positive terminal, while holes from the p-type material are attracted to the negative terminal, widening the space charge region and increasing the potential gradient until it approaches that of the external battery. There is now little or no voltage difference across each region and little or no current flow. The junction is reverse biased.

If we reverse these polarities (Fig. 6b) electrons in the p-type material break their bond and enter the battery

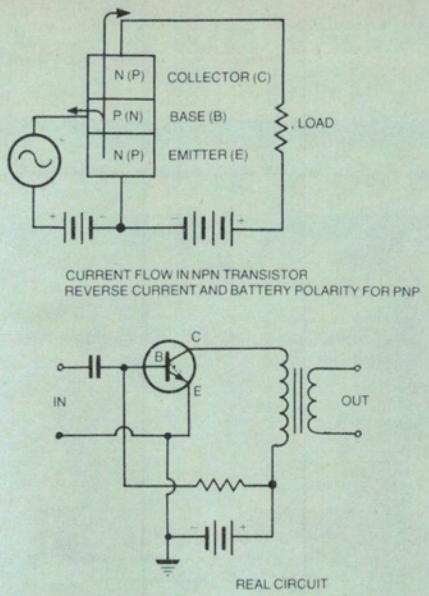


Fig 7a. Current flow in a semiconductor and circuit diagram.

creating new holes, while electrons from the battery negative terminal enter the n-type material and diffuse toward the junction. The space charge region narrows and the energy barrier becomes insignificant, so that excess electrons from the n-type material can penetrate the junction and move via the p-type holes to the positive battery terminal, for as long as voltage is applied. The junction is now forward biased.

Work!

In the device shown in Figure 7, the forward-biased emitter-junction injects electrons into the base region. The impurity or doping levels chosen are such that almost all the emitter current is composed of these electrons, and very few holes are injected into the emitter. The base region is very thin so that nearly all injected electrons diffuse to the edge of the depletion region of the reverse-biased base-collector junction where the field sweeps them across the collector bulk. Since for an equal current more power is developed across a high resistance than a low resistance, amplification occurs as a result of current being transferred from the low-resistance emitter-base junction to the high resistance collector junction.

The curves show that, as with the pentode tube, current is controlled mostly by the control electrode (base), but in this case the controlling parameter is current, not voltage. We have an inherently low-impedance device, and since it requires current into its input impedance, its signal source must be capable of delivering power. An ideal transistor requires input current, unlike an ideal vacuum tube. This reduces efficiency but we don't have to heat up a cathode to shake a few electrons loose, so our overall efficiency is vastly greater.

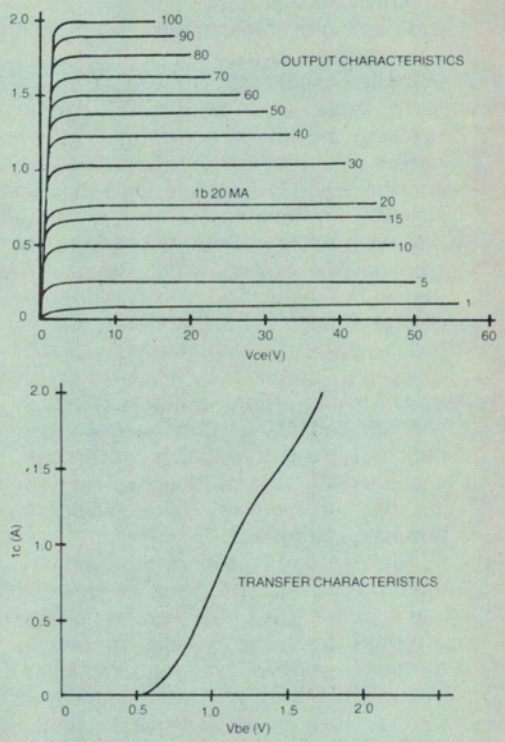


Fig 7b. Output and transfer characteristics of the 2N3054.

Disadvantage

The major disadvantage of this type of device lies in the nature of the depletion layers at the junctions, particularly the emitter-base. When current flows in a transistor, excess charge is stored in the base region. If the base-emitter junction is changed from a forward to reverse bias state, as in the negative swing of a class B or AB stage, or when a class A stage is overdriven, the junction cannot immediately switch to the reverse blocking state due to the presence of these excess charge carriers. They have the effect of allowing current to flow in reverse as if forward biased, until these charge carriers are removed.

In addition, there is capacitance effect associated with the barriers of a reverse-discharge time. The result is a switching transient during part of a cycle, sometimes erroneously referred to as crossover distortion (the latter occurs in any device in push-pull and is due to a discontinuity in the transfer function, usually caused by incorrect bias). This can be reduced by reducing the junction area but this reduces the dissipation capability. In fact, a transistor design favouring one characteristic usually does so at the expense of others.

Also, as temperature rises in the

device (due to current flow, for example) carrier mobility at the junctions increases, causing further increase in current. The current increase further raises temperature, which raises current – which further raises temperature – and so on. The resulting thermal runaway can quickly destroy the device. In milliseconds!

In large area transistors, current tends to become nonuniform in distribution. The temperature rise in the high current region leads to localized thermal runaway until equilibrium is reached by a sharp drop in collector voltage, (called secondary breakdown) frequently destroying the device. This is more true at high voltage and low current than the reverse, and frequently means that rated dissipation cannot be reached. This leads to overdesign, unnecessarily high voltage and dissipation ratings (and remember, a design which favours one characteristic often does so at the expense of others) plus elaborate protective circuits.

High levels of feedback are generally used to control distortion, and this in conjunction with the excess charge condition in the base, leads directly to transient overload, and resultant transient intermodulation. Output is delayed during this charge/discharge, which delays application of feedback. It simply isn't available. The input signal is not immediately reduced by feedback, and passes through at high initial level.

The millenium has not quite arrived after all!

The FET

Since a semi-conductor is precisely that, a battery connected across the ends of a p-type or an n-type bar will cause current to flow through the material, just as it does through a vacuum tube. We discussed earlier the characteristics of a pn junction. If, for example, a p-type material is joined to the surface of an n-type bar, located between the battery terminals, a pn junction is formed, and if this junction is reverse biased, a space charge or field is produced of opposite polarity which will inhibit current flow, just as the control grid inhibits current flow in a vacuum tube. Changing this reverse voltage causes a large current change, and amplification results.

A simple junction FET is shown in Figure 8. With a given drain-source voltage, maximum current flows at zero gate voltage, and at some reverse voltage, determined by device geometry and doping levels, no current will flow. Also, as in the vacuum tube, load characteristics are not reflected to the input circuit, because current is not controlled by carrier injection as in bipolars, but by voltage levels.

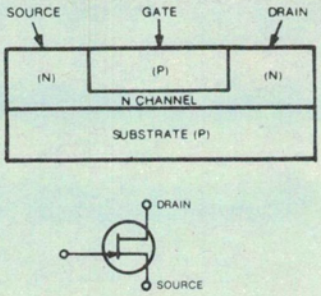


Fig 8. N-channel JFET construction and symbol.

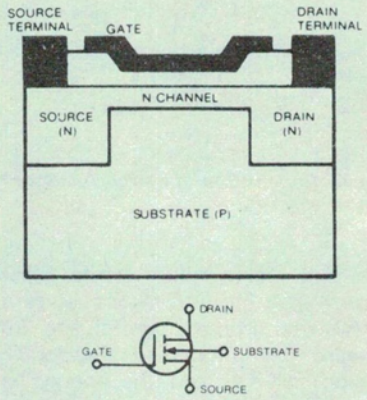


Fig 9a. N-channel depletion horizontal MOSFET construction and symbol.

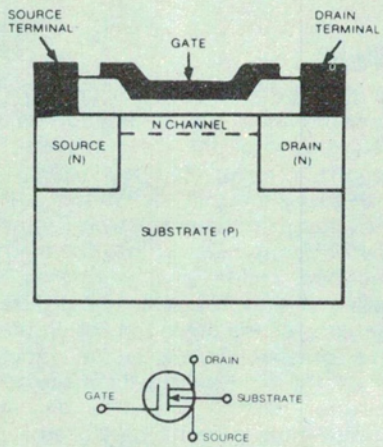


Fig 9B. N-channel enhancement horizontal MOSFET construction and symbol.

A variation is the Metal Oxide Semiconductor Field Effect Transistor. (MOSFET) (Fig. 9) a far more versatile device whose technology is virtually the cornerstone of modern computer technology, although it has had less use to date in linear applications such as audio amplification.

MOSFETS come in two basic types. In both the gate consists of a metal electrode separated from the channel by a thin oxide layer. In the depletion type current flow is controlled by the electrostatic field of the gate when biased. When a depletion MOSFET is so biased the device may be driven on both sides of the zero volts point as with vacuum tubes. Unlike vacuum tubes, under these conditions, the gate draws no current, therefore does not require the driver to deliver power.

The enhancement type MOSFET shown in Figure 9b, is more widely used. The source and drain are separated by a substrate of opposite material, and under zero gate volts no current flows. However, when sufficient forward bias is applied to the gate the region under the gate changes to its opposite type (e.g. p-type becomes n-type) and provides a conductive channel between drain and source. Carrier level, and conduction is controlled by the magnitude of gate voltage.

Although MOSFETS are handy devices they are not capable of handling high power levels. The channel depth available for conduction is limited by the practical limits on gate voltage. The lower current density has been the primary limitation due to the horizontal current flow.

VFETS

Recent years have seen the introduction and commercial use of Vertical Channel J-FETS, notably by Sony and Yamaha (Fig. 10). The vertical channel permits a very high width-length ratio, permitting a decreased inherent channel resistance and high current density. Unfortunately it suffers the same disadvantages as the small signal J-FET, plus, in currently available devices, a very high input capacitance, ranging from 700 pF to around 3000 pF, limiting high frequency response. In addition, since they must be biased into the off condition, bias must be applied before supply voltage and removed after the supply if it is to be operated anywhere near its maximum ratings. This problem doesn't exist with vacuum tubes because of heater warm-up time, although some

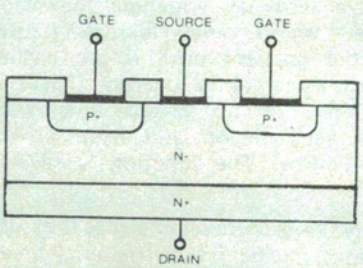


Fig 10. Vertical junction FET construction.

"instant-on" circuits impose heavy turn-on surges.

This necessitates a complex power supply, and Yamaha, for example, uses more devices in the supply than it does in its amplifier circuits. However, the construction does make possible the design of complementary types and both Nippon Electric and Sony have high power devices available.

However, the Vertical MOSFETS by Siliconix are readily available, at reasonable prices, and the manufacturer most generous in providing data. The following information is extracted from their application note AN76-3, Design Aid DA 76-1, plus device data sheets.

The device

Notice in Figure 11, that the substrate and body are opposite type materials separated by an epi layer (similar to high speed bi-polars). The purpose of this structure is to absorb the depletion region from the drain-body junction thus increasing the drain-source breakdown voltage. An alternative would have involved an unacceptable trade-off between increasing the substrate-body depth to increase breakdown voltage (but increasing current path resistance)

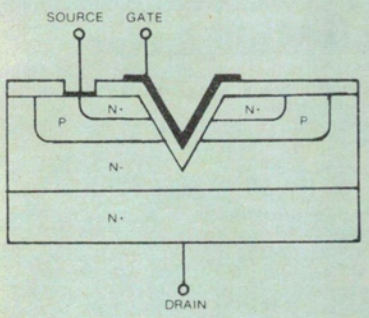


Fig 11. Vertical MOSFET construction (Siliconix).

and lengthening the channel. In addition, feedback capacitance is reduced by having the gate overlap n-epi material instead of n+.

In manufacture, the substrate-drain and epi layer are grown, then the p-body and n+ source diffused into the epi layer, in a simiar manner as the base and emitter of a diffusion type transistor. A V groove is etched through the device and into the epi layer, an oxide layer grown, then etched away to provide for the source contact and an aluminium gate deposited. This type of device allows current flow in one direction only; this is not always so with a similar type of horizontal FET, where source and drain may be identical in structure and of the same material. Therefore, no reverse current flows (we hope) when used in switching applications, as was also the case with vacuum tubes.

In-circuit operation is refreshingly simple: Supply voltage is applied between source and drain, with the drain positive with respect to the source, under which conditions no current flows, and the device is off. This is an enhancement type device, and is turned on by taking the gate positive with respect to the source and body. The electric field induces an n channel on both surfaces of the body facing the gate, and allows electrons to flow from the negative source through the induced channel and epi and through the substrate-drain. The magnitude of current flow is controlled almost entirely by the gate voltage, as seen in the family of curves (Fig. 12) with no change resulting from supply voltage changes above 10 V.

Advantages

The vertical structure results in several advantages over horizontal MOSFETS.
1) Since diffusion depths are controllable to close tolerances, channel length, which is determined by diffusion depth, is precisely controlled. Thus, width/length ratio of the channel, which determines current density, can be made quite large. For example, the VMP1 channel length of about 1.5 μ, as against a minimum of 5 μ in horizontal MOSFETS, due to the lower degree of control of the shadow masking and etching techniques used in such devices.
2) In effect, two parallel devices are formed, with a channel on either side of the V groove, thus doubling current density.
3) Drain metal runs are not required when the substrate forms the drain contact, resulting in reduced chip area, and thus reduced saturation resistance.
4) High current density results in low chip capacitance. Also, unlike horizontal MOSFETS, there is no need to provide extra drain gate overlap to allow for shadow mask inaccuracies, so feedback capacitance is minimized.

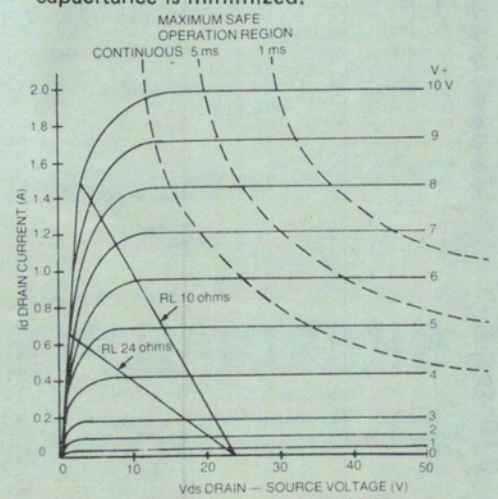


Fig 12a. Output characteristics VMP1.

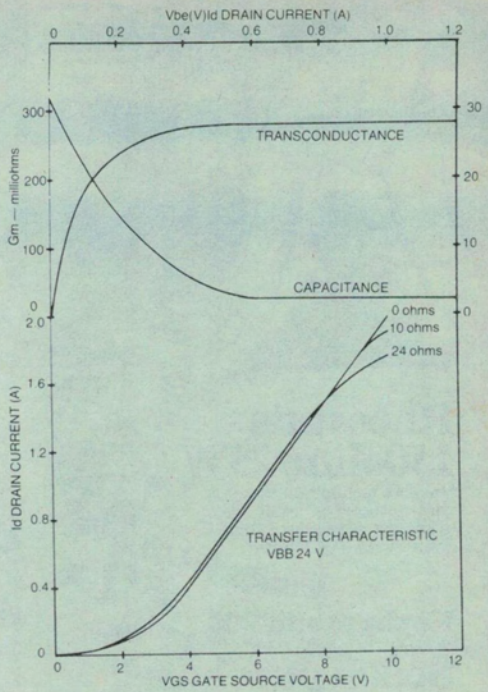


Fig 12b. Other VMP1 characteristics.

In comparison with bi-polars, especially power devices, the advantages are even more impressive.
1) Input impedance is very high, comparable to vacuum tubes, since it is a voltage controlled device, with no base circuit drawing current from the driver stage. A 7 V swing at the gate, at virtually 0A, represents almost 0W of power, but can produce a swing of 1.8 A in output current. This represents considerable power gain and will interface directly with high impedance voltage drivers.
2) There is no minority carrier storage time, no injection, extraction, recombination of carriers, resulting in very fast switching and no switching transient in class B and AB amplifiers. Switching time for a VMP1 is 4 ns for 1 A, easily 10-200 times faster than bi-polars, and rivalling many vacuum tubes.
3) No secondary breakdown, and no thermal runaway. VMOS devices exhibit a negative temperature coefficient with respect to current, since there is no carrier recombination activity to be speeded up with temperature. Thus, as current increases so does temperature, but the temperature rise reduces current flow. It is still possible to destroy the device by exceeding its maximum ratings, but a brief near-overload does not result in an uncontrollable runaway condition. Usually, simple fusing and/or thermistor protection is sufficient for maximum safety, and even this may be unnecessary with conservative design. Absence of secondary breakdown means that full dissipation can be realized even at higher supply voltages. In this respect they resemble vacuum tubes.

VFETS for everyone — Part II

In the first part of this article we examined the structure and features of a new type of semiconductor, the vertical channel power metal oxide semiconductor, Vertical MOSFET, or V-MOS, introduced by Siliconix. The second part of the article covers the actual use of V-MOS.

Wally Parsons

V-MOS POWER FETS like signal MOSFETS, may be used to perform many different functions. However, no matter what the circuit, certain conditions, common to all applications, must be provided. These are supply power, loading, drive signal, and establishment of appropriate operating points.

The electrical characteristics of the VMP1, VMP11, and VMP12, are shown in Fig. 1, and Fig. 2 shows them in graphic form. Since these are unidirectional devices, the source and drain are not interchangeable, and as they are n-channel devices conduction can occur only if the drain is positive with respect to the source, and high enough to ensure operation in the linear region — as with a vacuum tube, bi-polar transistor, or signal FET.

Like the vacuum tube, the absence of secondary breakdown allows full dissipation at any voltage supply up to maximum voltage and current ratings. Thus, where two different designs require the same dissipation but different voltage/load current, no derating is required. This is shown in the "safe operating area" curves. The only bi-polar transistor possessing this characteristic is the single-diffused type, which is also the least suitable for any application requiring wide bandwidth and/or high speed.

This characteristic also simplifies the establishment of suitable load-lines allowing greater safety margin in driving reactive loads where the load-line may be elliptical to the point of leaving the safe-operating area. Designers accustomed to using high voltage high dissipation devices to assure adequate safety margins at relatively low power levels need not therefore be too disconcerted at the 25 watt rating of these devices.

A 10 watt class A amplifier suitable for driving a tweeter in a bi-amped speaker system, for example, need not suffer excessive dissipation except perhaps with an electrostatic unit where such a power level would be inadequate anyway, unless it were operating at a very high cross-over frequency.

Output

These devices may use any of the types of output circuits in general use with tubes and bi-polars, including transformer coupled (Fig. 12) where the benefits of the absence of charge carrier storage become apparent in the absence of severe ringing at the cross-over point, conventional series output such as in Fig. 3, which is a straightforward transformation from a bi-polar

Fig. 2 Typical VMP1 performance curves (Siliconix).

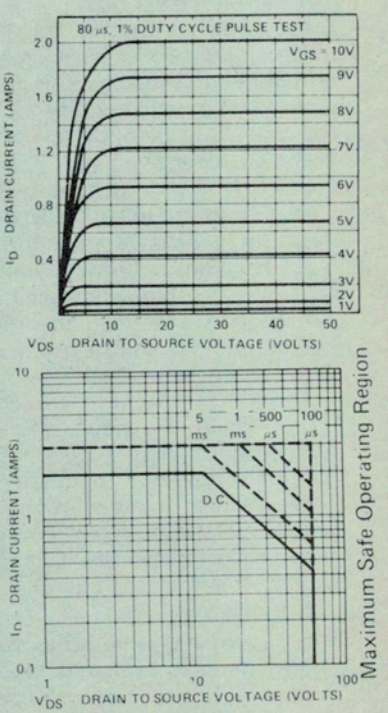


Fig. 1 Electrical characteristics of the VMP devices (Siliconix).

		Characteristics		VMP 11			VMP 1			VMP 12			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0; I_D = 100 μA
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{GS} = V_{DS}; I_D = 1 mA
3	STATIC	I_{GSS}	Gate-Body Leakage			0.5			0.5			0.5	μA	V_{GS} = 15 V; V_{DS} = 0
4	STATIC	$I_{D(off)}$	Drain Cutoff Current			0.5			0.5			0.5	μA	V_{GS} = 0; V_{DS} = 24 V
5	STATIC	$I_{D(on)}$	Drain ON Current*	1	2.0		1	2.0		1	2.0		A	V_{DS} = 24 V; V_{GS} = 10 V
6	STATIC	$I_{D(on)}$	Drain ON Current*	0.5			0.5			0.3			A	V_{DS} = 24 V; V_{GS} = 5 V
7	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		2.0	2.5		3.0	3.5		3.7	4.5	Ω	V_{GS} = 5 V; I_D = 0.1 A
8	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		2.4	3.0		3.3	4.0		4.6	5.5	Ω	V_{GS} = 5 V; I_D = 0.3 A
9	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		1.2	1.5		1.9	2.5		2.6	3.2	Ω	V_{GS} = 10 V; I_D = 0.5 A
10	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		1.4	1.8		2.2	3.0		3.4	4.0	Ω	V_{GS} = 10 V; I_D = 1 A
11	DYNAMIC	g_m	Forward Transconductance*	200	270		200	270		170			mΩ	V_{DS} = 24 V; I_D = 0.5 A
12	DYNAMIC	C_{iss}	Input Capacitance		48			48			48		pF	V_{GS} = 0; V_{DS} = 24 V f = 1 MHz
13	DYNAMIC	C_{rss}	Reverse Transfer Capacitance		7			7			7		pF	V_{GS} = 0; V_{DS} = 24 V f = 1 MHz
14	DYNAMIC	C_{oss}	Common Source Output Capacitance		33			33			33		pF	V_{GS} = 0; V_{DS} = 24 V f = 1 MHz
15	DYNAMIC	t_{ON}	Turn ON Time**		4	10		4	10		4	10	ns	See Switching Time Test Circuit
16	DYNAMIC	t_{OFF}	Turn OFF Time**		4	10		4	10		4	10	ns	See Switching Time Test Circuit
														VMC

*Pulse Test **Sample Test
Pulse Test Pulse Width = 80 μsec, Duty Cycle = 1%

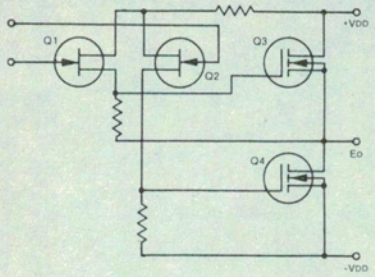


Fig. 3 Series output arrangement

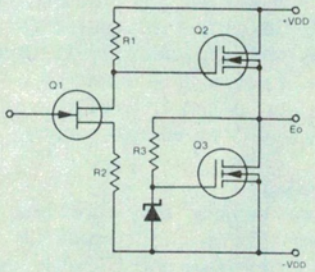


Fig. 4 Single ended output with current source.

circuit (1), and single-ended output with current source, also transposed from an excellent bi-polar circuit (2) (Fig. 4).

Bias and drive

These series of devices are n-channel, enhancement type MOSFETS, and may be biased and driven using methods appropriate to signal types and bi-polars. The drain is made positive with respect to the source and the gate enables conduction by being forward biased with respect to the source, that is to say it is biased in a positive direction. Unlike bi-polars, however, they are voltage, rather than current controlled, and circuit values are selected to provide the required voltage. Any current drawn is by the bias network itself.

Three bias methods are shown in Fig. 5. Figure 5a shows bias supplied from a fixed bias supply. It is the simplest possible method, allows extremely high input impedances since Rg may be almost any very high value desired, and its stability is limited only by the stability of the bias supply.

The design shown in Fig. 5b has the advantage of requiring no extra supply voltage since it is taken from Vdd. Disadvantages are low impedance and stability. Input impedance consists of the parallel combination of R1 and R2 (disregarding input capacitance of the MOSFET and the very low input leakage.) There are practical limits as to how high this combination can become; if for example, we have a 60 volt supply and require 6 volts bias, we might have some difficulty obtaining higher values than 9 megohms and one megohm for R1 and R2.

Higher values become more difficult to obtain, stability becomes less reliable, internal inductance and distributed capacitance become problems, and overcoming these difficulties usually costs money. In addition, if Vdd is subject to variation, then bias varies. In a class AB amplifier this could be quite serious, since Vdd varies considerably with output level; at high levels, Vdd can be expected to drop, causing a reduction in bias.

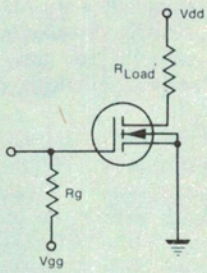


Fig. 5a. Hi-Z separate bias supply.

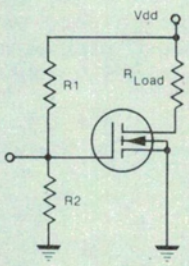


Fig. 5b. Moderate impedance supply.

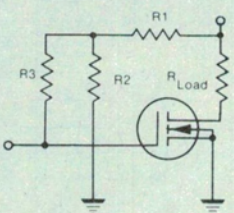


Fig. 5c. Hi-Z common supply.

While this may reduce the danger of over-driving the device, it will be forced to operate in its non-linear region which may result in unacceptable performance characteristics unless taken into consideration in the overall circuit design (e.g. choice of feedback values). It does provide some degree of overload protection, and with correct choice of values can provide for class AB operation at low levels, shifting to class B at high levels. With these considerations in mind, and/or where moderate impedances are required, it offers a low cost, simple, and reasonably reliable method of establishing the operating point.

The method used in Fig. 5c is similar except that with the addition of R3 higher input impedances are possible. Its configuration is similar to a noiseless biasing system frequently used in low-level bi-polar amplifiers and integrated circuits (e.g. National LM381A) but its function is somewhat different. Resistors R1 and R2 form a voltage divider as in Fig. 5b, but their junction now forms a fixed bias source as in Fig. 5a. Resistor R3 can be quite high since no current flows. Meanwhile, since the parallel combination of R1 and R2 are effectively in series with R3 they can be reduced to more manageable values. Alternatively R2 can be replaced by Zener diode for stability comparable to Fig. 5a.

Input protection

Unlike most signal MOSFETS, the gate of each of these devices, with the exception of the VMP4, is protected with an internal 15 volt, 10 mA zener diode. Most signal MOSFETS, as well as the VMP 4, are unprotected, or where extremely high impedances are not required, are protected by back to back zeners. I have no information as to why this different technique is used.

This different technique is used, but it is obvious that a negative signal swing on the gate will result in forward current through the zener. If the device is to be driven beyond cutoff, the driver must be capable of delivering current during its negative swing. Alternatively, a constant current source can be used, a series limiting resistor or a driver biased to the same class of operation as the V-MOS FET.

A constant current source (we'll examine an example of its use a little later) will limit current drive to the value of the constant current diode used; a series resistance will drop the drive voltage as the diode draws current. In both cases, diode current must be limited to 10 ma maximum. Higher currents will damage the protective zener diode.

In amplifier applications, a class A driver is commonly used. However, if a class B output is used, conduction only occurs during positive half-cycles. Therefore drive signal is not required during negative half-cycles. If a source or

emitter follower driver stage is biased so as to pass no negative drive, the problem does not occur. However, great care must be exercised in the design of such a stage to ensure that drive does not disappear before the output device is cut off.

This is not too difficult with a class B or near class B stage; If the output device is operated at zero bias, then a small amount of bias on the driver will ensure conduction during slightly more than 180 degrees. Class AB operation is a little more tricky. If conduction is to occur for 270 degrees, for example, the driver should conduct for slightly more than this period.

Two types of drive circuits familiar to designers of bi-polar circuits are the Darlington and super beta, commonly used together to provide a quasi-complementary circuit. Both circuits are current amplifiers designed to provide a compound device with very high hfe and provide base current to the output device. However, similar circuits can be used with these devices to provide phase inversion in a series output stage.

Thermal considerations

As described earlier (Part 1) these devices exhibit a negative temperature coefficient with respect to current, so that as temperature rises, current is reduced, thus providing a self-inhibiting action which provides some protection against overload. However, this is not an unconditional effect Fig. 6 shows the relationship between RDS(on) and temperature (3), based on a worst case temperature coefficient of 0.7 per cent per degree C.

Suppose that the device when 'on' passes a current of 1 amp which causes it to heat up. The 'on' resistance increases (which is why current drops), increasing the voltage drop across the device and the device dissipation. Now, if adequate heat sinking is used there is no real problem but if it isn't, the 'on' resistance and junction temperature will rise to the point where extra charge carriers are generated, thus stabilizing

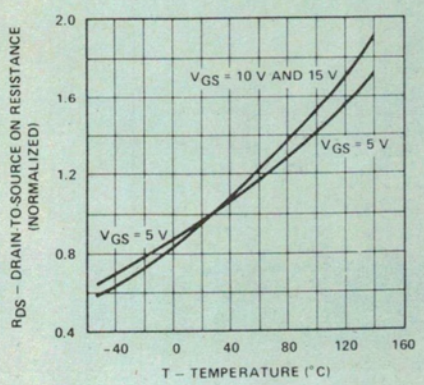


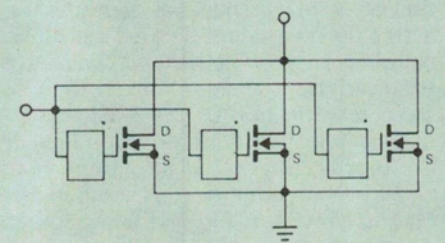
Fig. 6 Drain to source resistance against temperature (Siliconix).

RDS(on). That's great, except for the fact that this doesn't occur until the maximum safe junction temperature of 150 degrees has been exceeded.

You'll remember that we said earlier that the device was free of thermal runaway problems because of its negative temperature coefficient, but it isn't free of thermal destruction problems, and in any case, excessive temperatures will reduce output conductance. Heat-sinking requirements are, therefore, similar to those of bi-polars. The calculations of thermal operating conditions are beyond the scope of this article, but interested readers are referred to the Siliconix literature listed in the references, (4).

Extending the ratings

The current handling and therefore total dissipation capability may be increased by simply connecting several devices in parallel (Fig. 7). No ballast resistors are needed to ensure proper current sharing since if one device draws more current than another it simply gets a little warmer which causes it to draw less (assuming adequate heat sinking, of



*TO PREVENT SPURIOUS OSCILLATIONS, A 500 Ω 1K Ω RESISTOR OR FERRITE BEAD (FOR HIGHER SPEED) SHOULD BE CONNECTED IN SERIES WITH EACH GATE.

Fig. 7 Basic circuit for parallel operation (Siliconix).

course). The only major precaution needed is to keep lead inductance in the gate and source connections to a minimum to prevent parasitic oscillations, unless the devices are driven from a low impedance source.

It may be advisable to insert what the British call "stoppers" – small resistors (100 to 1000 ohms) in series with each gate, wired directly to the socket, or ferrite beads mounted on the leads close to the socket terminals. An additional plus when paralleling several devices is that the gm is multiplied by the number of devices used. Mutual conductance gm is specified as the ratio of a large change in current to a small change in control voltage. If, for example, a change of 0.4 volts on the gate produces a change of 0.1 amp through one device, connecting two devices in parallel will give us an output swing of 0.2 amps, but it will still require only the original 0.4

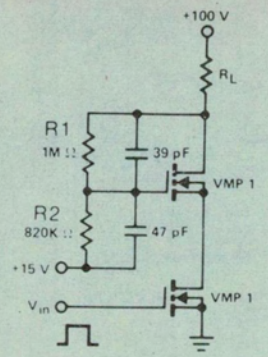


Fig. 8 Diagram for series operation (Siliconix).

volts gate swing. Since voltage gain A=gm x RL, if gm is increased, A is increased.

In real use, of course, the internal resistance of two devices in parallel is less than of one, the optimum load is less, so in amplifier applications, the net amplification A is the same. But notice that the drive requirements have not changed. With bi-polars current would have to be supplied to each base, thus increasing the output requirements of the drivers. Indeed, with many high-power amplifiers using multiple output devices the drivers are also power devices.

We can also extend the voltage ratings by series operation of two or more devices Fig. 8 shows the technique. Resistors R1 and R2 bias Q2 'on', while C1 and C2 ensure fast switching. The input control signal is inserted between gate and source of Q1. Ordinarily the bottom of the divider chain is at ground potential for signal frequencies, so that circuit is really a cascade.

Maximum current and gm are the same for one device.

Practical applications

An efficient light dimmer circuit as proposed by Siliconix is shown in Fig. 9. The 4011 acts as a pulse width modulated oscillator whose duty cycle is determined by the ratio of R1 to R2, with R2 adjusted to control the brightness of the W-90 bulb. Of special interest here is the fact that with its fast switching time, the VMP1 is especially suited to pulse width modulation at power levels and suggests it as being suitable for use in switching, or class D linear amplifiers.

A DC to DC converter is outlined in Fig. 10. The VMP1s form an oscillator with positive feedback provided by the additional coil in the gate circuits. In operation the upper V-MOSFET is biased 'on', and the lower V-MOSFET

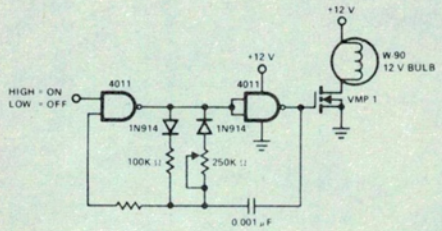


Fig. 9 Circuit of a high efficiency light dimmer (Siliconix).

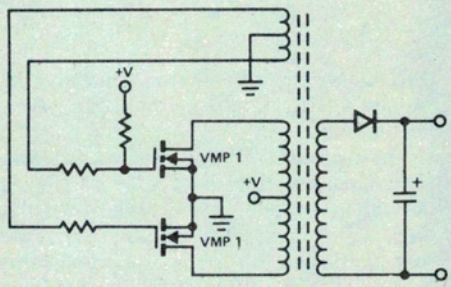


Fig. 10 A d.c. to d.c. converter (Siliconix).

is 'off'. When power is applied the upper device conducts causing current to flow from Vdd through the upper half of the transformer primary and the upper V-MOSFET to ground. The induced current flow through the feedback coil develops a voltage such as to shift the bias in the upper device 'off' (if the winding is connected with the correct polarity) and the lower device 'on'. This causes current flow from Vdd through the lower half of the transformer primary and the lower V-MOSFET to ground.

The secondary circuit consists of a single rectifier and filter. The resistor in the upper gate prevents shorting out gate bias, and the one in the lower gate keeps both sides balanced. In addition, each resistor limits current through the protective diodes. These are expensive devices for such an application, but the high reliability, the reduced rf radiation (due to reduced switching transients) and the circuit simplicity easily make up for the cost. The very high circuit impedance enables running frequency to be set by the self-resonance of the transformer.

Single-ended push-pull transformer coupled audio amplifiers are shown in Figs. 11 and 12. Both utilize the biasing system described in Fig. 5b. A load-line drawn on the output characteristic will show the optimum load to be 24 ohms. In Fig. 11 gate drive is supplied by a single junction FET, and voltage feedback is taken from the output transformer secondary and series fed to the source of the input device. Distortion is under 2% at full output (try to get that with a single ended tube or bi-polar) and could probably be reduced even further by adopting a source follower output stage.

A push-pull version of Fig. 11 is shown in Fig. 12 using a differential input to provide phase splitting, drive, and a feedback point. Although the transformer winding ratio implies the use of a low impedance loudspeaker, a step-up ratio could be used for direct coupling to an electrostatic speaker, a balanced transmission line (both with some modification of the feedback circuit) an unbalanced transmission line, or a 70 volt speaker distribution line.

Notice in both circuits, and in the biasing circuits of Fig. 5, that no source resistors have been used, either for local feedback or for bias setting. In tube and bi-polar circuits it's a useful technique, and with bi-polars can be used to stabilize bias and control thermal runaway by using the increased current flow to increase the voltage drop, thus reducing base-emitter voltage. However, if used with these devices, it will actually impair the self-limiting action of its negative temperature co-efficient. If temperature rises due to high current, current flow is reduced. This would reduce the voltage drop across a source resistor, lowering the source voltage and increasing the gate-to-source voltage, causing an increase in current flow. The circuit would work great while it lasted – which wouldn't be for long.

Record amp

Figure 13 shows a magnetic recording amplifier derived from a tube circuit. Its biggest advantage lies in its ability to provide equalization for head losses by incorporating the head within the feedback loop. Additional equalization is then required only for gap losses and tape self-demagnetization. Q1 acts as a driver for Q2, the output stage, which, with series resistor R9, provides a high impedance current source for the record head, as well as providing a mixing pad between audio and bias currents.

The record head's return path to ground is through R11. The inductance of the record head results in an impedance characteristic which rises with frequency. At frequencies at which the impedance of the head is low in comparison with R9 and R10 in series, load current is essentially constant. As frequency rises, however, head impedance becomes appreciable. With appropriate selection of R9 and R11, depending on head characteristics, the voltage across R11 decreases as the head impedance becomes significant. If feedback is taken across R11 it will decrease with rising frequency, causing an increase in gain, at a rate of 6dB/octave.

Feedback is applied across R3 via R10 and C8 (which supplies bass boost below 80 Hz) C5 and C6 provide additional high frequency boost for a total ultimate slope of 12 dB/octave. This circuit is so effective that no additional boost is needed at 15 ips, and only a small amount at 7.5 ips with high coercivity tape.

The biasing method used is that of Fig. 5c. The large amount of local current feedback provided by R2 and R3 results in a high output impedance

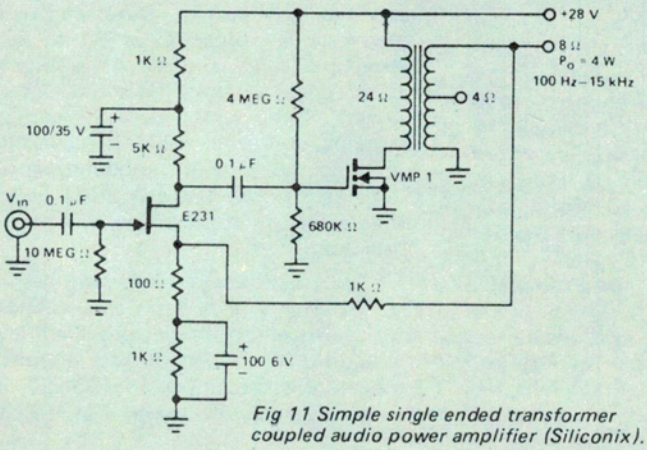


Fig 11 Simple single ended transformer coupled audio power amplifier (Siliconix).

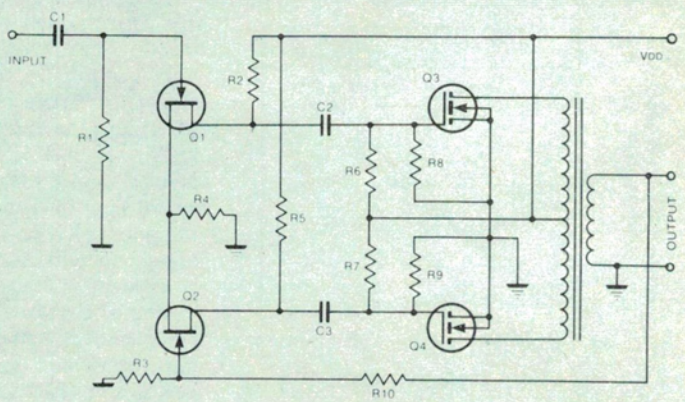


Fig. 12 Transformer coupled output.

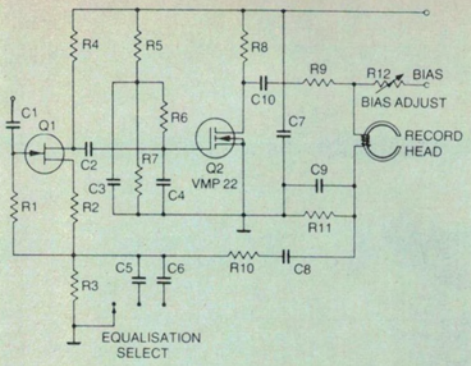


Fig. 13 Tape recording amplifier.

for Q1, so the biasing network is selected to provide high impedance with reasonable values. Capacitors C3, C4, C7 and C9 bypass bias signal to avoid overloading Q2, and to prevent attenuation of bias current.

Power amp

Figure 14 shows a high quality power amplifier designed by Siliconix Inc. (5) and described in their application notes. Output current capability is increased by using three VMP12's in parallel, providing for 6 amp current 75 watt dissipation and load optimized at 8 ohms. Q11-13 operate as a source follower, while Q8-10 form a quasi-source follower. This is accomplished by applying local feedback from drain to gate via R14, R15, and driving the gate by a modified current source. This consists of a cascade circuit with a constant current diode as the load.

For the benefit of those not familiar with these devices, a constant current diode is really a FET connected internally as shown in Fig. 15. Since current in a FET is controlled essentially by the gate-to-source voltage, changes in load or in applied drain-to-source voltage have negligible effect since gate-to-source voltage is held constant. This is a current analogue to the zener diode and is described in detail in Siliconix literature (6).

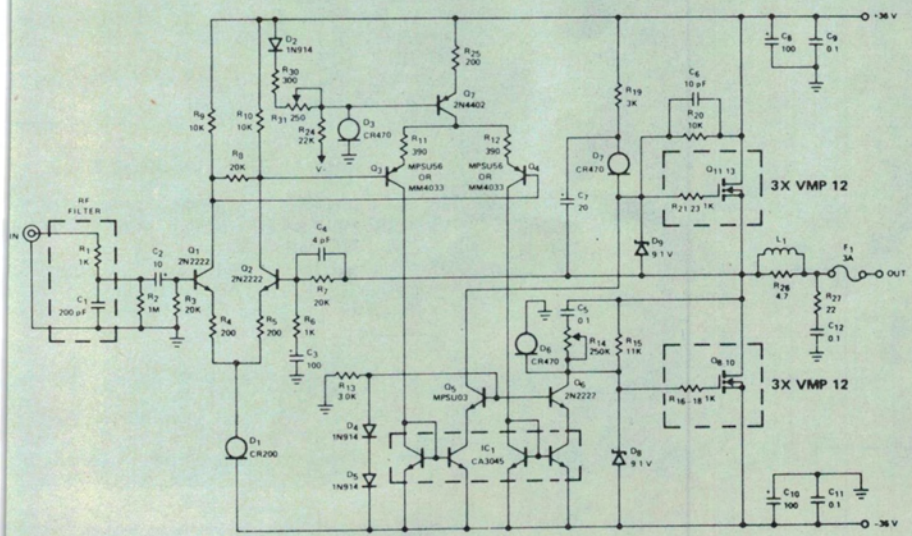
The design is push-pull from input to output, thanks to differential circuitry throughout, prior to the drivers. Open loop distortion is low, bandwidth wide, allowing satisfactory performance with only 22 dB of feedback. Lead compensation only is used (via C4), along with the liberal use of local feedback (R4, R5, R11, R12,). The result is very low transient IM and a slew rate of over 100 V/microsecond. THD is quite respectable even though the numbers might not impress the average audiophile accustomed to amplifiers with great specs and poor sound.

Incidentally, D8 and D9 illustrate an excellent method of providing output current limiting. In this case, 9.1 volt zener diodes limit drain current to slightly less than 2 amps. At first one might be tempted to depend on the built-in protection diodes to accomplish this, but it should be remembered that these devices are for protection against static discharge. Their zener voltage of 15 volts at 10 mA cannot possibly be used since the absolute maximum permissable drain current occurs at a gate-to-source voltage of 10 volts.

Commercial amps

A simplified version of Yamaha's B1 amplifier is shown in Fig. 16, (8). In this circuit a cascade drive system is used, but in a differential form with the constant current source in the

Fig. 14 A high quality 40W amplifier (Siliconix).



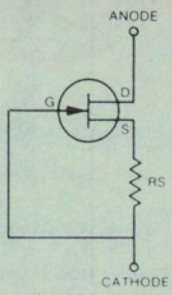


Fig. 15 A FET as a constant current diode.

common source circuit. This is an example of all FET design of excellent performance and received rave reviews in several publications including ETI. It's also inexpensive!

The VHF linear amplifier in Fig. 17 will deliver 5 watts peak envelope with second and third order intermodulation at -30 dB from 144-146 MHz. It will also prove useful as a receiver pre-amp with a noise figure of 2.4 dB. V-MOSFETS show considerable promise in rf applications because of their linear transfer characteristic, the high gain capabilities even with Ft somewhat above 600 MHz, low noise and (in receiver front ends) very wide dynamic range. Although this article has dwelt on the VMP 1 family, there is also the VMP 4, designed specifically for rf applications and which is now available.

Finally, how about something elegant for its simplicity, such as the tapered current voltage limiting battery charger shown in Fig. 18. This is especially useful with Ni-Cad batteries which are intended for stand-by use and are permanently on charge, such as electronic clocks. Overnight shut-downs of a few hours are occasionally but irregularly experienced. You know what this can do to clocks. Especially alarm clocks which are supposed to make noises, turn on radios, start the coffee at a pre-set time in the morning so you can go to work. Battery operation is not too satisfactory if the readout is on continuously, and Ni-Cads should not be on permanent floating charge.

With this little device current is supplied to the battery via the VMP-1. Gate voltage is set at a value equal to the desired end-of-charge voltage. As the battery charges, its voltage increases, reducing gate-to-source voltage, thus reducing charging current. When the battery reaches full charge its voltage, and that of the source, equals gate voltage, and charge is terminated. If a load is placed across the battery it will draw current, and as the battery voltage drops slightly below gate voltage, charging at a trickle rate occurs – automatically.

Experimentation

The various applications shown are intended as suggestions for further experimentation. They are mainly designed to illustrate various characteristics of the device under consideration, and are not necessarily representative of commercial practice or of finished designs. In some cases this may be just as well! But we would be delighted to hear of any readers' experience with any of these or other circuits.

The author's feeling is that V-MOS constitutes a genuine breakthrough in semi-conductor technology, as important as the silicon transistor and the FET itself. We'll be seeing more of these devices, with higher ratings (a 10 amp 200 volt unit is already under development) and specialized characteristics. They are said already to be in use commercially as magnetic core drivers.

Digital enthusiasts may be somewhat impatient with the strong emphasis on audio applications in this piece but other literature has placed great emphasis on digital applications, with little attention paid to linear techniques beyond the 40 watt amplifier described here. The serious reader in all areas is referred to the references at the end.

Have fun.

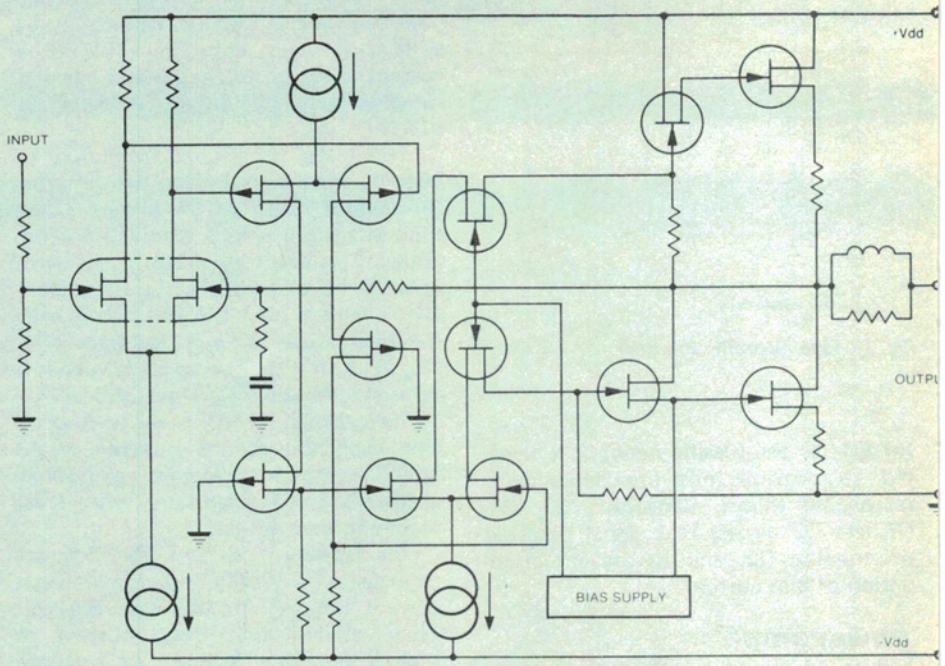


Fig. 16 Simplified Yamaha VFET amplifier diagram.

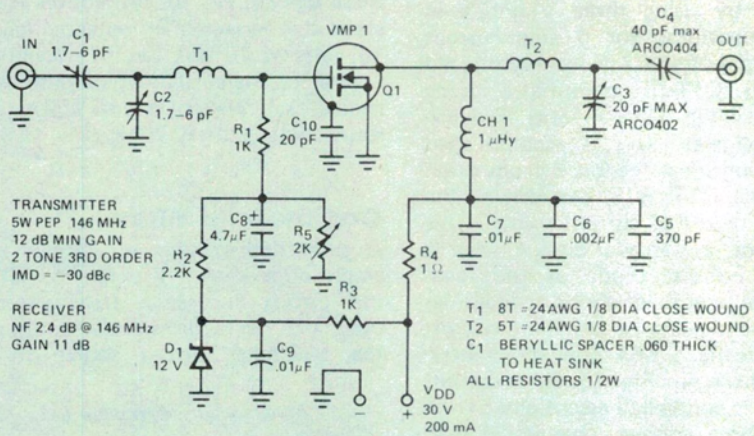


Fig. 17 144-146 MHz linear amplifier (Siliconix).

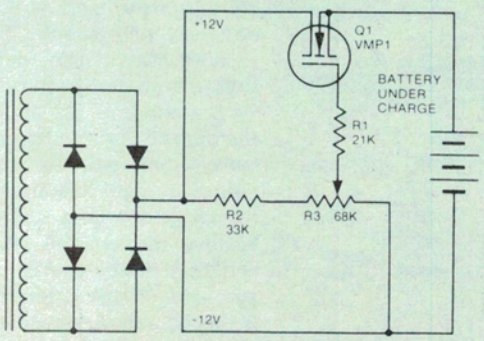


Fig. 18 Tapered current voltage limited battery charger.

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The junction FET — its haunts and habits

The first in a whole family of field effect transistors, the junction FET is found in many and varied applications. If you're new to electronics, or unfamiliar with the device, this article should introduce you to the haunts and habits of the JFET.

Brian Dance

THE JUNCTION Field Effect Transistor or JFET is a small electronic device much like a transistor in appearance which normally has three connections, although a fourth connection is attached to the metal case of some types for high frequency screening. Junction field effect transistors are one of the two main types of field effect transistor, the other type being known as the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) or as the IGFET (Insulated Gate Field Effect Transistor).

Field effect transistors can be used as amplifiers and oscillators as well as for other applications for which an ordinary or bipolar transistor could be employed, but have particular advantages for certain applications. Field effect transistors are also used in the internal circuitry of integrated circuits.

Connections

As in the case of npn and pnp bipolar transistors, junction field effect transistors can be obtained in two polarities, these being known as n-channel and p-channel types. A far wider variety of n-channel types is manufactured than p-channel devices, since they tend to have a better performance, but devices of both polarities are readily obtainable.

The electrodes and circuit symbols for the two types are shown in Figure 1. The current flowing in a channel between the drain and the source is controlled by a voltage applied to the gate electrode. The gate is therefore the input electrode and may be compared with the base of a conventional transistor. Similarly the drain and source may be compared with the collector and the emitter respectively.

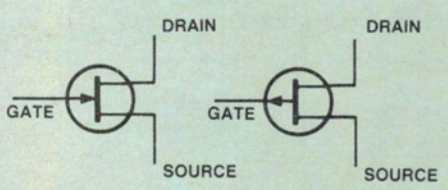


Figure 1. **Symbols for n-channel (a) and p-channel (b) junction FETs.**

One of the main differences between field effect transistors and bipolar transistors is that field effect transistors are essentially voltage amplifiers whereas bipolar transistors are basically current amplifiers. Thus the field effect transistor behaves more like the old thermionic valve in its circuits.

Field effect transistors tend to be more expensive than most of the common bipolar types — probably because the bipolar types are sold in much larger numbers. The economical 2N3819 n-channel field effect transistor is probably the most commonly used type and is very suitable for the readers who wish to carry out their first experiments with field effect transistors. This device is encapsulated in a black plastic or epoxy body and has the connections shown in Figure 2. The 2N3820 is a similar economical p-channel device.

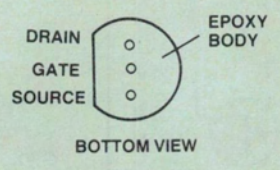


Figure 2. **Connections for the common 2N3819 plastic-encapsulated n-channel JFET.**

High input impedance

One of the main advantages of a field effect transistor is that it has a very high input resistance and therefore takes very little current from the circuit which feeds it — typically far less than a microamp. This means that it has very little effect on the circuit which feeds it, even if this circuit has such a high output impedance that it can deliver only a very minute current.

In order that an n-channel device shall operate correctly and have a high input impedance at its gate, it must be suitably biased with its gate negative with respect to the other electrodes. Similarly the gate of a p-channel device has a high impedance when it is positively biased.

APPLICATIONS

Pierce oscillator

In the circuit of Figure 3 the field effect transistor is employed in a Pierce type of oscillator whose frequency is controlled by the quartz crystal shown. The advantage of using a field effect transistor in this type of circuit is that the gate imposes only a very small load from the crystal and therefore the quality factor or Q factor of the crystal is not appreciably affected, so excellent frequency stability can be obtained.

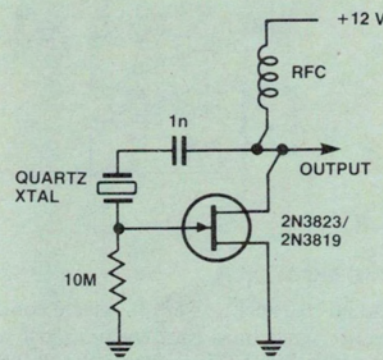


Figure 3. A Pierce crystal oscillator (National Semiconductor).

National Semiconductor recommend their 2N3823 n-channel device for use in this circuit, but the more economical 2N3819, which is made by the same type of process, is also suitable. The supply voltage is not at all critical, but the radio frequency chokes used in the supply lead should have a high impedance at the frequency of oscillation.

An advantage of this circuit is that one can change the crystal over quite a wide range of frequencies without making any other changes to the circuit and still obtain a satisfactory performance. The exact frequency range over

which the circuit will operate depends very much on the choke used and to some extent on the circuit layout.

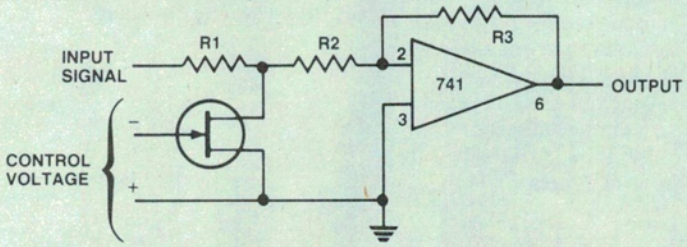
This type of circuit is suitable for use in a crystal calibrator for a receiver. If a 1 MHz crystal is employed, the output may be fed to a radio receiver to produce a signal at 1 MHz and at each multiple of 1 MHz up through the shortwave bands to provide calibration points.

Electronic attenuator

A junction field effect transistor can be used as a variable resistor, the value of which is controlled by the voltage applied to the gate electrode. As the applied bias becomes smaller, the resistance between the drain and source electrodes falls.

This property is used in the circuit of Figure 4 to design an electronic attenuator for audio signals. When the negative control voltage applied to the gate electrode is relatively large, little drain current passes through the device and the circuit behaves as if the field effect transistor were not present. However, as the control voltage falls at the gate electrode, the drain draws current from the junction of R1 and R2 so that the output signal amplitude is attenuated progressively.

Figure 4. **An electronic attenuator (Siliconix).**



Tone control

The circuit of Figure 5 is a tone control circuit with bass and treble boost and cut facilities. In this circuit the 2N3684 field effect transistor is used to enable the circuit to have a very high input impedance. It is used as a source follower circuit (analagous to an emitter follower) which provides a low output impedance signal coupled by a 1u capacitor to the tone control network. This network is in the feedback circuit of the LM301A operational amplifier circuit. The 2N3684 enables a good low-noise performance to be obtained.

Lambda oscillator

A very simple sinewave oscillator is shown in Figure 6; it is essential that one n-channel and one p-channel field effect transistor are used in this circuit. The two source electrodes are connected together and the gate of each device is connected to the drain electrode of the other device. This type of connection produces a negative resistance region in the current/voltage graph for the circuit with a peak in the graph like a Greek lambda (λ) — hence the name given to this type of circuit.

It is only necessary to connect the dual device circuit in series with a parallel tuned circuit, as shown in Figure 6, to produce oscillations at the resonant frequency of the tuned circuit used. It will oscillate at any frequency from the low audio region up to some tens of MHz, but the gate capacities of the devices used prevent operation in the regions above 100 MHz.

It is interesting to note that two separate parallel tuned circuits may be connected in series with the lambda circuit instead of the single tuned circuit shown in Figure 6. If one of these tuned circuits resonates at an audio frequency and the other at a radio frequency, the output will consist of an amplitude modulated radio frequency oscillation. This is perhaps one of the simplest possible modulated signal generators!

The output voltage from the circuit of Figure 6 is equal to twice the steady

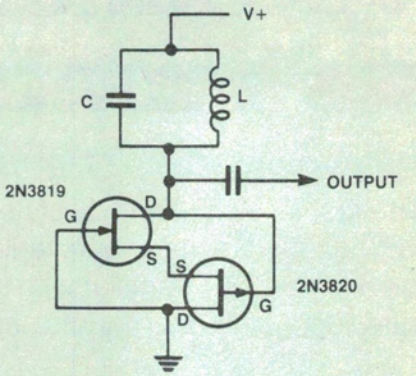


Figure 6. **Sinewave oscillator using a 'Lambda' circuit.**

power supply voltage applied to the circuit. Therefore this type of circuit can be very useful when one requires an output oscillation whose amplitude is accurately related to a steady applied voltage.

Complementary pairs of field effect transistors used in lambda circuits have other applications apart from simple oscillator uses.

High-impedance buffer stage

The circuit of Figure 7a shows a buffer or isolating amplifier which has a very high input impedance and low input capacitance. National Semiconductor recommend a 2N4416 field effect transistor for this circuit because it has a low input capacitance, but this is further reduced by the circuit feedback. The device is used as a source follower, so the voltage gain is about unity.

Although a 2N5139 pnp transistor is specified for this circuit, the 2N3906 plastic encapsulated type is much more readily available and is fabricated by the same process, so it can be used in this application.

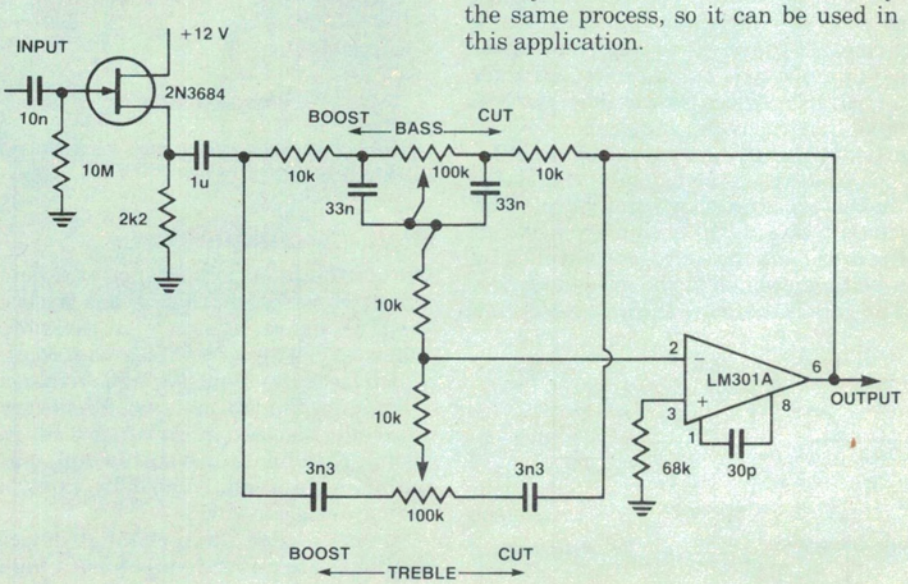


Figure 5. **High input impedance tone control circuit (National Semiconductor).**

High-impedance amplifier

The circuit of Figure 7b is very similar to that of Figure 7a except that the feedback circuit has been modified so that a voltage gain can be obtained. The circuit provides a gain of R2/R1 or 10 with the component values shown. Both the circuits of Figure 7 and of Figure 8 can be operated at high frequencies into the tens of MHz region.

RF amplifiers

Junction field effect transistors are much used in the radio frequency stages of HF, VHF and UHF receivers, since they offer a noise performance equivalent to that of bipolar transistors with improved crossmodulation and intermodulation performance. Crossmodulation is the transfer of the modulation of one carrier onto the carrier of another signal. Intermodulation occurs when two or more signals outside the passband combine in the circuit to form a signal within the passband which causes interference with the wanted signal.

The better linearity of field effect transistors over bipolar transistors is responsible for this improvement. Mullard have quoted a 12 dB improvement in crossmodulation in a narrow-band FM receiver and a 20 dB improvement in a VHF broadcast receiver as having been achieved by the replacement of a bipolar mixer circuit with a junction field effect transistor circuit.

Figure 8 shows a high-performance amplifier using two JFETs connected in 'cascode' (series) with automatic gain control (AGC) applied to the gate of the upper device. The supply is applied to the 'cold' or 'ground' end of L2 via a feedthrough capacitor. Only the L-C values need be changed to operate this stage on other frequencies to the limits of the JFETs.

Simple voltmeter

The high input impedance of a junction field effect transistor is used in the circuit of Figure 9 to produce a voltmeter with an input resistance of over 10M; in some measurements this high input impedance is necessary to prevent the current taken by a conventional voltmeter from dragging down the voltage being measured.

The input voltage being measured is divided by R1 and R2 so that a voltage of +0.2 V is present at the gate electrode when the full scale input voltage is applied for the range in question. In practice R1 should consist of a fixed resistor of a value somewhat less than that shown in the table, in series with a preset potentiometer so that the sensitivity of the range can be adjusted. If desired, R1 may be switched to provide a number of ranges.

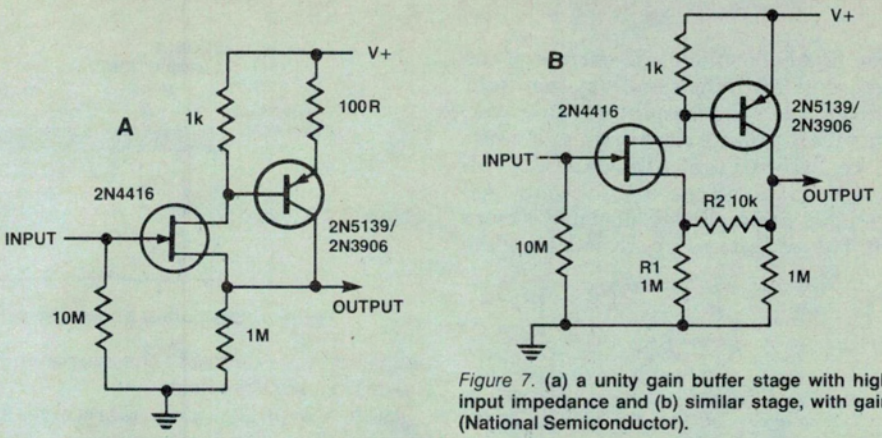


Figure 7. **(a) a unity gain buffer stage with high input impedance and (b) similar stage, with gain (National Semiconductor).**

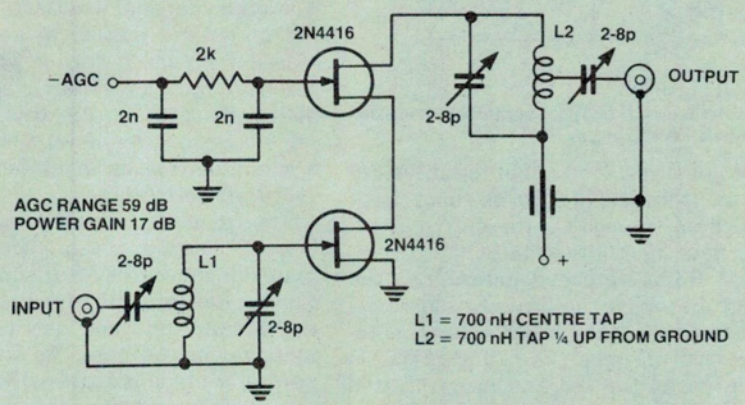


Figure 8. **Typical high-performance amplifier stage employing two FETs in 'cascode'. Values given for 200 MHz. A wide variety of RF FETs may be substituted (National Semiconductor).**

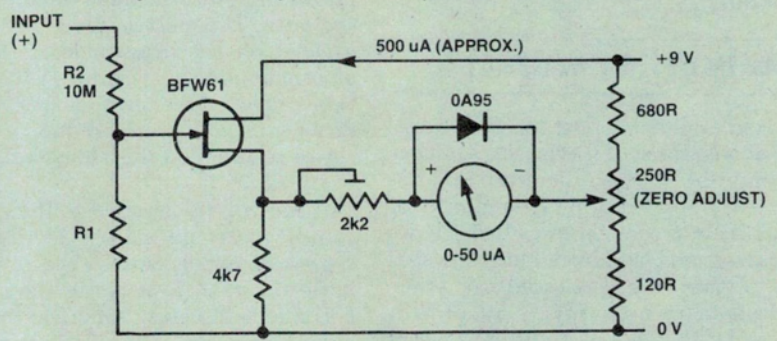


Figure 9. **High input impedance voltmeter. Note that a BFW10 could substitute for the BFW61 (Mullard).**

Table showing the value of R1 to be used in Figure 9 for various ranges.

Meter range	R1
250 mV	40M
500 mV	6M67
1 V	2M5
10 V	204k
50 V	40k
100 V	20k
250 V	8k
500 V	4k

the 2k2 resistor in series with the meter enables the full-scale meter current to be adjusted to allow for the characteristics of the particular device used. The diode protects the meter from overloading.

PhotoFET

Photosensitive field effect transistors (photoFETs) can be made which have a window or a lens, so that any light falling on this window affects the junc-

tion and hence the drain current of the device in much the same way that light affects a phototransistor. However, photoFETs are not very common devices.

An application of a Teledyne Crystallonics photoFET as a light-controlled variable attenuator is shown in Figure 10. The drain-to-source resistance of the

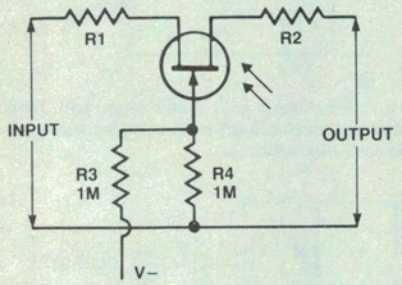


Figure 10. **Example of a light-controlled attenuator (Teledyne Crystallonics).**

photoFET is a function of the intensity of the illumination, so as more light shines on the device, the output rises. The negative voltage to which the resistor R3 is returned determines the range in which the drain-to-source resistance falls. Like other silicon photosensitive devices, the photoFET is sensitive to the red and near infrared regions of the spectrum, such as the radiation from an incandescent filament bulb.

HOW DO THEY WORK?

An n-channel field effect transistor consists of a channel of n-type semiconductor material between the drain and the source surrounded by p-type material of the gate electrode. Almost all of the devices are made of silicon, but a few special devices are produced in other semiconductor materials. As shown in Figure 11, the gate normally receives a

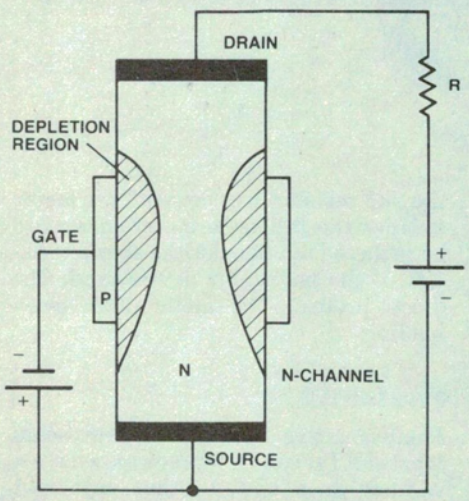


Figure 11. **Control of channel width in an n-channel device.**

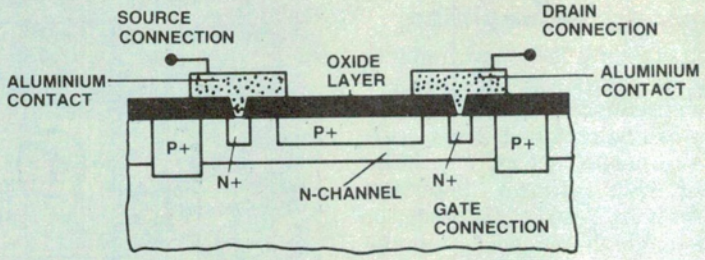


Figure 12. **Structure of a silicon planar device (Mullard).**

negative bias relative to the source and the drain a positive bias.

As the p-type gate material receives a negative bias, the junction formed between this material and the n-type channel is reverse biased. In any reverse-biased junction, a region which is depleted of charge carriers (electrons and holes) is formed. As this depletion region contains very few mobile charges, it acts almost as an insulator and has a very high resistance.

The gate is normally much more heavily doped than the channel material, since this results in the depletion region spreading fairly deeply into the channel and not very far into the material of the gate. As the drain is normally made positive with respect to the source electrode, the voltage between the drain and the negative gate is larger than that between the source and the gate. The electric field is therefore greater on the drain side of the gate electrode and this results in the depletion region becoming deeper on the drain side and thus producing a narrower channel on this side, as shown in Figure 11.

If the voltage applied to the gate becomes more negative, the depletion region goes deeper into the n-channel material until eventually the channel becomes completely cut off on the drain side of the gate. Very little drain current can then flow through the device. As the gate voltage becomes less negative, the channel opens again and becomes wider as the gate voltage approaches that of the source; the widening of the channel under the control of the gate voltage results in the channel current from the drain to source increasing.

As the gate-to-channel capacitance comprises a reverse-biased pn junction, the gate has a very high input resistance and passes only a very minute current (often in the pA region). However, the gate capacitance is appreciable and therefore an appreciable alternating current may flow to this electrode at high frequencies. Even when the gate and source potentials become equal, there is still a small depletion region and the gate input resistance is high. However, if the gate of an n-channel device receives a positive bias of more than about 0.65 V, current can flow in the gate circuit and this current may damage the device.

Structure

The design of a modern field effect transistor is not implemented in the form of Figure 11, which has been used for explanatory purposes, but silicon planar technology is usually employed to produce a structure such as that of the Mullard/Philips BFW11 shown in Figure 12. This has a surface or planar structure which is covered with a protective layer of silicon dioxide at all points except where electrode connections are attached. This oxide layer prevents impurities from contaminating the surface of the material and thus producing unwanted currents.

The aluminium contacts at the source and drain electrodes allow current to flow from them into the heavily doped small n+ regions, which make good contact with the n-channel region. In some devices a number of n-type channels are connected in parallel to enable a larger current to flow at the expense of an increased gate capacitance.

P-channel types

P-channel field effect transistors have the same type of structure as shown in Figures 11 and 12, but the p and n type materials are interchanged. The gate is made of n-type material and must therefore be biased positively, as shown in Figure 13. The drain is normally biased negatively.

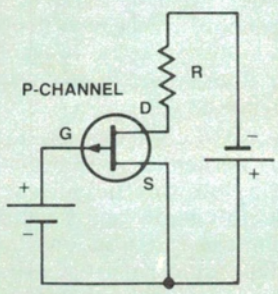


Figure 13. **A p-channel device requires supplies of the opposite polarity to those used with n-channel devices.**

Limiting voltages

If the bias applied to the gate is taken far beyond that required for normal operation, a point will eventually be reached at which reverse breakdown occurs. Similarly there is a limit to the voltage which should be applied between the drain and the source electrodes. However, junction devices cannot be damaged by the ordinary electrostatic charges which can accumulate on people and clothing and which can damage MOSFET devices.

Testing JFETS

It is relatively easy to check that a junction field effect transistor is able to function correctly. The circuit of Figure 14 may be used for an n-channel device and that of Figure 15 for a p-channel device.

If the gate is initially connected directly to the source (and not as shown), it will be found that the meter provides a reading of a few mA. This current is limited by the 1k resistor in the drain circuit to a safe value.

If the gate electrode is now connected to the 10M resistor as shown, the gate to channel junction is reverse biased. Thus the channel width decreases and with most devices the drain current will fall to zero in the circuits shown. As the gate circuit has a very high resistance, the voltage can be applied to it through a high-value resistor; indeed, it is interesting to note that the human body can be used in place of the 10M resistor shown when testing junction field effect devices.

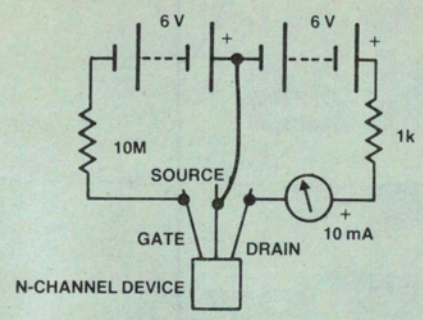


Figure 14. **Testing an n-channel device.**

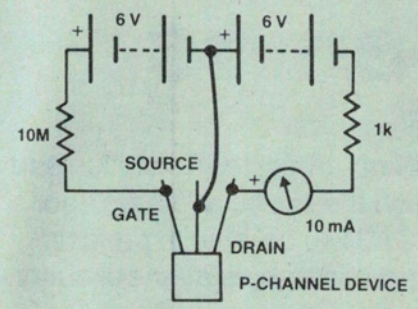


Figure 15. **Testing a p-channel device.**

If one wishes to test a device and does not know the connections, one can first find two connections in which a small current will pass in either direction. These are the source and drain connections.

A current should pass from the third electrode, the gate, only in one direction to either of the other two electrodes. If conduction takes place when the gate is positive, one has an n-channel device, whereas if conduction takes place when the gate is negative, the device is of the p-channel polarity.

One cannot easily determine which electrode is the drain and which is the source, but these electrodes are to some extent electrically interchangeable. ●

USEFUL BOOKS

Two very useful books, though difficult to obtain, are: 'FET Databook' from National Semiconductor and 'Field Effect Transistors' from Philips.