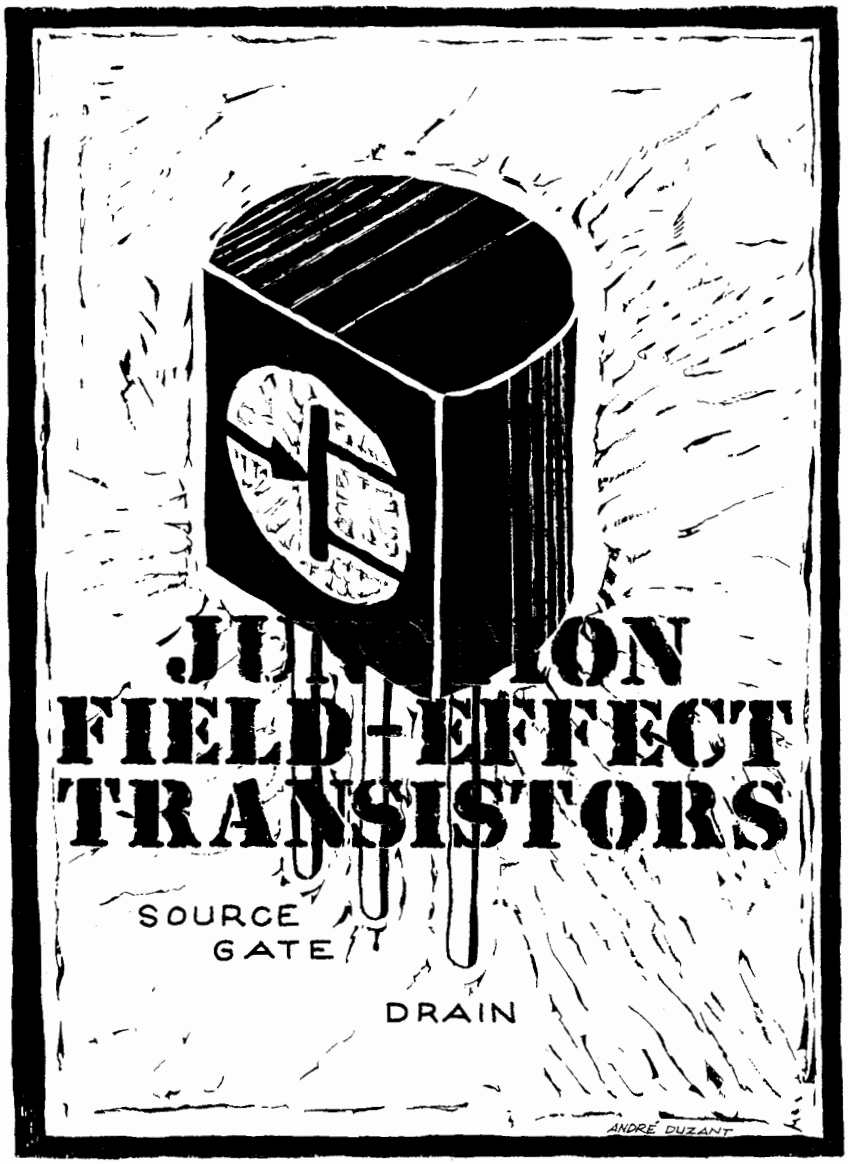

Learn how to bias junction FET's and apply them in practical amplifier, voltmeter, multivibrator, and converter circuits

RAY MARSTON

THE JUNCTION FIELD-EFFECT TRANsistor (JFET) has interesting characteristics that set it apart from the bipolar transistor. This article contains schematics for a selection of practical JFET circuits that range from amplifiers and analog voltmeters to a multivibrator and a DC- to AC-converter. Last month's article discussed the differences between JFET's and MOSFET's, and FET terms were defined.

You might want to read— or reread—last month's article before you tackle this one unless you are really "up to speed" on FET's, their operation, symbols and terms. The many combinations and permutations of N- and P-channel FET's operating in *enhancement* and *depletion* modes can be very confusing even for the experienced circuit designer.

The JFET reviewed

The subject of this article, the small-signal, general-purpose JFET, has the same terminals as other FET's: *source*, *drain* and *gate*. The JFET is a unipolar device whose operation depends only on the movement of majority carriers—electrons or holes—not both as in bipolar transistors. As a voltage-operated transistor, the appropriate voltage applied to the JFET's gate controls the flow of current between the drain and source.

Figure 1-a is a cross-section view of a modern diffused planar N-channel JFET showing its three terminals and three doped regions: *substrate*, *source-to-drain channel*, and *gate*. Figure 1-b is the schematic symbol for an N-channel JFET. The vertical bar represents the normally conductive channel region. (Symmetry within the JFET permits the source and drain terminals to be interchanged.)

Figure 2-a illustrates the structure of a P-channel JFET. It is made the same way as the N-channel JFET shown in Fig. 1-a except that N- and P- doped regions are interchanged. The schematic symbol for the P-channel JFET, shown in Fig. 2-b, has its arrow pointed away from the bar representing the channel.

All JFET's operate in the *depletion* mode. This means that maximum current flows in the source-to-drain channel when the gate bias is zero. To reduce (*deplete*) or entirely *pinchoff* that current, the gate must be reverse biased. In an N-channel JFET, a negative bias must be applied, while in a P-channel JFET, a positive bias must be applied.

Figure 3 is a family of drain characteristic curves for an N-channel JFET. Note that the amplitude of the drain current (I_D) decreases as gate bias (V_{GS}) becomes more negative from V_{GS} equals zero. The family of curves for a P-channel JFET are similar except that the bias val-

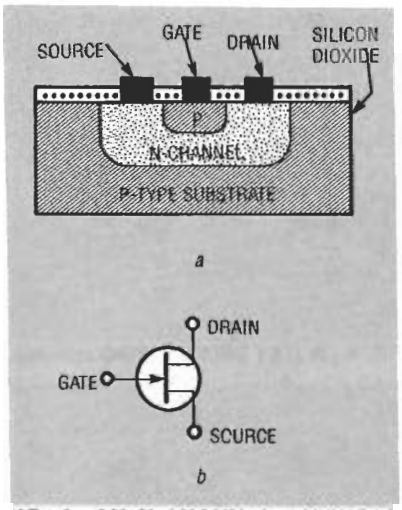

FIG. 1—AN N-CHANNEL DIFFUSED JFET (*a*), and schematic symbol (*b*).

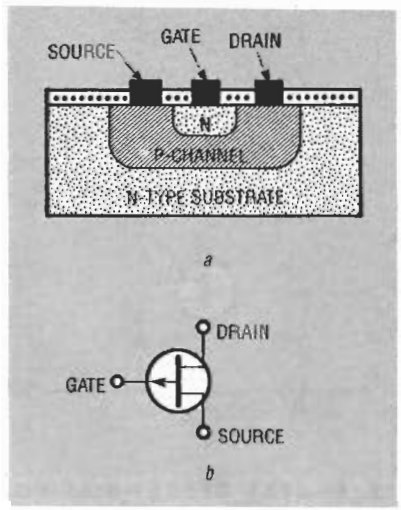

FIG. 2—A P-CHANNEL DIFFUSED JFET (*a*), and schematic symbol (*b*).

ues become more positive with decreasing drain current.

All of the schematics in this article are based on the classic 2N3819 N-channel JFET. First introduced more than 25 years ago, it is packaged in three-pin TO-92 plastic case. Table 1 gives the maximum ratings for this device at 25°C free-air temperature. If you want to build these circuits with an N-channel JFET other than the 2N3819, be sure that the substitute's electrical characteristics are closely matched to those of the 2N3819. Also, be sure that the pinout arrangements are similar.

Biasing the JFET

The JFET will work in digital as well as linear circuits. In a low-distortion analog amplifier, it must operated in its linear region by reverse biasing its gate relative to its source. There are three common JFET biasing techniques: *self-*, *offset-*, and *constant-current*.

Self-biasing is shown in Fig. 4. The JFET's gate is grounded through resistor R_G, and resistor R_S grounds the source. Any current flowing in R_S drives the source positive with respect to the gate, so the gate is effectively reverse-biased. If drain current (I_D) is to be set at 1 milliampere, and it is known that a gate-to-source bias voltage (V_{GS}) of -2.2 volts is needed, the correct value of source resistor (R_S) must be determined.

This correct bias can be obtained with a 2200-ohm value of resistor R_S. By Ohm's law, if 2.2 volts appears across a 2200-ohm source resistor, a 1 milliampere current will flow. If the drain current decreases, gate-to-source bias voltage also decreases. This causes drain current to increase and counter the original change. Thus, the bias is self-regulating through negative feedback.

The value of gate-source bias needed to set a desired drain current can vary widely even among identical JFET's in actual circuits. Thus, the only sure way to set a precise drain current is to pick a source resistor by trial and error or use a potentiometer. Regardless of how it is obtained, self-biasing is satisfactory for most practical applications, and only a few external components are needed. That's why it is still the most popular way to bias a JFET.

The second scheme, *offset-biasing* is illustrated in Fig. 5-a. It gives more accurate gate biasing than self-biasing. Here, the voltage at the junction of resistors R1 and R2 is applied as a fixed positive bias to the gate through gate resistor R_G. The voltage at the source equals this bias voltage minus the negative value of the gate-source bias.

Therefore, if positive gate voltage is large with respect to gate-source bias, drain current is controlled mainly by R_S and gate-voltage; it is not greatly influenced by variations of gate-source bias between individual JFET's. Offset biasing permits drain current to be set accurately, avoiding the chore of individual resistor selection. Similar results can be obtained by grounding the gate and coupling the low-end of the source resistor to a high negative voltage, as shown in Fig. 5-b.

The third scheme, constant-current biasing, is illustrated in Fig. 6. The source resistor is replaced by NPN bipolar transistor Q2, which is organized as a constant-current generator. Consequently it determines the

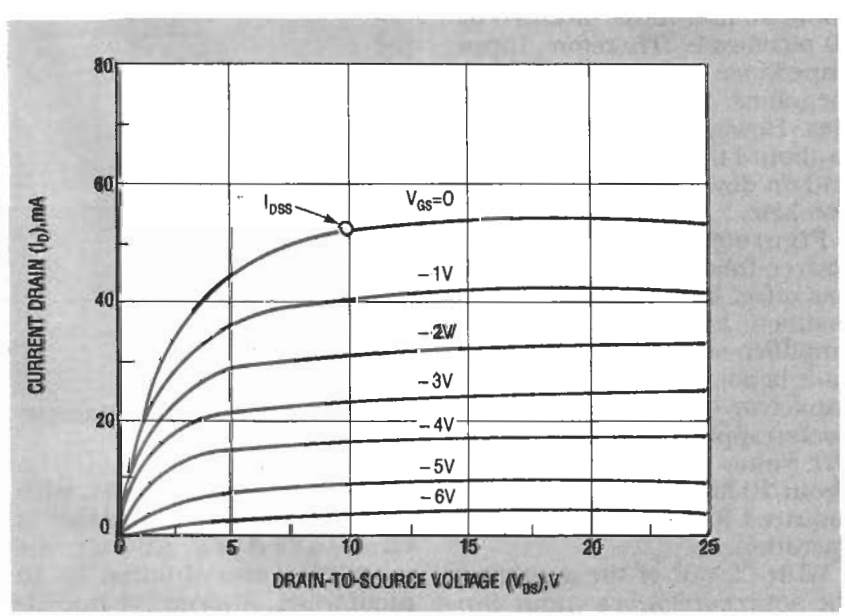

FIG. 3—N-CHANNEL JFET DRAIN characteristic curves.

TABLE 1
SILICON N- CHANNEL JFET: 2N3819
ABSOLUTE MAXIMUM RATINGS
(25°C Free air temperature

Parameter			Unit
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	−40	V
Zero-Gate Voltage Drain Current	I_{DSS}	20	mA
Forward Transconductance	g_{fs}	7.0	mmho
Reverse Gate Leakage	I_{GSS}	−100	pA
"ON" Resistance	r_{DS}	500	ohms
Pinchoff Voltage	$V_{GS(OFF)}$	−6	V
Output Conductance	g_{os}	10	umho
Feedback Capacitance	C_{rss}	0.9	pF
Input Conductance	C_{iss}	4.0	pF
Power Gain	G_{ps}	12	dB
Power Dissipation		360	mV

drain current. The constant current is set by Q2's base voltage, which is set from the R1-R2 voltage divider and emitter resistor R3.

Resistor R2 can also be replaced by a Zener diode or other voltage reference. Thus, in this bias circuit, drain current is independent of JFET characteristics, and high biasing stability is obtained. However, this improvement is gained at the expense of additional components.

In the three biasing schemes, resistor R_G can have any value up to about 10 megohms. That limit is imposed by the voltage drop across the resistor caused by gate leakage currents, which could upset biasing conditions.

Source-followers

JFET transistors in a linear amplifiers are usually configured as either a common-source or common-drain (*source-follower*) amplifier. These are the JFET equivalents of the bipolar common-emitter and common-collector (emitter-follower) amplifier, respectively.

The source-follower amplifier offers very high input impedance and near-unity overall voltage gain. (That's why it's also called a *voltage-follower*). A simple source-follower amplifier is illustrated in Fig. 7. It is self-biasing, and drain current can be varied with potentiometer R4.

That self-biasing source-follower amplifier will work from any positive 12- to 20-volt supply. Potentiometer R4 should be set so that the quiescent voltage across R2 is 5.6 volts, which provides a 1 milliampere drain current. Expect a voltage gain of about 0.95 between input and output.

Because of the voltage division at the junction of potentiometer R4 in series with R1 and resistor R2, some *bootstrapping* is applied to R3. In this circuit where the output is taken from the emitter, the output voltage directly affects the bias. In this amplifier, negative output pulses cause an increase in the negative voltage at the input, and positive output causes a reduction in the negative voltage at the input.

The input is applied between the source and the gate. In this circuit bootstrapping multiplies the effective value of R3 by a factor of about five. The input impedance to the circuit is about 10 megohms, shunted by 10 picofarads. Therefore, input impedance can be as high as 10 megohms at very low frequencies. However, this value drops to about 1 megohm near 16 kHz, and on down to about 100 K at 160 kHz.

Figure 8 is an alternative source-follower amplifier that has offset biasing. Resistor adjustment is not needed in this amplifier, and its overall voltage gain is about 0.95. Electrolytic capacitor C2, which provides bootstrapping, boosts the effective value of gate resistor R3 about 20 fold. However, it is not required for normal amplifier operation.

With C2 out of the amplifier, the source-follower's input impedance is about 2.2 megohms,

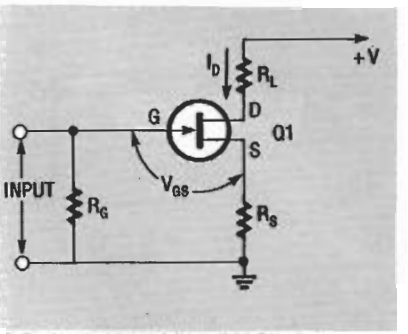

FIG. 4—A JFET SELF-BIASING scheme.

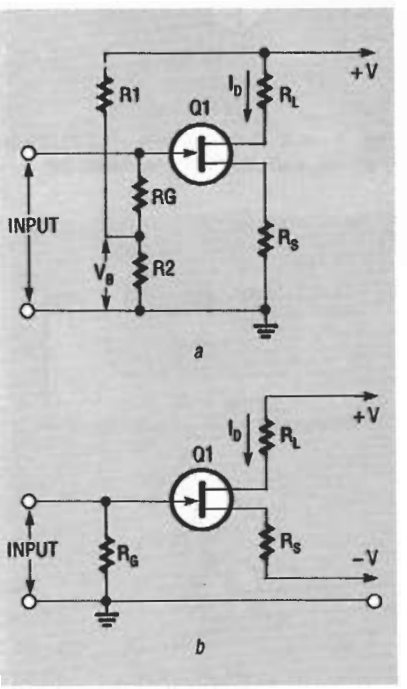

FIG. 5—JFET OFFSET-BIASING schemes for JFET's with +V supply (*a*) and +V and -V supplies (*b*).

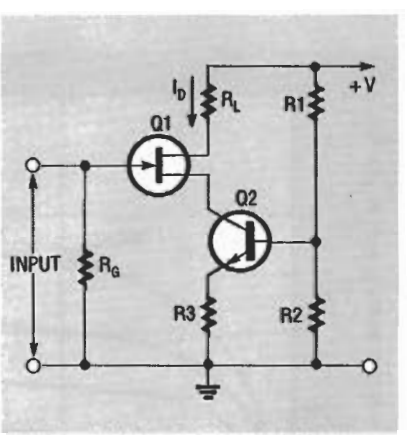

FIG. 6—A JFET CONSTANT-CURRENT biasing scheme

shunted by 10 picofarads; with C2 in place, input impedance is increased to about 44 megohms, also shunted by 10 picofarads. Alternative impedance values can be obtained by

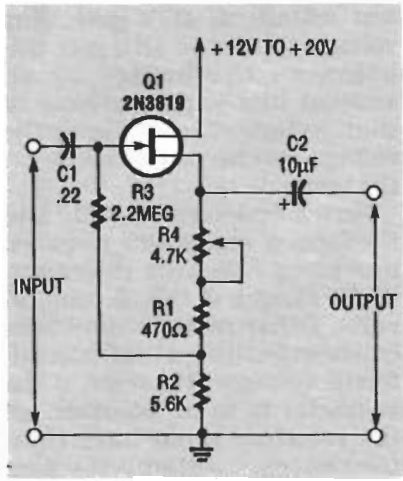

FIG. 7—A JFET SELF-BIASING source-follower with an input impedance of 10 megohms.

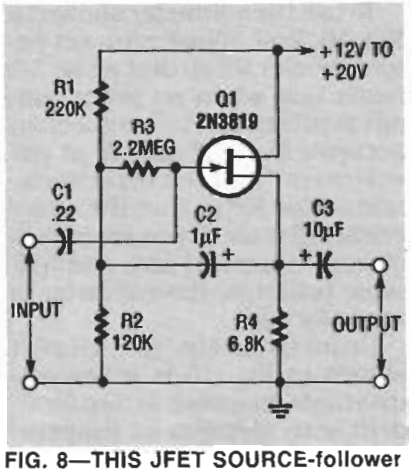

FIG. 8—THIS JFET SOURCE-follower with offset biasing has an input impedance of 44 megohms.

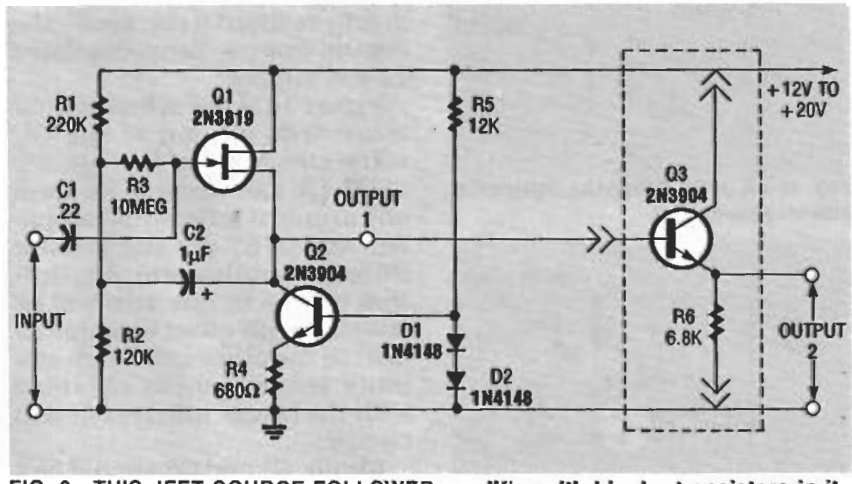

FIG. 9—THIS JFET SOURCE-FOLLOWER amplifier with bipolar transistors in its source circuit has an input impedance of 500 megohms.

increasing R3 up to a maximum of 10 megohms.

Figure 9 shows a JFET-bipolar "hybrid" version of a source-follower amplifier. Its input impedance is about 500 megohms, shunted by 10 picofarads. Here, offset biasing is applied through a voltage divider formed at the resistor R1-R2 junction. This configuration is similar to that of Fig. 8, but source resistor R4 is replaced by a resistor-transistor-diode network (R4, Q2, D1, and D2).

This network makes "source load" Q2 act as a constant-current generator with a high output (collector) impedance, which causes a quiescent drain-to-source current of about 1 milliampere to flow in Q1.

As a result, Q1 functions as a source follower, and the collector of Q2, acting as its source load, appears as a high impedance. Because of the high effective value of this load, JFET Q1 has a voltage gain of about 0.99. Electrolytic capacitor C2 passes a bootstrap signal from the source of Q1 to R3 at the R1-R2 junction. The high-voltage gain of the circuit permits this bootstrap signal to boost the effective value of R3 100 times to about 1000 megohms.

As a result of bootstrapping, the actual input impedance of the source-follower in Fig. 9 is equal to 1000 megohms-shunted by the JFET's gate impedance of about 1000 megohms. The equivalent resistance turns out to be about 500 megohms, shunted by 10 picofarads.

There are two ways to keep both the effective source load and input impedance of this circuit high: The output can be coupled to external circuitry with another emitter-follower stage (shown enclosed in dotted lines in Fig. 9), or all loads to which it is coupled must have high impedances.

Common-source amplifiers

Figure 10 is a schematic for a simple self-biasing, common-source amplifier that can powered from any 12- to 20-volt supply. Potentiometer R4 should be adjusted so that a quiescent 5.6 volts is developed across R3, providing a drain current of 1 milliampere. The biasing of potentiometer R4 in series with resistor R2 is decoupled by electrolytic capacitor C2.

The typical voltage gain for the circuit shown in Fig. 10 is about 21 dB (a multiplying factor of 12), and its frequency response is flat within 3 dB from 15 Hz to 250 kHz. The input impedance of the circuit is 2.2 megohms, shunted by 50 picofarads. This comparatively high value of shunt capacitance is the result of Miller feedback from drain-to-gate. That feedback boosts the JFET's internal gate-to-drain capacitance directly with respect to voltage gain.

Voltage-biasing potentiometer R4 in Fig. 10 can be adjusted so that the circuit accepts, with minimal distortion, strong input signals that generate large output-voltage swings. In applications where only low-level input signals are to be accepted (such as in preamplifiers), a fixed-bias network can be substituted for the potentiometer. Figures 11 and 12 show circuits with that substitution.

Figure 11 shows a simple amplifier for headphones with impedances of 1 K or greater. With an input impedance of 2.2 megohms, the amplifier includes an integral volume control potentiometer R3, and it can be powered from any 9- to 18-volt positive supply.

The circuit shown in Fig. 12 is a general purpose, add-on preamplifier that can be coupled to any amplifier operating from a single-ended 9- to 18-volt

positive supply. The voltage gain from this preamplifier exceeds 20 dB, bandwidth exceeds 100 kHz, and its input impedance is 2.2 megohms.

When exceptional biasing accuracy is required, JFET common-source amplifiers can be designed with either of two *constant-current* offset biasing techniques. Figures 13 and 14 illustrate both options. The common-source amplifier in Fig. 13, with offset gate biasing, can only be powered by a 16- to 20-volt positive supply. However, the "hybrid" version shown in Fig. 14 can be powered with any 12- to 20-volt positive supply. Both circuits offer voltage gains of 21 dB, input impedances of 2.2 megohms, and -3 dB bandwidths from 15 Hz to 250 kHz.

DC voltmeters.

Figure 15 is a schematic for a simple three-range JFET analog voltmeter offering a nominal sensitivity of 22.2 megohms per volt. Its maximum full-scale voltage sensitivity is 0.5 volt, and its input resistance remains constant at 11.1 megohms on all ranges.

In the analog voltmeter shown in Fig. 15, resistor R6, potentiometer R9, and resistor R7 form a voltage divider across the 12-volt battery supply. With the proper setting of R9, 4 volts will appear across R7. The upper end of resistor R7 is connected to circuit ground (zero-volt reference), and its lower end is at -4 volts, setting the upper end of at +8 volts.

JFET Q1 is configured as a source-follower with its gate grounded through a resistor network consisting of R1 through R4. However, Q1's source is connected to -4 volts through source load resistor R5. As a result, Q1 is offset gate-biased, and its drain current is about 1 milliampere.

A closer look at the circuit shows that R6 in series with R9, and Q1 in series with R5 act as the arms of a Wheatstone bridge. The adjustment of potentiometer R9 balances the bridge, and no current flows in the meter unless there is an input voltage at Q1's gate. Any voltage applied to Q1's gate unbalances the bridge by an amount that is proportional to that voltage. The value of the voltage can be read directly on the meter.

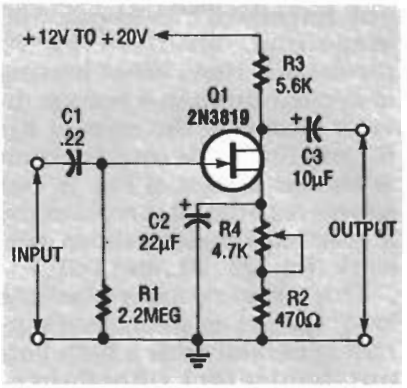

FIG. 10—A SELF-BIASING JFET common-source amplifier.

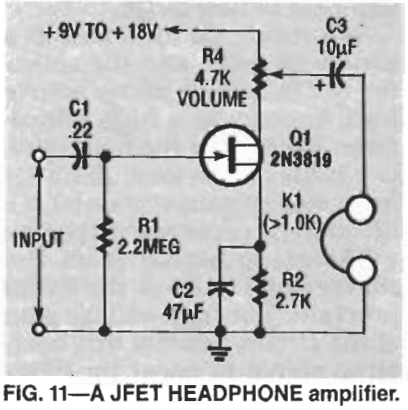

FIG. 11—A JFET HEADPHONE amplifier.

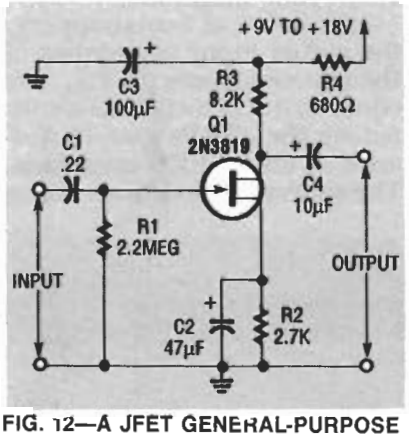

FIG. 12—A JFET GENERAL-PURPOSE add-on preamplifier.

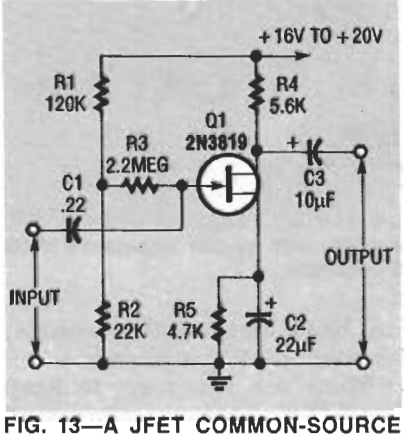

FIG. 13—A JFET COMMON-SOURCE amplifier with offset gate biasing.

To use the voltmeter shown in Fig. 16, first adjust zero- set potentiometer R9 so that meter M1 reads zero when no input voltage is present. Then connect an accurate 0.5-volt source at the voltmeter's input terminals, and adjust R9 so that the meter reads full scale. If you are able to obtain consistent zero and full-scale readings, the voltmeter is ready for use.

Unfortunately, the circuit shown in Fig. 15 is inherently unstable because it tends to drift with changes in temperature and supply voltage. That makes it necessary to adjust zero-set potentiometer R9 frequently. However, drift can be greatly reduced if you power the circuit from a Zener-regulated 12-volt supply.

Figure 16 is the schematic for a low-drift version of the DC voltmeter shown in Fig. 15. JFET Q1 and resistor R5 form one arm of a differential amplifier, and JFET Q2 and resistor R6 form the other arm. Any drift that occurs in one arm will be automatically offset by a similar drift in the other arm. High stability is one benefit obtained with the bridge inherent in this circuit.

Ideally, Q1 and Q2 should be a pair of JFET's with their drain-to-source currents (I_{DS}) matched within 10%. This DC voltmeter circuit will work from any 12- to 18-volt positive supply. The calibration procedure is similar to that specified for Fig. 15.

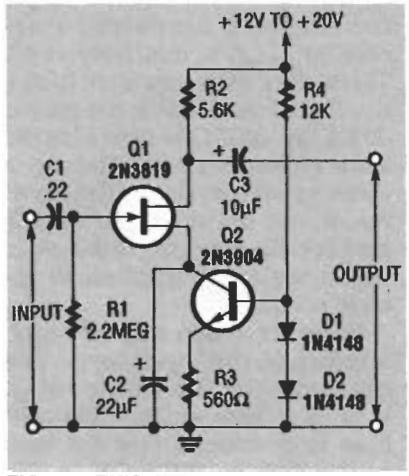

FIG. 14—THIS JFET COMMON-SOURCE amplifier has a bipolar transistor in its source circuit.

sistive factors of these time constants can be very large. This permits long time periods to be obtained with low capacitance values.

With the components shown in Fig. 17, the oscillator switches once every 20 seconds (0.05 Hz). Unfortunately, START button S1 must be held closed for at least one second to initiate the astable action. Because of this shortcoming, consider the circuit to be more of an experiment than a practical circuit.

Figure 18 illustrates how an N-channel JFET can combined with a classical µA741 operational amplifier to form a voltage-controlled amplifier/attenuator. Here, the op-amp is connected as an inverting amplifier with its gain determined by the ratio of input resistor R2 to feedback resistor R3. Thus, JFET Q1 functions as a voltage-controlled resistor. The circuit can attenuate an input signal to the amplifier.

When a large negative control voltage ($-V_E$) appears at its gate, JFET Q1 acts as a virtual infinite resistance because its drain current (I_D) is pinched off. Because there is no input signal attenuation, the circuit functions as a high-gain amplifier. However, if the gate bias falls to zero, Q1 becomes a virtual short circuit. (Drain current is maximum and gate-to-source resistance falls to a few hundred ohms.) As a result, the input signal is heavily attenuated by the circuit.

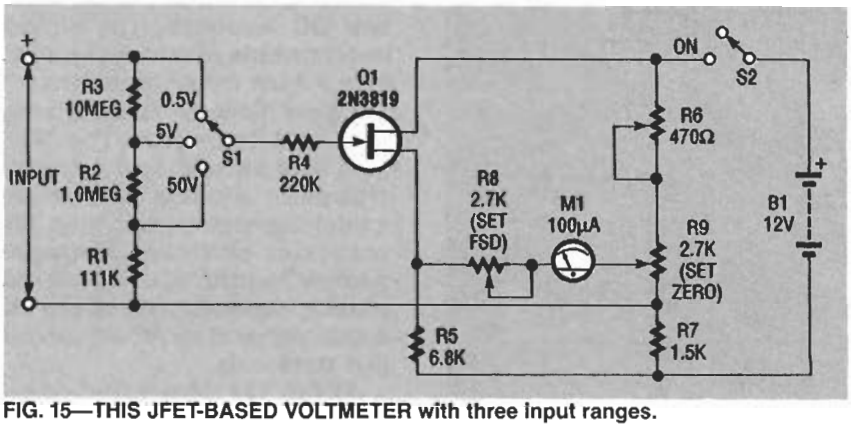

FIG. 15—THIS JFET-BASED VOLTMETER with three input ranges.

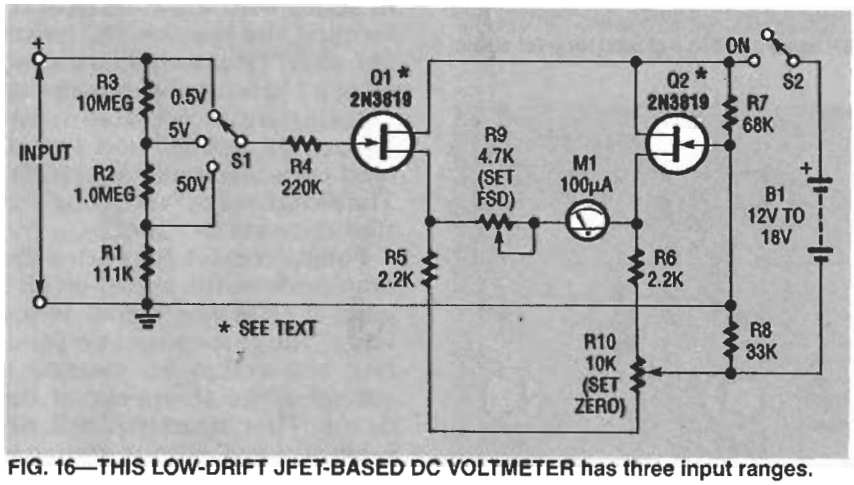

FIG. 16—THIS LOW-DRIFT JFET-BASED DC VOLTMETER has three input ranges.

Multivibrator and amplifier

Figure 17 is the schematic for a very low-frequency (VLF) free-running multivibrator that produces a squarewave output. The multivibrator's ON and OFF periods are controlled by the time constants from the resistor-capacitor pairs C1R4 and C2R3. Because of very high JFET input impedances, the re-

Amplifier and converter

Intermediate values of signal attenuation and overall gain or loss can be obtained by varying the control voltage (V_{GD}) applied to the gate of Q1 between the zero bias and pinchoff limits.

Figure 19 is a schematic for a *constant-volume* amplifier that exploits the voltage-controlled resistor characteristics of the JFET. The amplifier produces an output signal that shifts only 7.5 dB when the input signal is varied over a 40 dB range (from 3 to 300 millivolts, rms). The amplifier can accept input signals as high as 500 millivolts, rms.

In Fig. 19, JFET Q1 and resistor R4 are in series to form a voltage-controlled attenuator that controls the input signal level to bipolar transistor Q2, which is in a common-emitter amplifier. Signal output from Q2 is buffered by bipolar transistor Q3.

Part of the output signal from Q3 is fed back to the gate of

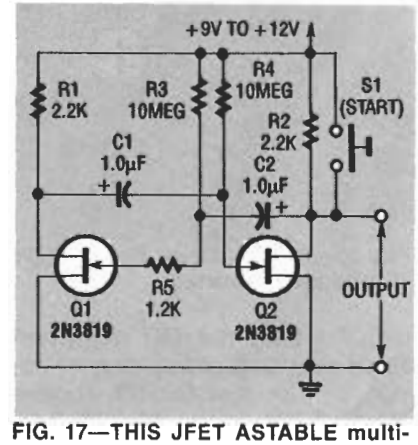

FIG. 17—THIS JFET ASTABLE multivibrator operates at very low frequencies.

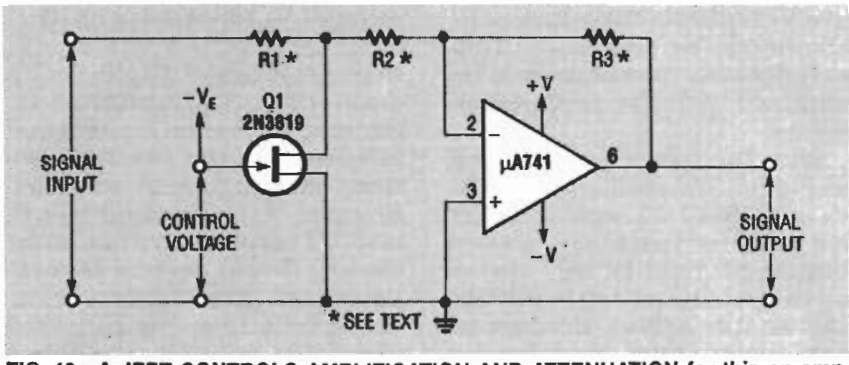

FIG. 18—A JFET CONTROLS AMPLIFICATION AND ATTENUATION for this op-amp.

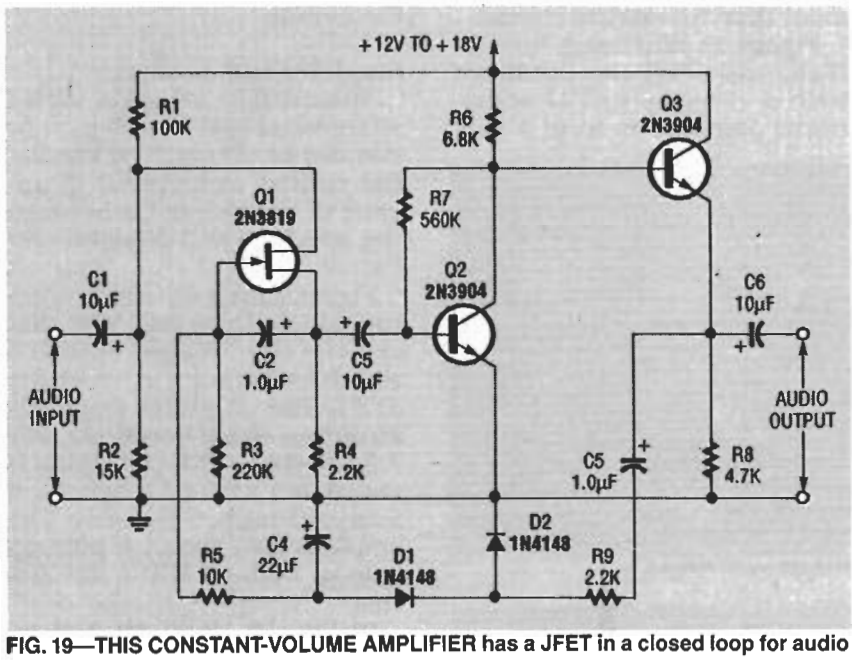

FIG. 19—THIS CONSTANT-VOLUME AMPLIFIER has a JFET in a closed loop for audio control.

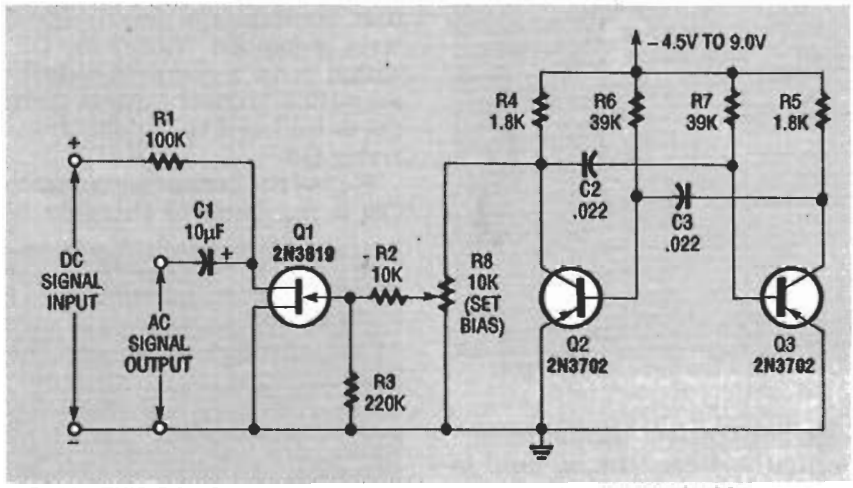

FIG. 20—THIS DC TO AC CONVERTER has a JFET switch and and a bipolar multivibrator pulse generator.

JFET Q1 by the DC negative-feedback loop consisting of capacitor C5, resistor R9, diodes D1 and D2, capacitor C4, and resistor R5. The negative-feedback automatically adjusts the constant-volume amplifier's voltage gain by holding the output signal level constant as the input signal level is varied.

When a small signal is applied to the audio input terminals of the amplifier, the output at the emitter of Q3 is relatively small. Thus, very little negative bias is developed and fed to the gate of JFET Q1. JFET Q1 now acts like a low resistance and little signal attenuation occurs in the series resistance of the drop across Q1 and R4. As a result, most of the input signal is applied to the base of Q2.

However, when a large signal appears at the input terminals, the output at the emitter of Q3 is large. Thus, a large negative bias is developed and fed back to the gate of JFET Q1. In this condition, only a fraction of the input signal is applied to the base of Q2. Because of the negative DC feedback, the output level remains relatively constant over a wide range of inputs.

Figure 20 is the schematic for a DC-to-AC converter. The JFET acts as a switch, and a bipolar transistor flip-flop acts as the switching-signal generator. The converter produces a square-wave AC output with a peak amplitude equal to that of the DC input signal at its AC signal output terminals.

JFET Q1, the electronic switch, has its drain connected in series with input resistor R1 forming the positive DC terminal. JFET Q1 is switched on and off at a 1 kHz rate by the flip-flop consisting of bipolar transistors Q2 and Q3 and associated resistors and capacitors. The switching or "chopping" action converts DC to AC.

Potentiometer R8 varies the amplitude of the signal on Q1's gate. If Q1's gate signal is too large, its gate-to-source junction will avalanche, causing a voltage *spike* to appear at the drain. That transient will develop a small output signal at the drain of Q1 even when no DC input is present.

To prevent this glitch, connect a DC input to the converter, and adjust potentiometer R9 until the amplitude of the AC output just starts to decrease. JFET avalanching will not occur when this adjustment is made. As a result, the converter can reliably convert DC voltages with amplitudes as low as a fraction of a millivolt. Ω