Measuring HEXFET® Characteristics

(HEXFET is the trademark for International Rectifier Power MOSFETs)

by **R. PEARCE, S. BROWN, D. GRANT**

Summary

Curve tracers have generally been designed for making measurements on bipolar transistors. While power MOSFETs can be tested satisfactorily on most curve tracers, the controls of these instruments are generally labeled with reference to bipolar transistors, and the procedure to follow in the case of MOSFETs is not immediately obvious. This application note describes methods for measuring HEXFET® power MOSFET characteristics, both with a curve tracer and with purpose-built test circuits.

Introduction

Testing HEXFETs on a curve tracer is a simple matter, provided the broad correspondence between bipolar transistor and HEXFET features are borne in mind. Table 1 matches some features of HEXFETs with their bipolar counterparts.

Table 1
HEXFET and Bipolar Equivalent Parameters (approximate)

HEXFET	Bipolar
Drain	Collector
Gate	Base
Source	Emitter
gfs	h_{FE}
BV_{DSS}	BV_{CES}
$V_{GS(th)}$	$V_{BE(on)}$
$V_{DS(on)}$	$V_{CE(sat)}$
I_{DSS}	I_{CES}
I_{GSS}	I_{EBO}

The HEXFET used in all the examples was the IRF630. The control settings given in the examples are those suitable for the IRF630. The user must modify these values appropriately when testing a different device.

The IRF630 was selected since it is a typical mid-range device with a voltage rating of 200 volts and a continuous current rating of 9 amps (with T_C = 25°C). For measurements with currents above 20 amps, or for pulsed tests not controlled by the gate, the Tektronix 176 Pulsed High Current Fixture must be used instead of the standard test fixture.

The IRF630 is an N-channel device. For a P-channel device, all the test procedures are the same except that the position of the polarity selector switch must be reversed — that is, for P-channel devices, it must be in the PNP position.

The curve tracer used as an example in this application note is a Tektronix 576, since this instrument is in widespread use. However, the principles involved apply equally well to other makes and models.

Figure 1 shows the layout of the controls of the Tektronix 576 curve tracer, with major controls identified by the names used in this application note. Throughout this application note, when controls are referred to, the name of the control is printed in capitals.

For all tests, the initial state of the curve tracer is assumed to be as follows:

- LEFT/RIGHT switch in "off" position.
- VARIABLE COLLECTOR SUPPLY at zero.
- DISPLAY not inverted.
- DISPLAY OFFSET set at zero.
- STEP POLARITY not inverted.
- VERTICAL DISPLAY MAGNIFIER set at normal.
- The REP button of the STEP FAMILY selector should be IN.
- The AID button of the OFFSET selector should be IN.
- The NORM button of the RATE SELECTOR should be IN.

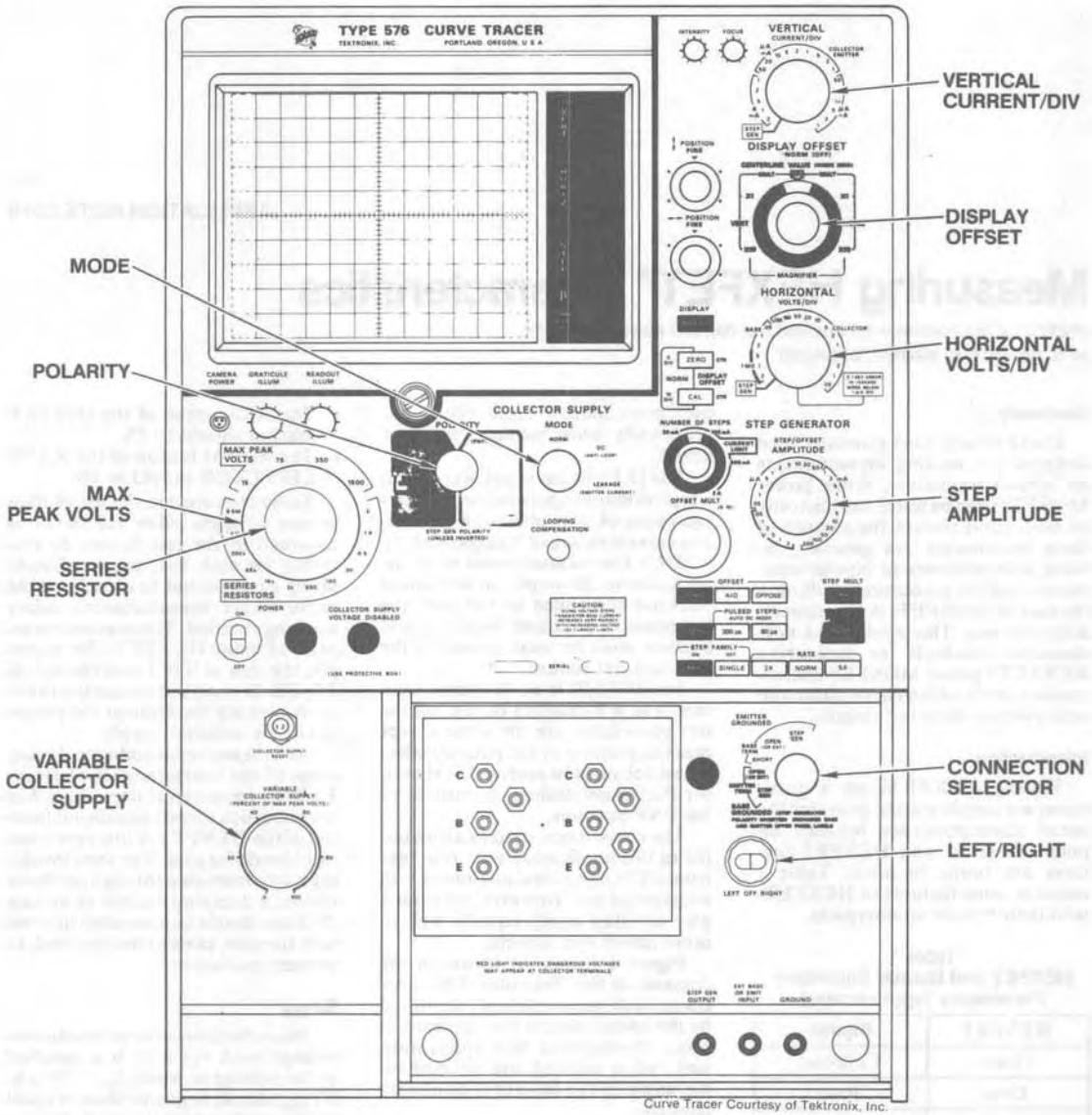
Some tests require the use of dangerous voltages. After the device is mounted in the test fixture as described for each test, the test fixture safety cover should be closed and the curve tracer manufacturer's safety warnings heeded. The exposed metal parts of many HEXFETs (for example, the can of TO-3 and the tab of TO-220 devices) are connected to the drain and are therefore at the potential of the collector supply.

As with any semiconductor device, some of the characteristics of HEXFETs are temperature dependent. For tests in which there is significant heating of the HEXFET, a low repetition rate should be used. For tests involving a slow transition through the linear region, a damping resistor of at least 10 Ohms should be connected in series with the gate, close to the gate lead, to prevent oscillation.

BV_{DSS}

This is the drain-source breakdown voltage (with V_{GS} = 0). It is specified as the voltage at which I_D = 250 μA. BV_{DSS} should be greater than or equal to the rated voltage of the device.

1. Connect the device as follows: drain to "C", gate to "B", source to "E".
2. Set the MAX PEAK VOLTS to 350V.
3. Set the SERIES RESISTOR to limit the avalanche current to a safe value, i.e., tens of milliamps. A suitable value in this case would be 14kΩ.
4. Set the POLARITY switch to NPN.
5. The MODE control should be set to normal.
6. HORIZONTAL VOLTS/DIV



Curve Tracer Courtesy of Tektronix, Inc.

Figure 1. Location of Curve Tracer Controls

should be set at 50 volts/div on the "collector" range.

7. VERTICAL CURRENT/DIV should be set at 50 μA/div.
8. On the plug-in fixture, the CONNECTION SELECTOR should be set to "short" in the "emitter grounded" sector. This action grounds the gate and disables the step generator.
9. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control until the current, as indicated by the trace on the screen reaches 250 μA. (See Figure 2.) Read BV_{DSS} from the screen.

I_{DSS}

This is the drain current for a drain-source voltage of 100% of rated voltage, with $V_{GS} = 0$. The HEXFET data sheet also gives a value of I_{DSS} for 80% of rated voltage and a junction temperature of 125°C.

This measurement is made in the same manner as BV_{DSS} except that:

1. The MODE switch is set to "leakage".
2. Connect the device using the LEFT, RIGHT switch and adjust the collector supply voltage to the rated voltage of the HEXFET

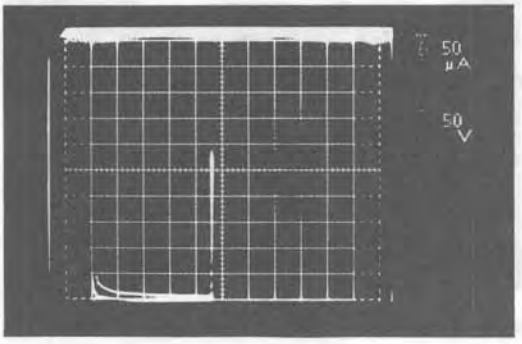


Figure 2. Drain-Source Breakdown Voltage (BV_{DSS})

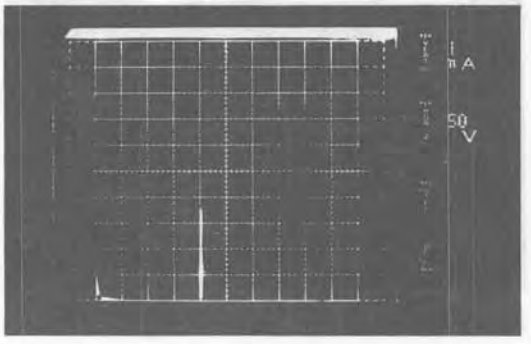


Figure 3. Drain-Source Leakage Current (I_{DSS})

(200V for the IRF630). Read the value of I_{DSS} from the display (see Figure 3). The vertical sensitivity may need altering to obtain an appropriately sized display. Often, I_{DSS} will be in the nanoamp range, and the current observed will be capacitive currents due to minute variations in collector supply voltage.

$V_{GS(th)}$

This is the gate-source voltage which produces 250 μA of drain current ($V_{DS} = V_{GS}$). It is the gate-source voltage at which the device enters the active region. In circuits in which devices are paralleled, switching losses can be minimized by using devices with closely matched threshold voltages.

1. This test requires the gate to be connected to the drain. Connect the device as follows: source to "C", gate to "B", drain to "E". This connection arrangement may require the construction of a special test fixture. Bending of the device leads can cause mechanical stress which results in the failure of the device.
2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR to 0.3 ohms.
4. Set POLARITY to PNP. This causes the drain (collector) terminal to be negative with respect to the source (emitter) terminal.
5. Set the MODE control to normal.
6. Set the VERTICAL CURRENT/DIV to 50 μA/div.
7. Set the HORIZONTAL VOLTS/DIV to 500 mV/div.
8. Set the CONNECTION SELECTOR to "short" in the "emitter grounded" sector.
9. DISPLAY should be inverted.
10. Connect the device using the LEFT/RIGHT switch. Increase the VARIABLE COLLECTOR VOLTAGE until the drain current reaches 250 μA as indicated by the trace on the screen. Read the voltage on the horizontal center line (since this line corresponds to I_D = 250 μA). (See Figure 4.)

I_{GSS}

This is the gate-source leakage current with the drain connected to the source. An excessive amount of gate leakage current indicates gate oxide damage.

1. The device is connected as follows: gate to "C", drain to "B", source to "E". This is not the usual connection sequence, and a special test fixture will be required if bending of the leads is to be avoided.
2. Set MAX PEAK VOLTS to 75V.
3. Set the SERIES RESISTOR to a low value (for example, 6.5 ohms).
4. Set the MODE switch to leakage.
5. Set the CONNECTION SELECTOR to the "short" position in the "emitter grounded" sector.
6. HORIZONTAL VOLTS/DIV should be set at 5V/div.
7. VERTICAL CURRENT/DIV should be set to an appropriately low range.
8. Connect the device using the LEFT/RIGHT switch. Increase the collector supply voltage using the VARIABLE COLLECTOR SUPPLY control, but do not exceed 20V, the maximum allowable gate voltage. It may be necessary to adjust the vertical sensitivity. Read the leakage current from the display (see Figure 5). In many cases, the leakage current will be in the nanoamp range, in which case the trace will be dominated by currents which flow through the device capacitance as a result of minute fluctuations in the collector supply voltage.
9. The above procedure is for determining gate leakage current with a positive gate voltage. To make the same measurement using a negative voltage, reduce the VARIABLE COLLECTOR SUPPLY voltage to zero, change the POLARITY switch to the PNP position, and reapply the voltage (see Figure 6). The trace will take time to settle because of the gate-source capacitance.

g_{fs}

This is the forward transconductance of the device at a specified value of I_D. It represents the signal gain (drain current divided by gate voltage) in the linear region.

This parameter should be measured with a small ac superimposed on a gate bias and the curve tracer is not the appropriate tool for this measurement.

Even with specific test equipment, the dc bias tends to overheat the MOSFET very rapidly and care should be exercised to insure that the pulse is suitably short.

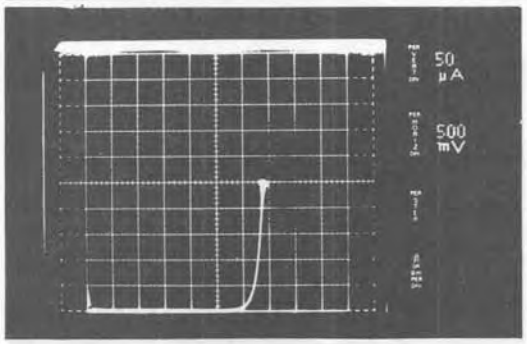


Figure 4. Gate-Source Threshold Voltage ($V_{GS(th)}$)

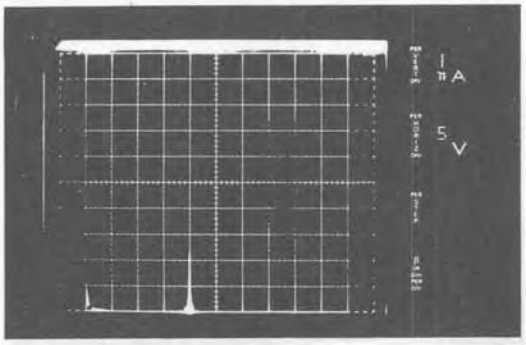


Figure 5. Gate-Source Leakage Current (I_{GSS}) at +20V

12. Set VERTICAL CURRENT/DIV at 1 amp/div.
13. Connect the device using the RIGHT/LEFT switch. Increase the VARIABLE COLLECTOR SUPPLY voltage to increase I_D, but do not exceed I_{DM}. The display will be similar to that shown in Figure 7. The device under test will get hot within seconds. It may therefore be necessary to photograph the trace as soon as possible after connecting the device in order to permit careful analysis fo the trace. It may be necessary to vary the offset voltage in order to center the traces about the desired current level. The transconductance is obtained by dividing the value of the current step between traces in the linear region by the value of gate voltage step used. In this case, the current step value is 0.45 amps in the region of I_D = 5 amps, and the gate voltage step is 0.1 volts. Thus, the transconductance is 4.5 Siemens.

To reduce device dissipation, the test must be performed in the pulse mode as g_{fs} is temperature dependent. The 80 μS or 300 μS button should be depressed. The trace obtained is shown in Figure 8.

$R_{DS(on)}$

This is the drain-source resistance at 25°C with V_{GS} = 10V. Since $R_{DS(on)}$ is temperature-dependent, it is important to minimize heating of the junction during the test. A pulse test is therefore used to measure this parameter.

The test is set up in the same manner as the g_{fs} test, except that:

1. Set NUMBER OF STEP to 10.
2. Set STEP AMPLITUDE to 1V. Alternatively, the STEP AMPLITUDE could be set to 2V as long as the number of steps is reduced so that the max gate voltage is not exceeded.
3. The CURRENT LIMIT should be set to 500 mA.
4. The STEP MULTIPLIER button should be OUT — that is, .1X not selected.
5. On the PULSED STEPS selector, the 80 μS button should be IN.
6. On the RATE selector, the .5X button should be IN.
7. Connect the device using the LEFT/RIGHT switch and raise the VARIABLE COLLECTOR SUPPLY voltage until the desired value of drain current is obtained. $R_{DS(on)}$ is obtained from the trace by reading the peak values of current and voltage (see Figure 9). $R_{DS(on)} = V_{DS}/I_D$.

V_{SD}

This is the source-drain voltage at rated current with V_{GS} = 0. It is the forward voltage drop of the body-drain diode when carrying rated current. (If pulsed mode testing is required, use high current test fixture.)

1. Connect the device as follows: gate to "B", drain to 'C", source to "E".
2. Set the MAX PEAK VOLTS to 15V.
3. Set the SERIES RESISTOR at 1.4 ohms or a value sufficiently

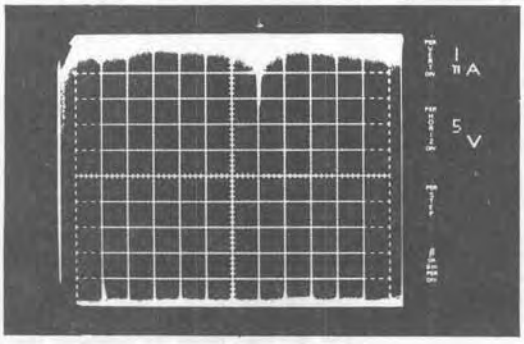


Figure 6. Gate-Source Leakage Current (I_{GSS}) at -20V

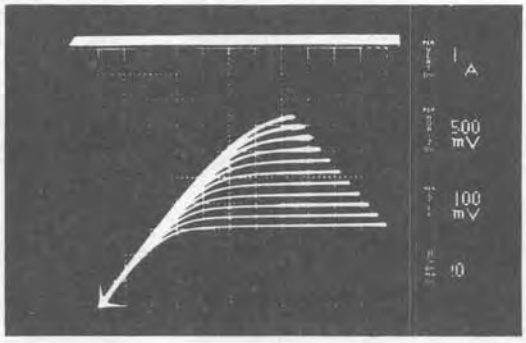


Figure 7. Forward Transconductance (g_{fs})

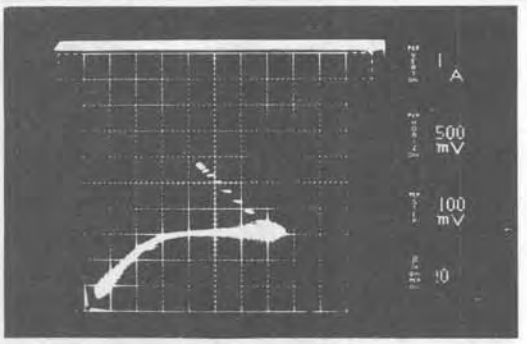


Figure 8. Forward Transconductance-Pulsed (g_{fs})

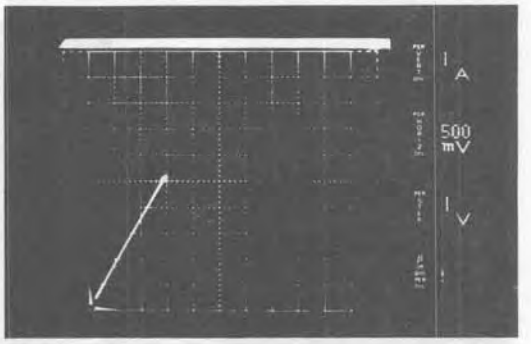


Figure 9. Drain-Source Resistance ($R_{DS(on)}$)

low that rated current can be obtained.
4. Set POLARITY to PNP.
5. Set MODE to "normal".
6. The 80 μS button of the PULSED STEPS selector should be IN.
7. The CONNECTION SELECTOR should be set to the "short" position in the "emitter grounded" sector.
8. HORIZONTAL VOLTS/DIV should be on 200 mV/div.
9. VERTICAL CURRENT/DIV should be on 1A/div.
10. The DISPLAY button should be set to invert.
11. The device is connected using the LEFT/RIGHT switch. Increase the VARIABLE COLLECTOR SUPPLY voltage until rated current is reached (9A for the IRF-630). Read V_{SD} from the trace (see Figure 10).

Composite Characteristics

The forward and reverse characteristics of the HEXFET may be viewed at the same time. This display can be used to obtain an appreciation of the HEXFET's behavior in applications in which current flows in the channel in either direction, such as synchronous rectifiers and analog waveform switching.

The procedure is the same as for g_{fs} except that:

1. The STEP MULTIPLY .1X button should be OUT (to give 1 volt steps).
2. OFFSET is set to zero.
3. The POLARITY control is set at "AC".
4. The device is connected using the LEFT/RIGHT switch. The VARIABLE COLLECTOR SUPPLY voltage is increased to obtain the required peak value of I_D. Beware of device heating. Figure 11 shows the trace obtained with the IRF630. To obtain the reverse characteristics of the diode alone, invert the step polarity. The FET is inoperative, and the display will resemble that shown in Figure 12. The step polarity should also be inverted to obtain the composite characteristics of P-channel devices.

Transfer Characteristics

The transfer characteristic curve of I_D versus V_{GS} may be displayed using the pulse mode.

The test is set up in the same manner as the g_{fs} test, except for the following:

1. OFFSET MULTIPLY should be set at zero.
2. Set HORIZONTAL VOLTS/DIV on "step gen".
3. The 300 μS button of the PULSED STEP SELECTOR should be IN.
4. Increase the VARIABLE COLLECTOR SUPPLY voltage to obtain the trace shown in Figure 13. The transfer characteristic is outlined by the displayed points.

MEASUREMENT OF HEXFET CHARACTERISTICS WITHOUT A CURVE TRACER

HEXFET parameters may be measured using standard laboratory equipment. Test circuits and procedures for doing this are described in the following sections, with the IRF-

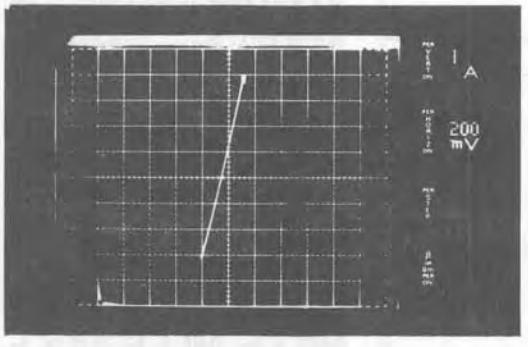


Figure 10. Source-Drain Voltage (V_{SD})

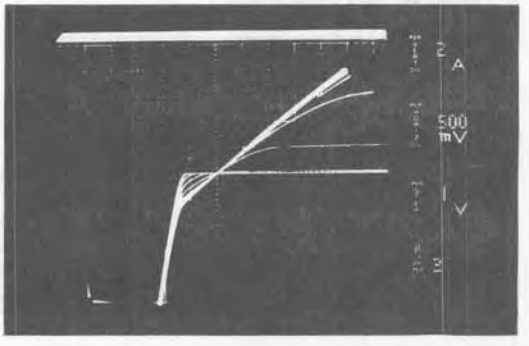


Figure 11. N-Channel Composite Characteristics

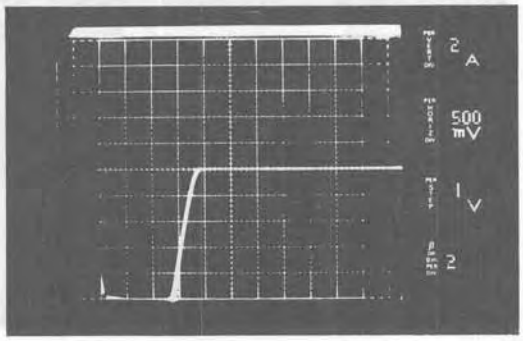


Figure 12. N-Channel Composite with no Gate Drive

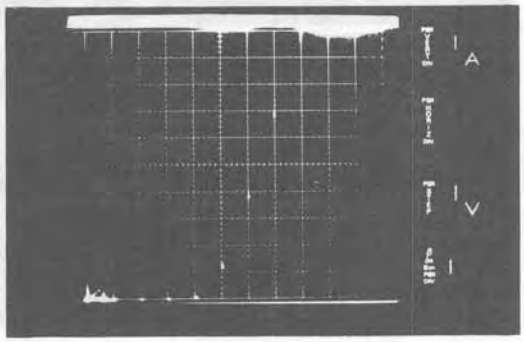


Figure 13. Transfer Characteristics (I_D versus V_{gs})

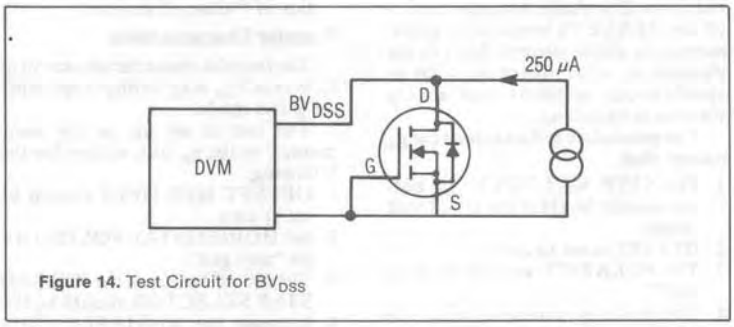


Figure 14. Test Circuit for BV_{DSS}

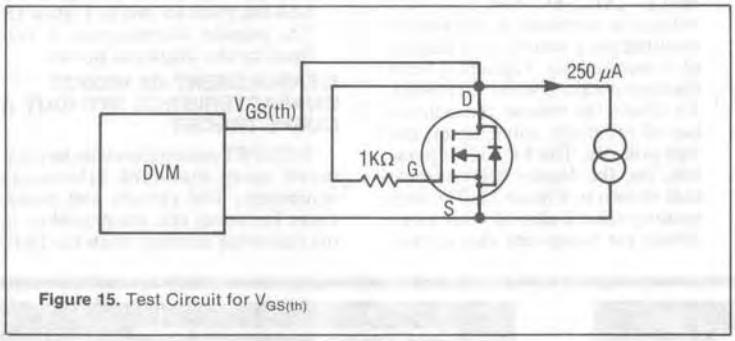


Figure 15. Test Circuit for $V_{GS(th)}$

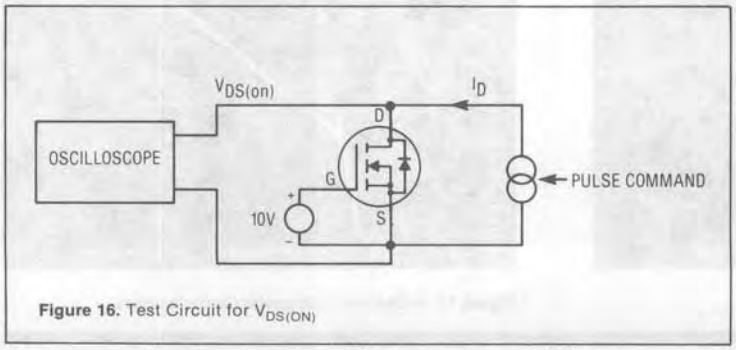


Figure 16. Test Circuit for $V_{DS(ON)}$

630 used as an example. The test arrangement should be varied appropriately for other devices.

BV_{DSS}. The Drain-Source Breakdown Voltage

The current source will typically consist of a power supply with an output voltage capability of about 3 x BV_{DSS} in series with a current defining resistor of the appropriate value. When testing high voltage HEXFETs, it may not be practical or safe to use a supply of 3 x BV_{DSS}, in which case some other form of constant current source must be used.

$V_{GS(th)}$. The Threshold Voltage

The 1k ohm gate resistor is required to suppress potentially destructive oscillations at the gate. The current source may be derived from a voltage source equal to the voltage rating of the HEXFET and a series resistor.

$V_{DS(on)}$. Saturated On-Resistance

The pulse width should be 300 μS at a duty cycle of less than 2%. The value quoted is at a junction temperature of 25°C. $R_{DS(on)}$ is calculated by dividing $V_{DS(on)}$ by I_D. Connect the ground of the gate supply as close to the source lead as possible.

g_{fs}. Transfer Characteristics

Connect a 50V power supply between drain and source. Use a current probe to measure I_D. A signal generator, operating at a low duty cycle to prevent heating of the device, is used to obtain 80 μS pulses of the required voltage (V_{GS}) to obtain the following currents: 0.015 x I_D, 0.05 x I_D, 0.15 x I_D, 0.5 x I_D, and 1.5 x I_D where I_D is the rated I_D at T_C = 25°C. Plot a graph of V_{GS} versus I_D. The transconductance

is equal to the slope of the graph at the appropriate value of drain current.

C_{iss}, C_{oss} and C_{rss}. Output, Input and Reverse Transfer Capacitances

A 1 MHz capacitance bridge is used for all these tests. The capacitance to be measured is connected in series with a capacitance of known value to provide dc isolation.

If C_u is the unknown capacitance, C_k is the known capacitance, and C_m is the measured capacitance, then C_u can be calculated as follows:

$$C_u = \frac{C_m C_k}{C_k - C_m}$$

$t_{d(on)}$, t_r, $t_{d(off)}$, t_f. Turn-on Delay Time, Rise Time, Turn-Off Delay Time, Fall Time

The gate pulses should be just long enough to achieve complete turn-on, with a duty cycle of the order of 0.1%. The series resistor is chosen according to the HEXFET die size as shown in Table 2. The penultimate digit of the HEXFET device designation, so that an IRF630 uses a HEX-3 die.

The definitions of rise, fall and delay times are given in Figure 22.

Q_g, Q_{gs}, Q_{gd}. Total Gate Charge, Gate-Source Charge, Gate-Drain Charge

The total gate charge has two components: the gate-source charge and the gate-drain charge (often called the Miller charge).

The drain current may be obtained from a voltage source of 0.8 x V_{DS} in series with a resistor of the appropriate value. The pulse of gate voltage, which should be long enough to ensure complete turn-on of the HEXFET, may be obtained from a function generator operating with a low duty cycle.

Figure 24 shows the test waveforms.

From the relationship $Q = \int i$, the following results are obtained:

$Q_g + (t_3 - t_0)\, i_g$, $Q_{gd} = (t_2 - t_1)\, i_g$, $Q_{gs} = Q_g - Q_{gd}$

V_{SD}. Body-Drain Diode Conduction Voltage

The current source may consist of a voltage source and a series resistor. The voltage should be applied in short pulses (less than 300 μS) with a low duty cycle (less than 2%).

t_{rr}, Q_{rr}. Body-Drain Diode Reverse Recovery Time and Reverse Recovery Charge

The principal of operation is as

Table 2. HEX Die Size Resistance Values

HEX-Z HEX-1	24Ω	HEX-2 HEX-3	12Ω	HEX-4 HEX-5	6.2Ω

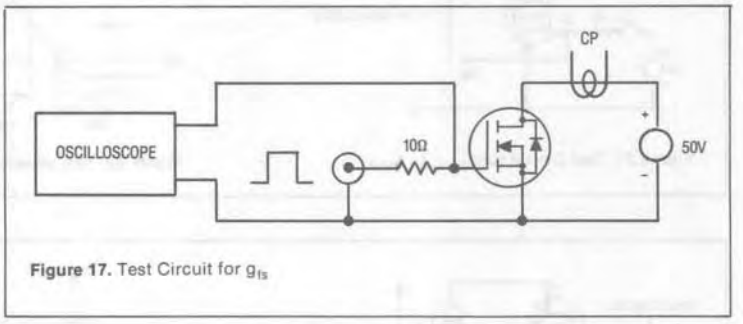


Figure 17. Test Circuit for g_{fs}

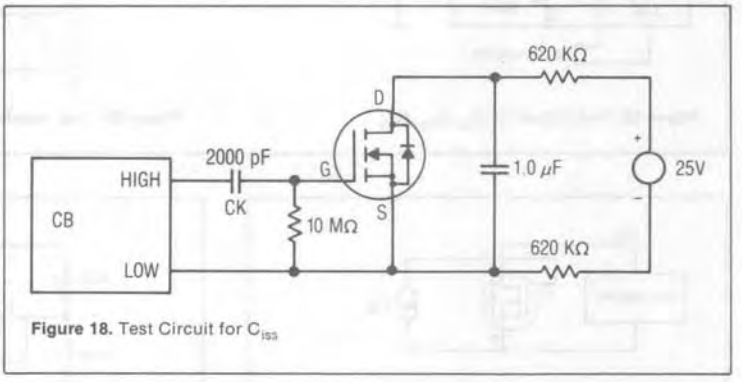


Figure 18. Test Circuit for C_{iss}

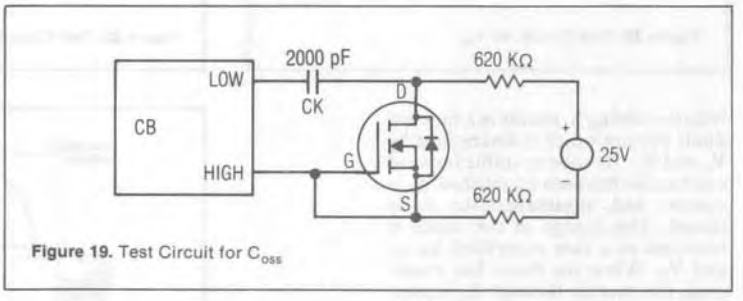


Figure 19. Test Circuit for C_{oss}

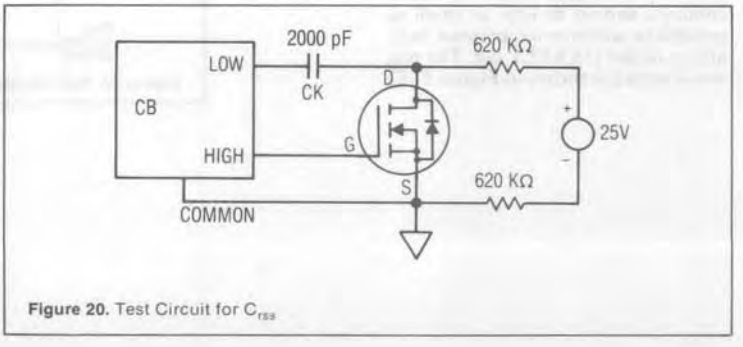


Figure 20. Test Circuit for C_{rss}

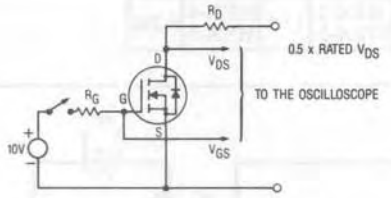


Figure 21. Test Circuit for $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

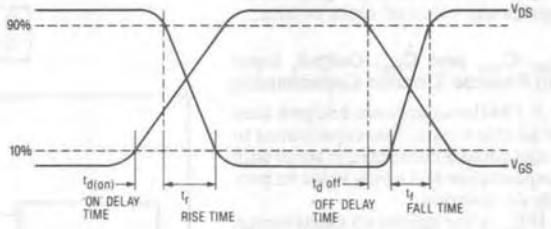


Figure 22. Test Waveforms

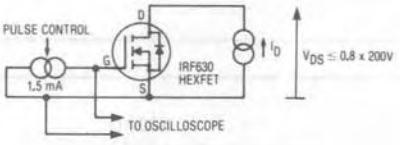


Figure 23. Test Circuit for Q_g, Q_{gs}, Q_{gd}

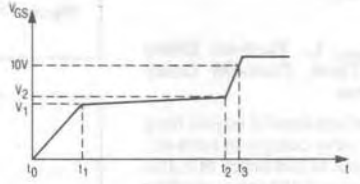


Figure 24. Test Waveforms

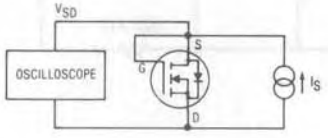


Figure 25. Test Circuit for V_{SD}

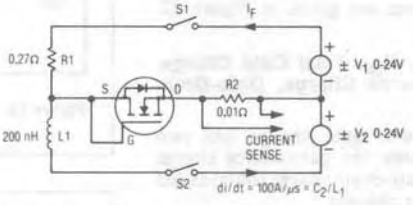


Figure 26. Test Circuit for t_{rr}, Q_{RR}

follows: closing S_1 results in a forward diode current which is determined by V_1 and R_1. As soon as stable forward conduction has been established, S_1 is opened and, simultaneously, S_2 is closed. The charge in the diode is removed at a rate controlled by L_1 and V_2. When the diode has recovered, the current through L_1 ceases. The length of time which the diode conducts should be kept as small as possible to minimize temperature variations of the HEXFET die. The test waveforms are shown in Figure 27. □

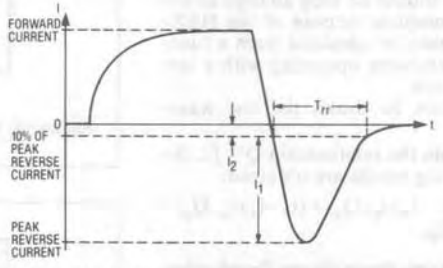


Figure 27. Test Waveforms