The Junction F.E.T. as a Voltage-controlled Resistance

— with particular reference to communications receivers

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The wide range of drain-source channel resistance of junction f.e.ts, under control of the gate-source voltage, makes them useful in high-performance a.g.c. systems. This two-part article first outlines shunt and series a.g.c. systems, discusses design problems and then in part 2 gives practical circuits for a series and shunt a.g.c. system, volume compression and expansion, squelch and battery saving. Circuits are especially suitable for mobile communications receivers.

The current in a typical *n*-channel, depletion mode f.e.t. is transported by electron flow between the source and drain terminals by a channel of *n*-type material which is restricted in dimension by the depletion region of the reverse-biased gate junctions, Fig. 1. The interesting condition is when the two depletion regions merge, for then the current flowing through the device is limited only by carrier injection from the source region of the channel and is virtually independent of drain voltage variation.

Thus a junction f.e.t., operating in the saturation region of its output characteristic, may be considered as a resistance between the drain and source, R_{ds}, which is critically dependent on the gate-source voltage, V_{gs}, and independent of the drain voltage, V_d. This latter property renders the channel resistance, at a particular control voltage, V_{gs}, remarkably linear for signals applied to the drain terminal of the device.

The channel resistance characteristic of Fig. 2 illustrates the suitability of a variably-biased junction f.e.t. for controlled resistance applications. Within the saturation region of the channel resistance characteristic, the device exhibits:

- large range of channel resistance from 1kΩ to several MΩ.
- critical dependence of R_{ds} on the control voltage V_{gs}; a 0.5-V change in V_{gs} can change R_{ds} from 1kΩ to 1MΩ.
- high degree of linearity for constant V_{gs}.
- very low operating current; drain current $<30\mu$A.

As the curves show, a disadvantage of operation within the saturation region is the relatively large change in the drain voltage, V_d, over the channel resistance range. Within the linear region of operation ($R_{ds}<1$kΩ) the change of the drain voltage ceases to be a problem, but the above advantages of the saturation region do not apply to the linear region.

A.G.C. systems in general

There are two basic circuit configurations for a.g.c. of audio amplifiers—the shunt and series systems represented in Fig. 3—whose effect is shown in Fig. 4.

For output signals below V_{o1}, zero a.g.c. is delivered so that the overall gain of the

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†A. S. Grove, "Physics and Technology of Semiconductor Devices", Wiley, 1967, pp. 243–57.

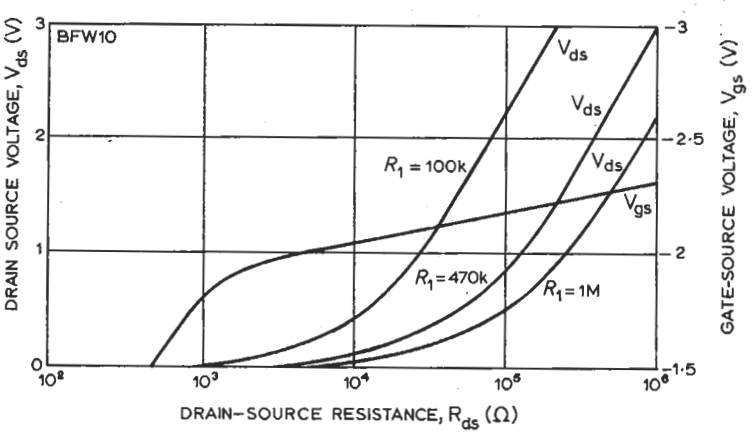

Fig. 2. Drain-source channel resistance characteristic of BFW10 for very low drain currents ($<30\mu A$). R_1 is a resistance in the drain circuit.

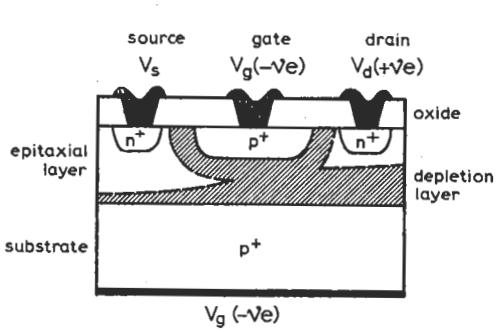

Fig. 1. When the two depletion regions meet in an epitaxial planar junction f.e.t., current in the device is independent of drain voltage variation.

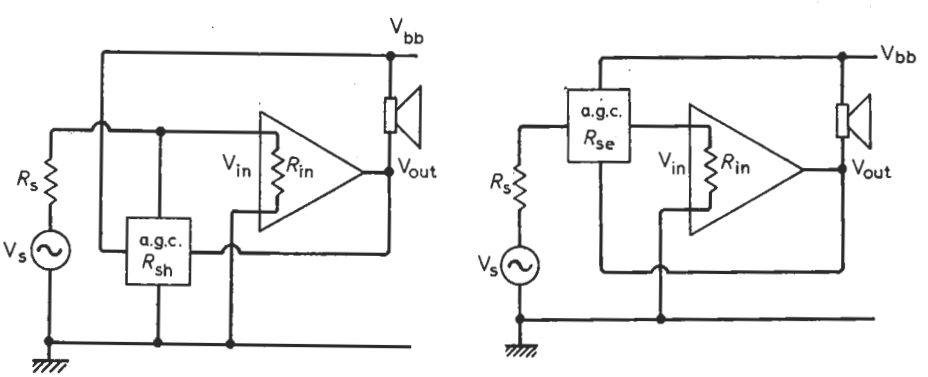

Fig. 3. Shunt a.g.c. system (a) has greater constraints on component values than series circuit (b).

amplifier is unaffected. For increasing V_s, above V_{s1}, the input to the amplifier is attenuated to prevent a corresponding increase in V_{out}. The limit of a.g.c. is shown for values of V_s approaching V_{s2} when maximum attenuation is supplied. Thus for effective a.g.c.

- $\dfrac{V_{o2}-V_{o1}}{V_{o1}} \ll \dfrac{V_{s2}-V_{s1}}{V_{s1}}$
- Attack time must be so short that sudden peaks of input signal can be controlled.
- Recovery rate must be slow enough for the distortion of 'volume compression' not to be detectable.
- For a given level of attenuation the a.g.c. element should behave as a linear circuit component.

In a shunt system, a.g.c. effectively shunts the input to the audio amplifier with a variable resistance, R_{sh}, controlled by the amplifier's output audio level V_{out}—Fig. 3(a). Using the terminology of Figs 3 and 4, the amount of attenuation provided by the shunt a.g.c. element is

$$\frac{V_{in}}{V_s} = \frac{R_{sh}.R_{in}}{R_s.(R_{in}+R_{sh})+R_{sh}.R_{in}} \quad (1)$$

There are two cases of shunt operation. With no shunt a.g.c. applied, $R_{sh} \gg R_{in}$, so equation 1 becomes

$$\frac{V_{in}}{V_s} \approx \frac{R_{in}}{R_s+R_{in}} \quad (2)$$

Thus for an output audio level less than the threshold a.g.c. level (V_{o1}) then R_{sh} should be very large compared with R_{in} and R_s should be very small compared with R_{in} for maximum signal transfer.

With shunt a.g.c. applied, $R_{sh} \ll R_{in}$, equation 1 becomes

$$\frac{V_{in}}{V_s} \approx \frac{R_{sh}}{R_s+R_{sh}} \quad (3)$$

Thus for appreciable attenuation of input signals greater than the threshold level then R_{sh} should be very much smaller than R_{in} and R_s. Indeed, for maximum attenuation the source impedance, R_s, should be very large indeed.

From these considerations there are two opposing requirements for the value of R_s. It can be shown by partial differentiation of equations 2 and 3 that there is an optimum value of R_s necessary to obtain the maximum attenuation range of the a.g.c. system, i.e. $R_s = R_{in}$. Thus a limitation of the shunt system is that, for a wide range of input signal attenuation, the choice of source impedance or input impedance of the amplifier is restricted.

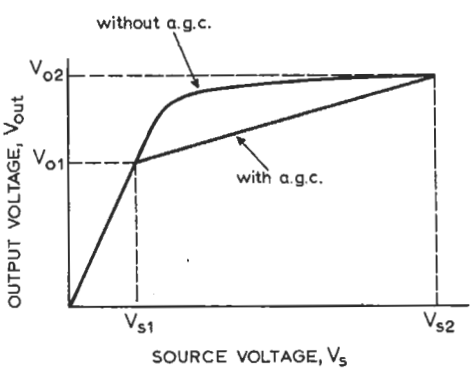

Fig. 4. Effect of a.g.c. on amplifier characteristic.

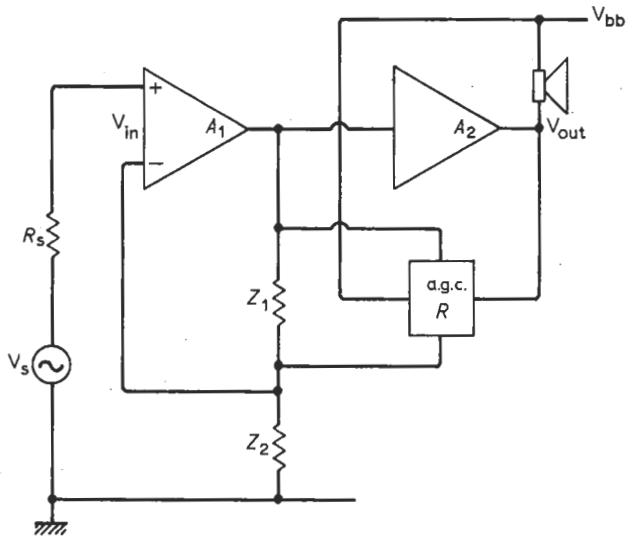

Fig. 5. Application of shunt circuit to feedback loop of first stage only, to avoid operating near knee of f.e.t.

For example, a shunt system having a minimum R_{sh} value of 1kΩ and designed to deliver 40dB of input signal attenuation, is useful only for an audio amplifier having R_s and R_{in} equal to and greater than 100kΩ.

The series a.g.c. stage provides a variable series resistance, R_{se}, in the input circuit of the amplifier, controlled by the amplifier's output audio level, V_{out}, Fig. 3(b). For larger audio output the series a.g.c. resistance increases, whereas the shunt resistance would have reduced in value.

Using the terminology of Figs 3 and 4, the amount of attenuation provided by the series element is

$$\frac{V_{in}}{V_s} = \frac{R_{in}}{R_s+R_{se}+R_{in}}$$

Thus for series a.g.c. there is no restriction on the value of the source impedance—for maximum signal transfer it should be as low as possible. But there is a restriction on the value of the input resistance of the amplifier. For an output audio level less than the a.g.c. threshold level the value of R_{se} should be very much less than R_{in} for unimpeded signal transfer. As there must be a lower limit to the value of R_{se}, it is beneficial for the value of R_{in} to be fairly high. For appreciable attenuation of input signals greater than the threshold value R_{se} should be very much larger than R_{in}. For maximum attenuation it would be beneficial for the value of R_{in} to be fairly low.

For example, a series system having a minimum R_{se} value of 1kΩ applied to an audio amplifier having a 10kΩ input impedance and driven from a 1kΩ source impedance would have the following characteristics

for $V_{out} \leqslant V_{o1}$ the input signal would be attenuated by 2dB;

for $V_{out} > V_{o2}$ the input signal could be attenuated by as much as the a.g.c. biasing circuitry allowed.

Hence, an advantage of the series a.g.c. system is that very large attenuation may be delivered as there is theoretically no limit on the maximum value of R_{se}. In practice the audio amplifier and associated circuitry of the series system limits the extent of available attenuation.

Feedback a.g.c.

A better system for a.g.c. would be to incorporate the controlled resistance element in the a.c. negative feedback loop of the audio amplifier. A shunt system of this type is shown in Fig. 5, where the a.c. negative feedback over the first stage of the amplifier is rapidly increased by shunting the impedance Z_1 with R, for output voltages above the required a.g.c. threshold, V_{o1}.

This type of a.g.c. system improves linearity, noise and amplitude response, but suffers from a limitation in signal handling capability.

Linearity of a controlled resistance arises because in saturation the drain of the f.e.t. is essentially isolated from the channel. However, large variations in drain voltage, especially when operating near to the knee of the output characteristic of the device, may introduce non-linear distortion. Thus there is a limit to the signal amplitude that can be applied to the drain.

Hence the system shown in the circuit of Fig. 5 incorporates shunt a.g.c. in the feedback loop of only the first stage of the amplifier.

Another way of overcoming this limitation is to apply series a.g.c. to the feedback loop. In applications where the d.c. and a.c. feedback loops are separated the f.e.t. could replace the impedance Z_2 of Fig. 5. This would allow the significant advantage of increased amplifier gain for low input signals thereby increasing the dynamic range of the audio amplifier.

Design considerations

A simple circuit is shown in Fig. 6 to illustrate the design requirements of a junction f.e.t. acting as a v.c.r.

The drain-source channel of the device provides the variable resistance, R, which is controlled by the voltage $V_{gs} = V_g - V_{so}$. It is convenient to keep the source voltage, V_{so}, constant so that the channel resistance, R, is rendered more sensitive to the gate voltage, V_g. This is effected by the potential divider incorporating resistors R_2 and R_3 which are chosen to give the required value of V_{so} and hold it constant against all drain-source current variations. When V_g is at earth potential, the value of V_{so} determines the maximum value of the channel resistance, and the a.g.c. threshold level, V_{o1}.

Resistor R_1 limits the drain current of the device to a convenient value and tends to speed up the change of the channel resistance with change of gate voltage. A large value of resistance must be chosen for R, as it shunts the channel resistance.

A stage is required to give a direct output voltage related to the output audio level, V_{out}, of the amplifier under a.g.c. Of the many circuits that can provide this function, a simple diode pump arrangement has been chosen as an example. Basic circuits for both shunt and series a.g.c. applications are shown in Fig. 7.

Although these driver circuits may be designed empirically, the process is much simplified by using a computer program for large signal analysis of simple non-linear systems. Such a program, specifically written for diode-pump applications, was used for the circuit shown in Fig. 9 (next issue).

Driver stage for shunt systems

Fig. 7(a) shows a basic pump circuit configuration for the driver stage of a shunt a.g.c. system. The transistor acts as a rectifier of controllable forward resistance and also as a high input impedance buffer stage, necessary to ensure that the audio output of the amplifier is not loaded by the a.g.c. circuitry.

It should be chosen for appreciable current gain at very low collector currents, very low leakage current and low collector series resistance. Hence a silicon epitaxial planar transistor such as the BC108, or possibly the BC109, would be suitable.

The resistors R_1' and R_2' bias the transistor off in its quiescent state and they must be sufficiently high-valued to avoid loading the output of the audio amplifier. It is important to bias the transistor just off to change the capacitor C to the maximum extent.

The requirements of the capacitor C are conflicting. It is necessary to find the best compromise between: a low value for a fast a.g.c. attack rate; a high value for a minimum of a.c. ripple on the output d.c. level of the driver stage; a low series impedance for minimum a.c. ripple; and a low leakage current, for the long period of charge storage necessary for slow a.g.c. recovery. These requirements suggest use of medium-valued solid tantalum electrolytic capacitors. However, the higher cost of these components would probably lead to their rejection in favour of the wet aluminium electrolytic capacitors. Although the use of these components is acceptable, the above requirements should be carefully considered.

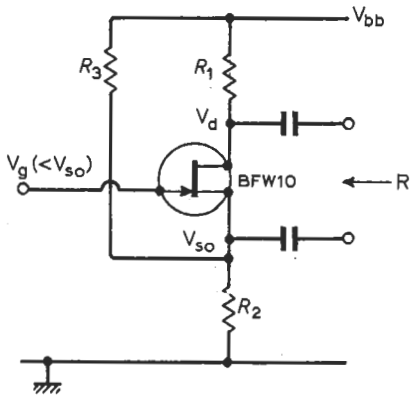

Fig. 6. Basic circuit for using a junction f.e.t. as a voltage-controlled resistance.

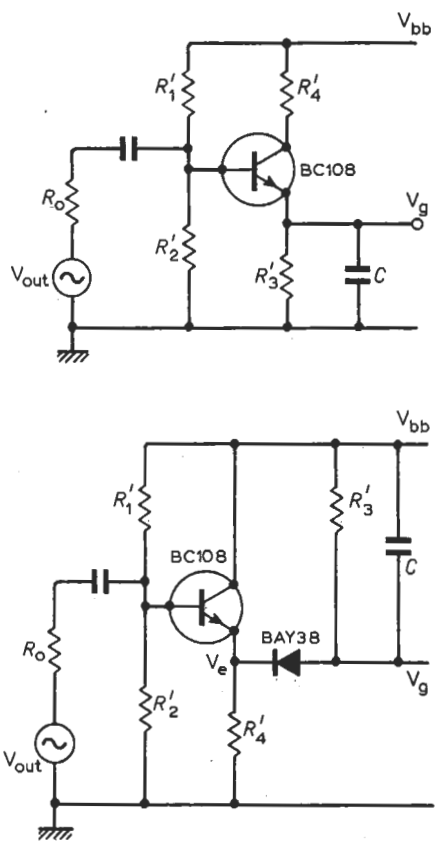

Fig. 7. Basic circuit of 'pump' driver stage for shunt system (a) and for series system (b).

Resistor R_4' determines the forward resistance of rectification and hence controls the charging rate of the capacitor C. Thus, the smaller the value of R_4' the faster the attack of the a.g.c. system.

Resistor R_3' can be chosen according to the required a.g.c. recovery time, the product CR_3' being the recovery time constant.

Driver stage for series systems

Fig. 7(b) shows a basic diode-pump circuit configuration for the driver stage of a series a.g.c. system. The circuit is almost identical to that shown in Fig. 7(a) for a shunt system and the same design considerations apply, except for two points. A diode is used in place of a transistor, for the essential non-linear element providing rectification. This diode should be chosen for very low leakage current and low series resistance. A silicon epitaxial planar diode such as the BAY38 would be suitable. The transistor in the circuit provides the same buffer impedance as in the shunt a.g.c. driver circuit. Also the transistor is biased so that the quiescent emitter voltage, V_e, provides the upper limit of the output d.c. level, V_g.

Parasitic a.g.c. action due to voltage spikes

Ideally there should be no transfer of signal between the gate and the drain of the f.e.t. In fact the gate should control only the channel resistance between the drain and source terminals. However, in the circuit configuration of Fig. 6 there is a d.c. transfer between the gate and drain (see Fig. 2) such that the a.g.c. attack is accompanied by a voltage spike at the input to the amplifier.

The presence of these voltage spikes is most critical at the threshold of operation and they can cause undesirable noises in the audio output of the amplifier and also aperiodic oscillation due to amplified spikes causing attack of the a.g.c. system followed by normal recovery. These deleterious consequences of the circuit arrangement of Fig. 6 may be satisfactorily minimized in one of three ways.

First, controlling the rate of change of the drain voltage, this transient condition can be altered to correspond to a signal well outside the frequency pass-band of the amplifier. As the higher transient speed is limited by the charging rate of capacitor C of the driver circuit (Fig. 7), it is advisable to slow the transient to correspond to a very low frequency. For example if the a.g.c. attack time-constant is 100ms then the transient will correspond to a signal frequency of less than 10Hz.

Secondly, by restricting the value of V_{ds} to a low value, for the a.g.c. off condition, the voltage spikes at the threshold can be effectively minimized. It can be seen from the curves of Fig. 2 that the higher the value of the resistance R_1 the lower the value of V_{ds} for a given value of channel resistance. Therefore in applications where the voltage spikes are problematic, it is advisable to choose a high-valued resistor for R_1—the upper limit being set by the extent to which the drain current may be reduced before noise problems occur. A good method of restricting V_{ds} is to shunt the drain of the f.e.t. to earth through a resistor. The value of V_d, and hence V_{ds} $(= V_d - V_{so})$ is fixed for the a.g.c. off condition by a potential divider, resistors R_1, R_{d1}, R_{d2} (not shown). The resistor R_{d1} is variable so that the required value of V_{ds} can be accurately set. The series resistance $R_{d1} + R_{d2}$ should be chosen to be very much larger than the input impedance of the amplifier to which a.g.c. is applied.

Thirdly, the drain voltage of the f.e.t. shown in the circuit of Fig. 6 can be kept constant during change of the channel resistance of the device, if the value of R_1 could be changed at exactly the same rate. This can be done by replacing R_1 with an identical f.e.t., as shown in Fig. 8. The operation of this circuit arrangement is

simply explained below, using the terminology of Fig. 8.

$$V_{d2} = \frac{V_{bb}}{1+\frac{R_{ds1}}{R_{ds2}}} \qquad (4)$$

$$V_{gs1} = V_{g1} - V_{d2}$$

$$V_{gs1} < 0$$

Consider two cases of a.g.c. operation. Suppose V_{d2} increases by a small amount due to a small increase in the value of R_{ds2}. In this case V_{gs1} becomes more negative. Therefore R_{ds1} increases, tending to restore the original value of V_{d2}. Suppose V_{d2} decreases by a small amount due to a small decrease in the value of R_{ds2}. In this case V_{gs1} becomes less negative. Therefore R_{ds1} decreases tending to restore the original value of V_{d2}.

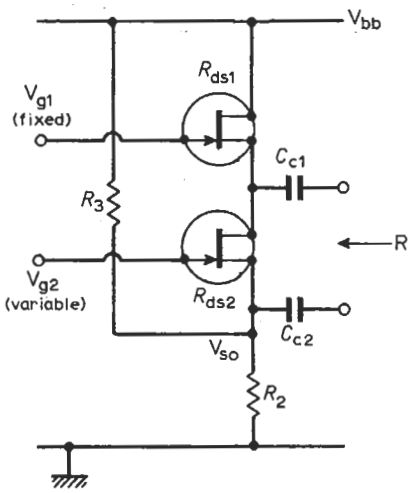

Fig. 8. Modification of Fig. 6 circuit to cancel voltage spikes that accompany a.g.c. attack.

Thus, the system is self-stabilizing, tending to reduce the change of V_{d2} to a minimum, for all values of the resistance, R. As can be seen from equation 4 this minimum depends on the degree of match of the characteristics of the two f.e.ts. The use of identical f.e.ts is becoming attractive for a.g.c. application with the advent of dual f.e.t. encapsulations and the facility to incorporate f.e.t. devices in bipolar integrated circuits.

Low frequency relaxation oscillation

For an amplifier with a.g.c., to maintain fidelity to incoming signals it is necessary that the a.g.c. system should have a fast attack and a very low recovery rate. Such a system is prone to low frequency relaxation oscillation for constant input signals of amplitude greater than the threshold.

This problem is obstructed by the voltage spike problem, which can also cause low frequency oscillation. However, these problems are independent, for if the d.c. transient at the drain of the f.e.t. is minimized the low frequency relaxation oscillation can still exist.

Referring to Fig. 3, it can be seen from the following argument that relaxation oscillation can occur in the a.g.c. system with a constant input signal that is sufficiently large to cause a.g.c. operation.

In practice there is a finite time delay in the attack of increases in input signal level. During this delay the amplifier's output signal has excessive amplitude, tending to cause the system to deliver maximum attenuation of the input signal. Thus for a short time the input signal to the amplifier is over-attenuated so that the amplifier output is reduced below the threshold, V_{o1}. The system recovers with a long time constant until V_{out} again exceeds V_{o1}, when the cycle repeats itself.

A solution to this problem would be found by speeding up the attack time. However, the minimum attack time is limited by the nature of the a.g.c. system's circuitry to several milliseconds. Consequently the problem must be solved by slowing down the attack time, to correspond to a low frequency at which the loop gain is insufficient for this oscillation to occur.

This delay can be effected by increasing the forward resistance of rectification of the driver circuit, shown in Fig. 7. Thus by increasing the value of the resistor R_4' the stability of the system can be improved. In practice resistor R_4' should be set at the lowest frequency for which a.g.c. is required.

As mentioned above this low frequency relaxation oscillation is complicated by the presence of the d.c. transient at the drain of the f.e.t., the so-called voltage spike. If the dual f.e.t. approach is adopted then it is probable that faster attack times would be possible without oscillation.

Failure of devices due to transients

During normal operation of an *n*-channel junction f.e.t. the controlling gate-source voltage is negative. Under this condition the input impedance at the gate terminal is very high indeed and very little gate current is taken. However, if this potential difference should become positive the input impedance would be very low indeed and an appreciable gate current would flow, limited only by external resistance in the circuit.

The limiting value of gate current for the BFW10 is given in the published data ratings as 10mA.

The junction f.e.t. in the circuit of Fig. 6 is most vulnerable during the transient conditions of switch-on and switch-off of the supply voltage. To provide protection for the device it is advisable to insert a large value of resistance in the gate circuit of the device.

(To be continued)