The Junction F.E.T. as a Voltage-controlled Resistance

2 — Practical circuits for communications use

by R. M. Lea, M.Sc.*

This article gives circuits for shunt and series automatic gain control, compression and expansion, squelch, and battery saving for communications receivers. The author concludes this two-part article by arguing that a.g.c. circuitry using function f.e.ts could be integrated into a.f. amplifier chips at very low cost. Part 1 of the article covered design points of a.g.c. systems and how to minimize unwanted effects.

The first article showed that the saturation region of the channel resistance characteristic of a junction f.e.t. renders the device suitable for operation as a voltage-controlled resistance. To demonstrate the ability of the device to operate in this role, a shunt a.g.c. system for an audio amplifier has been designed and constructed (Fig. 9).

The circuit has been designed to provide a.g.c. of an audio amplifier having the following characteristics

overall voltage gain	54dB
input impedance	50kΩ
output impedance	5Ω
sensitivity for maximum 'undistorted' output	8mV r.m.s.
3-dB bandwidth	250Hz to 3kHz

To avoid l.f. instability, two preset resistors are incorporated in the circuit. The 10kΩ potentiometer in the collector of the BC108 driver transistor controls the attack time and is adjusted to prevent oscillation for 250-Hz signals of amplitude greater than the a.g.c. threshold.

The 500kΩ potentiometer connected to the drain of the f.e.t. is adjusted to minimize the drain-source voltage for 250-Hz signals of amplitude well below the threshold level, without causing significant signal attenuation. By this means the parasitic a.g.c. attack due to voltage spikes at the drain of the f.e.t. is eliminated.

Performance of the shunt system is shown in Fig. 10 and its specification is

threshold	3.3V peak
attack time	20 to 50 ms
recovery time	15s
attenuation for 3dB increase in amplifier output	40dB
current consumption	200μA†

†Large peaks of input signal may cause instantaneous current of up to 5mA.

Suggested series a.g.c. system

A suggested circuit for the series system shown schematically in Fig. 3(b) is shown in Fig. 11. Designed according to the guidelines already given, it provides a.g.c. of an audio amplifier having the above performance. Input impedance of the amplifier has been changed to 10kΩ to give a wide range of attenuation.

Protection against l.f. instability is provided in the same way as for the shunt system. The series system should not suffer parasitic a.g.c. action because the audio amplifier is fed from the source of the f.e.t., which is at a constant potential.

Total current consumption of the series system should be a little more than 1mA. This increase over the shunt system is necessary because of the class A operation of the driver transistor.

Feedback series a.g.c. system

An example of a series a.g.c. system employed in the feedback loop of a simple pre-amplifier and driver stage is shown in Fig. 12. The a.g.c. system itself is that shown in Fig. 6 with a coupling capacitor omitted, and although a series system, the driver circuit is that shown in Fig. 7(a) for a shunt system, as channel resistance must decrease with increasing amplifier output.

Volume compression and decompression

Any of the series or shunt a.g.c. circuits discussed so far could be used for volume compression and decompression of audio signals with a simple modification to speed up the recovery of the v.c.r. stage so that the attack and recovery rates are the same.

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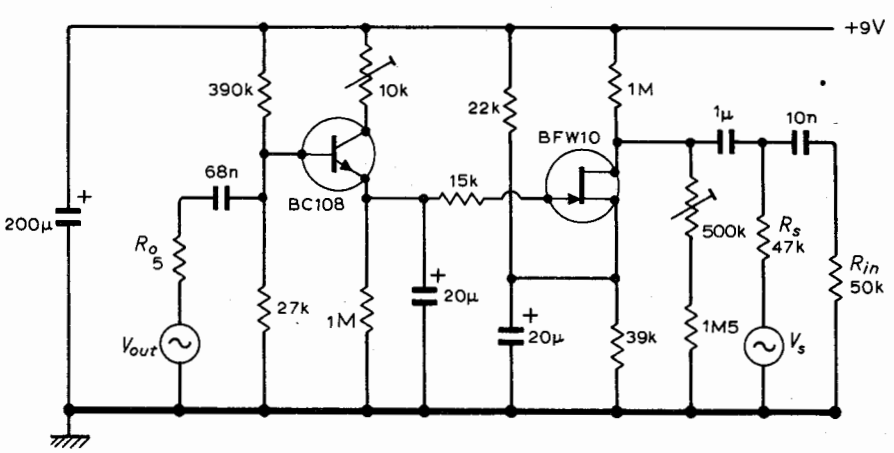


Fig. 9. Circuit of shunt a.g.c. system for voice operation (3-dB frequencies are 250Hz and 3kHz).

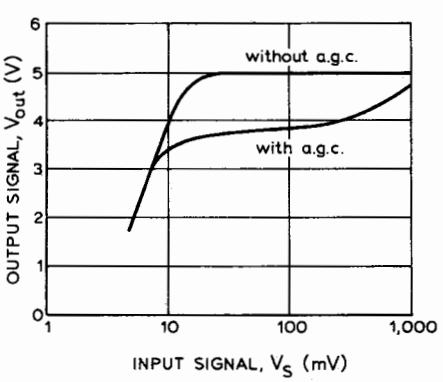


Fig. 10. Performance of Fig. 9 circuit. Attack time is tens of milliseconds and recovery time 15 seconds.

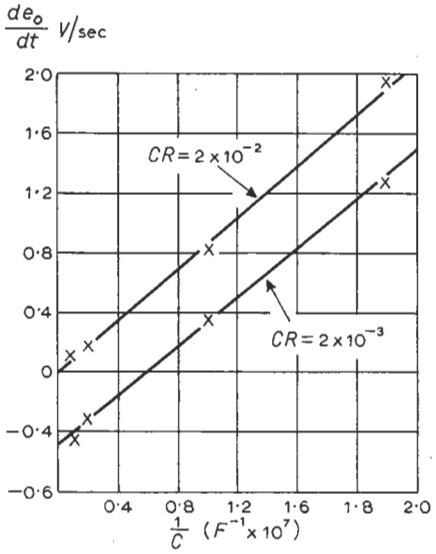


Fig. 4.2. Integrator drift rates.

For each CR value graphs of d_{eo}/dt against $1/C$ are plotted as shown in Fig. 4.2.

Inspection of eq. (4.2) shows that the slope of the graph gives the bias current, I_b^-, and the intercept on the d_{eo}/dt axis may be used to estimate a value for voltage V_{io}.

Examination of integrator action

The action of a simple integrator can be investigated using the circuit in Fig. 4.3.

A resistor equal in magnitude to the input resistor, R_i, is connected to the non phase-inverting input terminal of the amplifier in order to reduce drift due to amplifier bias current. The integrator input is connected to earth and the output is set to zero by momentarily closing the reset switch. The offset balance potentiometer (connected to terminals 1 and 5 of the i.c.) is now adjusted for minimum output drift, the output voltage being monitored with an oscilloscope or centre-zero voltmeter. It should be possible to obtain virtually zero drift.

The circuit performs the operation of integration on an input signal in the following manner. Suppose a −1V d.c. signal is applied to the input resistor (R_i = 1MΩ). This will draw a current of 1μA from capacitor C (1μF). In order to produce this

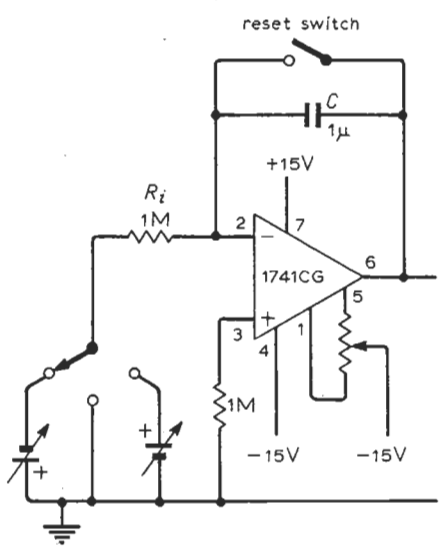


Fig. 4.3. Investigating integrator action.

current a continuously rising voltage must be generated at the output with a rate of rise equal to 1 volt/second. This rate of rise continues until the input voltage is changed or the amplifier output reaches saturation. If the input is switched to zero the output voltage of the amplifier ideally remains at the level reached when the input was removed. Suppose a +1V d.c. signal is now applied to R_i. This causes a charging current of opposite polarity in capacitor C and consequently a continuously falling voltage must be generated at the amplifier output with a rate of fall of 1 volt/second.

The integrator output level at the end of some interval of time is equal to: the sum of the products of each voltage times the period of each applied voltage divided by $-RC$. The change in output level during any time period is thus proportional to the area under the input volts/time graph for that period.

The action of the integrator can be verified experimentally by switching the input to known d.c. levels for measured periods of time while simultaneously monitoring the amplifier output voltage (see Fig. 4.4).

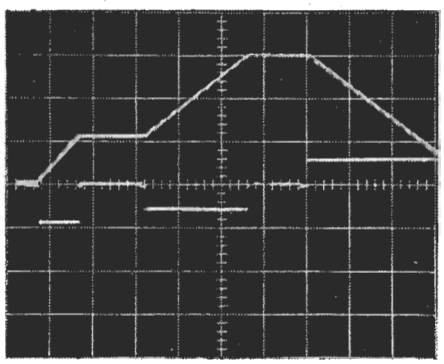


Fig. 4.4. Oscillograms showing integrator response to different input levels. Lower trace: input, 1V/div. vertically. Upper trace: output, 2V/div. vertically. Horizontal scale: 5s/div.

Staircase waveform generator

An operational integrator may be used to linearize the output of a simple diode pump circuit. A circuit is shown in Fig. 4.5.

A constant amplitude square wave, amplitude V_{in} (approximately 10V), and frequency f (say 400Hz), is applied to capacitor C_1. On the negative going part of the input square wave C_1 charged through diode D_1. On the positive going part of the square wave C_1 discharges through D_2, thus transferring a quantity of charge $C_1 V_{in}$ to the integrating capacitor C_2 and causing a step decrease in the output voltage of the amplifier. The step amplitude is equal to $C_1 V_{in}/C_2$ and the output falls in successive steps until the amplifier saturates or its output is reset to zero in some way. In the circuit in Fig. 4.5 the integrator output is reset to approximately zero by the action of the u.j.t., which is used to discharge capacitor C_2 when the voltage across it reaches some defined value. This value is determined by the d.c. voltage applied to b_2 (use about 6V).

Typical input and output waveforms are shown in Fig. 4.6. It is suggested that input frequency, input amplitude, unijunction b_2 voltage and finally capacitor values be changed in turn and the effects noted.

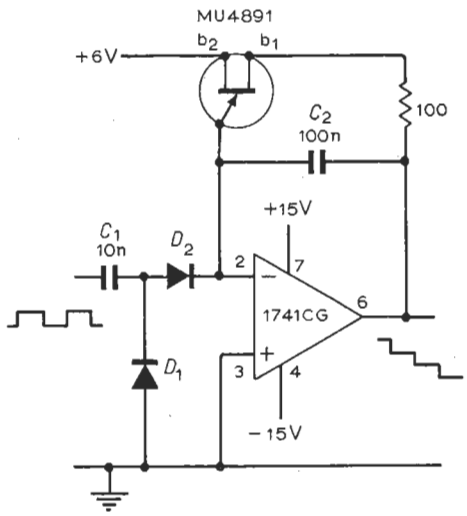


Fig. 4.5. Linear staircase generator.

Note. If a very low frequency square wave is used, integrator drift will cause the output to change appreciably between steps. In this case it will be necessary to add the usual offset balance potentiometer to the circuit and adjust for 'step flatness'.

Frequency to voltage conversion

The circuit in Fig. 4.5 may be modified so as to make the output of the amplifier a direct voltage of magnitude proportional to the frequency of a constant amplitude input square wave. The modification consists simply of replacing the u.j.t. with a resistor R connected in parallel with capacitor C_2. With this modification the charge transferred per second through D_2 (given by fC_1V_{in}), produces an average current

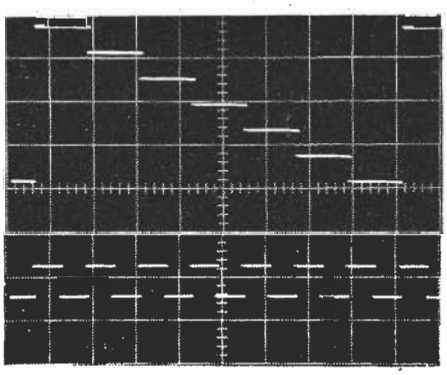


Fig. 4.6. Oscillograms showing typical input and output waveforms of Fig. 4.5 staircase generator. Lower trace: input square wave, 10V/div. vertically. Upper trace: output staircase, 1V/div. vertically. Horizontal scale: 2ms/div.

fC_1V_{in} through resistor R, and the amplifier gives an output voltage

$$e_o = -fC_1V_{in}R$$

It is suggested that resistor R be given a value 100kΩ. The input frequency should be increased in steps and the output voltage measured for each value of the input frequency. A graph of output voltage against input frequency should be plotted, the slope of this line being equal to $C_1V_{in}R$. Component values may be changed and the experiment repeated.

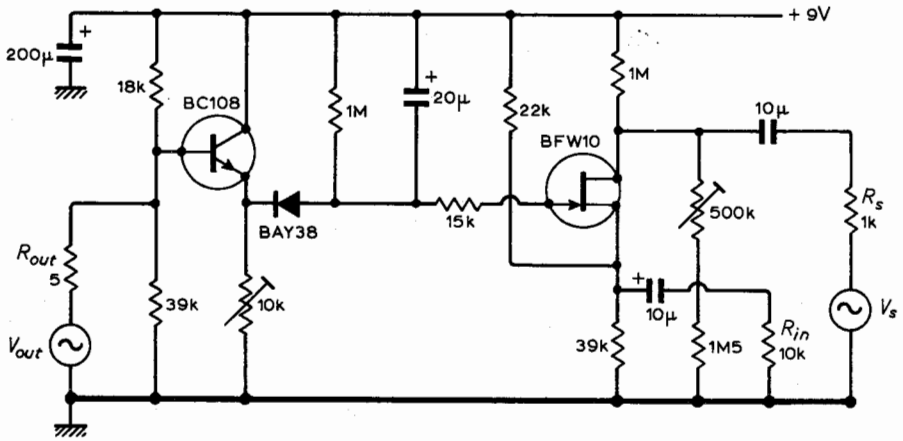
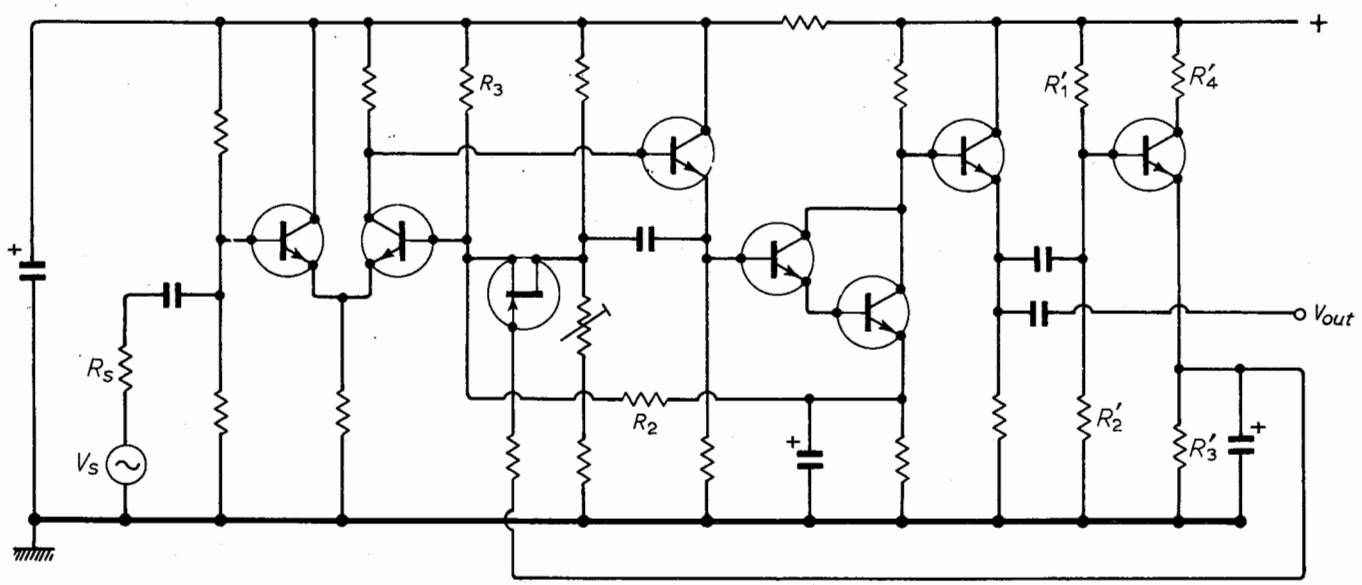


Fig. 11. Series a.g.c. circuit has same performance as shunt circuit.

Fig. 12. Simple pre-amplifier and driver with a.g.c. circuit of Fig. 6 incorporated into the feedback loop. Although a series circuit, it uses the shunt driver of Fig. 7(a).



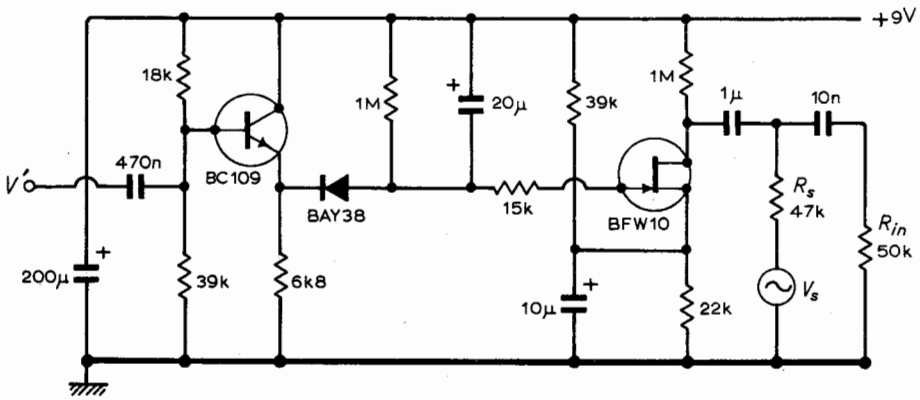


Fig. 13. Squelch system using shunt circuit. Output of the receiver detector is shown as V_s. Signal at V' is provided by pre-amplifier at Fig. 14.

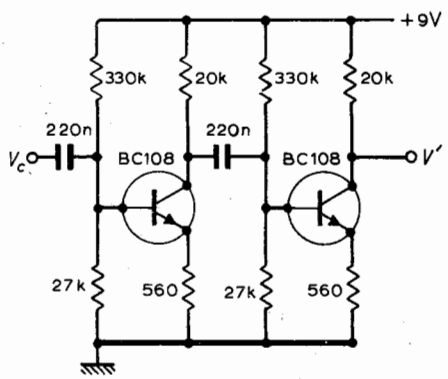


Fig. 14. Amplifier for control voltage fed to squelch circuit provides voltage gain of 56dB.

Recovery rate can be adjusted by varying the value of the resistor R_3' in the driver circuit of Fig. 7. In those cases where attack is very fast it is advisable to employ a variable resistor for R_3'. However, where the attack rate is retarded by a large-value resistor R_4' then the same value could be used for R_3' without need for a preset resistor.

A shunt volume compression system for audio signals would require a driver stage of the form shown in Fig. 7(a). However if the driver stage of Fig. 7(b) were used, the system would provide volume decompression. The system is not as sensitive as that suggested for a.g.c. operation because the d.c. output level reaches only half the peak output voltage.

Automatic squelch circuits

An a.g.c. system containing a junction f.e.t. offers an attractive squelch possibility for audio amplifiers in communications receivers. In this application the f.e.t. is used as a switch. Reference to Fig. 2 shows that a change in V_{gs} of less than 0.5 volts will turn the device from an off to an on state. Thus by preceding the a.g.c. system with a stage of voltage amplification, fairly small signals can operate the squelch circuit. The stage may be controlled either by received carrier or audio signal. The threshold level would be set just above the receiver noise level, so only the required audio signal would be amplified. The squelch would operate some several seconds after the cessation of carrier or audio signal. As the squelch circuit will be either on or off, the problem of l.f. instability, and consequent protective measures, does not apply.

Of course the squelch can be operated manually by supplying the required direct voltage at the f.e.t. gate. This would normally be effected when switching from the

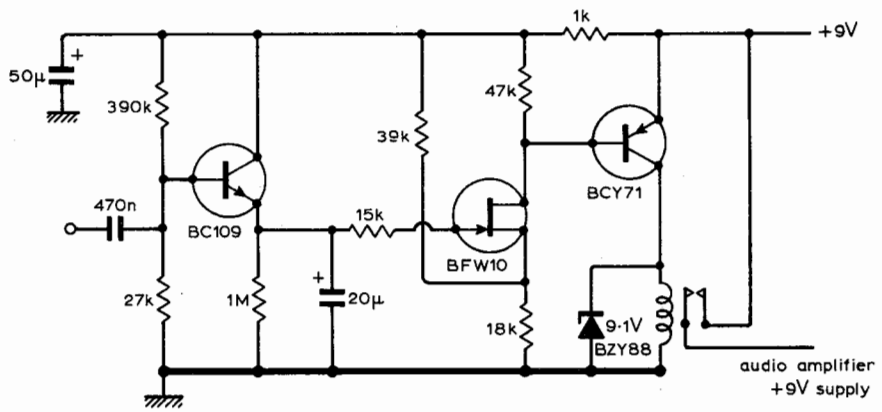


Fig. 15. Battery-saving circuit interrupts receiver supply 15 seconds after cessation of an audio signal, but switches on in a few milliseconds.

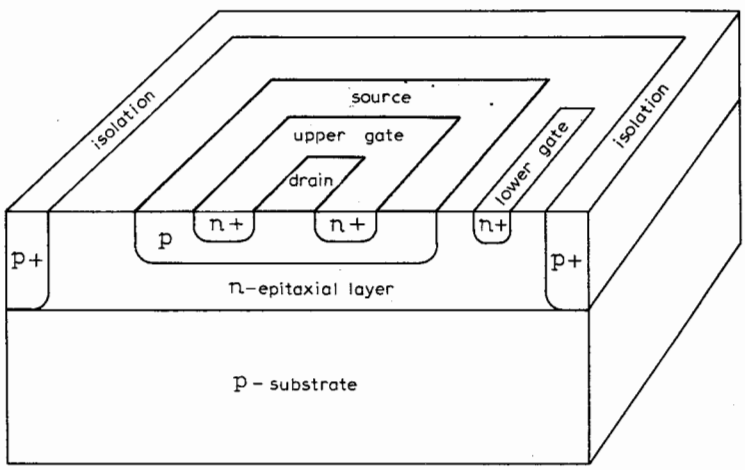


Fig. 16 Junction f.e.ts could be integrated with conventional bipolar i.cs, as the consequent degraded performance is probably acceptable for a.g.c. use.

receive mode to the transmission mode of operation of the transceiver.

A practical shunt circuit for a squelch facility is shown in Fig. 13. The circuit has been designed to provide squelch for an amplifier having an input impedance of 50kΩ, and a -3dB frequency of 250Hz. The output of the detector stage of the receiver is shown as the voltage source V_s in the diagram.

Pre-amplification of the control signal necessary for squelch operation may be attained using a circuit such as that of Fig. 14. This stage provides a voltage gain of about 56dB, with quiescent current of less than 500μA.

The control signal may be derived either from the carrier signal or the audio modulation in the receiver. In the case of a.m. receivers the control signal can be taken at the detector stage. The audio amplifier would then be 'un-squelched' by the d.c. output of the detector stage, due to carrier switch-on. As the squelch circuit is a.c. coupled, the squelch will operate about 15s after the cessation of audio signal.

In the case of f.m. receivers the squelch may be voice or carrier operated. For a voice-operated squelch the control signal can be taken from the detector output. However for carrier operation it is usual to monitor the d.c. output of a noise detector. For a noise output there is no carrier present and the squelch is in operation. For zero noise output a carrier signal exists and consequently the audio amplifier is un-squelched. In this case the v.c.r. stage of the squelch circuit would be driven by a circuit of the type shown in Fig. 7(a) rather than by that shown in Fig. 7(b).

Battery saving circuit

As an audio amplifier can incur a considerable power drain in portable transceivers it is preferable that the power supply to the amplifier is interrupted during the absence of received signal. Thus a switch, controlled either by the presence of a carrier or audio signals in the receive mode of operation, would be very useful for battery economy. A practical circuit for such a switch is shown in Fig. 15. This circuit supplies an a.f. amplifier with a 9-V potential within a few milliseconds of receiving a carrier or audio signal in the transceiver. Fifteen seconds after the cessation of the signal the supply potential is interrupted.

The junction f.e.t. in integrated circuits

The planar construction of present-day junction f.e.t. would seem to render the device suitable for integration in monolithic circuits. However integration has been found difficult due to the high degree of control required for impurity concentrations and dimensions of the device. For example, a small decrease in the channel resistivity can cause a large increase in the threshold voltage of the device*. Large values of the threshold voltage are clearly unsuitable for integrated circuit applications. Nevertheless these difficulties could disappear as integrated-circuit technology develops.

Of interest in the context of this article is the possibility of integrating a junction f.e.t. into monolithic audio amplifiers using bipolar transistors. It might be worthwhile to integrate a signal-amplitude control circuit on a separate monolithic chip.

Because the dimensional and resistivity requirements of the junction f.e.t. are different from those of n-p-n bipolar transistors a choice must be made between two options.

The first is a modified device fabrication process, in which the processes of epitaxy and diffusion are applied to arrive at the best compromise between bipolar and field-effect transistor performance. Being a deviation from the standard i.c. production processes this would result in a high cost per chip unless circuits of general applicability are considered. The process could be confined to production of signal amplitude control components suitable for most of the applications discussed.

The second option is the conventional bipolar fabrication process with an additional component having a degraded but f.e.t.-like performance. For applications like those discussed, where integration may be commercially viable, this second option may be useful. With this process the signal-amplitude control circuitry may be included in the audio amplifier monolithic circuits at very low cost.

As the f.e.t. is used at low frequencies for its well-controlled channel resistance property, a device having a degraded performance will quite likely be acceptable. An example of such a device is the p-channel depletion-mode junction f.e.t. shown schematically in Fig. 16. (For this particular device it would be necessary to reverse the polarities of the biasing circuitry shown earlier.)

*R. M. Berger and R. P. Donovan 'Fundamentals of silicon integrated device technology, Vol. 2' Prentice Hall 1968, pp.411-3.