APPLICATION NOTE 947

Understanding HEXFET® Switching Performance

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Abstract

A simple analytical technique for predicting the switching performance of the HEXFET is presented.

Closed-form solutions for the gate voltage, drain current, and drain voltage during the switching interval, in terms of each of the relevant device and circuit parameters, are derived.

A specific design example is considered, in which the effects are demonstrated of the drive circuit resistance, drain circuit inductance, and drive voltage, on the switching time and switching energy.

I. Introduction

The HEXFET is an almost ideal switch, which is characterized by very high gain and extremely fast switching characteristics. While users often ignore the intricacies of the switching operation, on the assumption that this is not critical to the overall design, the fact is that a clear understanding of the factors that affect switching can have a profound effect upon the system performance, particularly in high frequency circuits, and is, therefore, of vital interest to the user who needs to optimize his design.

Another reason why many users have a rather incomplete understanding of the HEXFET's switching operation is that the device is still relatively new, and HEXFET circuit design know-how has not yet matured. Users also tend to relate to their experience with bipolar transistors. The switching operation of bipolars is very difficult to analyze, and hence an empirical "try it and see" approach has generally held sway over more rigorous analytical techniques.

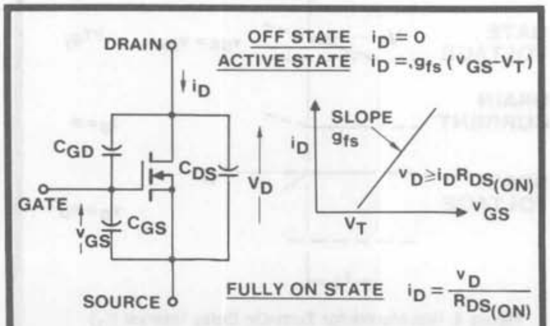


Figure 1. Electrical Model for HEXFET

One of the major "incidental" benefits of the HEXFET—in addition to its very real operating advantages—is that it lends itself rather well to analytical modeling; its operation can, therefore, be predicted rather easily at the design stage.

The primary objective of this application note is to show how, starting with a simple model of the HEXFET and using logical reasoning, the principles that govern the HEXFET's operation in a switching circuit can be readily predicted, and approximate mathematical relationships that describe these waveforms can be readily derived. Emphasis will be placed upon an understanding of basic principles.

II. The HEXFET Model

The electrical model for the HEXFET is shown in Figure 1. The self-capacitances are actually nonlinear functions of the applied voltage; also, to some extent, of the drain current. For purposes of analysis, however, these capacitances will be assumed to have fixed values; this does not detract from our basic objective, which is to understand fundamental principles.

This simple model of the HEXFET is assumed to have a linear transfer characteristic, with slope g_{fs} and gate threshold voltage V_T. The external drain current is assumed to be instantaneously responsive to the gate voltage, for operation in the active region.

Under transient switching conditions, charging and discharging currents flow through the various self-capacitive elements. The paths for components of these currents is through the drain-to-source terminals. The presence of these internal capacitive currents is assumed *not* to affect the transfer characteristic between the gate voltage and the external drain current.

The presence of C_{DS} will also generally be ignored for operations in the active region. This is valid because the effect of the gate-to-drain capacitance C_{GD}—providing, as it does, a coupling path from the drain circuit to the relatively sensitive gate circuit—generally "swamps" the effect of C_{DS}.

III. The Circuit Model

The clamped load is assumed to have sufficient inductance that the current flowing in it has a constant value I_O throughout the switching interval (Figure 2). The inductance L_ℓ represents "unclamped" stray circuit inductance.

The effect of the common source inductance L_S, shown dashed in Figure 2, will generally be neglected. This is not

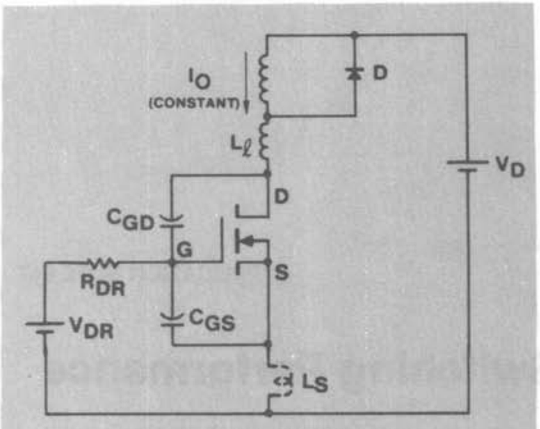


Figure 2. General Circuit Model

because it is necessarily negligible, but because to include it in a general analysis complicates the issue, making clarity of presentation and a grasp of fundamental principles more difficult. We prefer instead to consider the modifying effect of this inductance once the basic analysis is complete.

A number of switching circuits can be resolved into the equivalent circuit shown in Figure 2, or variants thereof, and in this sense the analysis is fairly general. The main point, however, is that the chosen circuit serves as a vehicle for obtaining an understanding of basic principles; once this has been accomplished the designer will be well equipped to deal with the switching operating of the HEXFET in any circuit.

IV. Nomenclature

v_D	Instantaneous drain-source voltage
v_{GS}	Instantaneous gate-source voltage
v_{GD}	Instantaneous gate-drain voltage
V_D	Steady applied drain circuit voltage
V_{DR}	Applied positive gate drive voltage (turn-on)
V_T	Gate threshold voltage
V_F	Positive gate drive "forcing" voltage ($V_{DR} - V_T$)
$-V_2$	Applied negative gate drive voltage (turn-off)
V_D*	Initial value of drain-source voltage at start of interval
$V_{GS}*$	Initial value of gate-source voltage at start of interval
V_{CLAMP}	Drain-source clamping voltage
i_D	Instantaneous current flowing into drain terminal
i_{GS}	Instantaneous current in C_{GS}
i_{GD}	Instantaneous current in C_{GD}
I_O	Steady current in clamped inductive load
I_D*	Initial value of current flowing into drain terminal at start of interval
R_{DR}	Gate drive circuit resistance
$R_{DS(ON)}$	On-state resistance of HEXFET
R_ℓ	Stray drain circuit resistance
L_ℓ	Stray drain circuit inductance
L_S	Inductance in series with source that is common to gate circuit
C_{GS}	Gate-source capacitance of HEXFET
C_{GD}	Gate-drain capacitance of HEXFET
C_{DS}	Drain-source capacitance of HEXFET
C_G	$C_{GS} + C_{GD}$
C_D	$C_{DS} + C_{GD}$
g_{fs}	Transconductance of HEXFET
p	Differential operator

V. Analysis of Switching Operation

Each switching sequence, either from the OFF to the ON condition, or vice versa, is subdivided into a number of separate intervals, for which different constraints and conditions apply. Each interval will be considered in sequence. The end-conditions for one interval become the starting conditions for the next. For simplicity we will take t = 0 at the start of each new interval.

The approach will be to consider each time interval in a qualitative manner, and through a process of reasoning based upon the known conditions and constraints, deduce as much as we can about the general shapes of the dynamic waveforms of drain voltage, drain current and gate voltage.

For certain time intervals this qualitative reasoning leads directly to the parametric analytic solution for that interval; for other time intervals, however, the analytic solutions are not so quickly obtained, except for parametric extremes at each end of the possible spectrum of external circuit conditions; a wide middle range of conditions remains for which derivation of the parametric solutions is rather too lengthy to be presented in its entirety, and in these cases we will simply state the final solutions.

A. TURN-ON

Turn-On Delay Interval 1

The circuit model for this interval is shown in Figure 3, and operating waveforms are shown in Figure 4. The applied drive

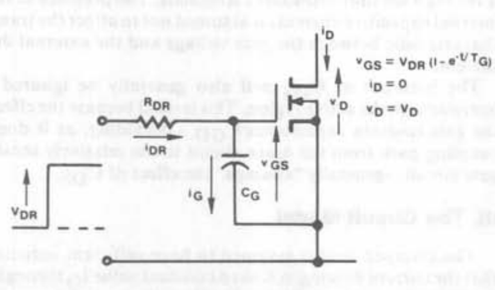


Figure 3. Circuit Model for Turn-On Delay Interval

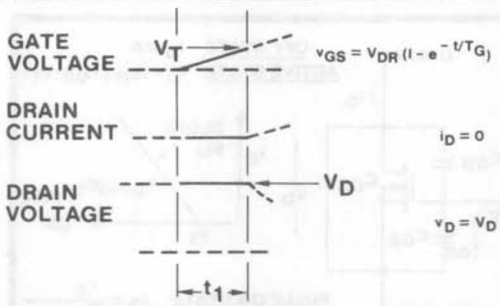


Figure 4. Waveforms for Turn-On Delay Interval (t_1)

voltage is assumed to rise instantaneously to its full value; however, the voltage actually appearing between the gate and source terminals, which directly controls the external drain current, rises at a finite rate determined by the gate-to-source and drain-to-source self-capacitances. No drain current flows so long as the gate voltage is less than the threshold voltage, V_T. The end of the turn-on delay period is defined as the point at which the gate-to-source voltage becomes equal to the threshold voltage.

The analytic solution for the turn-on delay is almost trivial. Since no drain current flows, the drain voltage remains at V_D. Both the "drain" terminal of C_{GD} and the "source" terminal of C_{GS} sensibly do not change their potentials. The drive source voltage, V_{DR}, 'sees' the parallel combination of $C_{GD} + C_{GS} = C_G$, through the series resistor R_{DR}. The gate-to-source voltage v_{GS} follows a classical exponential:

$$v_{GS} = V_{DR}\left(1 - e^{-t/T_G}\right) \tag{1}$$

where

$$T_G = R_{DR}C_G \tag{2}$$

Turn-On Interval 2

The general circuit model for this interval is shown in Figure 5. The drain current now rises as the drain voltage falls. Which of these events is completed first depends upon the external circuit parameters. When one of these events is completed (or both simultaneously) the interval ends.

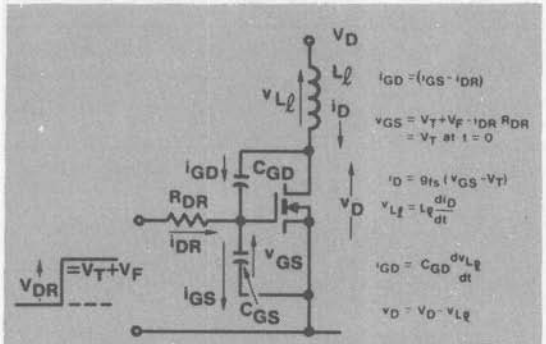


Figure 5. General Circuit Model for Switch-On Interval 2

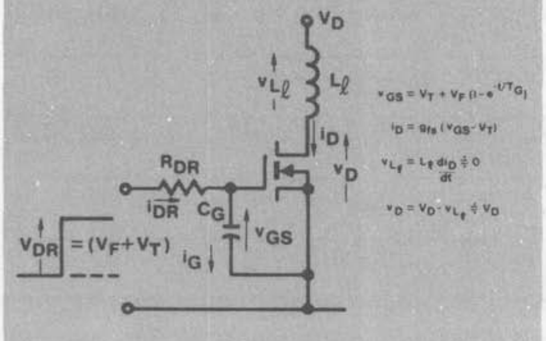


Figure 6. Circuit Model for Switch-On Interval 2 Small L_ℓ/R_{DR}

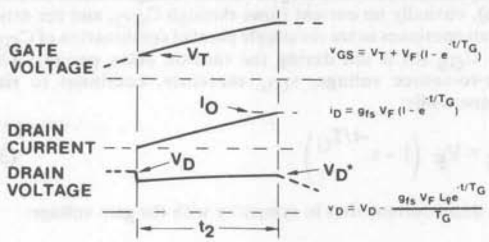


Figure 7. Waveforms for Turn-On Interval 2 Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10C_{GD}g_{fs}}$$

Since the drain current i_D is less than the current I_O throughout this period, the difference between I_O and i_D must continue to circulate in the freewheeling rectifier D, forcing this diode to stay in conduction. This keeps the potential at the "top" of L_ℓ virtually constant at V_D.

As the gate-to-source voltage rises above the threshold level, the drain current starts to increase since drain current is proportional to gate voltage. The drain voltage also starts to fall because the increasing drain current induces a voltage across L_ℓ. As the drain voltage falls, current i_{GD} flows out of the "Miller" capacitance C_{GD}; this current is drawn from the drive source, and deprives the gate-source capacitance C_{GS} of a portion of the charging current it would otherwise have received. This, in turn, reduces the rate of change of gate voltage, and hence also of drain current.

A dynamically "intertwined" situation obviously exists, by virtue of the "negative feedback" effect that couples the drain circuit to the gate circuit via the "Miller" capacitance C_{GD}. The "strength" of this feedback depends upon the ratio of the external circuit parameters L_ℓ to R_{DR}, as we will now see.

Large L_ℓ means large impedance to the rate of change of drain current, while small R_{DR} means fast gate circuit response, and hence potentially fast rate of change of drain current. With a high ratio of L_ℓ to R_{DR} the reactance of the drain circuit will therefore be high, the voltage drop across L_ℓ will be high, the "Miller" effect will predominate, and the rate of change of drain current will be unable to match the applied gate circuit stimulus. High L_ℓ/R_{DR}, therefore, means that the switching speed is severely limited by the constraints of the drain circuit; the drive circuit is "too fast" for the drain circuit.

Small L_ℓ/R_{DR} ratio means just the opposite; the potential rate of change of drain current is now much faster than the drive circuit actually allows. The voltage drop across L_ℓ is small, the "Miller" effect is small, and the gate circuit largely controls the switching time, virtually unimpeded by the drain circuit. Both of these extreme conditions are rather easy to analyze.

For intermediate L_ℓ/R_{DR}, the drain circuit and gate circuit responses can be envisioned as being reasonably "compatible" with one another. From a purist's viewpoint, compatibility of the gate and drain circuit responses might be considered to be the "correct" design point, because the gate circuit is neither too fast nor too slow for the drain circuit.

Small L_ℓ/R_{DR}

We will start the analysis by considering the situation when L_ℓ/R_{DR} is small. The circuit model is shown in Figure 6, and switching waveforms are shown in Figure 7. Since there is very little voltage developed across L_ℓ, the drain voltage v_D stays virtually at the circuit voltage, V_D, until the drain current has risen to its full load value I_O.

Because the rate of change of drain voltage is small (almost zero), virtually no current flows through C_{GD}, and the drive circuit continues to see the simple parallel combination of C_{GD} and C_{GS} (as it did during the turn-on delay period). The gate-to-source voltage, v_{GS}, therefore, continues to rise exponentially:

$$v_{GS} = V_F \left(1 - e^{-t/T_G}\right) \tag{3}$$

The drain current rises in sympathy with the gate voltage:

$$i_D = g_{fs} V_F \left(1 - e^{-t/T_G}\right) \tag{4}$$

The drain voltage is equal to the circuit voltage V_D, less the small (almost negligible) voltage drop across L_ℓ:

$$v_D = V_D \frac{g_{fs} V_F L_\ell e^{-t/T_G}}{T_G} \tag{5}$$

The period ends when $i_D = I_O$.

It remains to quantify how small the ratio L_ℓ / R_{DR} must be for equations (3) through (5) to remain valid. The essential condition is that the rise of drain current must, for all practical purposes, be exclusively under the influence of the applied drive voltage. This means that whatever voltage change occurs across L_ℓ should not be noticed in the gate circuit. The current through C_{GD} will, therefore, be small by comparison with the current through C_{GS} (C_{GS} is typically about 10 x C_{GD}; however, a sufficiently large voltage change at the drain would produce a current through C_{GD} which is comparable to or larger than that through C_{GS}.

The essential condition therefore is that i_{GD} [$\doteq C_{GD}$ (dv_D/dt)] should be small by comparison with i_{GS} [$\doteq C_{GS}$ (dv_{GS}/dT)].

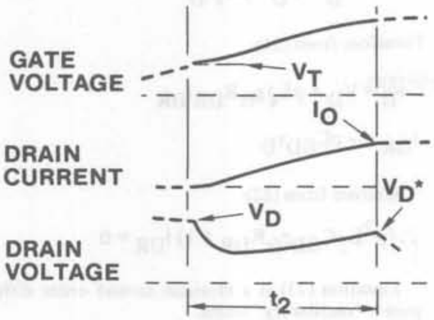
By differentiation of equations (3) and (5), this yields:

$$\frac{L_\ell}{R_{DR}} << \frac{C^2{}_{GS}}{g_{fs} C_{GD}} \tag{6}$$

Table 1 puts the above criterion into perspective, and shows typical value of L_ℓ and the corresponding "minimum" values of R_{DR}, for various HEXFETs. Clearly the values of R_{DR} needed to satisfy this condition are very high relative to most

Table 1: Limiting values of R_{DR} that define which equations (turn-on interval 2, and turn-off interval 3) are applicable, for various HEXFETs.

		Small L_ℓ/R_{DR}	Intermediate L_ℓ/R_{DR}		Large L_ℓ/R_{DR}
		$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}{}^2}{10C_{CG}g_{fs}}$	$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}{}^2}{4C_{GD}g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}{}^2}{4C_{GD}g_{fs}}$	$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}{}^2}{C_{GD}g_{fs}}$
Applicable Equations		3-5, 37-39	8-10, 40-42	14-16, 43-45	24-26, 46-48
IRF510 (100V, 2.5A)	L_ℓ 100 nH	R_{DR}-2.4kΩ min	R_{DR}-960Ω min	R_{DR}-960Ω max	R_{DR}-40Ω max
	L_ℓ 1 μH	R_{DR}-24kΩ min	R_{DR}-9.6kΩ min	R_{DR}-9.6kΩ max	R_{DR}-400Ω max
IRF130 (100V, 9A)	L_ℓ 100 nH	R_{DR}-1.3kΩ min	R_{DR}-520Ω min	R_{DR}-520Ω max	R_{DR}-20Ω max
	L_ℓ 1 μH	R_{DR}-13kΩ min	R_{DR}-5.2kΩ min	R_{DR}-5.2kΩ max	R_{DR}-200Ω max
IRF150 (100V, 25A)	L_ℓ 100 nH	R_{DR}-410Ω min	R_{DR}-165Ω min	R_{DR}-165Ω max	R_{DR}-6Ω max
	L_ℓ 1 μH	R_{DR}-4.1kΩ min	R_{DR}-1.65kΩ min	R_{DR}-1.65kΩ max	R_{DR}-60Ω max
IRF710 (400V, 1A)	L_ℓ 100 nH	R_{DR}-620Ω min	R_{DR}-325Ω min	R_{DR}-325Ω max	R_{DR}-13Ω max
	L_ℓ 1 μH	R_{DR}-6.2kΩ min	R_{DR}-3.25kΩ min	R_{DR}-3.25kΩ max	R_{DR}-130 max
IRF330 (400V, 3.5A)	L_ℓ 100 nH	R_{DR}-420Ω min	R_{DR}-170Ω min	R_{DR}-170Ω max	R_{DR}-7Ω max
	L_ℓ 1 μH	R_{DR}-4.2kΩ min	R_{DR}-1.7kΩ min	R_{DR}-1.7kΩ max	R_{DR}-70Ω max
IRF350 (400V, 9A)	L_ℓ 100 nH	R_{DR}-120Ω min	R_{DR}-50Ω min	R_{DR}-50Ω max	R_{DR}-2Ω max
	L_ℓ 1 μH	R_{DR}-1.2kΩ min	R_{DR}-500Ω min	R_{DR}-500Ω max	R_{DR}-20Ω max



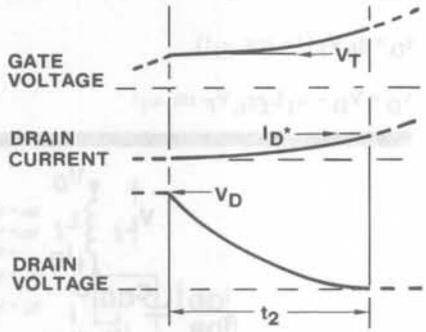
$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\}$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\left(T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right)\right\}$$

$$v_D = \frac{V_D - g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\}$$

Figure 8(a). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}{}^2}{10C_{GD}g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{C_{GS}{}^2}{4C_{GD}g_{fs}}$$



$$v_{GS} = V_T + V_F - V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$i_D = g_{fs} V_F - g_{fs} V_F e^{-t/T_3}\left\{\cos \omega_3 t + \frac{1}{\omega_3 T_3} \sin \omega_3 t\right\}$$

$$v_D = V_D - g_{fs} V_F \omega_3 L_\ell e^{-t/T_3}\left\{1 + \frac{1}{\omega_3{}^2 T_3{}^2}\right\} \sin \omega_3 t$$

Figure 8(b). Waveforms for Turn-On Interval 2, Intermediate L_ℓ/R_{DR}

$$\frac{C^2{}_{GS}}{4C_{GD}g_{fs}} < \frac{L_\ell}{R_{DR}} < 10\,\frac{C^2{}_{GS}}{C_{GD}g_{fs}}$$

normal application requirements. This condition will not, therefore, be frequently met in practice; its consideration here is useful, however, because it helps to introduce the overall problem.

Intermediate L_ℓ/R_{DR}

We will now consider the situation when the ratio of L_ℓ/R_{DR} is not small, but has some intermediate value; the voltage drop across L_ℓ due to the increasing drain current becomes significant, and the current through C_{GD} cannot be neglected. The general circuit model of Figure 5 applies, and typical switching waves are illustrated in Figure 8(a) and (b).

The mathematical analysis is a little too lengthy to keep touch with physical realities. We will, therefore, confine ourselves to a simple statement of the results.

There are two possible sets of solutions, depending upon whether or not the system is critically damped. If overdamped, then:

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}{}^2}{4C_{GD}g_{fs}} \tag{7}$$

Note the similarity of condition (7) to (6). Table 1 also shows typical values of L_ℓ and corresponding minimum values of R_{DR} that satisfy equation (7). This condition is certainly more likely to be encountered than condition (6), though once again it is generally not representative of most typical practical situations.

The gate voltage, v_{GS}, the drain current, i_D, and the drain voltage v_D, are:

$$v_{GS} = V_T + V_F - \frac{V_F}{(T_1 - T_2)}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \tag{8}$$

$$i_D = g_{fs} V_F \left\{1 - \frac{1}{(T_1 - T_2)}\right\}\left\{T_1 e^{-t/T_1} - T_2 e^{-t/T_2}\right\} \tag{9}$$

$$v_D = V_D - \frac{g_{fs} V_F L_\ell}{(T_1 - T_2)}\left\{e^{-t/T_2} - e^{-t/T_1}\right\} \tag{10}$$

where

$$T_1 = \frac{2L_\ell C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} + \sqrt{R^2{}_{DR} C^2{}_{GS} - 4L_\ell C_{GD} R_{DR} g_{fs}}} \tag{11}$$

$$T_2 = \frac{2L C_{GD} R_{DR} g_{fs}}{R_{DR} C_{GS} - \sqrt{R_{DR}{}^2 C_{GS}{}^2 - 4L_\ell C_{GD} R_{DR} g_{fs}}} \tag{12}$$

The end of the time interval will generally be marked by the drain voltage having fallen all the way to $i_D \times R_{DS(ON)}$, with the drain current not having completed its rise.

For an "underdamped" system, the converse of (7) applies:

$$\frac{L_\ell}{R_{DR}} > \frac{C_{GS}^2}{4C_{GD}g_{fs}} \tag{13}$$

The minimum values of R_{DR} shown in Table 1 that satisfy equation (7) now become the maximum values that satisfy equation (13). Generally, most practical situations will be covered by equation (13).

The gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are:

$$v_{GS} = (V_T + V_F) - V_F e^{-t/T_3} \left\{ \cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3} \right\} \tag{14}$$

$$i_D = g_{fs} V_F - g_{fs} V_F e^{-t/T_3} \left\{ \cos \omega_3 t + \frac{\sin \omega_3 t}{\omega_3 T_3} \right\} \tag{15}$$

$$v_D = V_D - g_{fs} V_F \omega_3 L_\ell e^{-t/T_3} \left\{ 1 + \frac{1}{\omega_3^2 T_3^2} \right\} \sin \omega_3 t \tag{16}$$

where

$$T_3 = \frac{2L_\ell C_{GD} g_{fs}}{C_{GS}} \tag{17}$$

$$\omega_3 = \frac{\sqrt{4L_\ell C_{GD} R_{DR} g_{fs} - R_{DR}^2 C_{GS}^2}}{2L_\ell C_{GD} R_{DR} g_{fs}} \tag{18}$$

The end of the time interval will be marked either by the drain circuit i_D reaching I_O, or the drain voltage v_D collapsing to $i_D \times R_{DS(ON)}$, whichever occurs first.

Large $L\ell/R_{DR}$

Now consider the situation when $L\ell/R_{DR}$ has a large value—representing a "fast drive" circuit with a "slow" drain circuit. The equivalent circuit model is shown in Figure 9, and switching waves are illustrated in Figure 10. Note that we are ignoring the gate-to-source capacitance C_{GS}. This is valid because with large $L\ell/R_{DR}$ ratio the "Miller" effect predominates and current through C_{GS} is small by comparison with that through C_{GD}.

The inductance $L\ell$ now presents such a high impedance that the increase of drain current "requested" by the drive circuit cannot be satisfied; the drive circuit is largely impotent to bring about the drain current that it asks for.

The drain voltage now collapses relatively quickly—generally well before the current rise is completed. The end of the period is marked by the HEXFET reaching the essential condition of a "closed switch"—the voltage across it having collapsed completely.

The mathematics are rather simple; in order to gain insight, it is useful to proceed through the analysis step by step:

$$v_{GS} = (V_T + V_F) - i_{DR} R_{DR} \tag{19}$$

$$i_D = g_{fs}(v_{GS} - V_T)$$

Therefore, from (19):

$$i_D = g_{fs}(v_F - i_{DR} R_{DR}) \tag{20}$$

$$\therefore pL_\ell i_D = -pL_\ell g_{fs} R_{DR} i_{DR} \tag{21}$$

$$v_D = V_D - pL_\ell i_D$$

Therefore from (21):

$$v_D = V_D + pL_\ell g_{fs} R_{DR} i_{DR} \tag{22}$$

$$i_{DR} = -pC_{GD} v_D$$

Therefore from (22):

$$\therefore (p^2 L_\ell C_{GD} g_{fs} R_{DR} + 1)\, i_{DR} = 0 \tag{23}$$

Equation (23) is a classical second order differential, with purely "oscillatory" terms.

By imposing the appropriate boundary conditions [$v_{GS} = V_T$ at $t = 0$, and $pLi_D = 0$ at $t = 0$ (since $i_{GD} \neq \infty$)], the following solutions are obtained:

$$v_{GS} = V_F(1 - \cos \omega_1 t) \tag{24}$$

$$i_D = g_{fs} V_F (1 - \cos \omega_1 t) \tag{25}$$

$$v_D = V_D - \omega_1 L_\ell g_{fs} V_F \sin \omega_1 t \tag{26}$$

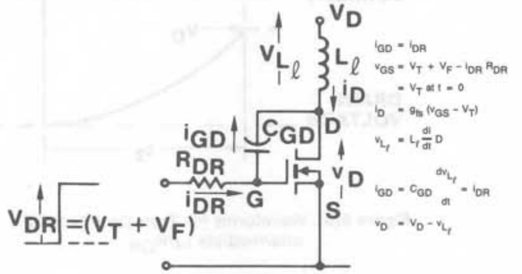


Figure 9. Circuit Model for Turn-On Interval 2, High $L\ell/R_{DR}$

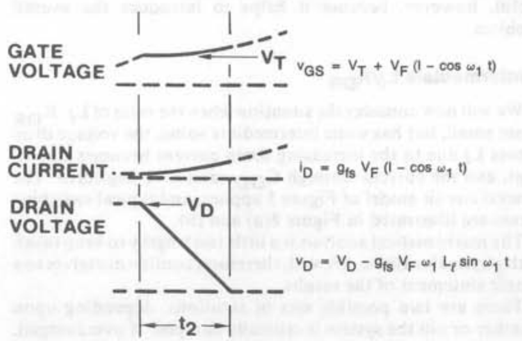


Figure 10. Waveforms for Turn-On Interval 2 Large $L\ell/R_{DR}$

$$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

$$= V_D - \sqrt{\frac{g_{fs} L_\ell}{C_{GD} R_{DR}}} \sin \omega_1 t \tag{27}$$

where

$$\omega_1 = \frac{1}{\sqrt{g_{fs} C_{GD} R_{DR} L_\ell}} \tag{28}$$

It remains now to establish how large L_ℓ / R_{DR} must be for the above simple relationships to be valid.

The starting assumption was that the current through C_{GS} is small by comparison with the "Miller" current i_{GD} through C_{GD}. This implies:

$$R_{DR} << \frac{1}{\omega_1 C_{GS}}$$

$$\therefore \; R_{DR} << \frac{\sqrt{g_{fs} C_{GD} R_{DR} L_\ell}}{C_{GS}}$$

$$\therefore \; \frac{L_\ell}{R_{DR}} >> \frac{{C_{GS}}^2}{C_{GD} g_{fs}} \tag{29}$$

Table I shows maximum values of R_{DR} for various HEXFET's for different values of L_ℓ that satisfy the above condition. It is clear that this condition, and hence expressions (24) through (26), will generally apply only to relatively low impedance drive circuits.

Simple qualitative checks on the above relationships will prove their validity. From equation (28), ω_1 increases as R_{DR} or L_ℓ decreases. The rate of rise of drain current, therefore, increases as either of these parameters decrease, which is to be expected. From equation (27), the voltage across L_ℓ is proportional to L_ℓ / R_{DR}. Thus increasing L_ℓ or decreasing R_{DR} gives increasing voltage across L_ℓ—again, to be expected.

The end of the interval occurs when either the drain current i_D reaches I_O, or the drain voltage collapses to zero [more precisely when it becomes equal to $i_D \times R_{DS(ON)}$]. If I_O or V_F, or both, are small, i_D could reach I_O before the collapse of drain voltage is complete. In practice, the voltage collapse will generally occur well before the current has risen to I_O. To take an example, with the IRF150 HEXFET (rated 25A at 100°C) operating in a 60V circuit, with a gate forcing voltage V_F of 7V, $L_\ell = 1\ \mu$H, and $R_{DR} = 2\Omega$, the voltage collapse will be completed by the time the drain current has risen to 0.25A (i.e., about 1% of rated current).

This result is to be expected; we have already reasoned that for large L_ℓ / R_{DR} ratio, the HEXFET essentially acts as a closed switch, the voltage across it collapsing quickly, with the current rising much more slowly, at a rate determined by the external circuit inductance.

Turn-On Interval 3

The second time interval ends at the completion either of the drain current rise or the drain voltage fall. The completion of the remaining event—voltage fall, or current rise—whichever it is, takes place during the third time interval.

Fortunately, since only the drain voltage *or* the drain current are now still changing, the analysis is easy, and is independent of the ratio of L_ℓ, R_{DR}. If the drain current is no longer changing, then L_ℓ is irrelevant, since there is no voltage drop across it, whilst if the drain voltage is no longer changing, the HEXFET already acts as a closed switch, and R_{DR} is irrelevant.

Consider first the situation when the voltage completes its fall during the third interval. The equivalent circuit model is shown in Figure 11. At the start of the period the drain voltage is V_D^*. Since the drain current is constant, v_{GS} must also be constant:

$$v_{GS} = V_T + \frac{I_O}{g_{fs}} \tag{30}$$

Therefore i_{DR} is also constant:

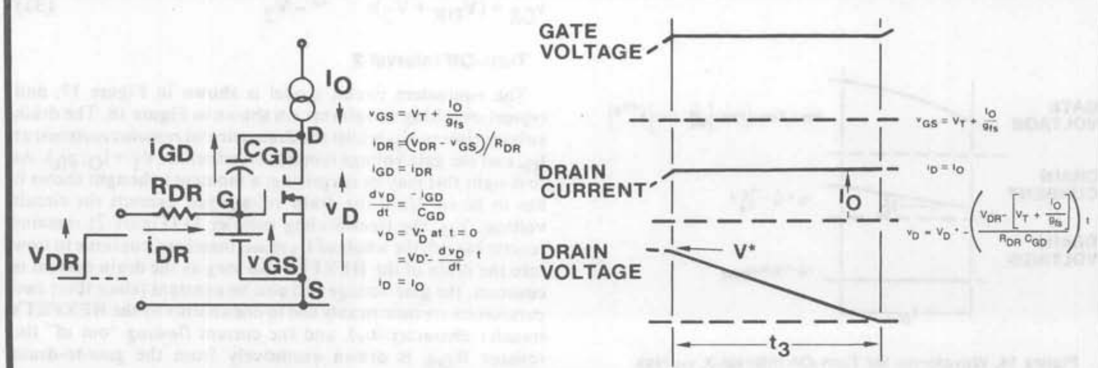
$$i_{DR} = \frac{1}{R_{DR}} (V_{DR} - V_{GS}) = \frac{V_{DR} - (V_T + I_O/g_{FS})}{R_{DR}} \tag{31}$$

Since v_{GS}, is constant, no current flows in C_{GS}, and all of i_{DR} flows in C_{GD}. The rate of change of voltage across C_{GD} is therefore:

$$\frac{dv_{GD}}{dt} = \frac{i_{DR}}{C_{GD}} = \frac{V_{DR} - (V_T + I_O/g_{fs})}{R_{DR} C_{GD}} \tag{32}$$

The rate of change of drain-source voltage is equal to the rate of change of drain-gate voltage, since v_{GS} is constant. Therefore, the drain voltage is:

$$v_D = V_D^* - \left(\frac{V_{DR} - (V_T + I_O/g_{fs})}{R_{DR} C_{GD}} \right) t \tag{33}$$



Figures 11 and 12. Circuit Model and Waveforms for Turn-On Interval 3, i_D is Already Equal to I_O. v_D Collapses.

We will now consider the situation when the current completes its rise during the third time interval, the drain voltage having already collapsed.

The equivalent circuit model is shown in Figure 13 and switching waveforms are shown in Figure 14. The drain current i_D is:

$$i_D = I_D^* + \frac{V_D}{L_\ell} t \qquad (34)$$

The gate voltage continues to increase exponentially during the third interval, at time constant T_G [equation (2)]. This, however, has no influence over the drain current or voltage, since the HEXFET is already "fully on."

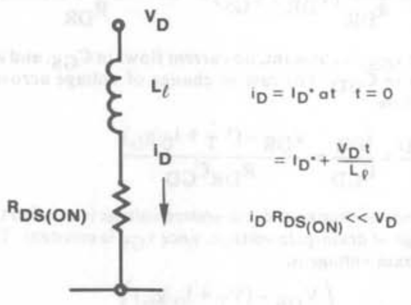


Figure 13. Circuit Model for Turn-On Interval 3, v_D Has Already Collapsed, i_D rises to I_O.

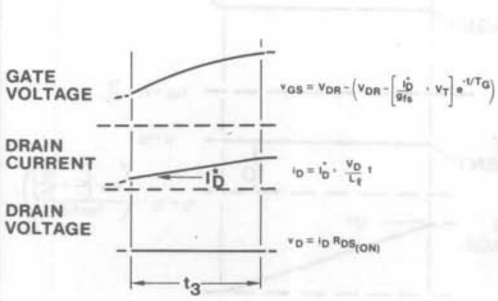


Figure 14. Waveforms for Turn-On Interval 3, v_D Has Already Collapsed, i_D rises to I_O.

Turn-On Interval 4

The gate voltage completes its exponential charge, at time constant T_G, to the level of the applied drive voltage V_{DR}. This has no influence over the drain current or voltage, since the switching sequence in the drain circuit has already been completed.

B. TURN-OFF

Turn-Off Delay Interval 1

The equivalent circuit model is shown in Figure 15, and operating waveforms are shown in Figure 16. The applied drive voltage V_{DR} is assumed to fall instantaneously to a negative

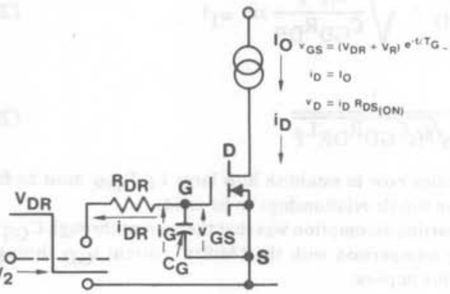


Figure 15. Circuit Model for Turn-Off Delay Interval

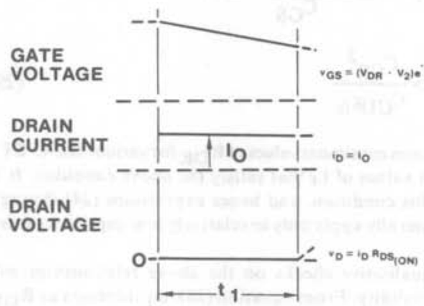


Figure 16. Waveforms for Turn-Off Delay Interval (t_1)

voltage $-V_2$ (this could, of course, be zero, or even positive, representing a small residual positive drive voltage). The voltage appearing between the gate and source terminals falls at a rate determined by the time constant $R_{DR}C_G$, and nothing happens in the drain circuit until the gate voltage falls to $V_T + (I_O/g_{fs})$, which corresponds to the gate voltage needed to sustain the drain current I_O. This point marks the end of the turn-off delay period. The gate voltage during the turn-off delay interval is given by:

$$v_{GS} = (V_{DR} + V_2)e^{-t/T_G} - V_2 \qquad (35)$$

Turn-Off Interval 2

The equivalent circuit model is shown in Figure 17, and typical switching waveforms are shown in Figure 18. The drain voltage rises to V_D whilst the drain current *remains constant* at I_O, and the gate voltage *remains constant* at $(V_T + I_O/g_{fs})$. At first sight this may be surprising; a moment's thought shows it has to be so. Until the drain voltage just exceeds the circuit voltage, V_D, the freewheeling rectifier D (Figure 2) remains reverse biased; the whole of I_O must, therefore, continue to flow into the drain of the HEXFET. So long as the drain current is constant, the gate voltage will also be constant (since these two parameters are inextricably tied to one another by the HEXFET's transfer characteristic), and the current flowing "out of" the resistor R_{DR} is drawn exclusively from the gate-to-drain capacitance.

Since the drain current is constant, the ratio of L_ℓ/R_{DR} has no bearing upon the operation during this period. By similar reasoning used to analyze the voltage fall during the third interval of switch-on, the following relationship is derived:

$$v_D = \frac{(I_O/g_{fs} + V_T + V_2)}{C_{GD}R_{DR}}\,t \tag{36}$$

Turn-Off Interval 3

The general circuit model for this interval is shown in Figure 19. At the end of the second interval, the drain voltage is just equal to the supply voltage V_D, while the current is equal to the full load value, I_O. The freewheeling rectifier D (Figure 2) is now poised at the point of conduction, ready to receive the load current I_O, and the potential at the "top" of L_ℓ is now fixed essentially at V_D. In order for the drain current to be commutated into the freewheeling rectifier, it is axiomatic that the drain voltage must increase above V_D. This reflects the fundamental property of inductance L_ℓ; the voltage across it must reverse in order for the current in it to reduce; a voltage-time integral must be developed, equal to $I_O \times L_\ell$, for the drain current to be returned to zero. This fundamental consideration relates directly to the inductance L_ℓ, and is quite independent of any other circuit considerations. The magnitude of the peak overvoltage developed across the HEXFET will be proportional to the size of the inductance L_ℓ, the magnitude of the current I_O, and the speed of switching.

In most practical circuits, the voltage transient at the drain can easily exceed the voltage rating of the HEXFET. In the absence of an externally connected local voltage clamp, the HEXFET will likely be driven into avalanche, acting, in effect, as its own voltage clamp, and preventing further substantial increase of voltage. This may or may not be permissible, depending upon whether the HEXFET is rated to handle the avalanche energy. If it cannot do so, then a local external voltage clamp, such as a zener diode, connected physically close to the drain and source terminals will be needed, and this will be functionally equivalent to the HEXFET itself avalanching, save that the energy is absorbed by the clamp, rather than by the HEXFET.

In this third time interval of turn-off, as during the second time interval of turn-on, both the drain current and the drain voltage change. Again, these two events are dynamically intertwined. A change of drain current produces a change of voltage across L_ℓ; this produces a current flow through the "Miller" capacitance C_{GD}; this restrains the rate of decrease of gate voltage, which in turn restrains the original rate of change of drain current.

As we would expect, the form of the analytic solutions depends upon the ratio of L_ℓ/R_{DR}. We will simply state the results, since the derivation follows the same general procedures covered for the second turn-on interval.

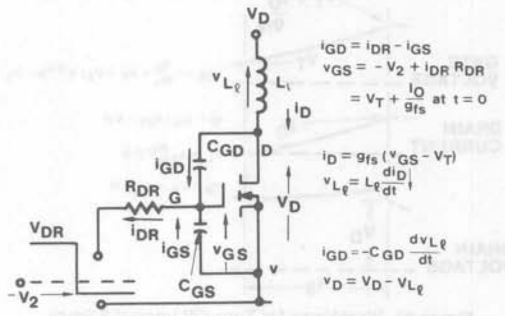


Figure 19. General Circuit Model for Turn-Off Interval 3

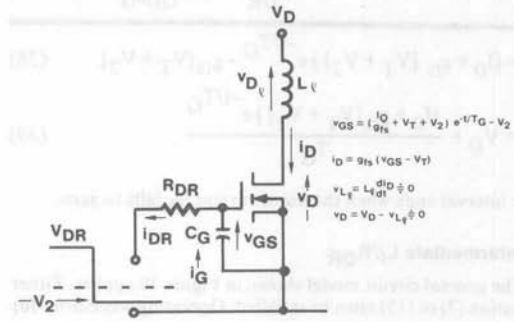


Figure 20. Circuit Model for Turn-Off Interval 3 Small L_ℓ/R_{DR}

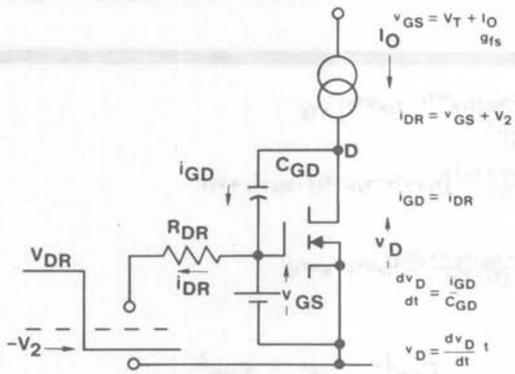


Figure 17. Circuit Model for Turn-Off Interval 2

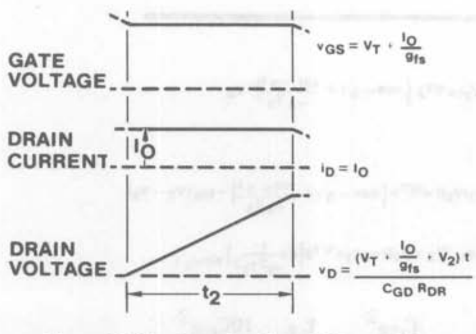


Figure 18. Waveforms for Turn-Off Interval 2

Small L_ℓ/R_{DR}

The equivalent circuit model is shown in Figure 20, and operating waveforms are shown in Figure 21.

For small L_ℓ/R_{DR}, equation (6) must be satisfied:

$$v_{GS} = (I_O/g_{fs} + V_T + V_2)\,e^{-t/T_G} - V_2 \tag{37}$$

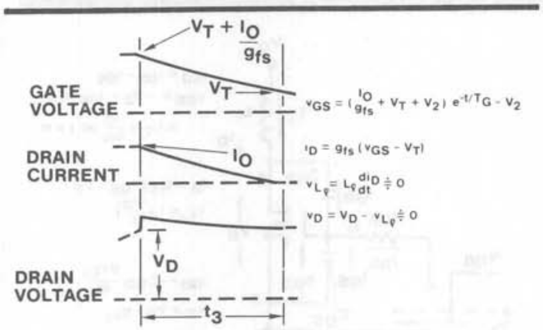


Figure 21. Waveforms for Turn-Off Interval 3 Small L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} < \frac{C_{GS}^2}{10C_{GD}g_{fs}}$$

$$i_D = (I_0 + g_{fs}[V_T + V_2])\, e^{-t/T_G} - g_{fs}[V_T + V_2] \quad (38)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}[V_T + V_2])\, e^{-t/T_G}}{T_G} \quad (39)$$

The interval ends when the drain current i_D falls to zero.

Intermediate L_ℓ/R_{DR}

The general circuit model shown in Figure 19 applies. Either equation (7) or (13) must be satisfied. Operating waveforms for L_ℓ/R_{DR} that satisfy equation (7) are shown in Figure 22(a). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = \frac{(I_0/g_{fs} + V_T + V_2)}{(T_1 - T_2)}\; T_1 e^{-t/T_1} - T_2 e^{-t/T_2} - V_2 \quad (40)$$

$$i_D = \frac{(I_0 + g_{fs}[V_T + V_2])}{(T_1 - T_2)}\; T_1 e^{-t/T_1} - T_2 e^{-t/T_2} \ldots$$
$$\ldots - g_{fs}[V_T + V_2] \quad (41)$$

$$v_D = V_D + \frac{(I_0 + g_{fs}[V_T + V_2])L_\ell}{(T_1 - T_2)}\; e^{-t/T_2} - e^{-t/T_1} \quad (42)$$

where T_1 and T_2 are given by equations (11) and (12), respectively.

Operating waveforms for L_ℓ/R_{DR} given by equation (13) are shown in Figure 22(b). Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2)\, e^{-t/T_3}\; \cos\omega_3 t + \frac{\sin\omega_3 t}{\omega_3 t_3} - V_2 \quad (43)$$

$$i_D = (I_0 + g_{fs}[V_T + V_2])\, e^{-t/T_3}\; \cos\omega_3 t + \frac{\sin\omega_3 t}{\omega_3 t_3} \ldots$$
$$\ldots - g_{fs}[V_T + V_2] \quad (44)$$

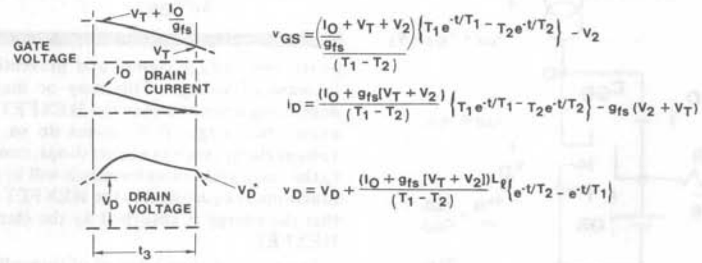


Figure 22(a). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{10C_{GD}g_{fs}} < \frac{L}{R_{DR}} < \frac{C_{GS}^2}{4C_{GD}g_{fs}}$$

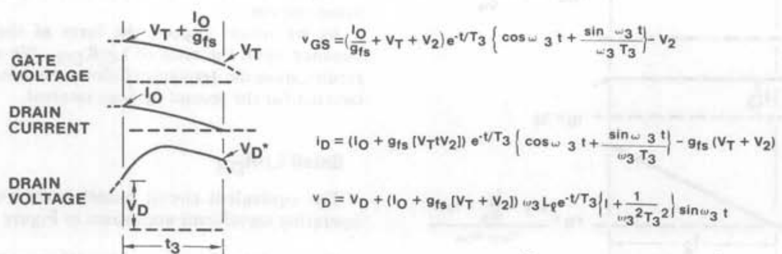


Figure 22(b). Waveforms for Turn-Off Interval 3 Intermediate L_ℓ/R_{DR}

$$\frac{C_{GS}^2}{4C_{GD}g_{fs}} < \frac{L_\ell}{R_{DR}} < \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

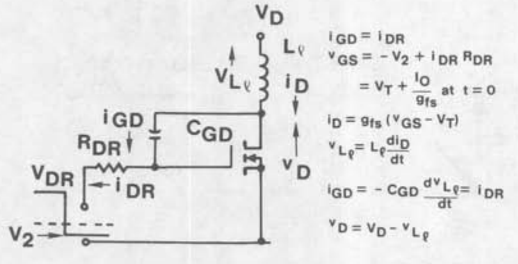


Figure 23. Circuit Model for Turn-Off Interval 3 Large L_ℓ/R_{DR}

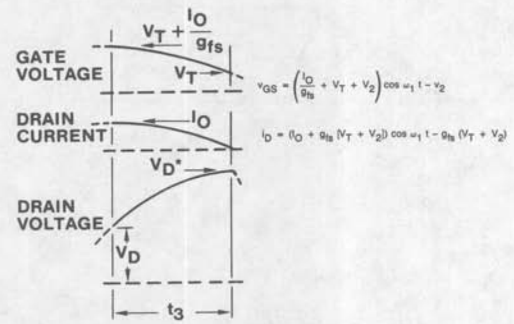


Figure 24. Waveforms for Turn-Off Internal 3 Large L_ℓ/R_{DR}

$$\frac{L_\ell}{R_{DR}} > \frac{10C_{GS}^2}{C_{GD}g_{fs}}$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2])\omega_3 L_\ell e^{-t/T_3}$$

$$\ldots \left\{1 + \frac{1}{\omega_3^2 T_3^2}\right\}\sin\omega_3 t \qquad (45)$$

where T_3 and ω_3 are given by equations (17) and (18), respectively.

Large L_ℓ/R_{DR}

Large L_ℓ/R_{DR} is defined by equation (29). The circuit model is shown in Figure 23, and operating waveforms are shown in Figure 24. Expressions for the gate voltage v_{GS}, the drain current i_D, and the drain voltage v_D, are as follows:

$$v_{GS} = (I_0/g_{fs} + V_T + V_2)\cos\omega_1 t - V_2 \qquad (46)$$

$$i_D = (I_0 + g_{fs}[V_T + V_2])\cos\omega_1 t - g_{fs}(V_T + V_2) \qquad (47)$$

$$v_D = V_D + (I_0 + g_{fs}[V_T + V_2])\,\omega_1 L_\ell \sin\omega_1 t \qquad (48)$$

where ω_1 is given by equation (28).

Turn-Off Interval 3a (Clamping of the Drain Voltage)

The expressions just derived assume that the drain voltage will increase to whatever extent the circuit operation dictates. In practice, as already stated, the instantaneous drain voltage is likely to exceed the voltage rating of the HEXFET; this is particularly true for high L_ℓ/R_{DR} ratio.

In this event, either the HEXFET will be driven into avalanche—in effect acting as its own "voltage clamp" and limiting further increase of voltage—or, if the HEXFET is unable to handle this, an external local voltage clamping device would have to be connected.

In either event, at the instant at which the drain voltage becomes equal to the "clamp" voltage, interval 3, as given by the previous equations, comes to an end, and interval 3a—the clamping interval—starts.

Figure 25 shows the equivalent circuit for the "clamping" interval, with an external clamp, and operating waveforms are shown in Figure 26. The drain voltage is assumed to stay constant at the "clamp" level, V_{CLAMP}, while the drain circuit current decays linearly to zero:

$$i_D = I_D^* - \frac{(V_{CLAMP} - V_D)}{L_\ell}t \qquad (49)$$

The period ends when $i_D = 0$. Note that if the HEXFET acts as its own clamp and is driven into avalanche, then equation (49) applies to the HEXFET's drain current; if an external clamp is used, drain current can be assumed to stop flowing at the start of this interval, and equation (49) then applies to the current in the external clamp.

Turn-Off Interval 4

At the end of interval 3 (or 3a) the drain current has fallen to zero, but the drain voltage V_D^*, is greater than the circuit

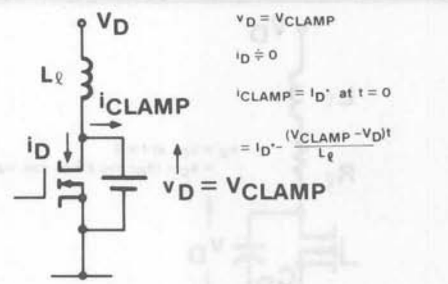


Figure 25. Circuit for Clamping Turn-Off Interval 3a

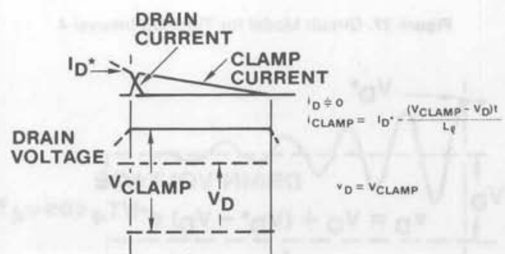


Figure 26. Waveforms for Clamping Turn-Off Interval 3a

voltage V_D. The drain capacitance C_D then "rings" with the stray circuit inductance L_ℓ, the oscillation being damped by the stray circuit resistance R_ℓ. Figure 27 shows the equivalent circuit for this interval, and Figure 28 shows a typical drain voltage waveform.

$$v_D = V_D + (V_D^* - V_D)e^{-t/T_4} \cos \omega_4 t \qquad (50)$$

where

$$T_4 = \frac{2L_\ell}{R_\ell} \qquad (51)$$

$$\omega_4 = \frac{\sqrt{4L_\ell C_D - C_D^2 R_e^2}}{2L_\ell C_D} \ell \qquad (52)$$

During this interval the gate voltage discharges exponentially with time constant T_G towards a final value of $-V_2$.

VI. A Worked Design Example

Figures 29 through 32 show switching waveforms for a specific design example, obtained from the analytic expressions presented in this paper. Various combinations of L_ℓ/R_{DR}, and amplitude of drive voltage, are considered in order to illustrate the effects of these parameters on the switching performance. The following data is used:

HEXFET type: IRF150

C_{GS}: 2650 pF
C_{GD}: 350 pF
V_T: 3 V
g_{fs}: 8 A/V
V_D: 50 V
I_O: 35A

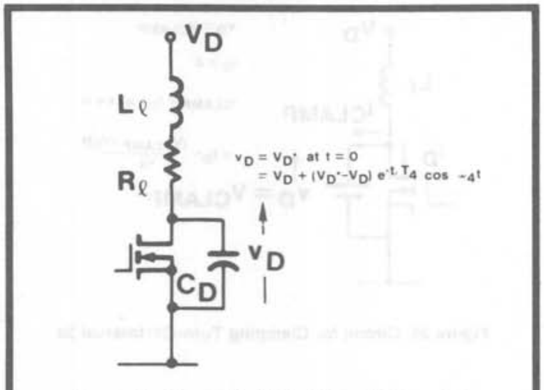


Figure 27. Circuit Model for Turn-Off Interval 4

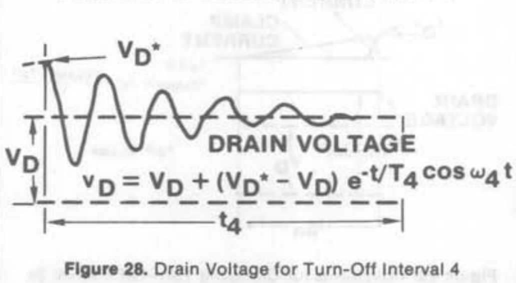


Figure 28. Drain Voltage for Turn-Off Interval 4

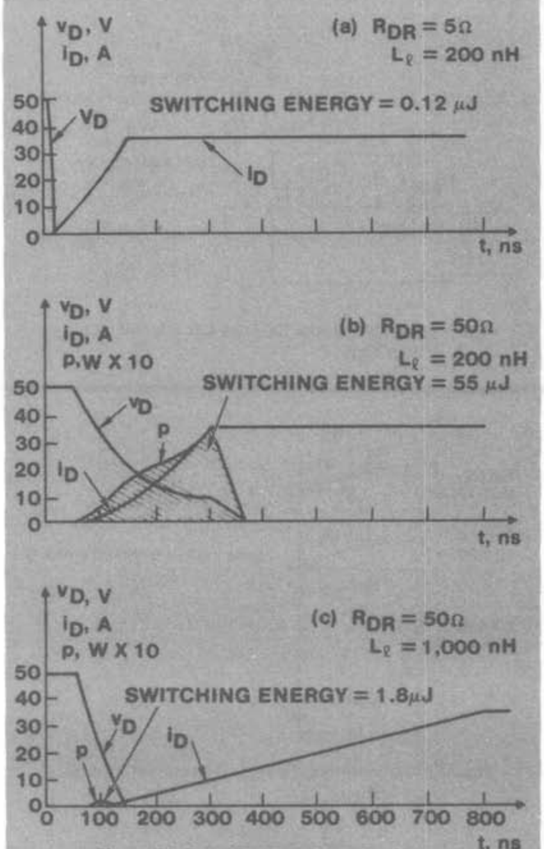


Figure 29. Turn-On Waveforms For Various Circuit Conditions

(a) $R_{DR} + 5\Omega L_S = 200$ nH
(b) $R_{DR} +50\Omega, L_S = 200$ nH
(c) $R_{DR} +50\Omega, L_S = 1\ \mu H$

IRF 150, $V_{DR} = 10V$
$V_2 = 0$

Figure 29 shows waveforms calculated for the turn-on interval for: (a) R_{DR} = 5 ohms, L_ℓ = 200 nH; (b) R_{DR} = 50 ohms, L_ℓ = 200 nH; and (c) R_{DR} = 50 ohms, L_ℓ = 1 μH. The drive voltage V_{DR} is 10 volts.

Condition (a) is representative of a fast drive circuit, and a relatively high impedance of L_ℓ. The drain voltage falls rapidly, and most of the current rise time occurs subsequent to the collapse of drain voltage. The switching energy is almost negligible —a mere 0.12 μJ. In Figure 29(b), the inductance is the same, but the drive resistance has increased to 50 ohms. The gate drive circuit is now much slower, and the drain voltage collapses much less rapidly; in fact, the drain current now completes its rise before the drain voltage collapses completely. The total switching time (current rise + voltage fall) increases from 150 ns in Figure 29(a) to 360 ns in Figure 29(b). More significantly, the switching energy increases from 0.12 μJ to 55 μJ.

In Figure 29(c), the drive circuit resistance is still 50 ohms, while the drain inductance L_ℓ has increased from 200 nH to 1 μH. The speed of the drive circuit is, therefore, the same as in Figure 29(b), but the impedance of L_ℓ increases by a factor of 5. The voltage drop in the drain circuit is, therefore, once again very significant, and the drain voltage collapses much more rapidly. Because of the increased inductance, however, the current rise time is much longer. The switching energy decreases from 55 μJ in Figure 29(b) to 1.8 μJ in Figure 29(c), because of the much faster voltage collapse. It would be wrong to believe, however, that the overall switching losses can be decreased by increasing L_ℓ. The energy saved during turn-on by increasing L_ℓ is more than offset by increased energy at turn-off. Increasing L_ℓ to reduce the turn-on losses is counterproductive; it simply postpones the "day of reckoning" to the turn-off interval.

Before studying the details of the turn-off waveforms in Figure 30, it will be instructive to make some basic comparisons between the operation during the turn-on and turn-off intervals.

At turn-on the peak dissipation is drastically effected by the L_ℓ/R_{DR} ratio, and is very small if this ratio is large. At turn-off, however, L_ℓ/R_{DR} has no real influence on the peak dissipation, and this is *always* relatively high. This is because the drain current cannot start to decrease *until* the drain voltage has risen all the way to the circuit voltage. The peak dissipation during the voltage rise interval (turn-off interval 2) will, therefore, always be $V_D \times I_O$. While the value of drive resistance, R_{DR}, controls the duration of this period, L_ℓ, has no effect upon it.

The next turn-off interval (t_3), is also one of relatively high power dissipation. Even with no drain inductance, the drain current must decay from I_O to zero with the drain voltage at the full circuit value, V_D. In practice L_ℓ will never be zero, and the energy stored in this inductance ($1/2\ L_\ell I_O^2$) will also be dissipated during this period. It is evident, therefore, that while the turn-on energy depends strongly upon the L_ℓ/R_{DR} ratio, and can be very small if L_ℓ/R_{DR} is large, there is no way of avoiding a much more significant turn-off energy. Generally, the larger is L_ℓ, the greater will be the *total* energy dissipation, even though the turn-on dissipation may be very low.

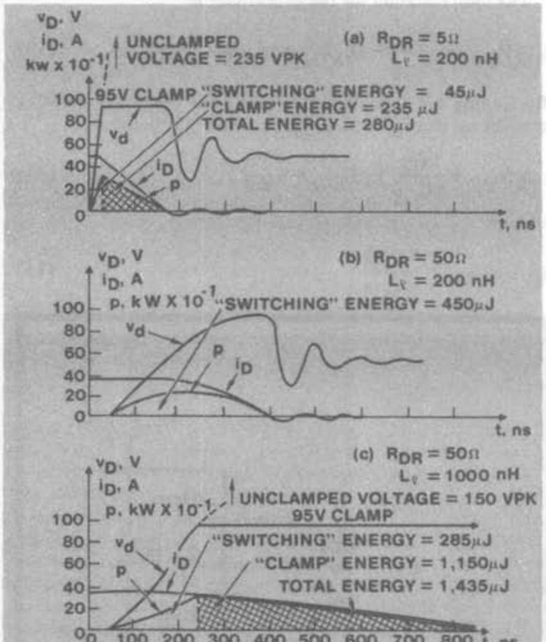


Figure 30. Turn-On Waveforms For Various Circuit Conditions

(a) R_{DR} = 5Ω, L_S = 200 nH
(b) R_{DR} = 50Ω, L_S = 200 nH
(c) R_{DR} = 50Ω, L_S = 1000 nH

IRF 150, V_{DR} = 10V
V_2 = 0

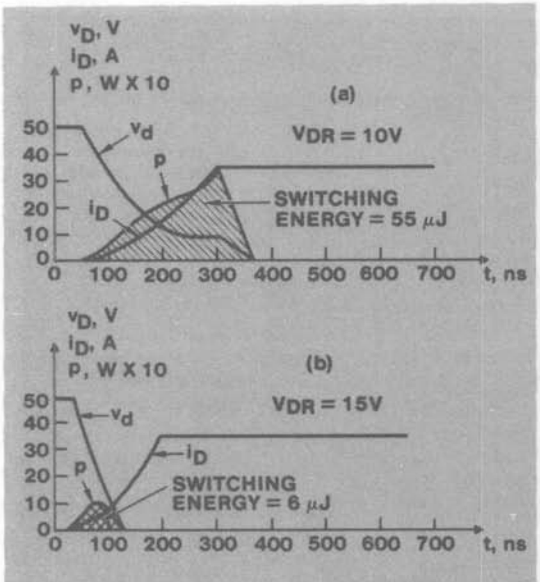


Figure 31. Turn-On Waveforms for:

(a) Drive Voltage V_{DR} = 10V
(b) Drive Voltage V_{DR} = 15V

IRF 150 R_{DR} = 50Ω
L_S = 200nH

Figures 30(a) through (c) show waveforms at turn-off that correspond to the same three sets of values of R_{DR} and L_ℓ as in Figure 29(a) through (c). The waveforms in Figure 30 (a) are for a fast drive circuit (R_{DR} = 5 ohms). The drain voltage rises rapidly to the clamping level of 95V. Note that in the absence of a clamp the drain voltage would rise to a hypothetical peak of 235V (assuming that this 100V rated HEXFET would take it!). The energy dissipated in the HEXFET during the time the drain voltage rises to the 95V clamp level is referred to in Figure 31 as "switching" energy, and is 45 μJ—more than two orders of magnitude greater than the energy at turn-on for the same values of R_{DR} and L_ℓ [Figure 29(a)].

Once the 95V clamp level is reached, the current decays approximately linearly, and an additional 235 μJ of energy is dissipated during the clamping period. This energy would be dissipated either in an external clamp, if this is used, or in the HEXFET itself—assuming that it is capable of operating in its avalanche mode.

Note that the energy stored in L_ℓ, $1/2\ L_\ell I_O^2$ = 122 μJ, is about half the total energy dissipated during the clamping period. Simple physical reasoning confirms the correctness of this; not only must the energy stored in L_ℓ be dissipated, but since the supply voltage V_D continues to feed energy to the circuit (i_D continues to be drawn from V_D), this energy also must end up being dissipated during this period.

Figure 30(b) shows waveforms for R_{DR} = 50 ohms, with L_ℓ the same as for Figure 30(a). The response of the gate drive circuit is much slower, and hence the rate of rise of drain voltage is also much slower —so slow, in fact, that the drain voltage never reaches the clamping level of 95V. In this case, all the switching energy must be dissipated in the device itself, and there is no opportunity for shunting some of this into an external clamp. The total switching time increases from 175 ns [Figure 30(a)] to 400 ns, and the total switching energy increases from 280 to 450 μJ. Once again, the turn-off energy of 450 μJ is much greater than the turn-on energy of 55 μJ for the same value of L_ℓ and R_{DR} [Figure 29(b)].

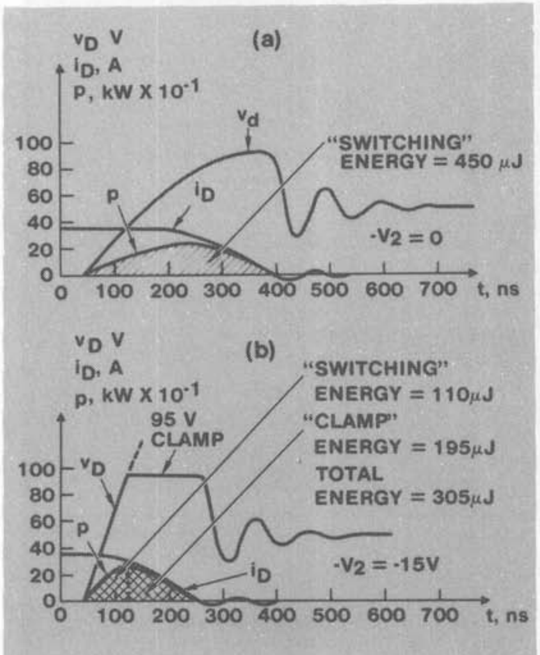


Figure 32. Turn-Off Waveforms for:
(a) "Negative Drive Voltage" ($-V_2$) = 0
(b) "Negative Voltage" ($-V_2$) = 15V

IRF 150 R_{DR} = 50Ω
L_S = 200nH

Figure 30(c) shows turn-off waveforms for R_{DR} = 50 ohms, but with L_ℓ increased to 1 μH. As would be expected, the initial rate of change of drain voltage is the same as in Figure 30(b); until the drain voltage becomes equal to the circuit voltage of 50V, the drain current remains constant at I_O, and L_ℓ has no effect. Thereafter, however, the drain voltage moves much more rapidly upwards, and has no difficulty in reaching the clamp level of 95V. The total switching time increases to 950 ns, because of the increased value of L_ℓ, and the total switching energy increases from 450 μJ in Figure 30(b) to 1435 μJ in Figure 30(c).

It is interesting to compare the energy reduction at turn-on when L_ℓ is increased from 200 nH to 1 μH, Figures 29(b) and (c), versus the energy increase at turn-off [Figures 30(b) and (c)]. The energy *reduction* at turn-on is (55 - 1.8) = (53.2 μJ, while the energy *increase* at turn-off is (1435 - 450) = 985 μJ. The net effect of increasing drain circuit inductance is a very substantial increase in the *total* energy dissipation.

The waveforms in Figure 31 show the effect of increasing the applied drive voltage from 10V to 15V, for R_{DR} 50 ohms and L_ℓ = 200 nH. The total switching time decreases from 360 ns to 160 ns, and the switching energy decreases from 55 μJ to 6 μJ.

Figure 32 shows the same comparison for the turn-off interval. The waveforms in Figure 32(a) are for no applied drive voltage during the turn-off interval, while those in Figure 32(b) are for a negative drive voltage of -15V. The total switching time decreases from 400 to 250 ns, and the switching energy from 450 to 305 μJ. The negative gate drive voltage not only reduces the total switching energy, but also, because it forces the drain voltage to reach the 95V clamping level, it offers the possibility for "dumping" 195 μJ of energy which would otherwise be dissipated in the HEXFET, into an external clamp.

VII. The Effect of Common Source Inductance

So far we have ignored the effect of the common source inductance L_S, shown dashed in Figure 2. This inductance will always be present to some extent; even with careful circuit layout, the user will have to accept, at a minimum, the internal lead inductance within the package of the device. For a TO-3 package, this inductance is in the order of 10 to 15 nH. We will now consider briefly the modifying effect of L_S on the switching operation.

Figure 33 shows the general equivalent circuit which includes L_S. As the drain current i_D starts to increase at turn-on, a voltage will be developed across L_S due to the rate of change of drain current. This voltage is common to the gate circuit, and its polarity is such to reduce the net voltage appearing between the gate and source terminals. Like the "Miller" effect, which provides a negative feedback from the drain to the gate, slowing down the rate of change of current, so the common source inductance also provides a negative feedback, from the source circuit to the gate, also slowing down the change of drain current.

A complete analysis of the switching operation that includes the effect of the common source inductance can be accomplished by means of the procedures already presented. This is beyond the scope of this paper. We will content ourselves instead with an approximate analysis, the main benefit of which is the extreme simplicity of the result.

Referring to the equivalent circuit in Figure 33, it is evident that L_S only has an effect when the drain current is changing, and the HEXFET is in its active region. This restricts the analysis to interval 2 during turn-on, and interval 3 during turn-off.

The loop equation for the gate circuit is:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_{GS} + pL_S i_D = V_{DR} \tag{53}$$

By making the approximation (valid for practical operating conditions) $pL_S i_D \gg pL_S i_{GS}$, equation (53) becomes:

$$i_{DR}R_{DR} + \frac{i_{GS}}{pC_{GS}} + pL_S i_D = V_{DR} \tag{54}$$

Now

$$i_D = g_{fs}v_{GS} = \frac{g_{fs}i_{GS}}{pC_{GS}} \tag{55}$$

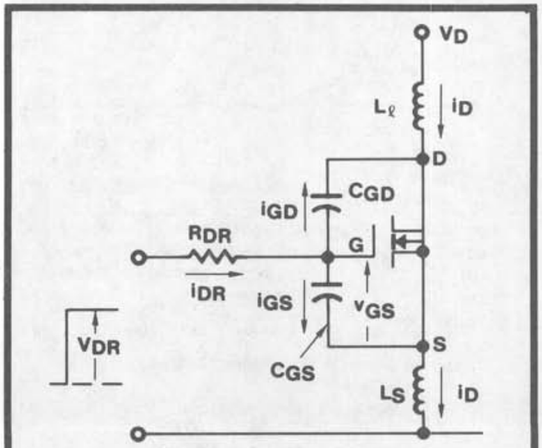


Figure 33. Equivalent Circuit Including the Effect of Common Source Inductance, L_S