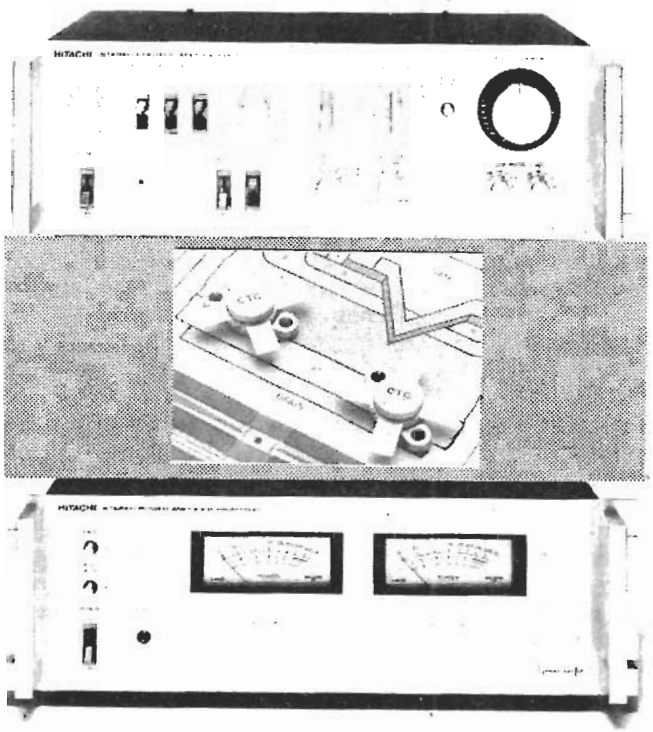
V·FETS FOR EVERYONE!

This article, by Wally Parsons, first appeared in our Canadian edition. We think that V-FETs represent a large step forward in power amplifier technology and so we have reprinted it, starting this month.

The first part of 'V-FETs for Everyone' covers the theory behind V-FETs and what their specifications mean. Next month, part two will describe how V-FETs are used at present and how to design V-FET circuitry.



SINCE THE SEMI-CONDUCTOR is precisely that, a battery across the ends of a *p*-type or an *n*-type bar will cause current to flow through the material, just as it does through a vacuum tube. If a *p*-type material is joined to the surface of an *n*-type bar, located between the battery terminals, a *pn* junction is formed, and if this junction is reverse biased, a space charge or field is produced of opposite polarity which will inhibit current flow, just as the control grid inhibits current flow in vacuum tube. Changing this reverse voltage causes a large current change, and therefore amplification results.

A simple FET (J-FET) is shown in Fig. 1. With a given drain — source voltage, maximum current flows under zero gate voltage conditions and at some reverse levels, no current will flow. Also, as in the vacuum tube, load characteristics are not reflected to the input circuit, because current is not controlled by carrier injection as in bipolars, but by voltage levels.

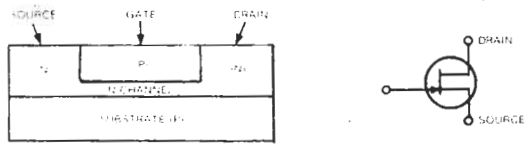


Fig 1: N-channel JFET construction and symbol

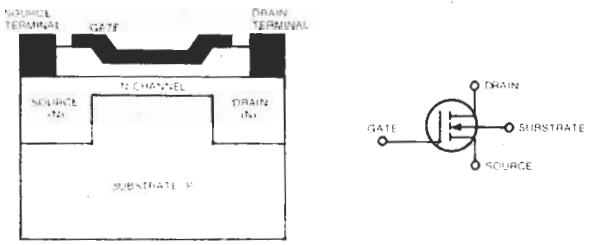


Fig 2: N-channel depletion horizontal MOSFET construction and symbol

A variation is the *M*etal *O*xide *S*emi-conductor *F*ield *E*ffect *T*ransistor. (MOSFET) (Fig. 2) a far more versatile device whose technology is virtually the cornerstone of modern computer technology, ▶

although it has had less use to date in linear applications such as audio amplification.

MOSFETS come in two basic types. In both types the gate consists of a metal electrode separated from the channel by a thin oxide layer. In the depletion type current flow is controlled by the electrostatic field of the gate when biased. Voltage relationships are the same as for the J-FET, except that when the J-FET is forward biased current will flow through the junction (after all, it *is* a *pn* junction). This does not contribute to amplification, and may even destroy the device. When a depletion MOSFET is so biased it may result in increased current flow and, provided current, dissipation, and breakdown ratings are suitable, the device may be driven on both sides of the zero volts point as with vacuum tubes. Unlike vacuum tubes under these conditions, the gate draws no cirrent and therefore does not require the driver to deliver power.

The enhancement type MOSFET shown in Fig. 3, is more widely used. The source and drain are separated by a substrate of opposite material, and under zero gate volts no current flows. However, when sufficient forward bias is applied to the gate the region under the gate changes to its opposite type (e.g. *p*-type becomes *n*-type) and provides a conductive channel between drain and source. Carrier level and conduction are controlled by the magnitude of gate voltage. Although J-FETS, and especially MOSFETS, have certainly delivered on their original promise, in one area they are particularly conspicuous by their absence, and that is in the area of power. Unfortunately, the channel depth available for conduction is limited by the practical limits on gate voltage. The lower current density has been the primary limitation due to the horizontal current flow.

VMOS

Recent years have seen the introduction and commercial use of Vertical Channel J-FETS, notably by Sony and Yamaha (Fig. 4). The vertical channel permits a very high width-length ratio, permitting a decreased inherent channel resistance and high current density. Unfortunately it exhibits the same disadvantages as the small signal J-FET, plus, in available devices, a very high input capacitance, ranging from 700pf to around 3000pf, limiting high frequency response. In addition, since they must be biased into the off condition, bias must be applied *before* supply voltage and removed after the supply if it is to be operated anywhere near its maximum ratings. This problem doesn't exist with vacuum tubes because of heater warm-up time, although some "instant-on" circuits impose heavy turn-on surges.

This necessitates a complex power supply, and indeed Yamaha, for example, uses more devices in the supply than it does in its amplifier circuits. However, the construction does make possible the design of complementary types and Nippon Electric and Sony both have high power devices available. Unfortunately, neither company seems anxious to make detailed information available, so there is little to disclose here beyond the fact that they are said to have characteristics similar to those of triode tubes.

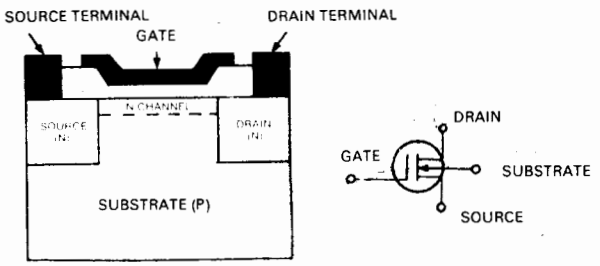


Fig 3: N-channel enhancement horizontal MOSFET construction and symbol

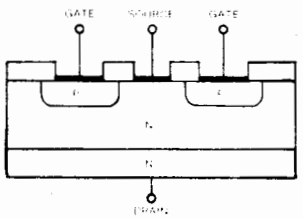


Fig 4: Vertical junction FET construction

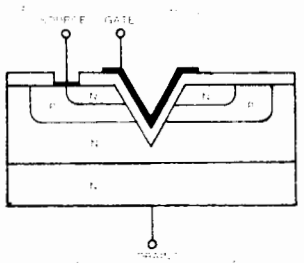


Fig 5: Vertical MOSFET construction (Siliconix)

However, the Vertical MOSFETS by Siliconix are readily available, at reasonable prices, and the manufacturer most generous in providing data. The following information is extracted from their application note AN76-3, Design Aid DA 76-1, plus device data sheets.

The Device

Notice in Fig. 5 that the substrate and body are opposite type materials separated by an epi layer (similar to high speed bi-polars). The purpose of this structure is to absorb the depletion region from the drain-body junction thus increasing the drain-source breakdown voltage. An alternative would have involved an unacceptable trade-off between increasing the substrate-body depth to increase breakdown voltage but increasing current path resistance and lengthening the channel. In addition, feedback capacitance is reduced by having the gate overlap n-epi material instead of $n+$.

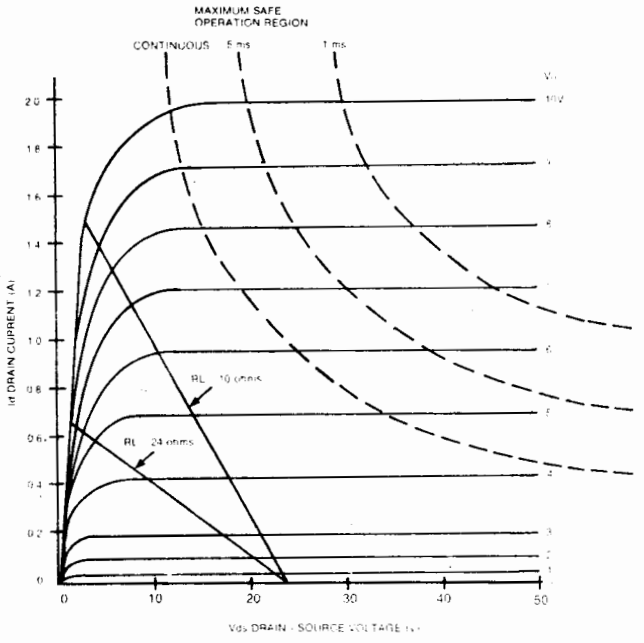


Fig 6: Output characteristics VMP1

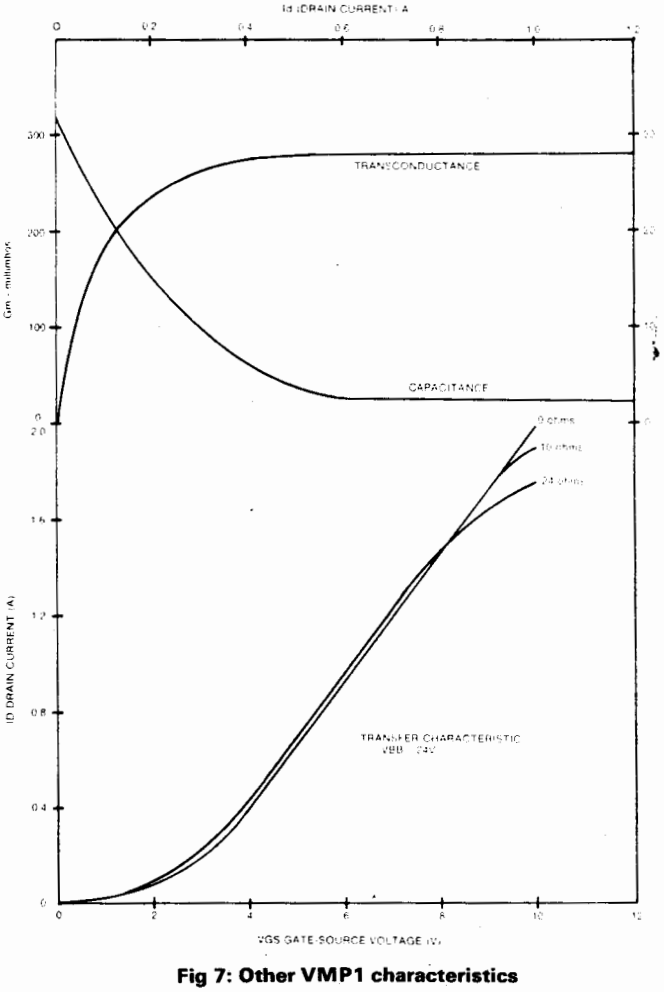


Fig 7: Other VMP1 characteristics

In manufacture, the substrate-drain and epi layer are grown, then the *p*-body and *n*+ source diffused into the epi layer, in a similar manner as the base and emitter of a diffusion type transistor. A V groove is etched through the device and into the epi layer, an oxide layer grown, then etched away to provide for the source contact and an aluminium gate deposited. It is apparent that this type of device allows current flow in one direction only; this is not always so with a similar type of horizontal FET, where source and drain may be identical in structure and of the same material. Therefore, no reverse current flows (we hope!) when used in switching applications, as was also the case with vacuum tubes.

In-circuit operation is refreshingly simple: Supply voltage is applied between source and drain, with the drain positive with respect to the source, under which conditions no current flows, and the device is off. This is an enhancement type device and is turned on by taking the gate positive with respect to the source and body. The electric field induces an *n* channel on both surfaces of the body facing the gate, and allows electrons to flow from the negative source through the induced channel and epi and through the substrate drain. The magnitude of current flow is controlled almost entirely by the gate voltage, as seen in the family of curves (Fig. 6 and 7) with no change resulting from supply voltage changes above 10V.

Advantages

The vertical structure results in several advantages over horizontal MOSFETS.

1) Since diffusion depths are controllable to close tolerances, channel length, which is determined by diffusion depth, is precisely controlled. Thus, width/length ratio of the channel, which determines current density, can be made quite large. For example, the VMP1 channel length is about 1.5 us, as against a minimum of 5 us in horizontal MOSFETS, due to the lower degree of control of the shadow masking and etching techniques used in such devices.

2) In effect, two parallel devices are formed, with a channel on either side of the V groove, thus doubling current density.

3) Drain metal runs are not required when the substrate forms the drain contact, resulting in reduced chip area, and thus reduced saturation resistance.

4) High current density results in low chip capacitance. Also, unlike horizontal MOSFETS, there is no need to provide extra drain gate overlap to allow for shadow mask inaccuracies, so feedback capacitance is minimized.

In comparison with bi-polars, especially power devices, the advantages are even more impressive.

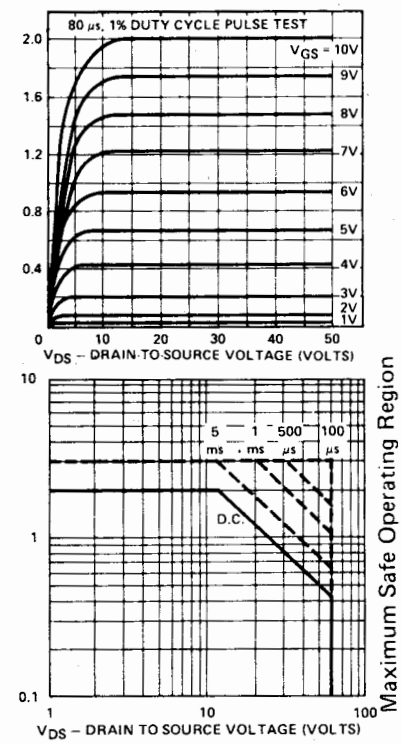
1) Input impedance is very high, comparable to vacuum tubes, since it is a voltage controlled device, with no base circuit drawing current from the driver stage. A 7 V swing at the gate, at virtually O A, represents almost O W of power, but can produce a swing of 1.8 A in output current. This represents considerable power gain and will interface directly with high impedance voltage drivers.

2) No minority carrier storage time, no injection, extraction, recombination of carriers, resulting in very fast switching and no switching transient in

		Characteristics		VMP 11			VMP 1			VMP 12			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1		BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0; I_D = 100 μA
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{GS} = V_{DS}; I_D = 1 mA
3		I_{GSS}	Gate-Body Leakage			0.5			0.5			0.5	μA	V_{GS} = 15 V; V_{DS} = 0
4		$I_{D(off)}$	Drain Cutoff Current			0.5			0.5			0.5		V_{GS} = 0; V_{DS} = 24 V
5		$I_{D(on)}$	Drain ON Current*	1	2.0		1	2.0		1	2.0		A	V_{DS} = 24 V; V_{GS} = 10 V
6		$I_{D(on)}$	Drain ON Current*	0.5			0.5			0.3				V_{DS} = 24 V; V_{GS} = 5 V
7	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance*		2.0	2.5		3.0	3.5		3.7	4.5	Ω	V_{GS} = 5 V; I_D = 0.1 A
8					2.4	3.0		3.3	4.0		4.6	5.5		V_{GS} = 5 V; I_D = 0.3 A
9					1.2	1.5		1.9	2.5		2.6	3.2		V_{GS} = 10 V; I_D = 0.5 A
10					1.4	1.8		2.2	3.0		3.4	4.0		V_{GS} = 10 V; I_D = 1 A
11		g_m	Forward Transconductance*	200	270		200	270		170			m℧	V_{DS} = 24 V; I_D = 0.5 A
12	DYNAMIC	C_{iss}	Input Capacitance		48			48			48		pF	V_{GS} = 0; V_{DS} = 24 V f = 1 MHz
13		C_{rss}	Reverse Transfer Capacitance		7			7			7			
14		C_{oss}	Common Source Output Capacitance		33			33			33			
15		t_{ON}	Turn ON Time**		4	10		4	10		4	10	ns	See Switching Time Test Circuit
16		t_{OFF}	Turn OFF Time**		4	10		4	10		4	10		

*Pulse Test **Sample Test
Pulse Test Pulse Width = 80 μsec, Duty Cycle = 1%

VMC



Figs 8, 9 & 10: Electrical characteristics of the VMP devices from Silconix, a freely available VFET.

class B and AB amplifiers. Switching time for a VMP1 is 4 ns for 1 A, easily 10-200 times faster than bi-polars, and even rivalling many vacuum tubes.

3) No secondary breakdown, and no thermal runaway. VMOS devices exhibit a negative temperature coefficient with respect to current, since there is no carrier recombination activity to be speeded up with temperature. Thus, as current increases so does temperature, but the temperature rise reduces current flow. It is still possible to destroy the device by exceeding its maximum ratings, but a brief near-overload does not result in an uncontrollable runaway condition. Usually, simple fusing and/or thermistor protection is sufficient for maximum safety, and even this may be unnecessary with conservative design. Absence of secondary breakdown means that full dissipation can be realized even at higher supply voltages. In this respect they resemble vacuum tubes.

Available Devices

Seven devices representing three families are available. Types VMP-1, VMP-11, and VMP-12 are 2 A, 25 W dissipation devices intended for switching and amplifier use and differ only in voltage rating (60 V, 35 V, 90 V, respectively). Types VMP-2, VMP-21, VMP-22, are 1.5 A, 4 W devices rated at 60 V, 35 V, 90 V respectively, and are intended mainly for high speed switching, but would also be useful for low power amplifiers and as linear drivers for bi-polars, where the latter offer advantages. And finally, type VMP-4, 1.6 A, 35 W, specifically intended for VHF amplifier use. All except VMP-4 devices feature gate protection to withstand static discharges and over-voltages, and all are currently available except the VMP-4. All are *n*-channel. One hesitates to pass premature judgement, but if the millenium hasn't arrived yet, at least it might just be on the way.

Conditions

V-MOS Power FETs like signal MOSFETS, may be used in a variety of circuit arrangements to perform many different functions. However, no matter what the circuit, certain conditions, common to all applications, must be provided. These are supply power, loading, drive signal, and establishment of appropriate operating points. These are conditions necessary for amplification and since *all* active devices function as amplifiers, no matter what the total circuit function, the in-circuit performance of any device depends on the establishment of these conditions.

The electrical characteristics of the VMP1, VMP11, and VMP12, are shown in Fig. 8, and Fig. 9 and 10 shows them in graphic form.Since these are uni-directional devices, the source and drain are not interchangeable, and as they are *n*-channel devices conduction can occur only if the drain is positive with respect to the source, and high enough to ensure operation in the linear region, as with a vacuum tube, bi-polar transistor, or signal FET.

Like the vacuum tube, the absence of secondary breakdown allows realization of the full dissipation at any voltage supply up to maximum voltage and current ratings. Thus, where two different designs require the same dissipation but different voltage/load current, no derating is required. This is shown in the "safe operating area" curves. The only bi-polar transistor possessing this characteristic is the single-diffused type, which is also the least suitable for any application requiring wide bandwidth and/or high speed.

TO BE CONTINUED
NEXT MONTH SOME PRACTICAL CIRCUITS, AND HOW TO DESIGN YOUR OWN

V·FETS FOR EVERYONE PART 2

In the second half of this article, reprinted from our Canadian edition, the practicalities of VFET circuitry are explained.

In general these devices may use any of the types of output circuits in general use with valves and bi-polars, including transformer coupled (Fig. 12) where the benefits of the absence of charge carrier storage become apparent in the absence of severe ringing at the crossover point, conventional series output such as in Fig. 1 which is a straightforward transformation from a bi-polar circuit (1), and single-ended output with current source, also transposed from an excellent bi-polar circuit (2) (Fig. 2).

Bias and Drive

These series of devices are *n*-channel, enhancement type MOSFETS, and may be biased and driven using methods appropriate to signal types and bi-polars. The drain is made positive with respect to the source and the gate enables conduction by being forward biased with respect to the source, that is to say it is biased in a positive direction. Unlike bi-polars, however, they are voltage, rather than current controlled, and circuit values are selected to provide the required voltage. Any current drawn is by the bias network itself.

Three bias methods are shown; Fig. 3 shows bias supplied from a fixed bias supply. It is the simplest possible method, allows extremely high input impedances, since *Rg* may be almost any very high value desired, and its stability is limited only by the stability of the bias supply.

The design shown in Fig. 4 has the advantage of requiring no extra supply voltage since it is taken from *Vdd*. Disadvantages are those of impedance and stability. Input impedance consists of the parallel combination of R1 and R2 (disregarding input capacitance of the MOSFET and the very low input leakage). There are practical limits as to how high this combination can become; if for example, we have a 60 volt supply and require 6 volts bias, we might have some difficulty obtaining higher values than 9 megohms and one megohms for R1 and R2.

Higher values become more difficult to obtain, stability becomes less reliable, internal inductance and distributed capacitance become problems, and overcoming these difficulties usually costs money. In addition, if *Vdd* is subject to variation, then bias varies. In a class AB amplifier this could be quite serious, since *Vdd* varies considerably with output level; at high levels, *Vdd* can be expected to drop, causing a reduction in bias.

While this may reduce the danger of over-driving the device, it will be forced to operate in its non-linear region which may result in unacceptable performance characteristics unless taken into consideration in the overall circuit design (e.g. choice of feedback values). It does provide some degree of overload protection, and with correct choice of values can ▶

We have just received a note from Siliconix giving the following changes in type number — VMP-11 becomes 2N6656; VMP-1:2N6657; VMP-12:2N6658; VUP-21:2N6659; VMP-2:2N6660; VMP-22:2N6661.

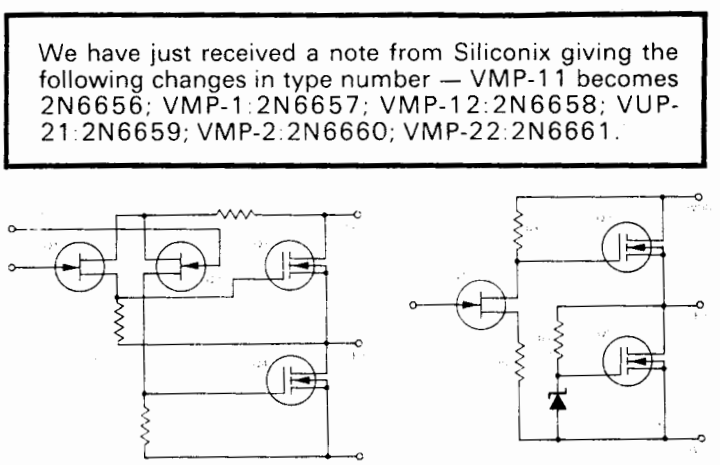


Fig. 1. Series output arrangement and Fig. 2 single-ended output with current source.

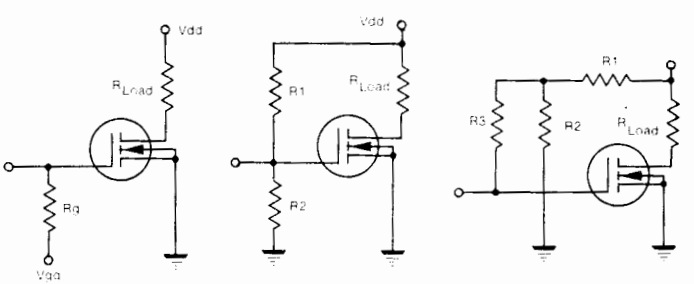


Fig. 3. High-impedance separate bias supply, Fig. 4 moderate impedance supply and Fig. 5 high-impedance common supply.

provide for class AB operation at low levels, shifting to class B at high levels. With these considerations in mind, and/or where moderate impedances are required, it offers a low cost, simple, and reasonably reliable method of establishing the operating point.

The method used in Fig. 5 is similar except that with the addition of R3 higher input impedances are possible. Its configuration is similar to a noiseless biasing system frequently used in low-level bi-polar amplifiers and integrated circuits (e.g. National LM381A) but its function is somewhat different. Resistors R1 and R2 form a voltage divider as in Fig. 4 but their junction now forms a fixed bias source as in Fig. 3. Resistor R3 can be quite high since no current flows. Meanwhile, since the parallel combination of R1 and R2 are effectively in series with R3 they can be reduced to more manageable values. Alternatively R2 can be replaced by a zener diode for stability comparable to Fig. 3.

Input Protection

Unlike most signal MOSFETS, the gate of each of these devices, with the exception of the VMP 4, is protected with an internal 15 volt, 10mA zener diode. Most signal MOSFETS, as well as the VMP 4 are unprotected, or where extremely high impedances are not required, are protected by back to back zeners. I have no information as to why this different technique is used, but it is obvious that a negative signal swing on the gate will result in forward current through the zener. If the device is to be driven beyond cutoff, the driver must be capable of delivering current during its negative swing. Alternatively a constant current source can be used, a series limiting resistor or a driver biased to the same class of operation as the V-MOSFET.

A constant current source (we'll examine an example of its use a little later) will limit current drive to the value of the constant current diode used; a series resistance will drop the drive voltage as the diode draws current. In both cases, diode current must be limited to 10mA maximum. Higher currents will damage the protective. Higher currents will damage the protective zener diode.

However, if a class B output is used, conduction only occurs during positive half-cycles. Therefore, drive signal is not required during negative half-cycles. If a source or emitter follower driver stage is biased so as to pass no negative drive, the problem does not occur. However, great care must be exercised in the design of such a stage to ensure that drive does not disappear before the output device is cut off.

This is not too difficult with a class B or near class B stage; if the output device is operated at zero bias, then a small amount of bias on the driver will ensure conduction during slightly more than 180 degrees. Class AB operation is a little more tricky. If conduction is to occur for 270 degrees, for example, the driver should conduct for slightly more than this period.

Two types of drive circuits familiar to designers of bi-polar circuits are the Darlington and Super beta, commonly used together to provide a quasi-complementary circuit. Both circuits are current amplifiers designed to provide a compound device with very high *h*fe and provide base current to the output device. However, similar circuits can be used

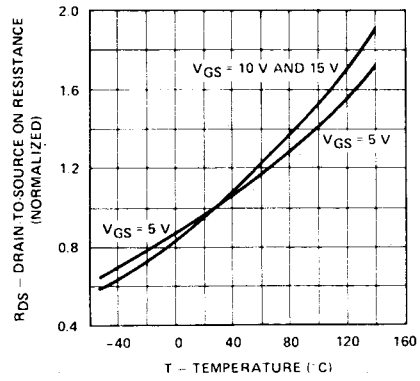
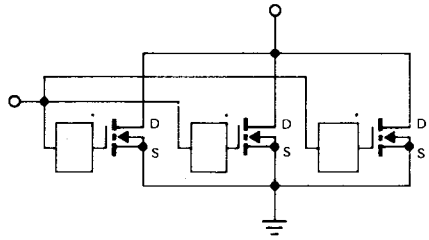


Fig. 6. Drain to source resistance against temperature (Siliconix).



*TO PREVENT SPURIOUS OSCILLATIONS, A 500 Ω 1K Ω RESISTOR OR FERRITE BEAD (FOR HIGHER SPEED) SHOULD BE CONNECTED IN SERIES WITH EACH GATE.

Fig. 7. Basic circuit for parallel operation.

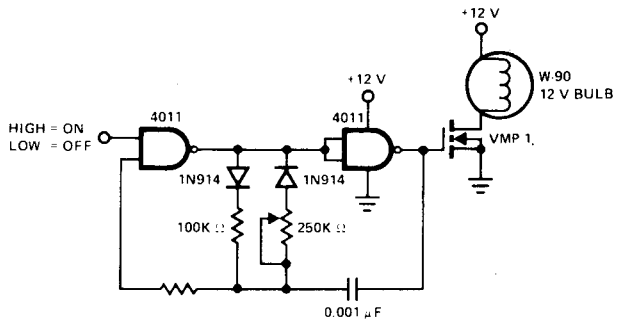


Fig. 8. Circuit of a high-efficiency light dimmer.

with these devices to provide phase inversion in a series output stage.

Thermal Considerations

As described earlier these devices exhibit a negative temperature coefficient with respect to current, so that as temperature rises, current is reduced, thus providing a self-inhibiting action which provides some protection against overload. However, this is not an unconditional effect. Fig. 6 show the

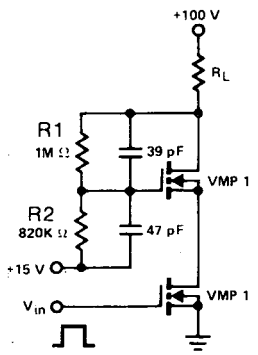


Fig. 9. Diagram for series operation.

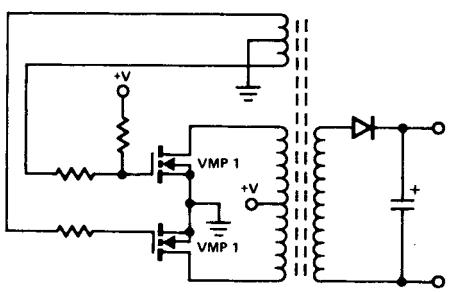


Fig. 10. A DC to DC converter (Siliconix).

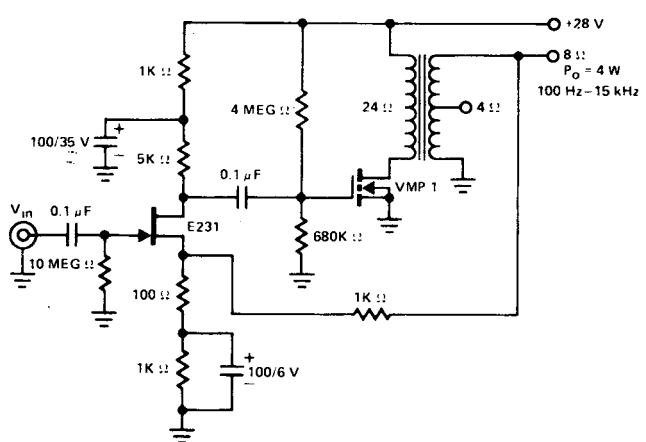


Fig. 11. Simple single-ended transformer-coupled audio power amplifier (Siliconix).

relationship between *RDS* (on) and temperature (3), based on a worst case temperature coefficient of 0.7 per cent per degree C.

Suppose that the device when on passes a current of 1 amp which causes it to heat up. The on resistance increases (which is why current drops), increasing the voltage drop across the device and the device dissipation. Now, if adequate heat sinking is used there is no real problem but if it isn't, the on resistance and junction temperature will rise to the point where extra charge carriers are generated, thus stabilizing *RDS*(on). That's great, except for the fact that this doesn't occur until the maximum safe junction temperature of 150 degrees has been exceeded.

You'll remember that we said earlier that the device was free of thermal runaway problems because of its negative temperature coefficient, but it isn't free of thermal destruction problems, and in any case, excessive temperatures will reduce output conductance. Heat-sinking requirements are, therefore, similar to those of bi-polars. The calculations of thermal operating conditions are beyond the scope of this article, but interested readers are referred to the Siliconix literature listed in the references, (4).

Extending The Ratings

The current handling capacity and therefore total dissipation capability may be easily increased by simply connecting several devices in parallel (Fig. 7). No ballast resistors are needed to ensure proper current sharing since if one device draws more current than another it simply gets a little warmer which causes it to draw less (assuming adequate heat sinking, of course). The only major precaution needed is to keep lead inductance in the gate and source connections to a minimum to prevent parasitic oscillations, unless the devices are driven from a low impedance source.

It may be advisable to insert "stoppers" – small resistors (100 to 1000 ohms) in series with each gate, wired directly to the socket, or ferrite beads mounted on the leads close to the socket terminals. An additional plus when paralleling several devices is that the gm is multiplied by the number of devices used. Mutual conductance gm is specified as the ratio of a large change in current to a small change in control voltage. If, for example, a change of 0.4 volts on the gate produces a change of 0.1 amp through one device, connecting two devices in parallel will give us an output swing of 0.2 amps, but it will still require only the original 0.4 volts gate swing. Since voltage gain A = gm x RL, if gm is increased, A is increased.

In real use, of course, the internal resistance of two devices in parallel is less than of one, the optimum load is less, so in amplifier applications, the net amplification A is the same. But notice that the drive requirements have not changed. With bi-polars current would have to be supplied to each base, thus increasing the output requirements of the drivers. Indeed, with many high-power amplifiers using multiple output devices the drivers are also power devices.

We can also extend the voltage ratings by series operation of two or more devices; Fig. 9 shows the technique. Resistors R1 and R2 bias Q2 on while C1 and C2 ensure fast switching. Input control signal is inserted between gate and source of Q1. Ordinarily the bottom of the divider chain is at ground potential for signal frequencies, so that circuit is really a cascode.

Maximum current and gm are the same as for one device. ▶

Some Practical Applications

An efficient light dimmer circuit as proposed by Siliconix is shown in Fig. 8. The 4011 acts as a pulse width modulated oscillator whose duty cycle is determined by the ratio of R1 to R2, with R2 adjusted to control the brightness of the bulb. Of special interest here is the fact that with its fast switching time, the VMP1 is especially suited to pulse width modulation at power levels and suggests it as being suitable for use in switching, or class D linear amplifiers.

A DC to DC converter is outlined in Fig. 10. The VMP1s form an oscillator with positive feedback provided by the additional coil in the gate circuits. In operation the upper V-MOSFET is biased on, and the lower V-MOSFET is off. When power is applied the upper device conducts causing current to flow from *Vdd* through the upper half of the transformer primary and the upper V-MOSFET to ground. The induced current flow through the feedback coil develops a voltage such as to shift the bias in the upper device off (if the winding is connected with the correct polarity) and the lower device on. This causes current flow from *Vdd* through the lower half of the transformer primary and the lower V-MOSFET to ground.

The secondary circuit consists of a single rectifier and filter. The resistor in the upper gate prevents shorting out of gate bias, and the one in the lower gate keeps both sides balanced. In addition, each resistor limits current through the protective diodes. These are expensive devices for such an application, but the high reliability, the reduced RF radiation (due to reduced switching transients) and the circuit simplicity easily make up for the cost. The very high circuit impedance allows for running frequency to be set by the self resonance of the transformer.

A single ended and push-pull transformer coupled amplifier for audio applications are shown in Figs. 11 and 12. Both designs utilise the biasing system described in Fig. 4. A load-line drawn on the output characteristic will show the optimum load to be 24 ohms. In Fig. 11 gate drive is supplied by a single junction FET, and voltage feedback is taken from the output transformer secondary and series fed to the source of the input device. Distortion is under 2 per cent at full output (try to get *that* with a single ended valve or bi-polar) and could probably be reduced even further by adopting a source follower output stage.

A push-pull version of Fig. 11 is shown in Fig. 12 using a differential input to provide phase splitting, drive, and a feedback point. Although the transformer winding ratio implies the use of a low impedance loudspeaker, a step-up ratio could be used for direct coupling to an electrostatic speaker, a balanced transmission line (both with some modification of the feedback circuit) an unbalanced transmission line, or a 70 volt speaker distribution line.

Notice in both circuits, and in the biasing circuits shown that no source resistors have been used, either for local feedback or for bias setting. In valve and bi-polar circuits it's a useful technique, and with bi-polars can be used to stabilize bias and control thermal runaway by using the increased current flow to increase the voltage drop, thus reducing base-emitter voltage. However, if used with these devices, it will actually impair the self-limiting action of its negative temperature co-efficient. If temperature rises due to high current, current flow is reduced. This would reduce the voltage drop across a source resistor, lowering the source voltage and increasing the gate-to-source voltage, causing an *increase* in current flow. The circuit would work great while it lasted – which wouldn't be for long.

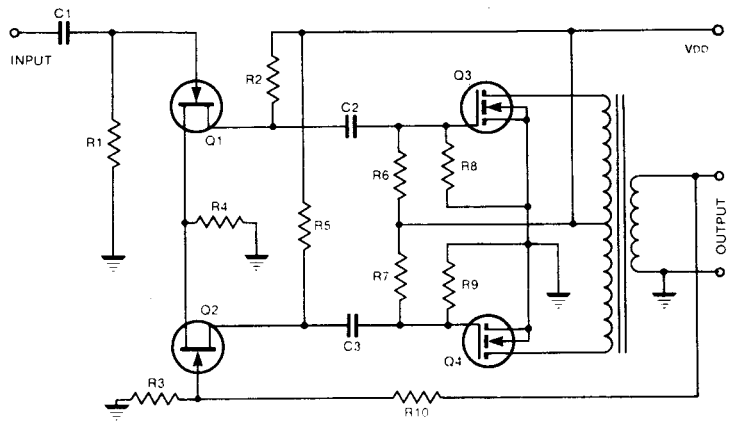


Fig. 12. Transformer-coupled output.

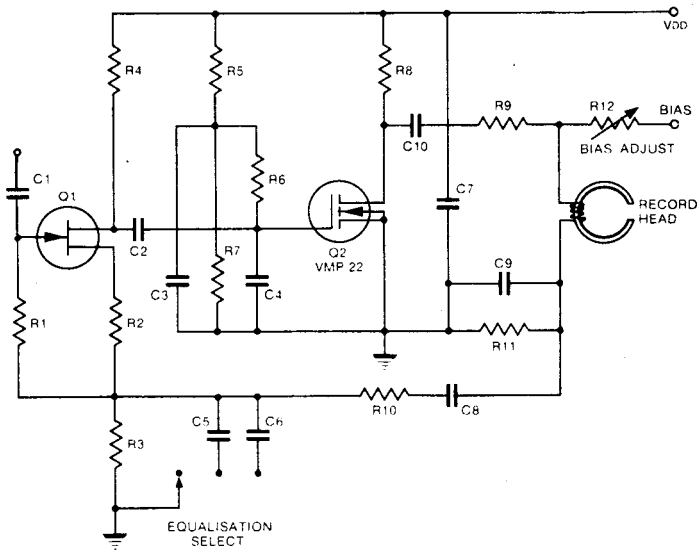


Fig. 13. Tape recording amplifier.

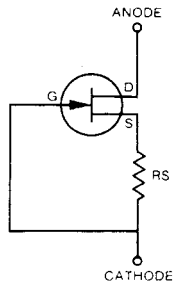


Fig. 14. A FET as a constant-current source.

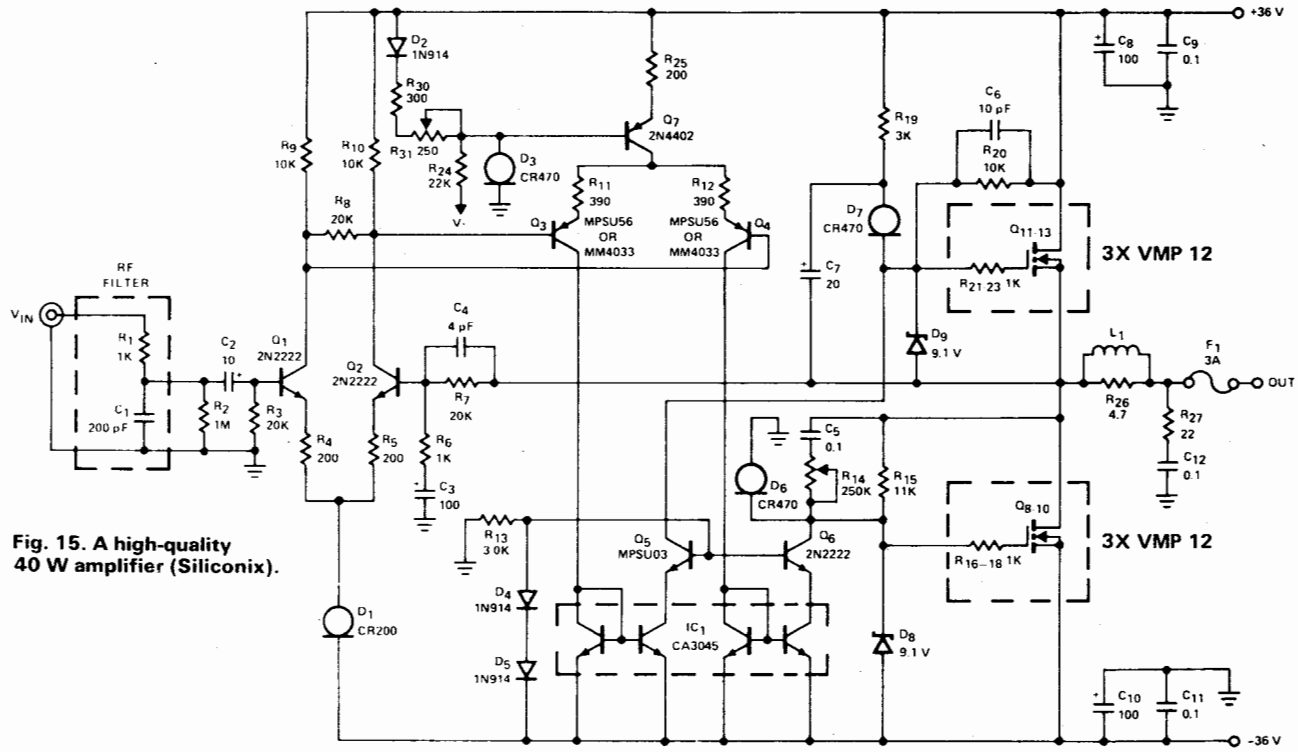


Fig. 15. A high-quality 40 W amplifier (Siliconix).

Power Amp

In Fig. 15 we have a high quality power amplifier designed by Lee Shaeffer of Siliconix Inc. (5) and described in their application notes. Output current capability is increased by using three VMP12s in parallel; providing for 6 amp current, 75 Watt dissipation and optimizing the load at 8 ohms. Q11-13 operate as a source follower, while Q8-10 form a quasi source follower. This is accomplished by applying local feedback from drain to gate via R14, R15, and driving the gate by a modified current source. This consists of a cascode circuit with a constant current diode as the load.

For the benefit of those not familiar with these devices, a constant current diode is really a FET connected internally as shown in Fig. 14. Since current in a FET is controlled essentially by the gate-to-source voltage, changes in load or in applied drain to source voltage have negligible effect since gate-to-source voltage is held constant. This is a current analogue to the zener diode and is described in detail in Siliconix literature (6).

The design is push-pull from input to output, thanks to differential circuitry throughout, prior to the drivers. Open loop distortion is low, bandwidth wide, allowing satisfactory performance with only 22dB of feedback.

Complete construction plans including PCB layout are available from Siliconix (7). A word of caution, however. Readers accustomed to construction articles in which the writer does everything but hold your soldering iron will find these plans rather sketchy. They consist of a spec sheet, schematic, board and parts layout, two paragraphs of construction suggestions; initial adjustments, and a parts list. Parts, generally, are specified as to value and rating, and that's it. These plans are excellent, but they assume some knowledge and experience on the part of the constructor. Regular 'eti constructors' should have little difficulty.

Finally, how about something elegant for its simplicity, such as the Tapered Current Voltage Limited battery charger shown in Fig. 16. This is especially useful with Ni-Cad batteries which are intended for stand-by use and are permanently on charge, such as

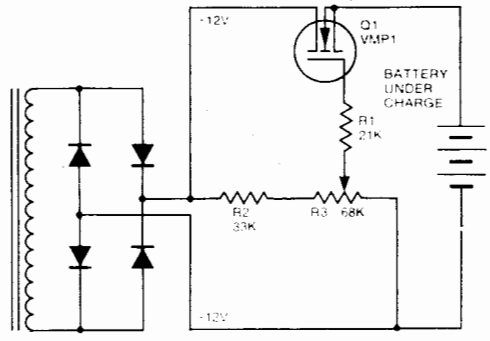


Fig. 16. Tapered-current voltage-limited battery charger.

electronic clocks. Overnight shut-downs of a few hours are occasionally but irregularly experienced. You know what this can do to clocks. Especially alarm clocks which are supposed to make noises, turn on radios, start the coffee at a pre-set time in the morning so you can go to work. Battery operation is not too satisfactory if the readout is on continuously, and Ni-Cads should not be on permanent floating charge.

With this little device current is supplied to the battery via the VMP-1. Gate voltage is set at a value equal to the desired end of charge voltage. As the battery charges its voltage increases, reducing gate-to-source voltage, thus reducing charging current. When the battery reaches full charge its voltage and that of the source equals gate voltage, and charge is terminated. If a load is placed across the battery it will draw current, and as the battery voltage drops slightly below gate voltage, charging at a trickle rate occurs – automatic.

Experimentation

The various applications shown are intended as suggestions for further experimentation on the part of the reader. They are mainly designed to illustrate various characteristics of the device under consideration, and are not necessarily representative of commercial practice or of finished designs. In some cases this may be just as well. But we would be delighted to hear of any readers' experience with any of these or other circuits.

The author's own feeling is that V-MOS constitutes a genuine breakthrough in semi-conductor technology, as important as the silicon transistor and the FET itself. We'll be seeing more of these devices, with higher ratings (a 10A 200V unit is already under development) and specialized characteristics. They are said already to be in use commercially as magnetic core drivers.

Digital enthusiasts may be somewhat impatient with the strong emphasis on audio applications in this piece but other literature has placed great emphasis on digital applications, with little attention paid to linear techniques beyond the 40 watt amplifier described here. The serious reader in all areas is referred to the references at the end.

Further literature may be obtained from the manufacturer, Siliconix Inc., 2201 Laurelwood Rd., Santa Clara, CA 95054, California. They have been most helpful in providing information for the preparation of this article.

Have fun.

ETI

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Designer's Notebook: VMOS FETS

The mysterious MOSFET dymystified, by Don Keighley.

FIELD EFFECT TRANSISTORS (FETs) are peculiar brutes. If you've used them you'll know what I mean — negative bias voltages, depletion layers, pinch-off voltages and so on, ad infinitum. If you haven't used a FET before, the theory is simple enough: a FET is essentially a doped-silicon resistor (Fig. 1), much like a normal carbon resistor. The doped-silicon, however, exhibits a change of resistance if an electric field through the resistor varies. The electric field depends on the voltage present at the gate of the FET (Fig. 2), so a change of gate voltage changes the current through (and hence the resistance across) the device. Essentially a FET forms a voltage controlled resistance. In the example shown in Fig. 2 (a P-channel FET) a gate voltage of 0V will produce a resistance of approximately 100R and a gate voltage of 5V will produce a 1M0 resistance. For a N-channel FET the opposite is true; a gate voltage of 0V will give a resistance of 100R, – 5V gives 1M0. For low drain-source voltages and low drain-source currents, the resistance change is linearly related to the gate voltage.

FETs have two enormous advantages over bipolar transistors. First, the gate input resistance is very high, meaning that virtually no current needs to be drawn from preceding circuitry. Second, FETs can exhibit very fast switching speeds — they can be used quite easily up to frequencies of many megahertz.

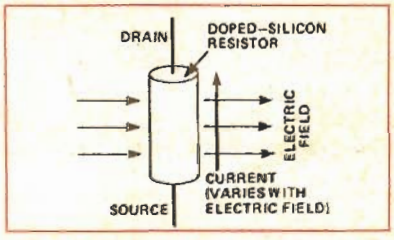

Fig. 1 A field effect transistor (FET) is a doped-silicon resistor, the resistance of which can be varied by changing the electric field through it.

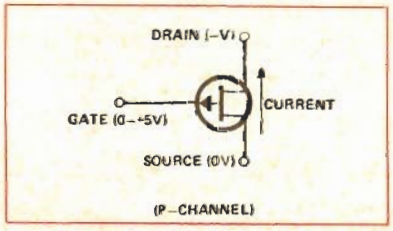

Fig. 2 The symbol for a FET. Current through the FET and hence the resistance across it is controlled by the voltage at the gate.

Problems, Problems

So, everything is fine — as long as you follow the rules. In low-power applications there is no reason why FETs can't be used anywhere a bipolar transistor can (they are, in fact, more versatile than bipolars — in low-power applications). But, therein lies the rub — power. It is very difficult (and expensive) to make a FET which can pass large currents: the main reason being the horizontal make-up of ordinary FETs. Bipolar transistors have vertical current flow and can pass larger currents because of it. Figure 3a shows the theoretical cross-section of a bipolar transistor and a similar cross-section of a FET is shown in Fig. 3b. Current flow in the bipolar is vertically upwards from collector to emitter and the large area through which the current passes allows large currents. FET current flow is from left to right (drain to source) and the small area of current flow means smaller currents than in a similar-sized bipolar transistor.

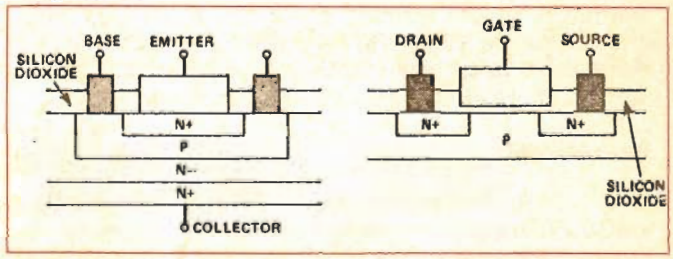

Fig. 3. Cross-sections through a) a bipolar transistor; b) a field effect transistor.

Recently, VMOS FETs have been manufactured which overcome the power problems normally associated with FETs. A typical VMOS FET cross-section is shown in Fig. 4. Current flow is now vertically upwards, from drain to source, in much the same way as in bipolar transistors. The larger chip area means large current. Hence we have transistors exhibiting all the advantages of FETs without the usual power limits. VMOS FETs also have some other very interesting advantages:

- low ON resistance — good for audio switching purposes.
- power amplification — as high as 10^8.
- positive temperature coefficient on the ON resistance — as the temperature goes up the transistor passes less current, therefore remaining thermally stable.
- easily operated in parallel to increase overall current flow — due to the inherent thermal stability no 'current hogging' by one device occurs.

We'll see applications using these advantages shortly.

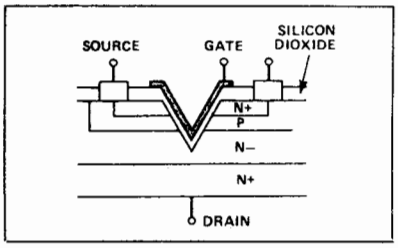

Fig. 4 Cross-section through a VMOS FET. Current flow is vertical, as in a bipolar transistor.

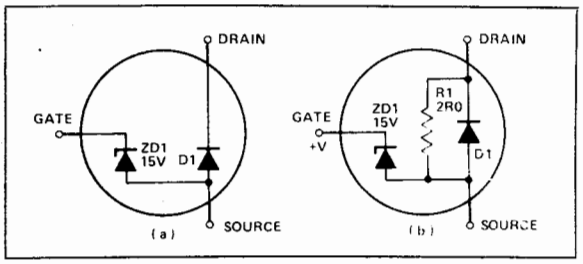

Fig. 5 Equivalent diagrams of a VMOS FET a) in the OFF state; b) in the ON state.

The equivalent circuits of a VMOS FET (such as the VN67AF) in its OFF and ON states, are shown in Fig. 5. The zener diode protects the transistor from overvoltage on the transistor gate — it is a feature on many VMOS FETs but not all! If a VMOS transistor does not have such a gate-protection zener diode, it must be handled as a CMOS IC. You must take care to avoid static build-up between connections.

In the VMOS FET's OFF state (gate is low), diode D1 is reverse-biased and no current can flow from drain to source. In the ON state the diode is effectively shorted by a 2R0 resistor, allowing current flow from drain to source. With gate-voltages between 0V and +V the resistor value is within the range 2R0 to cut in.

Applications

Low ON resistances and high OFF resistances make VMOS FETs ideal for use in audio switching networks. Figure 6 shows a simple on/off audio switch controlled by the voltage on the transistor gate: +15V turns the switch on and 0V turns it off. Audio signals can only pass in one direction, from drain to source, but any audio voltage of about −½V to +5V can be switched.

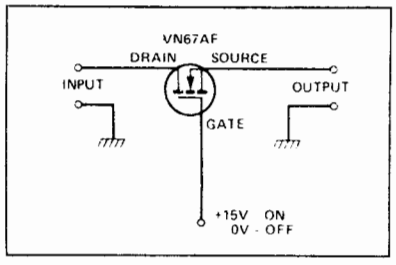

Fig. 6 A simple unidirectional audio switch formed by a single VMOS FET.

The extremely high gate-input resistance of VMOS FETs means that they can be switched by virtually any control method, such as CMOS, TTL, op-amps and so on. A four-channel audio multiplexer is shown in Fig. 7, which uses a bank of four VMOS FETs as input switches with the transistors being clocked in turn by a 4017 decade counter. The fourth output of the 4017 is connected to the reset pin, giving a 1-2-3-4 count to control the VMOS FETs. As each FET is enabled by the 4017 counter the audio input at its drain is connected, via the source and a 10k resistor, to the op amp.

If TTL logic is used to control VMOS FETs, gate pull-up resistor must be inserted (Fig. 8) to ensure that the gate voltage is pulled up to +5V when on — sufficient to give about 500 mA of current through the transistor. Figure 8 also shows the principle of VMOS current control through a load, in this case an indicatorlamp. The load can, however, be virtually anything requiring current e.g. relays, LEDs or loudspeakers.
an astable (formed by CMOS gates), a VMOS FET and a loudspeaker. When the transistor is on, its drain to source resistance is about 3R0 so about 1A (i.e. V/R = 11/11) passes through the loudspeaker. The average current (assuming a 50% duty cycle from the astable) is therefore about 500 mA. Audio output power is thus about 2W.

Paralleling two or more VMOS FETs in an output stage easily increases current-handling capacity. The siren circuit of Fig. 9 is redrawn in Fig. 10 with four paralleled output transistors. This more powerful siren will produce an output power in the region of 6W. You can see that no ballasting resistors are needed (as you would require with a similar circuit using bipolar transistors) because of the positive temperature coefficient of the drain-to-source 'on' voltage. The explanation of parallel operation is very simple: if any one of the VMOS transistors begins to conduct a larger than average current it will tend to get warmer and so current flow will reduce.

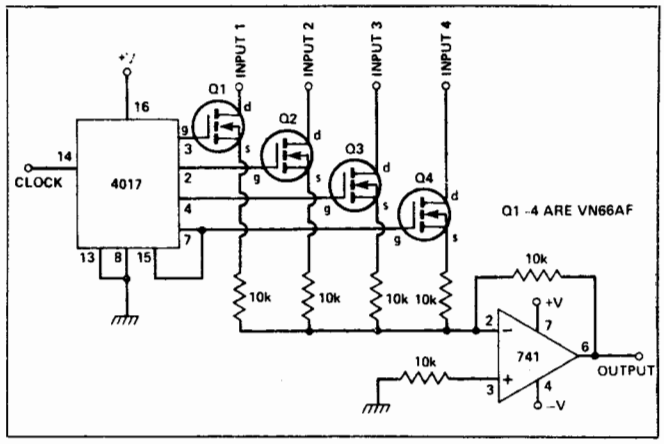

Fig. 7 Four VMOS FETs used in a four-channel audio multiplexer giving a time division multiplexed output signal.

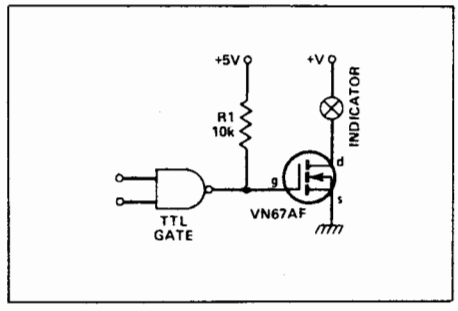

Fig. 8 TTL gate logic can be used to control VMOS FETs but a gate pull-up resistor must be used to ensure that the FET gate reaches a high enough voltage to allow sufficient current flow through the FET.

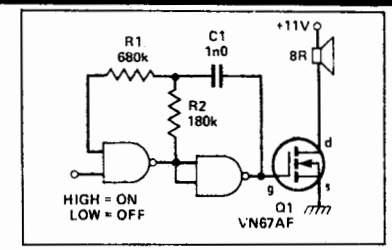

Fig. 9 Simple audio siren. An astable oscillator provides drive to switch the VMOS FET on and off at an audible rate.

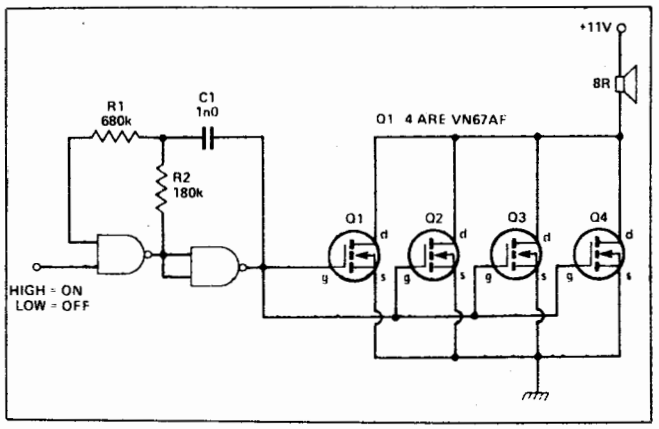

Fig. 10 Paralleling output VMOS FETs can be done simply because they are inherently thermally stable.

Linear Applications

So far we've only considered switching applications using VMOS FETs (i.e. on or off), but they can just as easily be operated in a linear mode (to act as voltage controlled resistors) in the same way as ordinary FETs.

Linear regulators in power supplies are easily constructed: such a circuit is shown in Fig. 11. An op-amp compares the output voltage with a reference voltage derived from a zener diode and parallel variable resistance. The reference voltage is thus variable from 0V to about 11V. If the output voltage is less than the reference voltage, the op-amp increases the drive voltage to the VMOS FET, and vice versa, in a negative-feedback controlled loop.

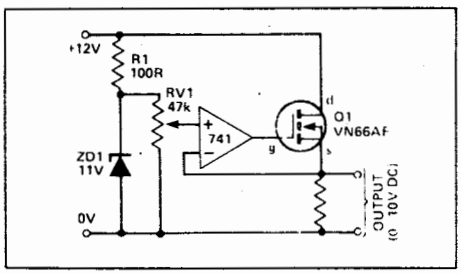

Fig. 11 A VMOS FET used in a linear voltage regulator. An op-amp is used in a negative feedback loop to provide the controlling gate voltage for the VMOS FET.

Constant-current sources suitable for charging Nicad cells can be made easily using VMOS FETs, and a simple unregulated circuit is shown in Fig. 12. The current output is defined primarily by the gate voltage of the transistor by altering the ratio of the two resistors R1 and R2. By varying the gate voltage between 0V and 5V, a range of currents of approximately 0-250 mA will be obtained. Although the high output impedance of the transistor (relative to that of a bipolar) provides a level

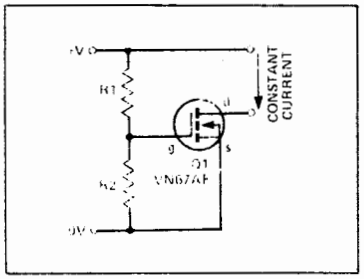

Fig. 12 Unregulated constant current source formed around a VMOS FET.

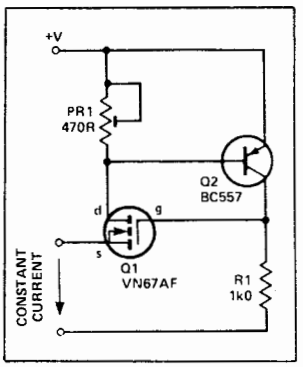

Fig. 13 Transistor Q2 holds the gate-to-source potential of the VMOS FET constant for any load. The current is therefore constant.

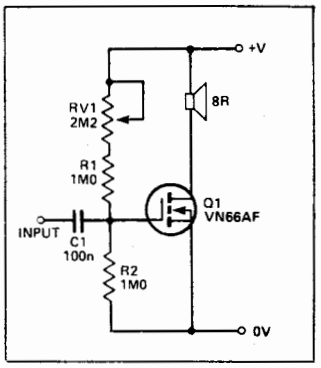

Fig. 14 A simple class A power amplifier.

of current regulation, differing loads will produce differences in current flow.

The circuit of Fig. 13 overcomes this problem with a negative feedback loop formed by Q2. This transistor holds the gate-to-source potential of the VMOS FET constant for any load. Thus the current flow is constant whatever the load.

A Class A power amplifier can be constructed with a VMOS transistor and because of the inherent thermal stability of the FET, very few precautions need be taken with the circuit (Fig. 14). The high transistor input resistance allows very high value biasing resistors. Although obviously an audio power amplifier (the transistor load is a loudspeaker!) the circuit itself will operate up to the megahertz regions.