SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HOW DESIGN RULES INFLUENCE THE HIGH FREQUENCY SWITCHING BEHAVIOUR OF POWER MOSFETs

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ABSTRACT

Starting from the basic structure of a Power MOSFET this paper describes the electrical equivalent circuit, it analyses in detail the relationship between the physical structure and the switching behaviour of the device, mainly in the high frequency range, introducing $R_{DS(on)}$, C_I and C_{OSS} gate charge concepts.

A comparison of power losses of devices rated at different BV_{DSS} of die size is carried out.

The influence of the state-of-the-art Power MOSFET structure on the ruggedness of the devices (dV/dt induced from the application circuit and unclamped inductive switching) is also briefly analysed.

Some future structural modifications improving both switching behaviour and resulting ruggedness are described.

Lastly a brief overview of IGBT technology is discussed underlining their advantages and drawbacks compared with Power MOSFET devices.

INTRODUCTION

In spite of their relatively recent introduction on the market Power MOSFET devices are becoming certainly the most successful "high runners" in the Power actuators and industrial application field because of the inherent advantages introduced in terms of switching times and simplicity of the drive.

This paper aims to outline some of the factors that are under the control of the Power device designer that enable him to improve the performance of Power MOSFETs for the benefit of system designers while leaving the basic Power MOSFET structure unchanged.

POWER MOSFET EQUIVALENT CIRCUIT

Fig 1 shows the cross section of an N-channel enhancement mode Power MOSFET structure while fig. 2 shows the equivalent electrical schematic of the device including the most important parasitic components playing a crucial role for the switching and ruggedness performance of the device.

A Power MOSFET is realized by fabricating thousands of elementary square cells where source regions are connected together by means of a common surface metallization[1].

A polysilicon layer interconnects the gates of all cells. The source region of a cell is inside a P-layer which forms the channel region necessary to control the vertical current flow of the device.

The following list is a key to the drawing of the simplified model shown in figure 2:

R_G = Polysilicon gate resistance

C_1 = Capacitance between gate and source

C_2 = Capacitance between gate and P region

C_3 = Capacitance between gate and N epytaxial layer

C_4 = Capacitance of the channel depletion zone

C_5 = Capacitance of the depletion zone in the superficial epitaxial layer

C_6 = Capacitance of the body-drain junction

In the text, reference is also made to the following capacitances:

C_{GD}: total equivalent capacitance between gate and drain

C_{GS}: total equivalent capacitance between gate and source

C_{DS}: total equivalent capacitance between drain and source

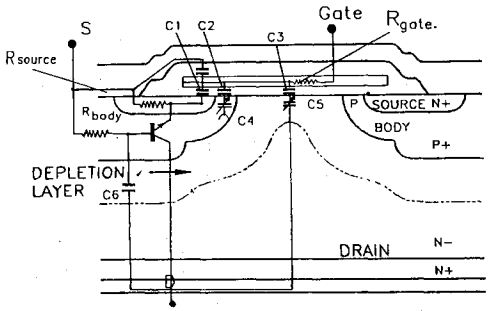


Fig. 1 - Power MOSFET structure.

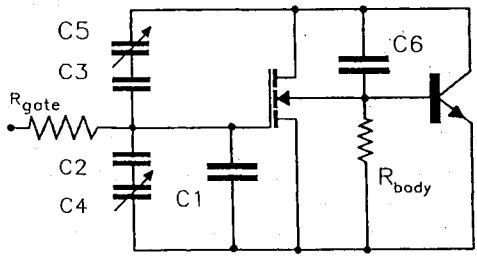


Fig. 2 - Power MOSFET equivalent circuit.

The parasitic bipolar transistor shown in fig.2 is formed by the body region between the N area of the source and the N epi layer of the drain.

The body-source resistor is due to the P-body bulk resistance and the P-body/metal contact resistance.

For most of the applications it is sufficient to substitute, on the schematic diagram, a "body-drain diode" in place of this parasitic bipolar transistor.

Device behaviour is straightforward in fact with positive drain-source biasing, as soon as the gate source voltage reaches the threshold voltage (V_{th}), necessary to invert the P-well region below the gate oxide, the current begins to flow from drain to source regions. The relationship between V_{DS}, V_{GS} and I_D is the typical input-output characteristic.

In switching applications, once the circuit topology has been established (type of converter, frequency, magnetics etc.), the optimization of the design requires the minimum of power losses possible.

During the device's on-state, $R_{DS(on)}$ is the parameter to be taken as low as possible to reduce losses; this parameter is normally defined as follows:

$$R_{DS(on)} = R_{CH} + R_{ACC} + R_{JFET} + R_{EPI}$$

Where:

- R_{CH} is the channel total equivalent resistance, depending on the horizontal layout of the device channel length and channel perimeter,
- R_{ACC} is due to excess charges within the drain region below the gate oxide,
- R_{CH} and R_{ACC} are the most dominant contribution for low voltage devices,
- R_{JFET} is the resistance of the drain region between the P body regions of two adjacent cells,
- R_{EPI} is due to the intrinsic epy bulk resistance therefore strongly dependent on BV_{DSS}.

SWITCHING BEHAVIOUR

The switching behaviour of a Power MOSFET is affected by the unavoidable parasitic capacitances of the structure. Therefore switching losses can be predicted taking into account the gate charge curve and the output capacitance, C_{DS}. Second order effects due to packaging and assembly will be neglected in the following discussion as they can be taken into account by means of suitable macromodels for computer simulation [2.3]

The gate charge curve (fig.3), obtained by injecting a constant gate input current is split into several areas.

At the beginning, starting from

$$V_{GS} = 0,\ Ci \approx C1 + C2 + C5,$$

I_D remains equal to I_{DSS} until V_{GS} reaches V_{TH} (region 1); C4 decreases further when V_{GS} increases so that when

$$V_{GS} = V_{TH},\ Ci \approx C1 + C4 + C5.$$

Therefore I_D builds-up while V_{GS} increases from V_{TH} up to $V_{TH} + I_D/gm$ (region 2). Due to the linear behaviour of the Miller body drain capacitance, V_{GS} remains constant while V_D decreases until the device becomes fully ON (region 3 and 4)

$$Ci \approx C1 + C4 + C3$$

In the saturation region (5) a further increase of V_{GS} yields a V_{DS} decrease down to $R_{DS(on)} * I_D$.

The gate charge curve is obtained at constant gate current hence the horizontal axis is proportional to the stored charge and to the time necessary to switch on and off under defined driving conditions.

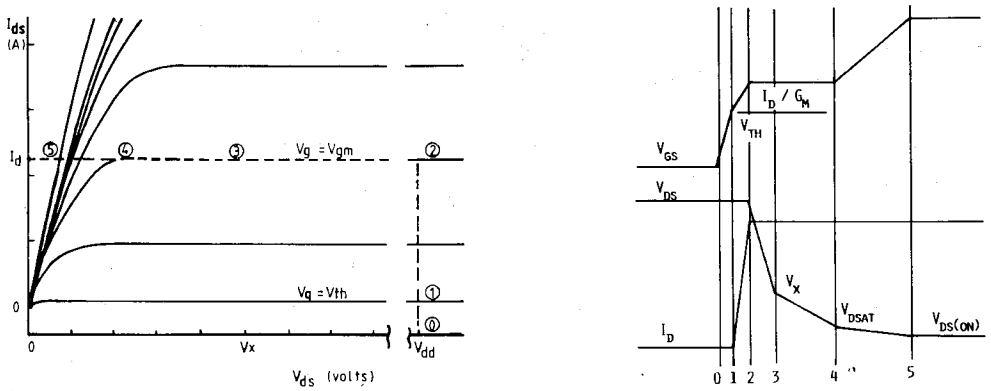


Fig. 3 - Load line and dynamic characteristics versus gate charge.

Therefore it follows that a first comparison between two devices rated at the same voltage and $R_{DS(on)}$ can be made by simply looking at their gate charge characteristics.
C_{DS} capacitance does not influence the evolution of the gate voltage but is responsible for the power losses during switching.
C_{DS} does not generally limit the dV/dt experienced by the drain region. In fact, for a high voltage device (IRF830) with the following bias conditions:

drain voltage V_{DD} = 400V

gate voltage max VG = 15V

gate external resistor R_G = 10 ohm

d_Q = charge variation inside zone 3 of the gate charge curve the dV/dt imposed by the drain voltage is:

$$dV/dt = V_{DD} \cdot (V_G - V_{TH})/(d_Q \cdot R_G) = \frac{400 \cdot (15-3.5)}{20 \cdot 10^{-9} \cdot 10} = 23 \text{ kV/msec}$$

As : $I_D = C_{DS} \cdot dV/dt$ and C_{DS} = 44 nF (typical)
I_D is about 1A

$$I_D = 44 \cdot 10^{-12} \cdot 23 \cdot 10^9 = 1A.$$

A current of roughly 1 Amp is then required to charge C_{DS} at the dV/dt set by the gate circuit: because the device has a nominal current of 5 Amps, C_{DS} has little influence when an IRF830 is used in standard applications.
This means that in most of the cases it is possible to take into account the effects of C_{DS} when calculating the power dissipation during both turn-on and turn-off.

The situation in resonant converters is quite different, where the current or voltage is negligible during switching and the previous approach is no longer valid. C_{DS} effects now influence the stored energy.

Fig. 4 shows how $R_{DS(on)}$ and C_{DS} limit the device working frequency in resonant converters.

The power dissipation versus working frequency for devices rated at different breakdown voltage, die size and $R_{DS(on)}$ has been analysed.

It can be observed that a high voltage Power MOSFET dissipation at low frequency is greater than the power dissipation of a medium voltage one with the same die size.

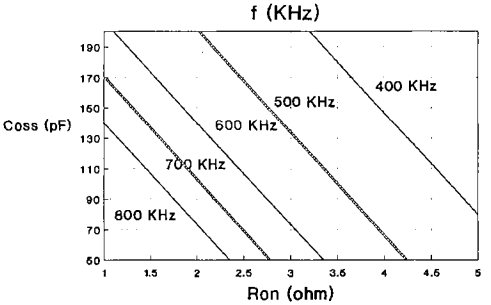


Fig. 4 -How $R_{DS(on)}$ and C_{DS} limit the device working frequency.

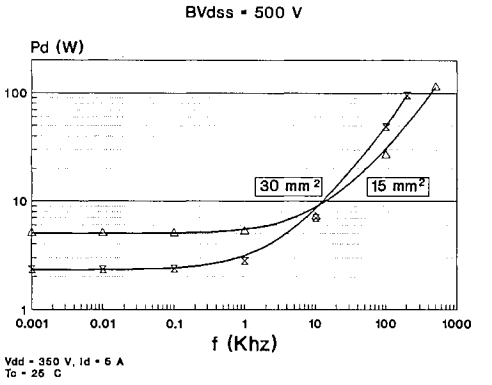


Fig. 5 - Power Dissipation versus frequency.

A simple explanation can be based on the higher value of R_{epi} of high voltage devices in comparison to medium voltage ones.
Increasing the cell packing density, especially for low voltage devices allows reduction of the die size while maintaining the same $R_{DS(on)}$ and gives an improvement in capacitance values and of the power dissipation at high frequency (where the power losses are more significant during switching).
Fig. 5 shows that a well defined application requires the right Power MOSFET device. A device with a large $R_{DS(on)}$ will be preferable for the same BV_{DSS} if the target is optimised efficiency at high frequency.

PERFORMANCE vs LAYOUT RULES

For low voltage devices it is possible to improve the $R_{DS(on)}$ and the gate charge curve by optimizing the horizontal layout and dopant profile. Fig. 6 shows the improvement obtained in gate charge characteristics for 3 devices rated at 60V, 20 milliohm, each with different cell packing density and bonding on the cells.

Cell dimension and the distance between adjacent cells are respectively 19μm and 15μm for standard devices, 14μm and 8 μm for very high density device, 10μm and 6μm for ultra high density devices.

The different behaviour is obtained because of better exploitation of the silicon area with reduced cell dimensions and distances which produce a reduced total device area for a given $R_{DS(on)}$

For high voltage devices the most significant term that contributes to $R_{DS(on)}$ is R_{epi}. Nevertheless, optimization of horizontal layout strongly influences the capacitance values (C_1 to C_5).

Starting from the standard 500V process of 0.35 Mcell/inch^2 performance can be improved by both increasing cell density up to 0.76 Mcell/inch^2 and the oxide thickness of critical cell areas (reducing C_{DS} capacitance) (see fig.7).

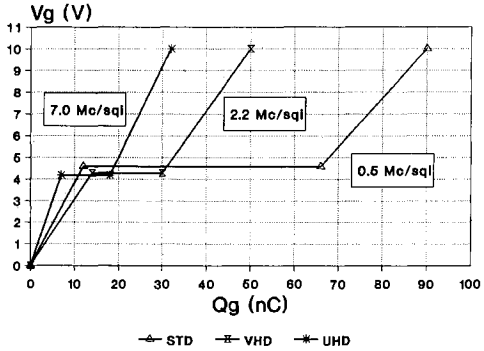


Fig. 6 - Influence of cell packing density on gate charge.

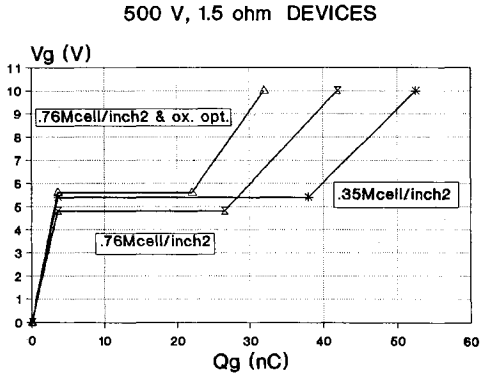
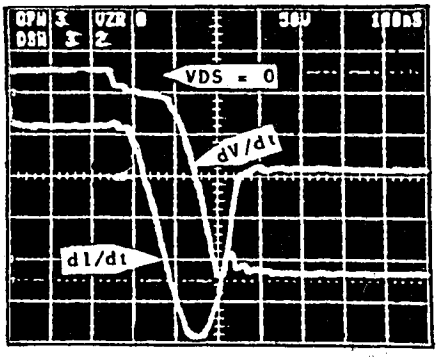
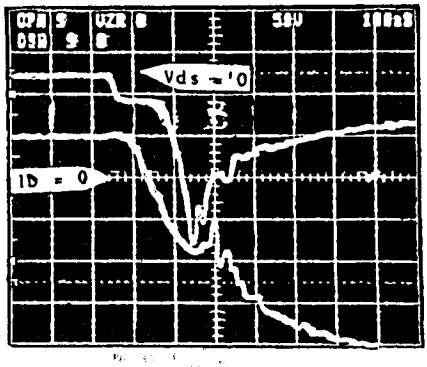


Fig. 7 - Oxide and layout influence on gate charge.



Diode recovery
V = 50V/div I = 5A/div
DI/dt = 200A/µS, dV/dt = 2V/ns



Parasitic turn-on during
Diode recovery I = 10A/div
dI/dt = 250A/µS, dV/dt = 4V/nS

Fig. 8 - Typical waveforms when failure occurs.

RUGGEDNESS

A very important characteristic of power devices is ruggedness.

A Power MOSFET must withstand a static and dynamic dV/dt U.I.S. (unclamped inductive switching) caused by the application and environment.

A failure due to static dV/dt occurs when a sudden voltage variation is experienced between the source and drain of a power MOSFET in the off state; this causes a current flow through both the body-drain capacitance and the body resistance: if the current is big enough the voltage drop across R_B causes the parasitic transistor to switch on and the device fails because of the simultaneous

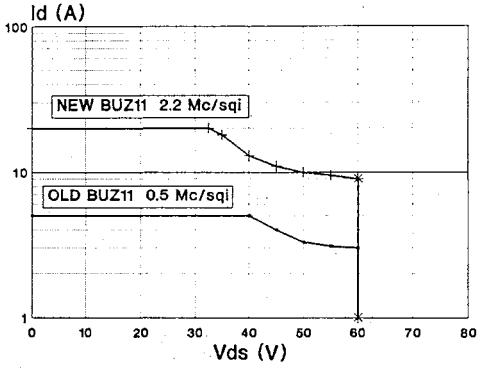


Fig. 9 - Ruggedness improvement.

presence of high voltage and high current with a subsequent hot spot generation.

The dynamic dV/dt occurs when fast voltage variation finds the body-drain diode in recovery conduction (after freewheeling behaviour). Now the current flowing through R_B is the sum of the recovery current and the current due to the body-drain capacitance.

Clearly a lower dV/dt than the previous case can now produce device degradation.

Fig. 8 shows a typical waveform during this kind of failure.

When the device switches an inductive load and the drain-source voltage overcomes the nominal defined breakdown value, then unclamped inductive switching occurs.

When this happens the energy stored in the load inductor discharges rapidly through the device at breakdown voltage, forcing I_D current, to flow in the device and increase junction temperature. Under effect of the temperature change the V_{BE} of the parasitic BJT decreases and can cause switch-on of the transistor itself, the current flowing in R_b (body bulk).

When even a small portion of the parasitic BJT switches on the whole Power MOS fails because of the current focusing effect.

The failure mechanism is almost the same for all described stress. A way to improve the ruggedness of the device is to optimise its vertical and lateral structure reducing R_B and the low current gain of the parasitic transistor as much as possible.

Fig. 9 shows the improved ruggedness obtained by the optimization of body doping in comparison with the first generation Power MOS.

IGBT VERSUS POWER MOS

From the results of measurements referring to switching speed and ruggedness the Power MOS is an almost ideal device due to unipolar conduction, but in some very high voltage applications, the device's $R_{DS(on)}$ becomes a real limitation.

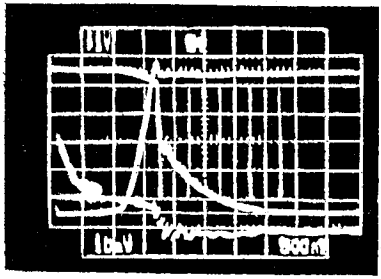
For applications at high voltage where $R_{DS(on)}$ losses are of primary importance, IGBTs find a suitable environment.

An IGBT has the same structure as the Power MOS and additionally has a P-layer under the standard N doped drain. When the device is on the P-N junction so realized injects minority carriers into the drain region modulating its total epi resistivity.

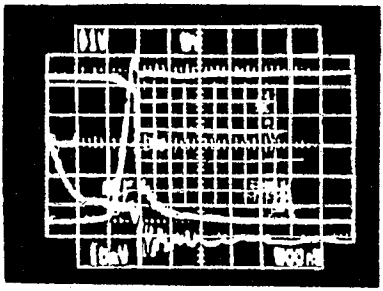
This means that the IGBT is a high voltage device with an insulated gate having a low voltage drop during the conduction phase.

In the structure of the IGBT it is easy to recognize a PNPN (degenerative) structure driven by a power MOS.

This implies that a device designer must realize a device with a degenerative current value (I_{LATCH}) greater than the nominal current in all working conditions, to ensure that the PNPN structure never turns-on. This is



Vds - 80 V/div
Id - 2 A/div
Vg - 5 V/div
Rg - 100 ohm
L - 180 µh
T - 100 °C



WITHOUT IRRADIATION

WITH IRRADIATION

Fig. 10 - IGBT switching characteristics.

well demonstrated in practice because $I_{LATCH} > 5\ I_D$ nominal in all conditions. An additional way to design latch free devices is to control transfer characteristic g_m so that for a given driving condition drain current never exceeds the permitted I_{Dmax}(I_D latch).

Currently the state-of-the-art fall time of an IGBT's drain current is longer than that of equivalent power MOSFET of same area. In fact when the power MOSFET in the IGBT structure is switched off, the charge stored in the base of the PNP parasitic transistor can be removed only by intrinsic carrier recombination.

Referring to fig.10 the first portion of t_{fall} is related to power MOSFET switch-off while the tail is due to the longer recombination time of the carriers.

A well known method to speed-up the switching off behaviour of the device is the lifetime killing technique using gold and platinum doping, ion implantation and ß irradiation. Fig.10 shows the improvement of

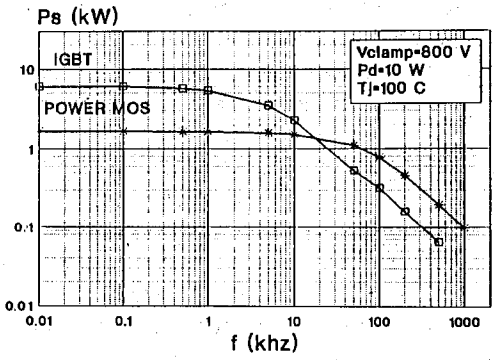


Fig. 11 - Power MOSFET versus IGBT.

IGBT's fall time obtained with ß irradiation of the device.

A comparison of the power handling capability of a 1000V IGBT and a 1000V Power MOS of both $25mm^2$ is shown in fig.11 where P_D is kept constant (10W).

It is undoubtedly advantageous to use IGBT's at a frequency below 20kHz to reduce losses and cut silicon costs.

The 3rd generation of IGBTs showing a fall time lower than 200nsec will allow the crossover point of fig.11 to move up to 50kHz.

CONCLUSION

State-of-the-art power MOSFETs and IGBTs have been shown to be rugged and reliable as a result of many years of production and technological know-how. Nevertheless, the uninterrupted progress of the technology and the constant relationship with final users and system designers is a challenge for the device designers. They must take into account second order effects and new demands to provide continuous improvement of field controlled devices both in terms of performance and lower cost.

With the aim of reaching better performance the main targets for improving the devices have been defined. These concepts will also be applied to the production of new devices. Detailed design rule variation will produce significant improvements in low voltage devices; increasing cell density and tuning dopant profiles. For medium-high voltage devices switching losses will be greatly reduced by varying the differentiating oxide thickness in conjunction with the covered active regions of the device layout.

These new design rules will therefore lead to better power conversion efficiency and greater ruggedness.

The predicted, reduced switch-off time as low as 0.2msec,obtained by new life-time control techniques (tested on 500V laboratory devices) will allow IGBTs to be cost effective competitors to power MOSFETs in the high voltage, medium frequency range (30 to 50kHz).

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