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> HB-60A P

## SCR Applications Handbook

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This handbook is the result of the efforts of a dedicated group of engineers. Not only those at International Rectifier, but also in numerous laboratories and factories throughout the world - a group of people we commonly refer to as our customers. Without our customers, the insight into the broad range of applications discussed in this book would be impossible.

Although this handbook is primarily intended for circuit and systems engineers, we hope it will also be found useful by educators, students and others interested in the use of semiconductor devices.

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## State of the Art

A new era in electric power conversion began with the development of the silicon controlled rectifier (SCR) in late 1957. From the first 16 ampere average current rated unit, an entirely new family of semiconductor devices was created. Thyristors are now available with current ratings from milliamperes to over a thousand amperes and with voltage ratings up to 2,600 volts. It is estimated that nearly one thousand domestic manufacturers use thyristor devices.

A large number of disc type (hockey-puk) SCRs are manufactured; high dv/dt and di/dt devices with fast turn-off are available for inverter applications; many plastic packages are being produced; and several manufacturers provide unpackaged SCRs and triacs in chip form. The continuing developments in both linear and digital integrated circuit components have made very complex thyristor gating and control circuits much more feasible. International Rectifier now has a line of SCR devices rated up to 2,500 amperes RMS. These devices are produced in a wide variety of packages including plastic, press-fit, conventional stud-mounted, and hockey-puk.

The triac is widely used for ac voltage control. Although the majority of these bi-directional triode thyristors are rated at or below 40 amperes and at voltages up to 600 volts, International Rectifier produces 60,100 and 200 ampere devices rated up to 1,000 volts.

The first thyristor applications involved simple phase control for lamp dimmers, heat controls, and ac motor voltage controls. As a wider range of triacs became available, they replaced the SCR in most of these applications. More advanced phase control circuits were pursued next including reversing dc motor drives with inversion to the ac system for regenerative braking of up to 6000 hp armature controlled motors for large mill drives.

A great variety of sophisticated static power conversion equipment is now being produced, ranging from small appliance controls to variable frequency 100 hp ac drives for a wide range of industrial applications.

In an electric power control system, the power converter is the critical link for matching the source to the load. The characteristics of both the source and the load and often the electrical and ambient environment determine the duty on the converter. It falls upon the circuit designer to choose the proper circuit arrangement for the specific application. However, he is often constrained by the capability of the available power switching devices. Recently, this device capability has become the major factor in determining the size and efficiency of a converter circuit, hence the optimum arrangement for the required duty. The most recent developments in thyristor characteristics have been to make this limiting factor in power system design less restrictive.


Figure 1. The International Rectifier thyristor line includes SCR devices rated from 1.6 amperes to 2,500 amperes of RMS current, peak reverse voltage ratings ranging from 50 to 1,700 volts, as well as power logic triacs. passivated assembled circuit elements, (PACE/paks), power assemblies and a wide variety of heat exchangers and mounting hardware.

The choice of power conversion systems can be divided into the four main categories shown in Figure 2. Figure 2(a) shows a dc source feeding a dc chopper which, in turn, converts the power and regulates it through a dc load. Figure 2(b) consists of an alternating current generator acting as a source for a cycloconverter. The load can require from the cycloconverter variable frequency and/or variable volt-seconds. Figure 2(c) shows a dc source feeding an inverter which feeds either an ac variable frequency load or a dc variable volt-second load. In this case the inverter may or may not be preceded by a variable de source, depending upon the requirements of the load and the type of inverter used. The fourth system (Figure 2(d)) is the familiar alternating current generator phase controlled converter which could
instead be a zero cross-over voltage triggered, pulse burst modulated system feeding a dc load. The cycloconverter is a special case of this system. A fifth category is forced commutated cycloconverters. This type of system combines the requirements of a cycloconverter and some classes of inverter so that the characteristics required of the switching device in this type of application can be derived from the other categories.

The three most critical applications are the dc chopper with timeratio control, the cycloconverter of a polyphase variety, and the inverter, whether in the chopping or pulse-modulated mode or in the alternating mode. In general, the dynamic requirements of the device in a cycloconverter application are greatly dependent upon high operating frequency. In other systems


Figure 2. Four Basic Power Conversion Systems
this frequency is low, as in the alternating inverter. In both of these cases, neither the di/dt nor the $\mathrm{dv} / \mathrm{dt}$ becomes an extreme limiting factor in the application of the device. In extreme cases where, for instance, a cycloconverter is employed as a variable speed, constant frequency drive in an aircraft application, where the designer attempts to limit the blanking time in the system in order to achieve the most usefulness from the devices and reduce the apparent output harmonic content, the cycloconverter takes on the characteristics of a pulse width modulated inverter. The semiconductor devices are required to operate conditions of high frequency operation, critical turn-off time under limited back bias conditions, and high reapplied dv/dt. The extreme case for the inverter is pulse width modulation or choppedmode operation.

The forced commutation, pulse width modulation inverter has been thoroughly described in the literature by McMurray and Shattuck [1], and Bedford and Hoft [2]. The circuit shown in Figure 3 is a typical single-phase, half bridge version of this type and is useful here for the purpose of analysis.

Referring to Figure 3, $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ conduct load current from the center tapped dc supply. $\mathrm{SCR}_{1 \mathrm{~A}}$ and $\mathrm{SCR}_{2 \mathrm{~A}}$ provide for commutation in conjunction with a properly charged capacitor $\mathrm{C}_{1}$. $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2 \mathrm{~A}}$ are triggered on simultaneously. Load current is conducted through $\mathrm{SCR}_{1}$. At the same time, the capacitor charges resonantly through the inductance $\mathrm{L}_{1}$, attaining voltage polarity as shown. SCR2A will cease conduction when the capacitor becomes fully charged. The circuit is then prepared for commutating $\mathrm{SCR}_{1}$


Figure 3. Impulse Commutated Inverter
off. When $\operatorname{SCR}_{1 \mathrm{~A}}$ is triggered on, $\mathrm{SCR}_{1}$ is back-biased through $\mathrm{L}_{1}$ and $C_{1}$ and diode $R D_{1}$. The capactor then supplies the sweepout energy of $\mathrm{SCR}_{1}$ and the load current, and may discharge its excess commutation energy through $\mathrm{RD}_{1}$. The capacitor $\mathrm{C}_{1}$ will then charge in the opposite direction to that shown and SCR $_{1 \mathrm{~A}}$ will cease conduction when this capacitor reverses its charge.

In order to provide both voltage and frequency control to a load, for example an induction motor, this circuit can be used in a multiplepulse modulation mode to be able to provide not only frequency contron, but also volt-second control. However, this mode of operation necessitates several switching and commutation cycles during a single load half cycle. Typical waveshapes of current and voltage for $\mathrm{SCR}_{1}$ are shown in Figure 4. Also shown are the current waveshapes of $\mathrm{SCR}_{2} \mathrm{~A}$
and $\mathrm{SCR}_{1} \mathrm{~A}$. The variation of these waveshapes with load and changes in circuit parameters are well explained in the references [1] [2]. In order to show distinctly the markedly different current conditons for the SCR in the commutadion and main portions of the power circuit, the duration of the commutation current has been extended with respect to the on-time of the main power circuit. In an actual case, these impulses of half sine wave current are generally much shorter in comparison to the on-time of the main SCR. Using these waveshapes as a guide, optimum device characteristics may be extracted.

The main devices see very rapidby rising current flowing into the load. They also conduct the current required to charge the commutalion capacitor. These devices switch from a very high voltage. Typically, on a rectified $460 \mathrm{~V}, 3$-phase power


Figure 4. Typical Waveshapes for Impulse Commutated Inverter
line, they will switch from approximately 550 volts when used in the full bridge version and, without external suppression, rates of rise of on-state current will be in the order of 100 to 200 amperes $/ \mu \mathrm{sec}$. By employing limiting reactance in series with the main device, this current can be quite easily limited to 20 amperes $/ \mu \mathrm{sec}$, even including the discharge of the capacitor in the snubber network, which is connected in parallel with the SCR to provide $\mathrm{dv} / \mathrm{dt}$ suppression in the circuit.

Using a circuit with a heavily inductive load, the purpose of the anti-parallel diode is obviously to provide a path for this reactive energy to flow. When the load is both active and reactive, such as a motor capable of regeneration into the system, the diode is necessary to provide a path for such regeneration without creating excess negative voltage on the main power devices. It is also useful in minimizing the harmonic content of the current in the load.

The requirements of this diode to have fast recovery and low declination rate of recovery current characteristics have been well discussed [3] [4]. The emphasis on fast recovery, however, has probably been overdone. True, it is desirable to minimize the stored charge characteristic of the diode in order to limit the amount of inductive energy stored in the external circuit. This is given by the relationship $1 / 2 \mathrm{~L} \mathrm{I} 2$. However, in order to provide an attractive electrical ambient for the main SCR, it is most important to demand a diode which has a soft declination characteristic, that is, returns from its peak negative sweepout current
to zero in a relatively soft manner. This will minimize the di/dt in the circuit, therefore minimizing the L di/dt in the external circuit. By this means the transient voltage and $\mathrm{dv} / \mathrm{dt}$ to which $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ are subjected when the anti-parallel diode does recover will be limited.

The diode, no matter how soft and quick its recovery, creates several problems. Just at the time the main SCR is required to be backbiased by the commutation circuit, the diode minimizes this back-bias by providing essentially a one-volt drop in anti-parallel with the SCR during the discharge period of the commutation circuit. This is a disadvantage for most thyristors, especially large power devices, because low back-bias on the SCR tends to extend the necessary recovery time of the forward and reverse junctions, extending the time interval before the SCR is capable of withstanding reapplication of forward voltage. In some applications, especially in drives rated several hundred horsepower, it has been found difficult to closely couple this inverse parallel diode with the main SCR; thus the circuit is no longer as simple as shown in Figure 3 but also includes some appreciable inductance in series with the anti-parallel diode. This inductance acts as a voltage divider with the commutation inductance L. As long as the net potential drop on the SCR and anti-parallel diode combination is negative with respect to the cathode of the SCR, the SCR forward blocking junction is not required to be recovered. Without lead inductance, reverse bias is maintained over the entire conduction interval of the diode. However, with inductance, the co-
sinusoidal voltage generated by the reactive voltage division, can shrink the reverse bias time by as much as $50 \%$, since the inductive potential drop is opposite to the forward drop of the diode at the midpoint of the commutation cycle. Thus, the effective commutation time is considerably reduced in the type of mechanical arrangement where the inductance in series with the antiparallel device cannot be minimized. In some cases, circuit designers have purposely inserted an inductance in this portion of the circuit, thus reducing the effective commutation time by $2: 1$ but providing increased negative bias on the SCR during the initial portion of the commutation period. By this means, some of the lost commutation time is regained by optimizing the magnitude of the reverse bias.

Some further observations can be made, referring to the waveshapes in Figure 4. The main SCR must exhibit a superior (very short) turn-off time, in addition to low switching losses and high di/dt capability. Since it is required to be commutated several times during a half cycle, short turn-off times are necessary to minimize the commutation storage energy and therefore the size of the commutation components. Since the $\mathrm{dv} / \mathrm{dt}$ in the system tends to be very high, it is also desirable that this SCR have a very short turn-off time with high reapplied $\mathrm{dv} / \mathrm{dt}$. In order to have successful pulse width modulation, it is necessary to recharge the commutation circuits before commutating the main SCR during a given half cycle to the load. Thus, for maximum utilization of the SCRs, it is desirable for the SCR charging the commutation circuit to recover
quickly, making it possible to turn on the next commutation SCR the earliest possible time after gating the main device. This provides maximum modulation in the system. The commutation device is required to have low switching losses under high sinusoidal current pulses at several times the pulse rate of the basic inverter circuitry in order to minimize its switching losses. Since the commutation circuit tends to ring, the auxiliary or commutation SCR is often required to have a high voltage rating unless an ạuxiliary resistor and an extra pair of feedback diodes are utilized from a common point of the commutation circuit to provide damping of the circuit resonance.

With these requirements in mind, International Rectifier designed an SCR capable of operation in a several hundred horsepower drive system which demanded all of the required attributes of the switching thyristors described. The accelerated cathode excitation (ACE gate) SCR with epitaxial emitter structure when tested using the circuit of Figure 5 exhibits rather low switching losses, as shown in Figures 6 and 7. Also shown in Figure 6 is a typical large junction alloy-diffused device without accelerated cathode excitation gating, tested under the same conditions. This device has considerably higher losses, namely 16,900 peak watts per pulse. Also shown in Figure 7 is a double diffused device tested under these conditions, having switching losses of 10,900 peak watts per pulse. The advantage, then, of the accelerated cathode excitation epitaxial emitter structure in terms of dynamic losses per pulse is as much as 7,300 peak watts. Using this

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Figure 5. Pulse Forming Network Test Circuit
device in a typical 60 Hz inverter motor drive application, with pulse width modulation at five pulses per half cycle, results in a difference in switching losses of 500 watts; therefore increasing the effective rating of the ACE epitaxial device over
alloy-diffused and double diffused devices tested and compared under the same conditions by a factor of 41\%.

Referring to the voltage fall shown on the turn-on waveshapes in Figure 8, it is obvious that with


Figure 6. Instantaneous Power Loss vs. Time

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Figure 7. Detail of Instantaneous Power Loss vs. Time


Figure 8(a). Instantaneous Turn-On Voltage vs. Time


Figure 8(b). Sinusoidal Current Pulse Used for Turn-Off Time Measurement with SCR in Anti-Parallel

$\mathrm{V}=200 \mathrm{~A} / \mathrm{div}$ AND $10 \mathrm{~V} / \mathrm{CM} ; \mathrm{H}=25 \mu \mathrm{SEC} / \mathrm{div}$

Figure 8(c). Trapezoidal Current Pulse Used for Turn-On Power Loss Evaluation
this new emitter structure, the turn-on of the device is completed in a much shorter period of time than that obtained using more standard emitter structures. Another important feature is the turnoff time of the device using the anti-parallel diode arrangement shown in Figure 3. However, to be useful in an induction motor drive of several hundred horsepower capacity, this turn-off time must be minimized in the 1,500 to 2,000 ampere range with the forward current declining at a rate of 40 or 50 $\mathrm{A} / \mu \mathrm{sec}$. Test results with and without an anti-parallel diode at high and low currents are shown in Table I. Figure 9 shows the percent change in turn-off time versus peak current.

Since the diode recovery is of prime importance it is interesting to observe that the SCR developed with the new emitter structure also exhibits an inherently soft recovery characteristic. An assembly using two of these SCRs is an application of this theory. One of the devices is chosen to have very good dynamics in terms of turn-off time, $\mathrm{dv} / \mathrm{dt}$, and low switching losses with the ACE epitaxial emitter structure. The other device in the assembly is connected in anti-parallel with this SCR, but is arranged to be anodetriggered through a resistor-diode network so that when it becomes forward-biased it automatically turns on. By using Hockey-Puk devices, an assembly arrangement was made in which the stray inductance of the anti-parallel loop was minimized, thus reducing the voltage divider effect discussed earlier. The turn-off time of a typical assembly tested under the identical conditions previously described, was re-
duced by $50 \%$, and the reapplied $d v / d t$ on the main commutated SCR was minimized, since the an-ode-triggered anti-parallel SCR had an inherently soft recovery characteristic. The voltage impressed on the main SCR at the initiation of commutation in the circuit remained as a forcing voltage to sweep out the main SCR during the delay period of the anode-triggered device connected in anti-parallel with it. In order to further study the advantages of this combination, a more complicated anode-triggering circuit was inserted which provided an adjustable delay period (see Figure 10). Increasing this delay period did not appreciably decrease the turn-off time of the main SCR (See Table I). Thus it was possible to maintain a simple diode resistor combination for anodetriggering of the anti-parallel device and still obtain minimum commutation time for the main thyristor.

The third device required in the system is the commutation or auxiliary thyristor. This device is required to periodically carry a high amplitude half sine wave impulse of current, providing charging and discharging of the commutation capacitor through the commutation inductance $\mathrm{L}_{1}$. This device is also required to turn off in a reasonable time under these conditions. The peak of this commutation current has to exceed the current in the main SCR previous to the turn-off since in the impulse commutated circuit the anti-parallel diode is only back-biased when the commutation current exceeds the load current. In Figure 11, $\mathrm{t}_{\mathrm{o}}$ indicates the commutation time allowed for the main device (the time the main device is back-biased), $\mathrm{I}_{\text {load }}$ indi-

Table I. Turn-Off Time

| DEVICE NO. | TURN-OFF TIME |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | WITH REVERSE BIAS ITM = 500A | WITH ANTIPARALLEL DIODE | WITH ANODE TRIGGERED ANTI- PARALLEL SCR (NO DELAY) | WITH ANODE TRIGGERED ANTI- <br> PARALLEL SCR (10 $\mu$ SEC DELAY) |
|  | $\mu \mathrm{sec}$ | $\mu \mathrm{sec}$ | $\mu \mathrm{sec}$ | $\mu$ sec |
| $\begin{gathered} X \\ \text { (1000V Rated) } \end{gathered}$ | 28 | 105 | 50 | 50 |
| $\begin{gathered} \mathrm{Y} \\ \text { (1000V Rated) } \end{gathered}$ | 20 | 74 | 35 | 35 |
| $\begin{array}{ll} \text { ITM } & =1500 \mathrm{~A} \text { Half Sine Wave } \\ \mathrm{tp} & =150 \mu \mathrm{sec} \\ \mathrm{dv} / \mathrm{dt} \text { reapplied } & =\mu \mathrm{sec} \end{array}$ |  |  |  |  |



Figure 9. Percent Change in Turn-Off Time vs. Peak Current

$\mathrm{V}=500 \mathrm{~A} / \mathrm{div}$ AND $50 \mathrm{~V} / \mathrm{CM} ; \mathrm{H}=20 \mu \mathrm{SEC} / \mathrm{div}$

Figure 10(a). Reverse Voltage with Anode Triggered Anti-Parallel SCR

$\mathrm{V}=500 \mathrm{~A} / \mathrm{div}$ AND $200 \mathrm{~V} / \mathrm{CM} ; \mathrm{H}=20 \mu \mathrm{SEC} / \mathrm{div}$
Figure 10(b). Reverse Voltage with Anode Triggered Anti-Parallel SCR Delayed with $R$-C Combination


Figure 11. Commutation Current for Impulse Commutated Inverter
cates the magnitude of the load current, and $I_{\text {com }}$ indicates the magnitude of the commutation thyristor current. Optimization requires the peak commutation current to equal 1.5 times the load current. Thus, for a load current of 1,200 amperes, the commutation device should see a peak current of 1,800 amperes. The accelerated cathode excitation epitaxial emitter device has been tested in an LC discharge circuit capable of applying turn-off conditions in order to properly simulate this commutation circuit duty.

The switching losses of the device are reduced, using an ACE epitaxial emitter structure, by a factor of $2: 1$ compared to double diffused or al-loy-diffused conventional gating emitter structures.

A significant reduction in switching losses in conjunction with good dynamic characteristics were the main objectives of the ACE gate device. However, an unexpected bonus, particularly interesting for inverter applications, is realized from the regenerative nature of the ACE gate. Once triggered into conduction, no matter how marginal the gate signal, the ACE structure
supersedes and expands the gating process. Consequently, $2 \mu \mathrm{sec}$ risetime gate pulses do not impair device operation even into high rates-of-rise of anode current. This characteristic allows the use of noise suppression capacitance, connected from gate to cathode, which is prohibited by normal devices which require hard gate drive with 0.1 $\mu$ sec rise-time. Since noise and pickup problems plague any inverter especially the high power, high frequency, impulse commutated variety - a simple method of suppression is most welcome.

Another type of suppression which is always a problem for the circuit designer is suppression of rate-of-rise of forward voltage as seen by the thyristors in the power circuit. Even in low frequency circuits, dv/dt suppression is often necessary. In high frequency systems the values necessary for the snubber network components to effectively influence the $\mathrm{dv} / \mathrm{dt}$ as seen by the SCRs are such that the snubber networks have very high dissipations and become extremely costly. Some of the work that has been done with new device geometries in the recent past, as evidenced by improved turn-on capabilities, has led to further studies in improving other dynamic characteristics of the devices by employing proper geometry.

False triggering of thyristors due to rapid changes of anode-to-cathode voltage (dv/dt) is caused by capacitive currents flowing in the thyristor. When a thyristor is in the blocking state, the center region supports the applied voltage, but this region has a certain junction capacitance as shown in Figure 12(a). The basic electrical equiva-
lent is shown in Figure 12(b). When the anode-to-cathode voltage is changing, a displacement current flows through this junction capacitance and into the gate cathode region. If this displacement current is sufficiently high, then the thyristor will become triggered into conduction by this $\mathrm{dv} / \mathrm{dt}$ generated gate current.

There is a circuit technique which is very widely used in the application of thyristors to control the $\mathrm{dv} / \mathrm{dt}$ applied to thyristors in operating circuits; this is shown in

Figure 13.
However, device manufacturers have been able to greatly improve the dv/dt capability of thy ristors by modifying the semiconductor structure. This device structure modification evolved from the use of external resistors connected from gate to cathode to improve $\mathrm{dv} / \mathrm{dt}$ capability (see Figure 14).

Obviously, this external resistor provides an alternate path for the displacement current, reducing the amount flowing through the gate cathode region. However, this re-


Figure 12. Current By-Passed by Low Impedance Negative Bias Gate Supply


Figure 13. Simple Thyristor Showing Displacement Current Collection


Figure 14. Theoretical Optimum Thyristor Geometry for External Gate Bias dv/dt Suppression
sistor provides maximum shunting of the gate to the cathode at the point where the internal gate wire is attached. At the opposite side of the silicon slice, the shunting is less efficient but with very small devices, the external resistor is useful in improving dv/dt capability. As the device area increases, a more efficient shunting (or emitter shorting) means is required. One way of achieving this is to extend the cathode metallization to cover part of the gate region as shown in Figure 15. This overlap provides an intern-
al resistor, which shunts the entire circumference of the gate cathode region, thus providing a more efficient shunt. Unfortunately, as thyristors become larger, this internal shunt becomes less efficient because of the effects of the internal lateral resistance of the gate region, as shown in Figure 16.

To provide the most efficient internal shorting, large area thyristors are fabricated with distributed internal shorts as shown in Figure 17. Small islands of gate (P) material are created which extend


Figure 15. Gate-Cathode Region Showing Edge Shorting


Figure 16. Simplified Circuit of Large Area Thyristor
through the cathode $(\mathrm{N})$ region and are connected to the cathode metallization. Through the use of this technique, it is now possible to manufacture thyristors with dv/dt capability well in excess of $1500 \mathrm{~V} / \mu \mathrm{sec}$.

IR's ACE gate device illustrates the thyristor innovations that have made possible a new generation of sophisticated solid-state power control techniques.

(b)

(c)


Figure 17. Thyristor Internal Shorts

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International Rectifier's custom-built test equipment is used to check the performance of each SCR before it is marked and shipped. This test is used to measure forward voltage drop, surge capability, gate characteristics and blocking voltage.

## Device Characteristics

## REVERSE BLOCKING TRIODE

 THYRISTOR - SCRThe most widely used member of the thyristor family of semiconductor devices is the reverse blocking triode thyristor or silicon controlled rectifier, the SCR. The SCR is a rectifier since it has a forward direction in which it may have a very low resistance and a reverse direction in which it has a very high resistance. It is controlled, since it can be switched from a high forward resistance (off-state) to a low forward resistance (on-state). Although the change in resistance is great (high voltages can be blocked, high currents can be conducted), it can be achieved with very small values of control voltage, current, and power. Also, once the SCR has been triggered on, it will remain on, even with the triggering signal removed.

The circuit symbol and block diagram of the silicon controlled rectifier are illustrated in Figure 1-1. Figure $1-2$ shows the cross-


Figure 1-1. SCR Cross-Section, Block Diagram and Graphic Symbol
section of a typical silicon wafer used in an SCR.

As a circuit element, the silicon controlled rectifier can be used to block the normal flow of current for any length of time desired. To initiate conduction, a signal is applied to the gate to trigger the device on. When used in an ac circuit, conduction may be initiated at the beginning of any given positive half cycle, thus providing a


Figure 1-2. Cross-Section of SCR
simple on-off control. Or conduction may be initiated at some later time in the positive half cycle, thus varying the average voltage impressed upon the load. This process is known as phase control, and the interval of delaying the initiation of current is the triggering angle or angle of phase retard, $a$ (in electrical degrees). The interval of current conduction (in a simple, half-wave resistive circuit) is known as the conduction angle.

In more complicated rectifier circuits having two or more rectifying devices, varying the triggering angle $a$ reduces the average output voltage, but does not necessarily change the conduction angle, since this is determined primarily by the particular circuit used.

Controlled rectifiers may be used to control ac power by connecting them in an anti-parallel (inverse parallel) manner, so that one conducts load current in one direction while the other conducts in the opposite direction. (IR's logic-triac, discussed later in this Chapter, controls ac as well as dc, depending on gate signal characteristics.) The gate triggering signal may be used to switch the flow of current on and, by using phase control, the average voltage applied to the load may be varied.

In dc circuits where the voltage across the controlled rectifier does not reverse, the gate may be used to initiate current flow, but some specific means must be provided to turn the flow off. (In operation in resistive ac circuits, current flow ceases when the supply voltage reverses at the end of each positive half cycle.) In a de circuit, a mechanical switch may be used to interrupt the current, or a more com-
plex circuit can be used in which triggering a second controlled rectifier causes a momentary flow of reverse current through the first controlled rectifier, causing it to turn off. This process is known as commutation, and is the basis of operation of the controlled rectifier inverter. Devices having a maximum rated turn-off time are useful for such applications.

Gate triggering circuits should provide a well-defined pulse of current which is several times greater than the maximum required dc gate current to trigger (at the minimum anticipated operating temperature) given for the particular device to be used. Curves in Product Data Bulletins show the range of gate voltage and current within which satisfactory operation can readily be achieved without exceeding the voltage, current, and power dissipation ratings of the gate. When conventional gate SCRs are used in applications where the initial anode current rises very steeply (high di/ dt ), gate pulses approaching the maximum permitted by the gate characteristic curve are most desirable to minimize device heating while it is first turning on. Triggering by varying a dc bias, commonly used with thyratron tubes, is not recommended for controlled rectifiers since gate sensitivity varies markedly with changes in junction temperature as well as from one device to another.

A graph of the on-state, off-state and reverse characteristics of a typical controlled rectifier is shown in Figure 1-3.

## SCR Operation [1]

A relatively straightforward representation of the SCR that demon-


Figure 1-3. SCR Forward and Reverse Characteristics
strates its regenerative switching action is shown in Figure 1-4.

For this method of analysis, the SCR is considered as two transistors. The center N-P regions of the SCR are common to both the PNP and NPN transistors. For the PNP transistor, the base current is given by the relationship in Formula 1-A.

$$
\begin{aligned}
& \mathrm{I}_{\mathrm{B}} 1=\mathrm{I}_{\mathrm{A}}-\mathrm{I}_{\mathrm{E} 1}=1_{\mathrm{A}}-a_{1} \mathrm{I}_{\mathrm{A}}- \\
& \mathrm{I} \mathrm{I}_{\mathrm{CO}}=\left(1-a_{1}\right) \mathrm{I}_{\mathrm{A}}-\mathrm{I}_{\mathrm{CO}}(1-\mathrm{A})
\end{aligned}
$$

The collector current for the NPN transistor is given in Formula 1-B: $\mathrm{I}_{\mathrm{C} 2}=a_{2} \mathrm{I}_{\mathrm{K}}+\mathrm{I}_{\mathrm{CO} 2}$

Equation 1-C:
$\left(1-a_{1}\right) \mathrm{I}_{\mathrm{A}}-\mathrm{I}_{\mathrm{CO}}^{1}=a_{2} \mathrm{I}_{\mathrm{K}}$
$+\mathrm{I}_{\mathrm{CO}} 2$
Defining $\mathrm{I}_{\mathrm{K}}$ gives Equation 1-D:
$\mathrm{I}_{\mathrm{K}}=\mathrm{I}_{\mathrm{A}}+\mathrm{I}_{\mathrm{g}}$
The final expression is given in Equation 1-E:
$\left(1-a_{1}\right) \mathrm{I}_{\mathrm{A}}-\mathrm{I}_{\mathrm{CO}}=$
$a_{2}\left(\mathrm{I}_{\mathrm{A}}+\mathrm{I}_{\mathrm{G}}\right)+\mathrm{I}_{\mathrm{CO} 2}$
$\mathrm{I}_{\mathrm{A}}\left(1-a_{1}-a_{2}\right)=a_{2} \mathrm{I}_{\mathrm{g}} \mathrm{I}_{\mathrm{CO}}{ }^{+\mathrm{I}} \mathrm{CO} 2$
$\mathrm{I}_{\mathrm{A}}=\frac{a_{2} \mathrm{I}_{\mathrm{g}}+\mathrm{I}_{\mathrm{CO}}+\mathrm{I}_{\mathrm{CO} 2}}{1-a_{1}-a_{2}}$


Figure 1-4. SCR - Transistor Analogy

## Where:

$\mathrm{I}_{\mathrm{B} 1}=$ Base current of PNP transistor
$\mathrm{I}_{\mathrm{A}}=$ Anode current of SCR
$\mathrm{I}_{\mathrm{C} 1}=$ Collector current of PNP transistor
$a_{1}=$ Fraction of holes injected from anode which are collected at J2
$a_{2}=$ Fraction of electrons injected from the cathode which are collected at J2
$\mathrm{I}_{\mathrm{CO}}=$ Leakage current of PNP transistor
$\mathrm{I}_{\mathrm{K}}=$ Cathode current of SCR
$\mathrm{I}_{\mathrm{CO} 2}=$ Leakage current of PNP transistor
$I_{g}=$ Gate current of SCR
It is possible to obtain this same expression by equating the base drive current $\mathrm{I}_{\mathrm{G}}+\mathrm{I}_{\mathrm{C}} 1$ to the base current of the NPN transistor.

Equation 1-E indicates that if $a_{1}$ $+a_{2}$ becomes equal to unity, the anode current can increase without bound, which results in a type of regenerative action. Since the current gains of transistors are effected by changes in the emitter current, if the gate drive raises the emitter current to the point where the sum of the alphas is unity, SCR switching action will occur. This switching action may also be induced by other means. Exposing the junctions to
light, a sufficient increase in device temperature, or raising the anode voltage can also cause enough increase in the emitter current to produce the situation where $a_{1}+$ $a_{2}=1$.

For a somewhat deeper physical understanding of the regenerative action in the SCR, the hole and electron concentrations can be examined during device turn-on [2]. A schematic representation of the SCR for this discussion is shown in Figure 1-5.

If a forward voltage less than the breakover voltage is slowly applied, the anode becomes positive with respect to the cathode, and junction $\mathrm{J}_{2}$ becomes reverse-biased while junctions $\mathrm{J}_{1}$ and $\mathrm{J}_{3}$ are lightly forward-biased. The device remains in the off condition. Electrons near junction J2 move toward the positively biased anode leaving behind donor impurities that are stripped of electrons; and in a similar fashion, holes in the $P_{2}$ side of $\mathrm{J}_{2}$ move toward the cathode, leaving uncompensated acceptor impurities on the right side of $\mathrm{J}_{2}$. The result is that a depletion region composed of donors and acceptors uncompensated by mobile charge carriers develops in the region of $\mathrm{J}_{2}$ creating a high electric field which sustains the applied voltage.

The equilibrium carrier concentrations in the regions of the device


Figure 1-5. SCR Two Terminal Representation
of Figure 1-5 are assumed to be as follows:
$\mathrm{P}_{1} 1019$ acceptor/ $/ \mathrm{cm}^{3}$
$\mathrm{N}_{1} 1014$ donor/cm ${ }^{3}$
$\mathrm{P}_{2} 1016$ acceptor/cm ${ }^{3}$
$\mathrm{N}_{2} 1019$ donors/cm ${ }^{3}$
These relative concentrations are typical of those required for desirable operation of practical devices.

When the forward voltage is raised to the breakover voltage level, the following events occur:
A. The increased forward voltage produces a larger forward bias on $\mathrm{J}_{1}$. This means that more holes are injected from region $\mathrm{P}_{1}$ to $\mathrm{N}_{1}$ as in a normal forwardbiased diode. Since the electron density in $N_{1}$ is much less than the hole density in region $\mathrm{P}_{1}$, electron injection from right to left across $\mathrm{J}_{1}$ may be neglected.
B. The holes injected from $\mathrm{P}_{1}$ to $\mathrm{N}_{1}$ diffuse across region $\mathrm{N}_{1}$ and are then swept across $\mathrm{J}_{2}$ because of the large electric field at $\mathrm{J}_{2}$. This junction had been reversedbiased by nearly the full anodecathode applied voltage.
C. The holes swept across $\mathrm{J}_{2}$ increase the hole density in region $\mathrm{P}_{2}$. This produces a momentary build-up of positive charge in region $\mathrm{P}_{2}$, which raises the effective forward bias on $\mathrm{J}_{3}$.
D. The greater forward bias on $\mathrm{J}_{3}$ causes more electrons to be injected from $\mathrm{N}_{2}$ to $\mathrm{P}_{2}$ as in a normal forward conducting diode. Because of the relative carrier concentrations, hole injection from $\mathrm{P}_{2}$ to $\mathrm{N}_{2}$ is negligible compared to the increased electron injection from right to left across $\mathrm{J}_{3}$.
E. The electrons injected into region $\mathrm{P}_{2}$ diffuse across this region and are swept into the $\mathrm{N}_{1}$ region
by the electric field across $\mathrm{J}_{2}$.
F. The additional electrons swept into the $\mathrm{N}_{1}$ region momentarily raise the negative charge in this region, which results in greater forward bias on $\mathrm{J}_{1}$. This increased forward bias causes more holes to be injected from $\mathrm{P}_{1}$ to $\mathrm{N}_{1}$. This is the beginning of event A above, and thus a regenerative switching action occurs.
The regenerative switching action continues until the anodecathode voltage across the device drops to about one volt. This low value of voltage results because the electric field across $\mathrm{J}_{2}$ continues to sweep holes from $\mathrm{N}_{1}$ to $\mathrm{P}_{2}$ and electrons from $\mathrm{P}_{2}$ to $\mathrm{N}_{1}$ until a sufficient number of the uncompensated donors and acceptors in the space charge region of $\mathrm{J}_{2}$ have become compensated to forward bias this junction. In the steady-state forward conducting condition, the major carrier flow involves holes from left to right across $\mathrm{J}_{1}$ and electrons from right to left across $\mathrm{J}_{3}$. Recombination in the relatively long $N_{1}$ and $P_{2}$ regions must occur to provide the necessary hole and electron current across $\mathrm{J}_{2}$ to sustain the carrier flow at the terminals of the device.

Although the turn-on action has been discussed, assuming it was initiated by increasing the anodecathode voltage to the breakover level, a similar action is initiated when gate current is applied. This increases the forward bias on junction $J_{3}$, producing a sequence of events, starting with event $D$, which again produces the regenerative switching action.

The anode-cathode voltage across the device in the forward conducting condition is the sum of
the voltages on the three junctions as shown in Formula 1-F:
$\mathrm{V}_{\mathrm{AK}}=\mathrm{V}_{\mathrm{J} 1}-\mathrm{V}_{\mathrm{J} 2}+\mathrm{V}_{\mathrm{J} 3}$
Since the "back-injection" on $\mathrm{J}_{2}$ is not as great as the injection across the other two junctions, the forward voltage of the SCR, when it is on, is somewhat greater than the forward drop of a similar diode conducting the same current. For example, the corresponding diode and SCR drops might be typically 0.8 volt and 1.1 volts respectively.

An interesting feature of the "turned-on" condition of the SCR is that the middle junction, $\mathrm{J}_{2}$, is forward-biased, while the current flowing through it is a reverse current with respect to this junction [3]. Thus, junction $\mathrm{J}_{2}$ in this condition is similar to the thermoelectric generator or the recovery state of a silicon rectifier.

However, the "generator" behavior of the plain rectifier is a short duration carrier recombination or clean-up period, while the "generator" character of junction $\mathrm{J}_{2}$ is maintained continuously when the SCR is in its forward conducting state. Thus, the forward power loss is less than the sum of the theoretical losses in junctions $\mathrm{J}_{1}$ and $J_{3}$. It may be calculated from the observed terminal voltage drop vs. current characteristic as in a simple rectifier.

This has been a brief discussion of the operation of the SCR. For a more complete discussion of this subject, the reader may refer to a number of semiconductor texts and articles, including references [4], [5], and [6].

[^1]are strongly influenced by temperature. Since there are two dependent variables (voltage and current) and four independent variables (con-duction-state, gate current, time, and temperature), the presentation of the complete set of characteristics is impracticable, and only the most essential characteristics are discussed.

## Off-State with No Gate Signal

In the off-state, with no gate signal applied, the controlled rectifier has the characteristics of two conventional silicon rectifier diodes connected in series, back-to-back. As seen in Figure 1-3, the off-state characteristic is essentially symmetrical and consists of a saturation current region where the current is substantially independent of applied voltage but is strongly temperature dependent, and an avalanche region where the current rises rapidly for only a small increase in applied voltage. In the reverse direction, the avalanche breakdown is similar to that in a silicon rectifier diode, where excessive avalanche current can destroy the device.

In the forward blocking, or offstate, region, avalanche current above a certain value will switch the device to the on-state and the offstate characteristic is terminated at the voltage where this occurs. This is known as the forward breakover voltage. Both the reverse breakdown voltage and the forward breakover voltage are temperature dependent. Devices are normally assigned the same voltage rating in both the off-state and reverse directions. However, most devices exhibit a slightly higher reverse avalanche voltage than off-state ava-
lanche voltage and, therefore, in practice, it is the off-state voltage rating that becomes the final rating of the device. The off-state and reverse power losses are small compared to the forward conduction and switching losses.

The breakover voltage and current are stable and reproducible for a particular device at a given temperature and the quoted breakover voltage is equal to, or greater than, rated peak repetitive voltage over the entire range of operating temperatures. The current to assure the device remaining in conduction after triggering but with gate current removed (the latching current) is of the same order of magnitude but is somewhat greater than the holding current, the minimum current at which the device will remain in the on-state, although there may be a considerable spread between devices.

At the point of breakover, the SCR suddenly switches to the onstate, where it exhibits a characteristic similar to a conventional silicon rectifier diode, having a very low forward voltage and a high current carrying capability.

The device will not return to the off-state until the anode-to-cathode current has been reduced by external means to a value below the holding current. The holding current is the minimum value that will continue to sustain the device in the on-state and any further reduction will cause the device to switch off.

The blocking currents are strongly temperature dependent. Figure 1-6 shows the variation of this leakage for a typical device over the temperature range from $-65^{\circ} \mathrm{C}$ to $+130^{\circ} \mathrm{C}$. This example is only typical, and there will be variations
among individual devices and among series of devices.

Of greater significance is the temperature dependence of the breakover voltage. This relation is shown in Figure 1-7. From this figure, it can be seen that the use of breakover as a means of controlling the device would be difficult since the operating temperature would have to be accurately controlled.

## Off-State with Gate Signal

When gate current is present, an appreciable increase in both offstate and reverse current is observed. This results in additional power losses which could damage the device if not considered when determining the permissible onstate current.

When a small gate current is applied to an off-state biased device (anode positive with respect to cathode), in addition to an increase in off-state leakage current, the breakover voltage will be substantially reduced. Figure $1-8$ shows the effect of increasing gate current on the off-state characteristic. To avoid the possibility of the device triggering on when it is not supposed to, most designers utilize pulse triggering techniques. The triggering pulses are then made large enough to insure positive triggering at all temperatures, thereby reducing the possibility of a triggering failure.

## On-State

In the on-state, a controlled rectifier has a forward characteristic similar to that of a silicon rectifier diode. Average current turned on is independent of gate current, except at very low levels. The characteristic is dependent on temperature,


Figure 1-6. Typical SCR Blocking Current


Figure 1-7. Typical SCR Breakover Voltage


Figure 1-8. SCR Off-State and On-State Voltage
but the change in on-state voltage with temperature is small. Typical on-state voltage versus on-state current characteristics are shown in Figure 1-9.

The limiting factors for maximum permissible on-state current are power loss and current density. On the other hand, at low on-state currents approaching the holding current, the on-state characteristic becomes unstable. At levels below the holding current, the device turns off and reverts to the offstate, when the gate trigger pulse is removed. The value of the holding current decreases with increasing temperature as shown in Figure 1-10.

At low levels of on-state current, the on-state voltage increases with decreasing current and in this region, the device has a tendency to turn off. Over an appreciable range,
the on-state voltage is substantially constant, and at high current levels (above rated current), the device becomes primarily resistive, particularly at high temperatures. In this region, the resistances of the silicon-to-metal contacts and the internal conductors become significant and are of particular importance with regard to devices carrying high surge current pulses of short duration. The temperature dependence of the on-state voltage at high levels of current is such that a self-sustaining temperature rise is produced. The familiar loop observed on a volts-versus-current oscilloscope trace is caused in part by this transient heating hysteresis.

It is important to differentiate between holding current and latching current. Holding current is the current below which a controlled rectifier fails to conduct when the


MAXIMUM INSTANTANEOUS ON-STATE VOLTAGE
(VOLTS)
Figure 1-9. SCR On-State Voltage
anode current has been smoothly decreased. Latching current, on the other hand, is the minimum level of anode current at which the controlled rectifier will latch on and maintain itself in the on-state after an applied gate trigger current has been removed. Again, latching current occurs when the device is in the off-state and is being triggered on. The holding current occurs when the device is in the on-state, and current through the device is decreasing until the device turns off. Latching current may be sev-
eral times greater than holding current.

## Voltage Rating

In selecting controlled rectifiers, the voltage and current ratings are the first considerations. The voltage rating should be high enough to withstand anticipated voltage transients, as well as the repetitive peak off-state and reverse blocking voltages that the device will see. In heavy industrial rectifier diode equipment, it is common practice to provide a margin of two and


Figure 1-10. Typical SCR Holding Current
one-half times between the working peak reverse voltage applied by the circuit and the repetitive peak reverse voltage rating of the rectifier diodes.

In the case of controlled rectifiers, a somewhat smaller margin is quite often employed. This is the result of two factors. First, the maximum junction operating temperature for controlled rectifiers is usually lower than for rectifier diodes. Diodes usually may be operated up to $190^{\circ}$ or $200^{\circ} \mathrm{C}$. Most controlled rectifiers are limited to $125^{\circ} \mathrm{C}$ although a few may be operated at $150^{\circ} \mathrm{C}$. At these lower temperatures, reverse leakage is less and there is reduced danger of a catastrophic failure due to a reverse voltage spike. Second, it is possible, by using selenium surge suppressors, such as IR's Klip-Sels, to engineer clamping circuits which prevent transients that appear across the
controlled rectifiers from exceeding about 1.7 times the device peak voltage rating ( 2.4 divided by $\sqrt{2}$ ). Thus, equipment designed for operation directly from a 480 -volt power circuit under conditions of five percent high ac line voltage and protected with Klip-Sels, can make use of controlled rectifiers rated 1200 volts. (The ac supply voltage will be 505 volts under five percent high line conditions, and this will impose a working peak reverse voltage on the controlled rectifiers of 715 volts. Since 1.7 times 715 is 1215 volts, a 1200 -volt device is suitable.)

## Current Rating

Controlled rectifiers are assigned both an average current rating (based on $180^{\circ}$ current conduction angle and averaged over a full cycle) and an RMS current rating. The RMS rating (which is also the de
rating) is useful, because it is essentially independent of the angle of current conduction, whereas the average current rating decreases as the conduction angle is made less than $180^{\circ}$. Also, the RMS rating for a given device is larger than the average rating, which makes RMS values more appealing when comparing one unit with another.

For conventional alternating current, the RMS value is the peak value divided by $\sqrt{2}$. In contrast to this, for a current which consists of only one $180^{\circ}$ (half sine wave) pulse each cycle, the RMS value is the peak current divided by two. (In this latter case, the RMS value can also be expressed as $\pi / 2$ or 1.57 , or $1.11 \sqrt{2}$ times the average current).

The RMS value of two half sine wave current pulses in one cycle is $\sqrt{2}$ times the RMS value of one such pulse per cycle. Thus, when two identically rated controlled rectifiers are connected in anti-parallel (see Figure 1-11), they can handle 1.41 times the RMS current rating of either one (this is 2.22 times the average current rating of either one).

On the other hand, when one controlled rectifier is fed by the
output of a single phase bridge rectifier, as shown in Figure 1-12, there is a current pulse through the controlled rectifier each half cycle. The maximum alternating current (in the ac line feeding the bridge) which can be controlled is 1.11 times the average current rating of the controlled rectifier for this mode of operation. It will be seen that this should be just half the RMS current that two identical units can carry when connected in anti-parallel, except that when conducting two half sine wave current pulses each cycle, a controlled rectifier has an average current rating, at any given case temperature, which is approximately 30 percent greater than the average rating for the more usual case of only one half sine wave pulse per cycle. This is true, because the peak current that must be carried for a given average current, when there are two current pulses per cycle, is only half of what it would be if there were only one pulse per cycle, and this causes less heating of the semiconductor material for a given value of average current and permits higher current rating. These ratings are extended in Table I-I.


Figure 1-11. SCR Anti-Parallel Circuit


Figure 1-12. Hybrid Bridge Rectifier Circuit

Table I-I. RMS Values

|  |  | RMS RATINGS |  |
| :---: | :---: | :---: | :---: |
|    <br> IT(AV) IT(RMS)  <br> MAX. MAX. RMS ONE DEVICE, | DEVICES |  |  |
| AVERAGE | ON-STATE | TWO PULSES | IN ANTI- |
| ON-STATE | CURRENT | PER CYCLE (A) | PARALLEL* |
| CURRENT | RATING (A) | $(1.11 \times 1.3$ | (A) (V) |
| RATING (A) | $(\pi / 2$ IT(AV)) | IT(AV)) | $\pi / 2$ IT(AV)) |
| 3 | 4.7 | 4.3 | 6.7 |
| 4.7 | 7.4 | 6.8 | 10.4 |
| 10 | 16 | 14.4 | 22.2 |
| 16 | 25 | 23 | 35.5 |
| 22.3 | 35 | 32 | 49.5 |
| 35 | 55 | 51 | 78 |
| 40 | 63 | 58 | 89 |
| 50 | 80 | 72 | 111 |
| 70 | 110 | 101 | 156 |
| 80 | 125 | 115 | 178 |
| 100 | 160 | 144 | 222 |
| 150 | 235 | 216 | 333 |
| 250 | 400 | 361 | 555 |
| 300 | 470 | 433 | 666 |
| 350 | 550 | 505 | 777 |
| 420 | 660 | 606 | 933 |
| 500 | 785 | 722 | 111 |
| 550 | 865 | 794 | 1222 |
| 700 | 1100 | 1010 | 1555 |
| 850 | 1350 | 1227 | 1888 |
| 1000 | 1600 | 1447 | 2221 |
| 1600 | 2500 | 2309 | 3554 |

Rounded off for ease of handling.
*Based on maximum allowable case temperature being the same as maximum allowed at rated half sine wave current.

The waveform of currents carried by inverter thyristors seldom is a simple half sine wave or rectangle. Yet, the designer needs to know the RMS value of this current when selecting the thyristor to be
used. The following procedure may be used to calculate the RMS value of any current waveform that can be broken up into segments for which the RMS value can be calculated individually.

The RMS value of the current wave is determined by dividing the waveform into segments, calculating the $I^{2} t$ value for each segment, adding up these values and from this sum, determining the RMS value. Thus, it is possible to quickly determine the RMS value of current waveforms of any degree of complexity.

Figure 1-13 tabulates the $\mathrm{I}^{2} \mathrm{t}$ values (more precisely the integral of $\mathrm{i}^{2} \mathrm{dt}$ values) for a number of commonly encountered current waveforms. The mathematical expressions describing these waveforms are given under the heading "Function." In addition, a formula for $\mathrm{I}^{2} \mathrm{t}$ is shown for each case. Both expressions are in terms of the peak value of the current wave in question, $\mathrm{I}_{\mathrm{cm}}$. The duration of time term, $t$, is defined in the waveshape sketches. Note, in the case of an exponentially decaying current wave, the time used is the value to the first time constant of the exponential curve.

Figure 1-14 illustrates how a complex wave may be split up into segments which are appropriate for this method of analysis. A waveshape can be found in Figure 1-13 which will match the shape of each segment of the complex wave. By inserting the peak value of each segment and the duration of each segment into the formula for the I 2 t of a wave having the same waveform, the $I^{2} t$ value of each segment can be obtained.

The RMS value of the complex current wave can then be calculated from Formula 1-G:
$I_{R M S}=\sqrt{\frac{\Sigma \mathrm{t}_{1} / \mathrm{t}_{0} \mathrm{I}^{2} \mathrm{t}}{\mathrm{t}_{1}-\mathrm{t}_{0}}}$

Where:
$\mathrm{t}_{0}=$ Time at start of complex waveform.
$\mathrm{t}_{1}$ = Time at end of the wave.
If the waveform being analyzed includes a period where current is zero, it is only necessary to include the duration of this period in the term $\mathrm{t}_{1}-\mathrm{t}_{0}$.

This method may be used to calculate the RMS value of an alternating current wave, as well as of a rectified wave. This results from the fact that the current is squared in $I^{2} t$, so that $I^{2} t$ is positive for either polarity of current.

## Calculation of Rectangular Waveform

Current Rating of Thyristors
Most data sheets for power thryistors (silicon controlled rectifiers and triacs) give current ratings only for the case of a single phase (half wave) resistive load. These ratings are usually given in the form of curves showing the maximum allowable current vs. case temperature for various conduction angles such as $180,120,90,60$ and 30 degrees. These current waveforms are shown in Figure 1-15(a). In the case of stud-mounted thyristors, the highest value of average current given for any particular waveform has an RMS value equal to the maximum RMS rating of the thyristor in question.

The designer quickly finds that in a great many applications current flow is nearly rectangular so that the above published ratings do not apply. For a given conduction period and average current value, the heating effect of a rectangular current wave is less than that of a multilated sine wave of equal con-


Figure 1-13. Evaluating Current Waveshapes


Figure 1-14. Analyzing Complex Waveshapes


Figure 1-15. Comparison of Conduction Angle Waveforms
duction time, because the peak current is less. This can be seen from Figure 1-15(b). Thus, the thyristor current ratings for rectangular waveform current are greater for any given conduction period, and advantage should be taken of this.

The current waveshapes observed in single phase, full wave (bi-phase) and polyphase rectifier units usually are more rectangular than sinusoidal. Load inductance tends to prevent rapid variations in load current, making the current waves flat topped. On the other hand, inductance in the ac supply (including rectifier transformer reactance) prevents instantaneous transfer (commutation) of current from one rectifying element to the next, resulting in overlapping current flow through the circuit elements that are commutating. The resulting current waveforms are illustrated in Figure 1-15(c). When phase retard is used in such rectifier equipment to control the average
output voltage, the angle of current flow remains essentially fixed; the initiation of the current wave is simply delayed by the angle of phase retard, $a$, as can be seen from Figure 1-16. It is interesting to note that as $a$ is increased, for a given value of load current, commutation takes less time so that the current waveform becomes more rectangular.

The duration of current flow (the conduction period) is determined by the rectifier circuit and not by the angle of phase retard. Conduction periods for common rectifier circuits are given in Table I-II.

The current flow through thyristors in many inverter circuits also tends to be rectangular. The current flows through an inductance from a source having a fixed direct voltage and the thyristors serve to switch the current from one load winding to another; thus, essentially rectangular current waves result.

Table I-II. Conductive Periods of Common Rectifier Circuits, Inductive and Resistive Loads

| CIRCUIT | CONDUCTION PERIOD |
| :--- | :---: |
| Single-Phase, Center Tap <br> (bi-phase, single-way) | $180^{\circ}$ |
| Single-Phase Bridge (double-way) | $180^{\circ}$ |
| Three-Phase Wye (single-way) | $120^{\circ}$ |
| Three-Phase, Double Wye with Interphase <br> Transformer (single-way) | $120^{\circ}$ |
| Three-Phase Bridge (double-way) | $120^{\circ}$ |
| Six-Phase Star (single-way) | $60^{\circ}$ |
| Twelve-Phase Quadruple Zig-Zag <br> (single-way) | $30^{\circ}$ |



Figure 1-16. Effect of Phase Retard

## Calculation Procedure

The calculation of thyristor current rating for rectangular waveform currents is not difficult. Basically, all the device data that are required is the on-state voltage curve at maximum rated junction temperature, the transient thermal impedance curve for times between 1 and 10 milliseconds, and the rated thermal resistance of the device, junction-to-case. If a curve of instantaneous on-state power loss vs. instantaneous on-state current is available, this will simplify the procedure, because it will not be necessary to calculate the instantaneous on-state power loss from the onstate voltage curve.

Junction temperature rise above case temperature can be calculated by formula $1-\mathrm{H}$.

$$
\begin{gather*}
\Delta \mathrm{T}_{\mathrm{J}(\mathrm{JC})}=\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{P}_{\mathrm{TM}} \mathrm{R}_{\theta \mathrm{JC}}+ \\
\left(\mathrm{P}_{\mathrm{TM}}-\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{P}_{\mathrm{TM}}\right) \mathrm{Z}_{\theta\left(\mathrm{t}_{\mathrm{p}}\right)}= \\
\mathrm{P}_{\mathrm{TM}}\left[\frac{\mathrm{t}_{\mathrm{p}} \mathrm{R}_{\theta \mathrm{JC}}}{\tau}+\right. \\
\left(1-\frac{t_{p}}{\tau}\right) \mathrm{Z}_{\left.\theta\left(\mathrm{t}_{\mathrm{p}}\right)\right]} \tag{1-H}
\end{gather*}
$$

Where:
$\mathrm{T}_{\mathrm{J}(\mathrm{JC})}=$ Junction temperature rise above case temperature
$\mathrm{P}_{\mathrm{TM}}=$ Peak on-state (triggered) power loss at a given
peak anode current.
$\mathrm{t}_{\mathrm{p}}=$ Duration of one rectangular wave of current (conduction period).
$\tau$
$\mathrm{R}_{\theta \mathrm{JC}}$
$=$ Time interval between the start of one current pulse and the start of the next (the period, i.e., the reciprocal of the supply frequency).
$=$ Thermal resistance of the thyristor, junction-to-case.
$Z_{\theta}\left(t_{p}\right)=$ Transient thermal impedance of the thyristor for the time duration of one current pulse.

In the above formula, the average junction temperature rise is calculated by the expression $t_{p} / \tau$ ( $\mathrm{P}_{\mathrm{TM}}$ ) $\left(\mathrm{R}_{\theta \mathrm{JC}}\right)$ (average power dissipated times thermal resistance). To this is added a term which represents the temperature response of the junetion in the final pulse of load current. This additional rise is calculated by multiplying the increment of power dissipated during the pulse which is greater than the average power dissipated $\left(1-t_{\mathrm{p}} / \tau\right) \mathrm{P}_{\mathrm{TM}}$, by the transient thermal impedance for the time of one current pulse, $\mathrm{Z}_{\theta}\left(\mathrm{t}_{\mathrm{p}}\right)$. More complex expressions have been published for this temperature rise, but the above expression gives a conservative answer that is within a few degrees of the more precise value, and is far easier to calculate.

A further refinement is to allow for the heating effect of the losses during the reverse and off-state blocking periods. In power thyristors, these losses generally are only a few watts, and so cause only a small additional temperature rise of 1 to 2 degrees Celsius (Centigrade).

## Temperature Rise Above Cooling Fluid Temperatures

The equipment designer must know junction temperature rise above cooling fluid temperature (temperature of incoming air, water, oil, etc.), not simply junction temperature rise above device case temperature. The additional rise of the case above the cooling fluid is calculated by multiplying the total average on-state, off-state and reverse blocking losses by the thermal resistance from case to cooling fluid.

There are usually two thermal drops in series in the path of heat flow from case to cooling fluid, these being:
A. Thermal resistance from case to heat exchanger (often referred to as case to heat sink).
B. Thermal resistance from heat exchanger to cooling fluid.
Thermal resistance from case to heat exchanger is a function of the size of the thyristor base and presence or absence of silicone grease on the mating surfaces. Representative values are given in Table I-III.

Thermal resistance from heat exchanger to cooling fluid must be determined from the configuration and size of the heat exchanger used, the velocity of the cooling fluid, the surface finish of the heat exchanger, etc. The thermal resistance, device-mounting-surface-tocoolant, of the heat exchanger can be obtained from the heat ex-
changer manufacturer or from tests.

An expression for calculating junction temperature rise above cooling fluid temperature can now be written, taking into account the factors just discussed (see Formula 1-J):

$$
\begin{gather*}
\triangle T_{J(J A)}=\left(\frac{t_{p}}{\tau} P_{T M}+P_{B(A V)}\right. \\
\left(R_{\theta J C}+R_{\theta C H}+R_{\theta H A}\right)  \tag{1-J}\\
+P_{T M}\left(1-\frac{t_{p}}{\tau}\right) Z_{\theta\left(t_{p}\right)}
\end{gather*}
$$

Where:
$\mathrm{T}_{\mathrm{J}(\mathrm{JA})}=$ Junction temperature rise above ambient cooling fluid temperature.
$\mathrm{R}_{\theta \mathrm{CH}}=$ Thermal resistance, case to-heat exchanger.
$\mathrm{R}_{\theta \mathrm{HA}}=$ Thermal resistance, heat-exchanger-to-ambient .
$\mathrm{P}_{\mathrm{B}}(\mathrm{AV})=$ Average power losses during reverse and offstate blocking periods.
(The other terms are the same as those for Formula 1-H).

The RMS value of the current rating calculated by the above procedures should not exceed the RMS current rating of the thyristor being considered.

## Example:

To illustrate the principles discussed above, consider a 70 ampere (average), 110 ampere (RMS) studmounted thyristor operating in a three-phase bridge rectifier circuit with inductive load. The on-state voltage and the transient thermal impedance curves for this device are given in Figures 1-17 and 1-18, respectively. Maximum thermal re-

Table I-III. Thermal Resistance, Case to Heat Exchanger

| SIZE OF THYRISTOR CASE |  |  | $\mathrm{R}_{\theta}$ CS THERMAL RESISTANCE TO HEAT EXCHANGER $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ |  |
| :---: | :---: | :---: | :---: | :---: |
| HEX BASE (INCH) | THREADED STUD | $\begin{gathered} \text { JEDEC } \\ \text { NO. } \end{gathered}$ | DRY | GREASED |
| 7/16 | 10-32 | TO-64 | 0.90 | 0.60 |
| 9/16 | 1/4-28 | TO-48 | 0.50 | 0.35 |
| 11/16 | 1/4-28 | TO-65 | 0.35 | 0.25 |
| 1-1/16 | 1/2-20 | TO-49, 83, 94 | 0.15 | 0.10 |
| 1. $1 / 4$ | 3/4-16 | TO-93 | 0.10 | 0.08 |
| 1-11/16 | 3/4-16 | - | 0.05 | 0.04 |



Figure 1-17. Maximum Instantaneous On-State Voltage
sistance, junction to case, is $0.30^{\circ} \mathrm{C} /$ watt, and maximum rated junction operating temperature is $125^{\circ} \mathrm{C}$. The device is mounted on an air-cooled heat exchanger having a thermal resistance to ambient air of $0.30^{\circ} \mathrm{C} /$ watt at a cooling air
velocity of $1000 \mathrm{lf} / \mathrm{min}$. The maximum ambient air temperature in which the device is to operate is $45^{\circ} \mathrm{C}$. The supply frequency is 60 Hz and therefore the supply period, $\tau$, is $1 / 60=0.0167$ seconds. From Table I-II, the conduction period is 120 deg., or $0.0167 \times 120 / 360=$ $5.6 \times 10^{-3}$ seconds, and from Figure 1-18, the transient thermal impedance for a square wave pulse of this duration is found to be 3.6 x $10^{-20} \mathrm{C}$ /watt.

From Table I-III, the thermal resistance from case to heat exchanger is $0.10^{\circ} \mathrm{C} /$ watt (greased). The average power loss during the reverse and off-state blocking periods can be calculated from the maximum leakage current for the thyristor, 5 mA . A conservative, worst-case estimate is 3 watts, full cycle average.

The above data may be used in Formula 1-J to solve for the peak power loss required to raise the peak junction temperature to $125^{\circ} \mathrm{C}$ :


Figure 1-18. Maximum Transient Thermal Impedance, Junction-to-Case
$\left(1 / 3 \mathrm{P}_{\mathrm{TM}}+3\right)(0.30+0.10+0.30)$
$+\mathrm{PTM}_{\mathrm{TM}}(1-1 / 3) 0.036=125-45$
$0.257 \mathrm{P}_{\mathrm{TM}}=77.9$
$\mathrm{P}_{\mathrm{TM}}=303 \mathrm{~W}$
From the on-state voltage curve for $125^{\circ} \mathrm{C}$ junction temperature, the peak current producing this amount of power loss can be found (by successive approximations) to be: $303 / 1.68=180$ amperes. The maximum permissible average current is then $180 / 3=60.0$ amperes.

Referring to Figure 1-15(b), the RMS value of this current is $180 / 1.732=104 \mathrm{~A}$, which is within the 110A RMS rating of the thyristor in this example.

The manufacturer will usually publish a curve of on-state power loss vs. direct current, such as the dc curves shown in Figures 1-19 and 1-20. Such curves permit reading the value of permissible peak amperes directly without the need for calculating them from the onstate voltage curve.

If the manufacturer has provided curves of average on-state power loss for rectangular current wave operation, such as shown in Figures $1-19$ and 1-20, the average current may be read directly by converting the peak power to average power. In the example, the average power is 101 watts, which is one-third the peak power, since the conduction period is one-third of a cycle ( 120 degrees). From the 120 degree curve in Figure 1-19, the average current is found to be 59 amperes.

## Using Rectangular Current Waveform Rating Curve

When the manufacturer provides curves of average on-state current vs. maximum allowable case temperature for rectangular current waves, such as the curves in Figure 1-21, calculations can be simplified even more. In this case, the main step in determining the current rating is to calculate the temperature rise of the case above ambient due to the on-state losses, which is the


Figure 1-19. Average Low Current Level On-State Power Loss, Rectangular Current Waveform


Figure 1-20. Average High Current Level On-State Power Loss, Rectangular Current Waveform


Figure 1-21. Average On-State Current vs. Case Temperature, Rectangular Current Waveform
product of these losses and the thermal resistance from case to ambient. Taking the example, this thermal resistance is $0.40^{\circ} \mathrm{C} /$ watt. The average reverse and off-state blocking power losses are 3 watts, and the temperature rise from case to ambient caused by these losses is $1.2^{\circ} \mathrm{C}$. In effect, this raises the maximum allowable ambient temperature to $46.2^{\circ} \mathrm{C}$. A current must now be found for which the maximum allowable thyristor case temperature, as read from Figure 1-21, will be just high enough to permit the average power generated in the thyristor to be dissipated to the cooling medium by the heat exchanger. This value of on-state current must be found by successive approximations. Since the answer in this case, 59 amperes, has previously been calculated, the procedure can be illustrated by a single calculation:

Maximum case temperature permitted at 59 amperes:
$86.0^{\circ} \mathrm{C}$ (from Figure 1-21)
Maximum temperature rise permitted between ambient and case at 59 amperes:

$$
\begin{aligned}
& 86.0-[45+(3 \times 0.40)]=86.0 \\
& -46.2=39.8^{\circ} \mathrm{C}
\end{aligned}
$$

Maximum average on-state power loss permitted:
$39.8 / 0.40=99.5$ watts
Maximum average on-state current permitted:
58.5 amperes (from Figure 1-19)

This is essentially the same as the 59 amperes used at the start of the calculation.

The manufacturer's data sheet provides a non-repetitive surge current rating, which may be imposed on the thyristor when it is operating at maximum rated current, voltage, and temperature conditions in a half-wave circuit. Following rated
non-repetitive overload, the thyristor is not expected to exhibit offstate blocking capability until its junction has cooled down to the maximum rated operating temperature. A fault sufficiently severe to cause an overload of this nature is not expected to be a normal operating condition, and a thyristor is not expected to be subjected to more than approximately 100 such faults during its useful life.

On the other hand, more moderate overloads are often encountered very frequently in rectifier equipments. These are known as repetitive overloads, and since they are of indeterminate number, they must not cause the thyristor junction temperature to be raised above the maximum rated operating temperature, if long thyristor life is to be assured. Consequently, a reduction in the continuous loading on the thyristor is required, to provide an additional temperature rise which can take place during the overload.

The required amount of this temperature rise margin depends upon the severity of the overloads and their durations.

Of the many possible overload schedules, one of the most common is that of a short overload following continuous loading. The following simplified formula, $1-\mathrm{K}$, an extension of Formula 1-J, may be used to calculate the junction temperature rise at the end of the overload:
$\Delta T_{J(J A)}=\left(\frac{t_{\mathbf{p}}}{\tau} \mathrm{P}_{\mathrm{TM}(\mathrm{SS})}+\mathrm{P}_{\mathrm{B}(\mathrm{AV})}\right)$
$\left(R_{\theta J C}+R_{\theta C H}+R_{\theta H A}\right)+$
$\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}\left(1-\frac{\mathrm{t}_{\mathrm{p}}}{\tau}\right) \mathrm{Z}_{\theta\left(\mathrm{t}_{\mathrm{p}}\right)}+$
$\frac{\mathrm{t}_{\mathrm{p}}}{\tau}\left(\mathrm{P}_{\mathrm{TM}}(\mathrm{OL})-\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}\right)$

$$
\begin{aligned}
& \mathrm{Z}_{\theta(\mathrm{OL})}+\left(\mathrm{P}_{\mathrm{TM}(\mathrm{OL})}-\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}\right) \\
& \left(1-\frac{\mathrm{t}_{\mathrm{p}}}{\tau}\right) \mathrm{Z}_{\theta\left(\mathrm{t}_{\mathrm{p}}\right)}
\end{aligned}
$$

Where:
$\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}=$ peak steady-state, onstate power loss (prior to overload).
$\mathrm{P}_{\mathrm{TM}}(\mathrm{OL})=$ peak on-state power loss during overload.
$\left.Z_{\theta(O L}\right)=$ transient thermal impedance of thyristor for overload period.
(The other terms are the same as those given for Formulas 1-H and $1-\mathrm{J}$.

Care should be taken in determining the transient thermal impedance for the overload period. A transient thermal impedance curve for the thyristor mounted on an infinite heat sink may be used only over the range where the transient thermal impedance is no more than ninety percent of the maximum value given on the curve. For longer overloads, a transient thermal impedance curve for the device mounted on the heat exchanger actually being used is required. Two such curves are given in Figure 1-18 for the thyristor used in the example.

If a temperature rise margin, $\triangle \mathrm{T}_{\mathrm{J}(\mathrm{OL})}$, is provided for overloads when determining the steady-state current loading of the thyristor, the repetitive overload which can be imposed can be found by solving Formula 1-L for PTM(OL), the peak on-state power loss during the overload period.

$$
\begin{align*}
& \Delta \mathrm{T}_{\mathrm{J}(\mathrm{OL})}=\left(\mathrm{P} \mathrm{TM}(\mathrm{OL})-\mathrm{P}_{\mathrm{TM}}(\mathrm{SS})\right) \\
& {\left[\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{Z}_{\theta(\mathrm{OL})}+1-\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{Z}_{\theta\left(\mathrm{t}_{\mathrm{p}}\right)}\right]} \tag{1-L}
\end{align*}
$$

Having found the maximum peak on-state power loss permitted during the overload period, the average current which can be carried during the overload period may be calculated as before.

## SCR Dynamic Characteristics <br> Triggering

The simplest means for triggering a controlled rectifier is to apply a positive dc potential between gate and cathode. This is the operating condition used to determine compliance with published specifications for maximum gate current and voltage required to trigger all units of a given type. The designer quickly learns that there are a number of considerations which require the application of greater current and voltage to the gate in order to achieve successful device operation in a practical piece of equipment.

Fortunately, in modern devices, the maximum gate current and voltage which may be applied greatly exceed the values required to trigger under de conditions. This is illustrated in Figure 1-22, which shows the gate characteristics for a 70 ampere (average) device. It can be seen that the designer has a large region within which to operate where the gate can be driven harder than the amount barely required to turn the device on and yet not be driven beyond its maximum peak power rating. In order to avoid exceeding the maximum continuous power rating of the gate when applying a high peak signal, it must be applied as a pulse and not continuously.

For reasons of economy, both to reduce the size of components used to build the gate excitation circuit and to reduce the power consumed


Figure 1-22. Gate Characteristics
by this circuit, a relatively short pulse is often applied to the gate, rather than a long pulse or a continuous de signal. As pulse width is reduced, it is found that the peak current and voltage required to trigger a given device becomes greater. This effect is most noticeable for pulse widths shorter than 15 microseconds, as shown in Figure 1-23. For such short pulses, it can be seen that essentially a fixed electrical charge is required to trigger the controlled rectifier.

A controlled rectifier does not turn on "all at once." When first the gate is pulsed, there appears to be no increase in current flow. This period is known as the delay time, $\left(\mathrm{t}_{\mathrm{d}}\right)$, and usually is shorter than one microsecond. Current then starts to flow through the wafer in a small region near the gate lead, then spreads throughout the silicon wa-
fer. This second period, during which the current through the device increases, from $10 \%$ to $90 \%$, is known as the rise time $\left(\mathrm{t}_{\mathrm{r}}\right)$. It varies from a few to more than 10 microseconds, being longer for the larger controlled rectifiers.

This action is sufficiently fast so that any controlled rectifier will be turned fully on long before a sine wave of current at a conventional power frequency (up to 400 Hz ) has reached its peak. On the other hand, when a controlled rectifier is used to switch high amplitude current pulses, large currents can flow before turn-on is complete. With the current confined to a small portion of the total semiconductor volume, the forward voltage will be greater than the published value, and the additional heat generated by large currents flowing at that time has been known to cause a


Figure 1-23. Gate Current to Trigger
local failure of the semiconductor material near the gate terminal.

There are several remedial steps which the circuit designer can take in overcoming these limitations:
A. Increase the magnitude of the current pulse carried by the gate. This increases the number of carriers injected into the semiconductor material. But published gate current and voltage limits must not be exceeded.
B. Add a self-saturating inductor in series with the controlled rectifier. This should require from 10 to 50 microseconds to saturate, during which time the controlled rectifier is being turned on by the small current which flows through the reactor before it saturates.
C. Select controlled rectifiers which are comparatively fast in turn-on action. (IR's ACE gate SCRs fall into this category.)
D. Use several smaller controlled rectifiers in place of one larger one, in one of two arrangements:

1) Several controlled rectifiers connected in parallel.
2) Several controlled rectifiers connected in series.
In the arrangement described in D1 all the controlled rectifiers would be triggered from a single gate pulse generator, each through a "ballast" resistor in series with its gate. In D2, the circuit would have to be redesigned to operate at a higher voltage and a lower current. All gates could be triggered simultaneously using a multi-secondary pulse transformer, or opto-electronic gating technique. A "sympathetic" ("slave") arrangement could also be used, so that triggering one controlled rectifier would cause the others to be triggered with a minimum of delay.

For most controlled rectifier types only a typical value of turnon time (the sum of $t_{d}+t_{r}$ ) is given. If units having a specified maximum turn-on time are required, standards for measuring this time are needed. Turn-on time is affected by the magnitude of the triggering pulse, the magnitude of the voltage applied between anode and cathode, the junction temperature, and the inductance in the test circuit.

A check on the magnitude of the inductance in the test circuit can be made by simultaneously observing anode-to-cathode current and inverted anode-to-cathode voltage on a fast-writing cathode ray oscilloscope. When the two traces are adjusted to overlap at beginning and end, they will overlap throughout the turn-on interval if the circuit is purely resistive. The effect of the inductance is to delay the rise of current, and speed up the fall of voltage. From this it is evident that turn-on time should not be measured by observing the fall in voltage, as this can give times which are too short

It is difficult to eliminate circuit inductance completely; on the other hand, a small amount should not seriously impair the accuracy of the turn-on time measurement.
di/dt
When an SCR is triggered, it does not immediately go into full conduction, as discussed in the section on Triggering. Current flow begins in a relatively small area; how small depends upon how the SCR is made, and in many units, how strong a signal is applied to the gate.

In a conventional SCR having a single gate, on-state current is initi-
ated in a small spot near the gate and turn-on action spreads, as indicated in Figure 1-24, at a rate which is roughly 0.1 mm per microsecond. Using this value, the time required to fully switch on SCRs of various current ratings can be calculated (Figure 1-25).

The time required to turn high current rated SCRs fully on is far longer than the published "turn-on time" of most devices, which is usually in the order of five microseconds. This is the result of the definition of turn-on time, which is specified as the length of time after


Figure 1-24. Turn-On Action


Figure 1-25. Time to Turn-On
the appearance of the gate triggex pulse that is required for the volt age across the SCR to decrease to ten percent of its initial value. If the SCR is switched on with 500 voits, it will only partially be to 50 volts, since when fully turned on, its on-state voltage will be in the order of two volts. Thus, the turn-on time rating of a power SCR performance throughout the entire turn-on interval.

The stress on an SCR is particularly severe during the first few microseconds of current flow. An excessive rate-of-rise of on-state failure.

Two di/dt ratings exist in the industry; the non-repetitive rating, determined from a test lasting $\mathbf{3 0 0}$ pulses, and the repetitive rating, looo-hour life test. The repetitive di/dt rating will often be about 33 percent of the non-repetitive rating.

In a conventional gate SCR, the di/dt rating is affected by the mag nitude of the gate drive; trigger pulses of over one ampere in ampliand less result in an improvement in di/dt capability
A typical triggering circuit is shown in Figure $\mathbf{1 - 2 6}$. In many cases, where the load is inductive and most certainly when the load consists of a de or ac motor, it is the full time the SCR is to remain in the conducting state. For low frequency operation of thyristors, this requirement can be very difficult to achieve without incorporathigh cost in the triggering circuit. For instance, in the case of a large power supply constructed as a magnetic supply for a plasma arc generator, it was necessary to drive six phase, full converter (bridge) configuration. Since the load was inductive, it was necessary to supply


Figure 1-26. Typical Triggering Circuit
the gating signals over about $140^{\circ}$ of the half cycle. Since this type of load also subjects the SCR to high inrush currents, it was necessary to provide the gating signals with a sharply rising leading edge to a relatively high level. The desired short circuit gate current is shown in Figure 1-27.

Since these gate signals had to be electrically isolated, the master driving circuit contained a gating transformer. To design such a transformer capable of the leading edge rise time shown in Figure 1-27, and yet with sufficient volt-second capacity to support the gate signal for 10 msec , is extremely difficult. The circuit shown in Figure $1-28$ was incorporated in order to accomplish the desired gate signal.

The cost involved in producing the leading edge of the pulse was moderate. Even with this added cost and complexity, the allowable di/dt in the circuit was less than 150 amperes per microsecond. The power SCR with IR's ACE geometry makes this circuit complexity unnecessary. This type of thyristor is capable of withstanding nonrepetitive inrush currents of 800 amperes per microsecond with a gate current requirement of 100 mA and a gate current rise time of $2 \mu \mathrm{sec}$. If one uses the suggested figure of merit for turn-on capability of an SCR (as given in Formula $1-\mathrm{M}$ ) and compares conventional SCRs to the ACE type of device, the ACE device is found to be more than 1000 times superior to conventional types of power thyristors.


Figure 1-27. Waveform of Gate Current


Figure 1-28. Addition to Triggering Circuit
F.M. $=\frac{\mathrm{d}_{1} / \mathrm{at} \cdot \mathrm{t}_{\mathrm{r}}}{\mathrm{I}_{\mathrm{GM}}}$

Where:
$\mathrm{di} / \mathrm{dt}=$ Maximum allowable rate-of-rise of inrush current.
$\mathrm{t}_{\mathrm{r}}=$ Required gate signal rise time.
$\mathrm{I}_{\mathrm{GM}}=$ Required gate current for high di/dt capability.

In the past, the ability of a thyristor to turn on rapidly has been limited not only by the gate drive requirements, but also by the necessary trade-offs used to achieve the other desirable characteristics in the device. Making a high voltage device demanded the use of high resistivity silicon, which decreased the spreading velocity of the turnon action. The requirement for high $\mathrm{dv} / \mathrm{dt}$ dictated the use of emitter shorting, which diminished the effectiveness of the gate to turn the device on efficiently. Now with the geometry available in the ACE family of thyristors, these trade-offs are no longer a consideration. It is possible to incorporate all of these desirable features in a single thyristor with high manufacturing yields and ultimately low cost to the user. Considering the cost savings realizable by reduction in driving circuit complexity and di/dt suppression components in the power circuit, and the availability of full-parameter production devices, the economic practicality of many circuits is accomplished, where it was strictly conjecture before.

The di/dt rating is also affected by the magnitude of the off-state voltage prior to switching the device on. More power will be dissipated in the silicon wafer when the device is switched on from a higher
voltage. in aquilion, uevices maue for the higher voltage ratings will be made with thicker silicon of higher resistivity, which means more losses.

Throughout the time an SCR is turning fully on, internal losses will be greater than stipulated by the published power loss curves for the device (which are based on fully turned-on operation), due to the higher current density in the portion of the silicon wafer which is turned on at any instant. In addition to being the cause of failure during initial turn-on (di/dt failure), extra losses during the entire turnon period contribute to average junction heating and require that the device be operated at a lower current level than would otherwise be expected.

This effect becomes more pronounced as operating frequency is increased, because the device is turned on more frequently in a given period of time. It is also more pronounced as the current rating of the SCR is increased, if this is done by increasing the size of the silicon wafer, since the time required for current flow to equalize throughout the wafer becomes greater.

The action of a conventional thyristor during turn-on may be seen in Figure 1-29. Here, the thyristor is conducting an essentially rectangular current wave. The curve of instantaneous power loss shows the internal power being dissipated, which is, at any instant, the product of the current through the device and the voltage across it.

Turn-on losses in a conventional thyristor can be reduced by using a "soaking reactor," which delays the appearance of the main power pulse for a short time, such as 10 microseconds, following the gate trigger


Figure 1-29. Values During Turn-On
pulse. During this time, the reactor, and possibly a resistor in parallel with it, permits enough anode current to flow to cause propagation of the turn-on action within the thyristor. When the reactor saturates, permitting full load current to flow, the power loss is reduced because of the larger area of the silicon wafer that is at that instant turned on. Figure 1-30 shows how turn-on losses in one thyristor were reduced as soaking time was increased.

Very often, snubber circuits, consisting of a resistor and a capacitor in series, are used across the thyristor to absorb transient voltages. Because of the low inductance in a typical snubber circuit, severe di/dt can be imposed at the very instant of turn-on. This can cause additional switching losses and even a thyristor failure. The effect of changing the value of R in a snubber across one particular thyristor is shown in Figure 1-31. A value of R
must be used that is high enough to prevent excessive di/dt in the thyristor, but at the same time, will not nullify the effect of the capacitor, rendering the snubber network useless.

Turn-on of large area devices can be speeded up by simultaneously triggering the device at more than one point. The calculated effect of adding a second gate to a device rated 110 amperes RMS is shown in Figure 1-32. Complete turn-on is seen to occur in 75 microseconds instead of in 105 . In addition, since current flow is initiated at two points instead of one, the di/dt capability of the device is improved by a factor of two. Substitution of this device for one having a single gate, but otherwise the same, in an inverter operating at several thousand hertz, will permit a significant increase in output power at the same case temperature.

This discussion of turn-on losses has been concerned with thyristors


HORIZONTAL $=5 \mu \mathrm{sec} / \mathrm{div}$
VERTICAL $=6400 \mathrm{w} / \mathrm{div}$
Figure 1-30. Power Loss During Turn-On


Figure 1-31. Turn-On Power Loss Snubber Resistance


TIME FROM INITIATION OF TURN-ON ( $\mu \mathrm{sec}$ )
Figure 1-32. Turned-on Area
having one or two conventional gates located at the periphery of the junction assembly. A single gate located at the center of the junction assembly is sometimes used. This configuration would appear to offer superior initial turn-on performance and a shorter propagation time to full conduction. In actual practice, devices made this way behave about the same as those having one gate located at the edge of the wafer because of slight non-uniformities in the junctions favoring current propagation in some directions from the center over others.

The ACE class of thyristors employs a mechanism whereby the anode current is caused to flow in a special geometry during turn-on, which results in an enhancement of the turn-on action initiated by a conventional gate. Several junction structures have been developed which have this regenerative effect, whereby the load current, when it
begins to flow, causes a much larger region to be turned on than could be turned on by one or even two conventional gates.

This action can be understood by referring to Figure 1-33, which shows the geometry used in one such thyristor. A single gate of the conventional type is seen to initiate current through an auxiliary cathode. To accomplish this, since the auxiliary cathode is not connected to the external circuit, current must flow across the narrow gap between the auxiliary and main cathode regions. This causes turn-on of the main cathode along the length of the narrow gap, resulting in the following improvement in performance:
A. Initial turn-on of a much larger portion of the junction than even a multiple gate is able to turn on, even with high gate drive.
B. Reduction in time required for the total junction of a large area thyristor to enter into conduction of the principal current.
C. Reduction in gate drive needed, because the above action takes place, even though a gate trigger pulse of moderate current amplitude and relatively long rise time is used.
Thyristors are available which make use of the main cathode current to initiate gating action along straight or circular segments of the main cathode region, or at a large (10 or more) number of points around the main cathode periphery. They are all capable of providing very high non-repetitive di/dt ratings, many being rated 800A per microsecond.

As all such devices rely on the regenerative effect caused by a rap-


Figure 1-33. Auxiliary Cathode Structure
idly rising load current flowing through special geometries, their performance is not improved by the addition of a soaking reactor. They are able to handle higher snubber currents and to control more usable amounts of power than conventional single gate or multiple gate thyristors when switching from high blocking voltages and at high repetition rates.

There is a small penalty to pay for the improved turn-on action of these devices with special cathode geometries. The active main cathode area is not as large as it is in a conventional thyristor having the same size junction assembly. Except in the case of devices having very complex cathode geometries, designed for operation well above 10 kHz , this reduction in active area is small. It does result in a slight reduction in the low frequency current rating. This is more than offset by the considerable increase in current rating at frequencies of 1 kHz and above, that these special thyristors exhibit as compared with conventional gate units.

## dv/dt

Silicon controlled rectifiers exhibit a tendency to switch from the off-state to the on-state when the anode-to-cathode voltage is abruptly increased. This tendency is a function of the rate-of-rise of the voltage. The rate which switches the controlled rectifier into conduction is known as the critical rate-of-rise, or more simply, "dv/dt."

The mechanism for this phenomena can be explained in terms of the internal capacitance which the controlled rectifier exhibits. When the voltage across the controlled rectifier is increased, charges flow through the controlled rectifier in a manner analogous to the charging current of a capacitor. The greater the rate-of-rise of the applied voltage, the greater will be this flow of charges. As the rate-of-rise is increased, sufficient charges will eventually flow to act in the same manner as the charges which are injected when the gate is energized with a positive potential with respect to the cathode, and the controlled rectifier will turn on. Figure $1-34$ shows the rate-effect-caused current due to a sharply rising voltage on a 740A RMS SCR.

The magnitude of rate-effectcaused current should not be confused with latching and holding currents, more familiar on SCR data sheets. At first glance, one might wonder how a device would remain in the blocking state with 2.1 A flowing anode-to-cathode, since latching currents are typically less than a single ampere. The important difference lies in the relative current densities involved. Rate effect currents are rather uniformly distributed over the entire semiconductor wafer, as is the blocking


Figure 1-34. Rate Effect Current
junction capacitance, while latching and holding currents are subject to low level injection phenomena, where only limited crystal domains are involved in conduction. Since internal device gain is a function of active region current densities, internal gain during dv/dt excursions will be held below unity even though total currents are in excess of conventional latching currents.

A quantitative specification of a controlled rectifier's ability to resist rate effect turn-on is the $\mathrm{dv} / \mathrm{dt}$ rating. A convenient definition employs an exponentially rising offstate voltage waveform. Definitions of terms are presented in Appendix I. The $d v / d t$ is defined as shown in Formula 1-N.
$\mathrm{dv} / \mathrm{dt}=\frac{(0.632) \mathrm{V}_{\mathrm{DM}}}{\tau}$

Where:
$\tau=$ time constant of the exponential (equals RC)
$\mathrm{V}_{\mathrm{DM}}=$ peak anode voltage.
In the testing of controlled rectifiers, the critical rate-of-rise of principal voltage is encountered under two different conditions. It is important to keep these two considerations distinctly separated to avoid ambiguity when discussing or specifying controlled rectifier characteristics.

The first test condition is with the controlled rectifier deenergized, and the off-state voltage is abruptly applied to it. This is the test condition for what is known as the critical rate-of-rise of applied off-state voltage (dv/dt).

There was, at one time, considerable discussion in the industry as to whether this voltage should be applied in a straight line or in an
exponential manner, and if it is applied in an exponential manner, whether the rate-of-rise should be defined as the initial rate-of-rise or some other, lower value. This lower value would take into account the fact that the voltage curve is exponential, and, therefore, the initial rate-of-rise does not exist throughout the entire time that the voltage is rising to its ultimate value.

The major controlled rectifier manufacturers have accepted as standard conditions that the applied off-state voltage should rise exponentially to a value equal to the minimum breakover voltage rating $\left(V_{(B O)}\right)$ or repetitive peak offstate voltage rating (VDM) of the device under test, and that the rate-of-rise shall be defined as the average rate-of-rise during the first time constant of the exponential voltage curve ( $\tau$ ). This situation is obtained by charging a capacitor, C, through a resistor, $R$, and is depicted in Figure 1-35. It can be seen that the voltage at the end of the first time constant is $63.2 \%$ of the total voltage applied to the device. The rate-of-rise of applied forward voltage, $\mathrm{dv} / \mathrm{dt}$, is defined in Formula 1-N.


Figure 1-35. Critical dv/dt Test Waveforms

The second test condition where the rate-of-rise of off-state voltage is encountered is in the test for turn-off time of a controlled rectifier. The turn-off time of a controlled rectifier depends in part upon the rate at which the off-state voltage is reapplied after the principal current has been interrupted and a time has elapsed during which the controlled rectifier regains its blocking ability. If the principal voltage is reapplied in a gradual manner, it may be reapplied sooner than if it is applied in a steeply rising manner. Of course, there is a limit to how rapidly the voltage can be reapplied, because the controlled rectifier cannot withstand a rate-of-rise greater than that which it can handle when the voltage is applied with the rectifier initially deenergized. Thus, the rate-of-rise of reapplied off-state voltage, which is a condition of the turn-off time test, is generally considerably less than the critical rate-of-rise of applied off-state voltage for the device under test.

In the test procedure which has been adopted by the industry for measuring the turn-off time of controlled rectifiers, the reapplied offstate voltage is forced to rise in a linear fashion until rated repetitive peak off-state voltage or some stated portion of it is reached. In this case, the rate-of-rise is defined as the slope of the voltage, since it is a straight line.

To summarize, for controlled rectifiers, two critical rates of application of principal voltage exist. One is the critical rate-of-rise of applied off-state voltage with the device initially de-energized. The other is the rate-of-rise of reapplied off-state voltage which defines the
end of the turn-off period and hence is a parameter in the measurement of turn-off time.

When a capacitor is charged from an infinite dc source through a resistor, the voltage across the capacitor will reach $63.2 \%$ of the source voltage in one time constant (the product of the capacitance being charged and the series resistance). This is derived from the Formula 1-P.
$\mathrm{V}=\mathrm{V}_{\mathrm{o}}\left(1-\mathrm{e} \frac{-\mathrm{t}}{\mathrm{RC}}\right)$
Where:
$\mathrm{V}_{\mathrm{O}}=$ voltage to which the capacitor ultimately charges (the source voltage).

At the end of the first time constant $\mathrm{t}=\mathrm{RC}$ and therefore, $-t / R C=-1$. The equation becomes Formula 1-Pa.

$$
\begin{gather*}
\mathrm{V}=\mathrm{V}_{\mathrm{O}}\left(1-\mathrm{e}^{-1}\right)=  \tag{1-Pa}\\
\mathrm{V}_{\mathrm{O}}(1-1 / \mathrm{e})
\end{gather*}
$$

Since $e=2.718,1 / e=0.368$ and 1 . $1 / \mathrm{e}=0.632$.

Thus, the average rate-of-rise at the end of the first time constant $=$ $0.632 \mathrm{~V}_{\mathrm{o}} / \mathrm{RC}$.

The rate-of-rise, at the first instant the voltage is applied to the circuit, can be found by differentiating the basic equation given above at $\mathrm{t}=0$. This calculation reveals that the initial rate-of-rise is $\mathrm{V}_{\mathrm{o}}$ / RC , which is $1 / 0.632$ or 1.58 times the average rate-of-rise at the end of the first time constant.

In many practical circuits using SCRs, they are subjected to a steady potential upon which the rising voltage pulse is superimposed. Such an initial bias will enhance the critical $\mathrm{dv} / \mathrm{dt}$ capability of the device, as compared with its perform-
ance when subjected to a voltage pulse having the same $d v / d t$, but rising from zero.

The ability of a given part to withstand an exponential $\mathrm{dv} / \mathrm{dt}$ pulse is enhanced by reducing the junction temperature and also by reducing the voltage applied at the end of the exponential ramp. The general effect of varying these two parameters on critical applied dv/dt is shown in Figure 1-36, based on the observed behavior of a 470 ampere RMS, 1300 volt, epitaxial SCR. This part exhibited a fairly low dv/dt at maximum rated voltage and junction temperature, so that the higher $\mathrm{dv} / \mathrm{dt}$ ratings observed at reduced voltage and current levels were not so high that they could not be measured.

It is also possible to improve the ability of an SCR not to trigger when the anode voltage is suddenly increased by providing a conducting path between the cathode (or emitter) layer of the device and the layer immediately below it. (These layers can be identified in the exaggerated thyristor cross section shown in Figures 1-2 and 1-24.) This conducting path can readily be provided around the outside of the cathode region. In high current devices which have large cathode areas, a pattern of small intrusions of the underlying layer into the cathode layer is very effective. These various "shorted emitter" constructions provide shunt paths for the charging current which flows through the thyristor because of junction capacitance. If not shunted around the emitter junction this way, this displacement current will very likely trigger the SCR on when the anode voltage suddenly increases in the positive direction.


Figure 1-36. Critical Rate-of-Rise of Applied Off-State Voltage Vs. Applied Off-State Voltage

A negative dc potential on the gate will tend to reduce the chances of the SCR triggering as the result of an abrupt change in anode voltage. Controlled rectifiers built without a shorted emitter show a much greater improvement in critical applied dv/dt with negative gate bias than newer units which have this construction; refer to Figure 1-37. The emitter shorting found in most inverter type SCRs today enhances dv/dt capability, as well as making it less influenced by the voltage applied to the device. Nevertheless, a negative gate bias may still be beneficial in that it will reduce the likelihood of false SCR triggering from stray signals inadvertently induced into the gate circuit.

The capability of an SCR to withstand $\mathrm{dv} / \mathrm{dt}$ can be increased if rate effect current is shunted around the gate cathode junction, thereby preventing an increase in
the internal loop gain. There are two well-known methods for shunting such current: external gate cathode resistance and negative gate bias. Either method can produce quite dramatic results, especially on small junction area devices. Figure $1-38$ is a plot of dv/dt capability as a function of gate condition for a 25A RMS alloy-diffused device. Unfortunately, as the current rating of the semiconductor wafer is increased, lateral base resistance also increases, and the efficiency of a point gate in shunting rate effect current diminishes. As a compromise, most high current devices internally edge- or spot-short the gate-cathode junction. This yields many of the same advantages (and disadvantages) as external gate cathode resistance, but isolates the base region from the effective use of negative bias. Consequently, the critical dv/dt of devices rated 100A


Figure 1-37. Critical Applied dv/dt Vs. Gate Bias


Figure 1-38. Improvement of dv/dt of 25A RMS SCR with Application of Gate Bias Resistance and Current

RMS and above is largely unaffected by gate condition.

## Turn-Off Time

The major factor which determines the turn-off time of an SCR is the rate at which the current carriers recombine in the central P-N junction, which blocks when the thyristor anode voltage is positive. Passing a reverse recovery current through the SCR at the end of the forward conduction will sweep out current carriers from the outer two junctions in the thyristor, but not from the central junction. In the central junction, the carriers disappear at a rate which depends upon the characteristics of the silicon. If this silicon contains dopants or dislocation centers which can serve as "traps" for the carriers, recombination will proceed more rapidly and turn-off time will be shorter. There are several ways to provide such traps; one of the most commonly used methods is to introduce a small number of gold atoms into the silicon. The drawback to this procedure is that it tends to increase the on-state voltage of the thyristor, and this has an adverse effect upon the current rating of the part.

Another aspect is the effect of designing the thyristor for a higher voltage rating. When this is done, a thicker silicon wafer must be used to support the higher voltage. This slows the rate at which recombination takes place, since it must occur in a larger volume of silicon. Thus, it is much easier to build very fast low voltage thyristors in the range of 600 volts and below, than it is to build units having the same turn-off time but able to block 1000 or 1200 volts. It is generally found
that very fast turn-off times are available only in low voltage units. Turn-off time is influenced by a number of parameters, including: A. Junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ).
B. Magnitude of on-state current (ITM).
C. Rate of change of principal current (-di/dt).
D. Magnitude of reverse voltage following reverse recovery $\left(\mathrm{V}_{\mathrm{R}}\right)$.
E. Rate-of-rise of reapplied offstate voltage ( $\mathrm{dv} / \mathrm{dt}$ ).
These operating conditions are depicted in Figure 1-39, which also shows that turn-off time $\left(\mathrm{t}_{\mathrm{q}}\right)$ is divided into two parts: reverse recovery time ( $\mathrm{t}_{\mathrm{rr}}$ ), which is much the same as reverse recovery time of a rectifier diode, and gate recovery time ( $\mathrm{tgr}_{\mathrm{g}}$ ).

Varying junction temperature above and below the maximum rated value has a pronounced effect on turn-off time. Figure $1-40$ shows the effect on devices rated for a maximum operating temperature of $150^{\circ} \mathrm{C}$. The data has been normalized to the turn-off time observed at $125^{\circ} \mathrm{C}$ junction temperature. This graph can be applied to units having a maximum junction operating temperature of $125^{\circ} \mathrm{C}$, provided it is recognized that such units may not block rated voltage above $125^{\circ} \mathrm{C}$.

Figure 1-41 shows the effect of varying on-state current. It can be seen that increasing on-state current above the value usually used to perform the turn-off time test has only a minor effect on turn-off time. This curve is for the condition of constant junction temperature. At high current levels, the accompanying heating of the junction will cause an apparent increase in turnoff time.


Figure 1-39. SCR Turn-Off Time Waveforms

The rate-of-change of principal current at the end of the on-state current pulse affects turn-off time, because of its effect on reverse recovery time. The higher the rate of change, the shorter the reverse recovery time. Turn-off time is shortened to the same extent that reverse recovery time is reduced.

The magnitude of reverse voltage applied to the SCR during the turnoff interval will influence turn-off time. A reverse voltage is required to produce reverse recovery current. Varying the reverse voltage will vary the rate of change of this current, which affects turn-off time as noted above. In addition, increasing the reverse voltage during the period following recovery will cause turn-off time to be reduced. This effect is most noticeable for reverse voltages up to 25 to 30 volts. Greater reverse voltage causes no appreciable further reduction in turn-off time.

In some inverter circuits, a diode is connected in anti-parallel with the SCR. This has the effect of clamping the reverse voltage to the forward voltage of the diode. Turnoff time under this condition may be considerably longer than under standard test conditions, where considerably more reverse voltage is applied. The amount that turn-off time changes as a result of the diode clamp is not a fixed percentage of standard turn-off time. To assure obtaining devices with the desired maximum turn-off time under this condition, they should be individually tested with an appropriate rectifier diode connected in anti-parallel, which can be done quite readily. During this test, the leads to the diode should be kept very short, to prevent lead inductance from delaying the clamping effect of the diode and nullifying its effect on the turn-off time.


Figure 1-40. Temperature Turn-Off Time Vs. Junction


Figure 1-41. Turn-Off Time Vs. On-State Current

Increasing the rate-of-rise of reapplied off-state voltage also has an adverse effect on turn-off time. This is shown in Figure 1-42. Reapplied dv/dt must be less than the critical applied $\mathrm{dv} / \mathrm{dt}$ capability of the SCR, or else the SCR will be triggered by $\mathrm{dv} / \mathrm{dt}$ alone and will appear never to turn off.

## SWITCHING LOSSES

Throughout the time an SCR is turning fully on, internal losses will be greater than stipulated in the published power loss curves for the device, which are based on fully turned on operation. In addition to being the cause of failure during initial turn-on (di/dt failure), losses during the turn-on period contribute to average junction heating and require that the device be operated at a lower current level than would otherwise be expected.

This effect becomes more pronounced as operating frequency is increased, because the device is turned on more frequently in a
given period of time. It is also more pronounced as the current rating of the SCR is increased, if this is done by increasing the size of the silicon wafer, since the time required for current flow to equalize throughout the wafer will increase. Reduction of turned-on area due to propagation rate limitations increases current densities and, therefore, power losses. Figure 1-29 shows waveforms during turn-on of a controlled rectifier switching from 400 volts. The maximum anode current is 300 amperes, with the leading edge rising at a rate of $85 \mathrm{~A} / \mu \mathrm{sec}$. Superimposed on this figure is the instantaneous power loss. The energy dissipation is approximately $180 \mathrm{~kW}-\mu \mathrm{sec}$ per pulse. Compare this to $76 \mathrm{~kW}-\mu \mathrm{sec}$ per pulse if the device were initially fully turned on. At high frequencies and short on-state current pulses, the power dissipation of a device can be 3 to 10 times the 60 to 400 Hz catalog values. Therefore, the turn-on losses of devices intended for high fre-


Figure 1-42. Turn-Off Time Vs. Reapplied dv/dt
quency applications are of paramount importance when trying to design a practical system.

There are several methods by which switching losses may be measured:
A. Comparison of case temperatures under dc and switching test conditions.
B. Energy conservation.
C. Visual readout of current and voltage followed by mechanical integration of V and I vs. time plot.
D. Electronic analog multiplier.

## DC Method

Turn-on losses may be evaluated thermally using a direct current comparison method. The method depends upon the linear relation between device case temperature, average power loss, and properly chosen system thermal impedance. Mounting a device on a heat exchanger ( $\operatorname{sink}$ ) of known thermal resistance at a known cooling rate allows the calculation of device power dissipation by Formula 1-Q.
$P_{(A V)}=\frac{T_{S}-T_{A}}{R_{\theta S}}$
This method can be used for evaluation of power loss under dc, 60 Hz , and inverter operation. The usefulness of this method lies mainly in the evaluation of power loss under inverter type operation. DC and 60 Hz evaluation, making use of computer aids, is more economical and much faster.

To use this system, a device is mounted on a calibrated heat exchanger and operated in an inverter system. Enough time is allowed for the system to reach thermal equilibrium. The average power dissipation is then calculated using Formula
$1-\mathrm{Q}$. In using this equation, it must be kept in mind that the average power loss includes turn-on, blocking, recovery, and gate losses. However, for devices rated 70 amperes and larger, blocking and gate losses are a minor portion of total losses. The average total switching loss (including recovery loss) then becomes Formula 1-R.

$$
\begin{gather*}
\mathrm{P}_{(\mathrm{AV})}(\text { total switching })= \\
\mathrm{P}_{\text {Turn-on }}+\mathrm{P}_{\text {Recovery }}  \tag{1-R}\\
\left(\mathrm{P}_{\text {Gate }}+\mathrm{P}_{\text {Blocking }}\right)
\end{gather*}
$$

Then, using (1-Q) and (1-R), and considering gate and blocking losses as being very small, Formula 1-T is the result.

$$
\begin{aligned}
& \mathrm{P}_{(\mathrm{AV})}(\text { total switching })= \\
& \mathrm{P}_{\text {Turn-on }}+\mathrm{P}_{\text {Recovery }}=(1-\mathrm{T}) \\
& \frac{\mathrm{TS}_{\mathrm{S}}-\mathrm{T}_{\mathrm{A}}}{\mathrm{R}_{\theta \mathrm{S}}}
\end{aligned}
$$

This method of determining total switching losses requires an inverter to simulate operating conditions and a de current source of sufficient power to cause a 35 to $50^{\circ} \mathrm{C}$ temperature differential between the heatsink and coolant ambient temperature. Lower temperature differentials can result in significant errors, due to temperature measurement ambiguities.

## Energy Conservation

A second approach to the measurement of switching losses is a capacitive energy conservation technique. The circuit shown in Figure $1-43$ can be used to evaluate SCR switching losses when the on-state current is sinusoidal. Using this circuit, switching losses can be evaluated at low repetition rates. The circuit operates in the following


Figure 1-43. Energy Conservation Test Circuit
manner: capacitor $\mathrm{C}_{1}$ is charged through rectifier $\mathrm{RD}_{1}$ to test Voltage $\mathrm{V}_{\mathrm{T}}$; the test SCR is then gated while the ac source is negative, isolating the charging supply from the test circuit. A sine wave of on-state current passes through the test device. Ringback of current is prevented by the rectifying action of the SCR. If the circuit has a high $Q$, the circuit losses are mainly SCR switching losses. Figure 1-44 illustrates actual circuit waveforms. The capacitor stored energy is shown in Formula 1-U.
Stored energy (watt-seconds) =

$$
\begin{equation*}
1 / 2 \mathrm{C}\left(\mathrm{~V}_{1}\right)^{2} \tag{1-U}
\end{equation*}
$$

Assuming a lossless circuit, the peak voltage after the first current pulse (if the current cannot reverse) would be equal to the initial capacitor voltage, but of opposite sign. In a circuit with an SCR and components that do have losses, the reverse voltage across the capacitor will be less than the initial capacitor voltage (see Figure 1-44.)

The stored energy after one-half period of conduction is shown in Formula 1-Ua.
Stored energy (Watt-Seconds) $=$
$1 / 2 C\left(V_{2}\right)^{2}$
Combining Equations $1-\mathrm{U}$ and 1-Ua results in Formula 1-Ub.

Total circuit losses (Watt-Seconds)

$$
\begin{aligned}
& =1 / 2 \mathrm{C}\left(\mathrm{~V}_{1}\right)^{2}-1 / 2 \mathrm{C}\left(\mathrm{~V}_{2}\right)^{2} \quad(1-\mathrm{Ub}) \\
& =1 / 2 \mathrm{C}\left(\mathrm{~V}_{1} 2 \cdot \mathrm{~V}_{2} 2\right)
\end{aligned}
$$

Unfortunately, the losses calculated in this manner include the losses in $\mathrm{L}_{1}$ and $\mathrm{C}_{1}$. Evaluation of circuit losses can be performed by operating the circuit at some higher frequency than 60 Hz and thermally measuring the SCR losses and comparing these losses with those calculated using $1-$ Ub. The difference between the two will be circuit component losses. There are other methods existing which allow the calculation of circuit losses [7]. Once the circuit losses have been determined, use Formula $1-\mathrm{V}$ to find the SCR switching losses.
SCR Switching Losses (watt-
seconds $)=1 / 2 \mathrm{C}\left(\mathrm{V}_{1} 2-\mathrm{V}_{2}{ }^{2}\right)-(1-\mathrm{V})$
circuit losses.
This technique of determining SCR switching losses is extremely useful in applications where onstate current waveforms are sinusoidal. It is not easily adapted to trapezoidal or other non-sinusoidal current waveforms.

## Mechanical Integration

Evaluation of switching losses by mechanical integration is self-

(b) SCR ON-STATE CURRENT AND CAPACITOR VOLTAGE

Figure 1-44. Waveforms for Energy Conservation Circuit
explanatory. Oscillograms of the on-state voltage and current vs. time are used to obtain the instantaneous power loss by multiplication. The instantaneous power loss plotted vs. time can then be integrated using a computer or mechanical means. This method, while time consuming and accurate to only $\pm 5 \%$ due to oscilloscope line
widths, is applicable to all current waveforms.

## Electronic Analog Multiplier

The evaluation of SCR switching losses, using the previously discussed methods, is not always practical when considering the complexity of most current waveforms and the complications of testing. A
study was initiated at IR to determine the feasibility of using electronic analog multipliers to calculate controlled rectifier switching losses.

The concept was enticingly simple: real-time waveforms in, multiplied power losses out. The SCR voltage and current waveforms would be appropriately scaled, of course, to conform to the input requirements of a given multiplier. With such scaling, input slopes could approach $-100 \mathrm{~V} / \mu \mathrm{sec}$ due to voltage fall times and $5 \mathrm{~V} / \mu \mathrm{sec}$ due to current rise times. To be meticulously accurate, a multiplier processing such signals should respond at a $105 \mathrm{~V} / \mu \mathrm{sec}$ slewing rate. This is a difficult constraint on the analog multiplier. However, for a moderately accurate ( $\pm 10 \%$ ) system, this requirement may be relaxed. Ultra high frequency components of the actual power loss are small when compared to total switching losses. For instance, Figure 1-45(a) shows the on-state voltage and current waveforms for a current pulse rising at $50 \mathrm{~A} / \mu \mathrm{sec}$. The rate of fall of voltage is 5000 V per $1 / 2 \mu \mathrm{sec}$. At the end of the first $1 / 2 \mu \mathrm{sec}$, current has risen to only $1 \%$ of its peak value. The loss contribution in this first moment is negligible, as the power loss curves in the figure demonstrate. An actual output slew rate of 5 to $10 \mathrm{~V} / \mu \mathrm{sec}$ would yield reasonable results.

Figure 1-45(a) is also a comparison of power loss via manual and electronic multiplication. The analog multiplier used was fairly inexpensive (less than $\$ 100$ ) and had a maximum guaranteed slew rate of $10 \mathrm{~V} / \mu \mathrm{sec}$. While there is a difference between waveforms from $t=0$ to $\mathrm{t}=0.75$, the multiplier does
recover fast enough to faithfully display the instantaneous power loss over the remaining length of the pulse. Figure $1-45(\mathrm{~b})$ is the oscillogram of the instantaneous power loss using the electronic multiplier. (The oscillatory reverse recovery losses at the tail of the pulse are real and faithfully represented.) The multiplier indicated a power loss $8 \%$ lower than the manual calculation. Experimental error and bias probably accounts for a significant portion of this $8 \%$ figure.

A set of test results for sinusoidal and trapezoidal current waveforms are summarized in Table I-IV.

It should be noted that the trapezoidal waveshapes represent a severe test of multiplier response, demanding an account of losses due to very steep current wavefronts. This observation seems to be reflected in the percentage difference column of Table I-IV. Electronic multiplier losses lag manual losses by 6 to $9 \%$. Figure $1-46$ presents a corroborating opinion by visual comparison of trapezoidal losses. In the first microsecond, the electronic multiplier lags the "actual" power loss by $25 \%$. Recovery is complete by the third microsecond.

## Test Methods

The several techniques presented above are all reasonably accurate from an experimental viewpoint. Vast differences exist, however, in versatility, maintainability, and simplicity. Table I-V offers a comparative summary of methods.

It is reasonable to class the various techniques by defining suitable applications. For instance, incoming inspection testing and general production testing might well be handled by energy conservation

(a) ON-STATE CURRENT AND VOLTAGE


HORIZONTAL $=2 \mu \mathrm{sec} / \mathrm{div}$
VERTICAL $=1700 \mathrm{~W} /$ div
(b) POWER LOSS

Figure 1-45. Measurement of Turn-On Losses

(a) GRAPHIC COMPARISON

HORIZONTAL $=10 \mu \mathrm{sec} / \mathrm{div}$
VERTICAL $=3200 \mathrm{~W} / \mathrm{div}$
(b) OSCILLOGRAM COMPARISON

Figure 1-46. Comparison of Trapezoidal Losses

Table I-IV. Summary of Switch Loss Test Results

| DEVICE NO. | PULSE <br> WIDTH <br> ( $\mu \mathrm{SEC}$ ) | PEAK <br> CURRENT <br> (AMPERES) | POWER LOSS PER PULSE |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | di/dt A/ $\mu$ SEC | MANUAL (kW) | MULTIPLIER (kW) | PERCENT DIFFERENCE* |
| Sinusoidal |  |  |  |  |  |  |
| 1 | 4.6 | 175 | 90 | 8.25 | 8.43 | +2.2 |
| 2 | 11.5 | 200 | 50 | 3.52 | 3.80 | +8.0 |
| 3 | 18.5 | 175 | 25 | 2.18 | 2.02 | -7.8 |
| Trapezoidal |  |  |  |  |  |  |
| 4 | 50 | 200 | 150 | 69.0 | 63.0 | -8.7 |
| 5 | 50 | 200 | 100 | 126.4 | 118.0 | -6.3 |
| 6 | 50 | 200 | 75 | 112.3 | 102.25 | -9.1 |

*Assumes manual calculation is correct.
Table I-V. Summary of Switching Loss Test Methods

| METHOD | - on-STATE CURRENT WAVEFORM | $\begin{aligned} & \hline \text { TIME } \\ & \text { TEST } \\ & \text { POINT } \\ & \hline \end{aligned}$ | ACCURACY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: |
| DC | Any | $1 / 2$ Hour | Medium High | Requires close control of ambient conditions |
| Energy Conservation | Most suitable for sine wave | 2 Minutes | High | Accuracy depends upon determination of Q of circuit |
| Manual Integration | Any | 1/2 Hour | High | Accuracy of readings determines accuracy of power loss calculations |
| Analog Multiplier | Any | ½ Minutes | Medium High | Fast readout on a go-no-go basis when using templet on oscilloscope. Direct readout of instantaneous peak power. |

power loss techniques. All parts could be given a specification based on a standard sine current pulse generated by simple apparatus. However, for infrequent laboratory testing, where waveshapes may vary considerably from a sinewave, the thermal calculation or manual integration methods are most suitable. Tedious experimentation and calculation are offset by a low initial investment.

The final technique, analog multiplication, is the most versatile, accepting any waveform and displaying power losses as a function of time. An initial investment of parts and time, coupled with a continuous investment in calibration time, represents the cost of analog multiplication. The electronic multiplier then becomes valuable to engineering groups with significant interest in power semiconductor design and application.

## PARAMETER TRADE-OFFS

As semiconductor manufacturing processes have been developed and refined, manufacturers are able to produce devices with desirable sets of characteristics by simply trading off one characteristic against the other. For instance, the turn-off time of a thyristor can be shortened in the case of an alloydiffused device by using a gold doping technique. At the same time, however, as turn-off time is reduced, the forward voltage of the device increases. This limits the steady-state operating current under an allowable ambient condition and reduces the surge capability of the device.

In other words, one can take, for instance, a silicon chip of large enough diameter which, with rela-
tively long enough turn-off time, could handle, say, 470 amperes in a pressure-assembled case and by doping the silicon heavily enough in the proper manner, cause the turnoff time to be reduced to tens of microseconds, at the same time increasing the forward voltage to lower the useful current handling capability of the device to 250 or 300 amperes.

By applying a shorting technique between the emitter and the underlying P-layer of a four-layer device, thus producing one or more low impedance paths around this P-N junction, the dv/dt capability of the SCR can be improved considerably. This technique, known as emitter shorting, however, also affects the triggering capability of the SCR. The inrush current capacity of the thyristor during the turn-on interval is also affected.

Blocking voltage capability of a thyristor in both the forward and reverse directions is affected by the resistivity of the basic silicon material used in producing the device and the thickness of the silicon used. This resistivity, however, also affects the propagation rate of the device as it is being turned on. This is another parameter of importance to consider in determining the inrush capabilities of a thyristor during the turn-on interval. A summary of parameter trade-offs for conventional SCR devices is shown in Table I-VI.

## SCR GEOMETRY

The original process used to manufacture silicon controlled rectifiers was the alloy-diffused process. In this process, after the original PNP sandwich is produced by diffusion methods, the final P-N

Table I-VI. SCR Parameter Trade-Offs

| $\begin{aligned} & \text { SCR } \\ & \text { PARAMETER } \\ & \hline \end{aligned}$ | VOLTAGE RATING | CURRENT | 'GT | $\begin{gathered} \text { CRITICAL } \\ \mathrm{dv} / \mathrm{dt} \end{gathered}$ | $\mathrm{ta}_{\square}$ | $\mathrm{V}_{\text {TO }}$ | $\begin{gathered} \mathrm{di} / \mathrm{dt} \\ \text { RATING } \\ \hline \end{gathered}$ | \$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Edge <br> Contouring | $\uparrow$ |  |  |  |  |  |  | $\uparrow$ |
| Emitter Shorting |  | $\downarrow$ | $\uparrow$ | $\uparrow$ |  |  |  | $\uparrow$ |
| Gold Doping (1) | $\downarrow$ | $\downarrow$ | $\uparrow$ | $\uparrow$ | $\downarrow$ | $\uparrow$ | $\downarrow$ | $\uparrow$ |
| Thinner | $\downarrow$ | $\uparrow$ |  |  | $\downarrow$ | $\downarrow$ | $\uparrow$ |  |
| Multiple Gates |  |  | $\uparrow$ |  |  | $\downarrow$ | $\uparrow$ | $\uparrow$ |
| Better Cooling |  | $\uparrow$ |  | $\uparrow$ | $\downarrow$ |  |  | $\uparrow$ |
| Reduced <br> Voltage <br> Operation |  |  |  | $\uparrow$ |  |  |  | $\uparrow$ |

(1) In addition to gold doping, other means of reducing minority carrier lifetime will have the same effect on the listed parameters except voltage rating may not be adversely affected by other methods.
junction is formed by using a gold antimony disc weighted down on the surface of the PNP sandwich and passing these parts through an alloying furnace, thus causing the gold antimony to alloy into the silicon, producing a final N region. It became obvious that if the dynamic characteristics of a 4-layer device were to be controlled carefully by the manufacturer, a new, more exact process of forming this last N region was necessary.

International Rectifier developed a new SCR series which incorporated an epitaxial emitter region. Instead of alloying a disc for the last N layer, a window was created in which the N layer was grown, thus producing the emitter in a much more exact geometry. With this new capability of control of large areas of the silicon, the tradeoff ability of the device designer and process engineer became much more predictable. Larger and larger devices of higher and higher current
capability became available with all of the necessary dynamic requirements for inverter application.

One of the most important limitations soon made itself even more evident in these large area devices. This limitation was the ability of the device to turn on non-destructively into high inrush (high di/dt) currents. When one of the SCRs in question did fail on di/dt, it was generally observed that a small burnt area appeared in proximity with the gate in the general vicinity of or at the edge of the shorting disc.

One of the approaches to a solution to this problem was to produce devices with a center-triggered gate construction, in order to propagate conduction throughout the device more rapidly at the beginning of the turn-on interval. Since the spreading rate of propagation in the silicon is a physical constant for given current and resistivity conditions, it is necessary to produce a
large initially turned-on area in order to cause a larger area to conduct in a given amount of time. However, the center-triggered gate will propagate more rapidly than an edge-triggered unit only if the gate is concentrically located with respect to the edge of the main cathode N region. This, of course, is physically impossible in production with a large number of units, so that any center-triggered configuration will yield a wide variation in turn-on capabilities over a number of production units, determined solely by the ability of the manufacturer to build perfectly concentric circles on the surface of the device.

Manufacturers then began to produce new geometries in order to help the turn-on capabilities and other dynamic properties of the device. The internal feed-back in SCRs of early edge-triggered and center-triggered constructions caused gate current starvation during the initial turn-on interval. This has been used in new geometries in order to produce an amplification or regeneration of a low level gating signal externally applied. What the manufacturer does with the geometry of the device in order to take advantage of this available energy determines 1) whether the device will propagate rapidly and, therefore, switch on efficiently, thus having high di/dt capability and low repetitive switching losses and 2) whether this geometry is or is not made independent of the main cathode N region resistivity and depth in order to make the device turn-on capabilities independent of turn-off time, $\mathrm{dv} / \mathrm{dt}$, voltage rating, etc. This geometry control arrangement, used in the ACE family
of devices, not only uses the internal amplification inherent in the thyristor, but also tends to cause a linear spreading action over the main cathode, thus minimizing any hot spots that can occur during the turn-on interval, at the same time leaving the delay time of the device unaffected.

The aluminum deposition or metallic contact also makes it possible for the device to operate at very high frequencies. Some early versions using wire connections, under high di/dt conditions, had such high internally amplified currents that at several kilohertz the wires tended to fuse, thus opening the gate connections in the device. Although the devices would still turn on in most cases, the amplified or regenerative turn-on action was no longer present. Thus, in order to produce a device which can be successfully manufactured in large quantities with reproducible inverter type characteristics, it is necessary to separate the N regions used for the main cathode and the amplified or regenerative gating completely so that the resistivity of one region can be made independent of the other; thus, short turnoff time, high $\mathrm{dv} / \mathrm{dt}$ and high voltage capability can be produced in the device independently of its turn-on characteristics.

Prior to techniques utilizing the shorted emitter to achieve high dv/dt ratings, it was observed that by using an inverse bias on the gate of a thyristor during its off period, it was possible to increase its $\mathrm{dv} / \mathrm{dt}$ rating considerably over the unbiased gate condition. The results, however, were rather spotty in that some devices appeared to improve much more than others. It was also
observed that in using a shorted emitter technique, this increased $\mathrm{dv} / \mathrm{dt}$ capability with negative gate bias was much less apparent.

## BIDIRECTIONAL TRIODE THYRISTOR-TRIACS

In the years that followed the advent of the first thyristor devices, it became obvious that as the inherent limitations in accuracy and response of the control elements were removed the industrial user became willing, in fact anxious, to include more sophistication in his equipment in order to reduce his maintenance requirements and increase productivity. At first, the engineer was able to satisfy these requirements with good assurance of reliability and a reasonable degree of complexity. As the demand for larger and more complex systems increased, however, it became apparent that a new limitation began to present itself. With more and more components required to make up a control system, both in the power control and in the logic and command circuitry, the maximum achievable reliability began to be a limiting factor in producing a system which would prove attractive economically to the user. The cost of packaging components began to approach and, in some extreme cases, exceed that of the components being packaged. The semiconductor designers' solution to the problem was, of course, the use of microcircuit techniques. Thick films, thin films, monolithics, hybrids and, most recently, large scale integration have extended the range of application for the most imaginative and resourceful circuit and system designers.

In the midst of this new tech-
nological revolution, the power semiconductor designers also began to respond. The design of the first triac marked a new departure for power device technology. By incorporating the functions of two SCRs into a single chip device both functions controlled by one gate - the way was opened for simplification in the power circuitry, as well as in the low power level control and logic circuits.

An exmination of the construction of International Rectifier's triac indicates that except for a modification of the gating in one portion of the device, the triac can be viewed as two anti-parallel connected silicon controlled rectifiers constructed in one wafer of silicon. This similarity is illustrated by Figure 1-47(a), a block diagram of two SCRs connected in anti-parallel, and Figure 1-47(b), a block diagram of a triac. If the gating on the right-hand SCR were changed and the control PNP regions connected as illustrated in Figure 1-47(c), the similarity would be complete.

## Gating

The gating characteristics of the triac are very different from those of two anti-parallel SCRs. For the anti-parallel SCRs, a positive gate signal is applied between Gate 1 and Main Terminal 1 when Main Terminal 1 is negative, and between Gate 2 and Main Terminal 2 when Main Terminal 2 is negative. This method of operation requires two separate gate circuits.

In the triac, Gate 1 and Gate 2 are connected together and operated from a single gate circuit connected between the gates and Main Terminal 1. The easiest triggering


Figure 1-47. Triac Block Diagrams
mode for ac control is achieved by biasing the gates positive when Main Terminal 1 is negative, and negative when Main Terminal 1 is positive. Triggering for ac control is also possible with negative bias on the gates during both half cycles. For dc control, a positive gate bias will result in operation similar to an SCR. This type of operation was made possible by a design in which a positive gate bias will not trigger the device when Main Terminal 1 is positive.

When Main Terminal 1 is negative, triggering takes place in the same manner as in an SCR. The
positive bias at Gate 1 with respect to the top N type cathode, causes injection of electrons from this cathode into the $P$ type region as shown in Figure 1-48(a). A large percentage of these injected electrons are collected by junction J2 which is reverse biased. This collector current in turn induces a forward bias across junction J3, which results in injection of holes into the central N type region. Some of these holes recombine with electrons, but a small percentage of them are collected by reverse biased junction J2. This hole injection occurs over a larger area of

(a) TRIAC TRIGGERING $-\mathrm{MT}_{1}$ NEG, G POS

(b) TRIAC TRIGGERING - MT 1 POS, G NEG

(d) TRIAC TURN-ON

Figure 1-48. Triac Internal Operations
junction J3 than the area of the initial electron injection from J 2 . The ratio of the areas is a function of the diffusion length of electrons in the upper $P$ region and the resistivity of the central $N$ region.

The collected holes induce an additional injection of electrons from J1 over an even larger area than the hole injection area. This counter injection continues until the entire area under the upper N type region or cathode is conducting and the reverse bias across J2 has collapsed. Although the counter injection has been described as a stepwise process, since collection is not an abrupt occurrence, the growth of the conduction area is a fairly smooth, continuous process.

Since Main Terminal 1 is also connected to the upper $P$ type region, some shunting of the gate signal will occur. This shunt current is, however, minimized by judicious placement of Gate 1. The same type of shunting occurs in an SCR with a shorted emitter construction.

As shown in Figure 1-48(b), when Main Terminal 1 is positive, a negative bias on Gate 2 will cause injection from the N type gate region. Many of these injected electrons will recombine with holes. This current can be considered to be as a parasitic diode current between Gate 2 and Main Terminal 1, since it has no useful function. Some of the injected electrons, however, will be collected by J2 in the vicinity of Gate 2 and cause J2 to become forward biased. Since Main Terminal 1 is positive with respect to Gate 2, J2 at point (1) will have a greater forward bias than at point (2). This forward bias will cause an injection of holes primarily at point (1) into the central

N type region. Some of these injected holes will be collected by junction J 3 , which is now reverse biased. This will induce injection of electrons from J4 into the lower $P$ type region, which, in turn, will be collected by J3. Here again, the counter injection will continue until the entire area over the lower N type region or cathode is turned on.

As long as the current through the device is maintained above a certain minimum level (holding current), this positive feedback will continue and the device will continue to conduct.

## Turn-Off Time

Except for gating, the triac is a symmetrical device. The turn-off mechanism, when the device has been conducting in one direction is virtually the same as turn-off in the other direction.

Consider the case depicted in Figure 1-48(c), where Main Terminal 1 is negative with respect to Main Terminal 2, and the left-hand portion of the device is conducting. Regions P1 and N2 in the left-hand portion are flooded with minority carriers. Majority carriers are not shown.

When the polarity of the device is reversed, some of these minority carriers will recombine with majority carriers, and most of the others will be collected by junctions J1 and J3. The collection of these stored minority carriers results in reverse recovery current. This current causes the injection of additional minority carriers from junction J2. Both electrons are injected into P1 and holes are injected into N2 by junction J2. The primary effect is the injection of holes into N2. This additional injection pro-
longs the recovery process, but since the $a$ of the P1, N2, P2 section is quite low at these current densities, only a small percentage of them ever reach J3.

If a sufficient number of holes are collected at section $R$ of J3 to induce injection of electrons by J4 into P2 section $R$ (see Figure 1-48(d)), the device will turn on. This can only occur if a large number of holes have diffused into section $R$ from section $L$ of N2 or if a sufficient number of holes are injected into section R of N2 by J2 during the recovery phase of section L.

This problem is minimized by constructing the device with a horizontal separation between N1 and N3 of several minority carrier diffusion lengths and obtaining a high enough sheet resistance of N2 to minimize injection of carriers from J2 into section R of N2.

## dv/dt

The load circuit in many applications will have a somewhat lagging power factor. This may result in appreciable reapplied $\mathrm{dv} / \mathrm{dt}$ of opposite polarity. Consider a single phase circuit shown in Figure 1-49,
controlled by a pair of anti-parallel connected SCRs. The resulting waveshapes when these two SCRs are triggered symmetrically (that is, if the respective triggering angles of their anode-cathode voltages are equal), are illustrated in Figure 1-50. Figure 1-51 illustrates instances when the triggering angle $a$ is less than or greater than the circuit power factor angle $\phi$.

Examining the waveshapes shown in Figure 1-51(b) in a qualitative manner is most useful in determining the characteristics required of a control device used in this type of circuit. It becomes apparent that the control device will be subjected to sudden applications of off-state voltage ( $\mathrm{e}_{\mathrm{S}}$ ) because of the inductive nature of the load. (iL lags eAC). A device incapable of remaining in a blocking state during this type of operation will cause full conduction to occur and loss of control to the load will result.

A pair of SCRs in anti-parallel, as in Figure 1-49, connected to a lagging power factor load will repeatedly be required to withstand high dv/dt stresses (as seen in Figure 1-51). However, since the de-


Figure 1-49. Single-Phase AC Controller Circuit


Figure 1-50. Characteristics of Anti-Parallel Connected SCRs


Figure 1-51. Characteristics of AC Controller Circuit
vice seeing this high rate-of-rise of off-state voltage has not been conducting for at least the previous half cycle, this would be termed "critical dv/dt." Thyristors, in general, display superior "critical $\mathrm{dv} / \mathrm{dt}$ " capabilities compared to their reapplied dv/dt capabilities. This is due to the fact that under "critical dv/dt" stress, there is no major carrier recombination that
must take place in the device before it can block conduction.

When considering a triac for this type of control, the contrary is true. Since the triac is a bi-directional device, it can have conducted in one direction prior to being asked to block in the other. A dv/dt impressed on a triac after it has been in conduction is called "commutating" $d v / d t$ and is a form of


Figure 1-52. Triac Commutating $d v / d t$
"reapplied" dv/dt. The choice between using a triac for the control element in Figure 1-49 or a pair of anti-parallel SCRs is determined by the inductive nature of the load and the availability of triacs with high "commutating" dv/dt ratings versus the availability of SCRs with high "critical" dv/dt ratings.

A comparison of typical commutating dv/dt ratings for various triacs and their dependence on temperature is shown in Figure 1-52. It remains with the designer to determine the $\mathrm{dv} / \mathrm{dt}$ conditions existing in the circuit and to choose the proper device accordingly. Fortunately, snubber circuits may be used to reduce the dv/dt stress on a triac when the device is used in conjunction with a highly inductive circuit. By using an R-C network connected across the device, as shown in Figure 1-53, it is possible to suppress the rate-of-rise of voltage ( $\mathrm{dv} / \mathrm{dt}$ ) seen by possible to suppress the rate-of-rise of voltage (dv/dt) seen by the device.


Figure 1-53. Triac with Snubber Circuit

Choice of a triac vs. two antiparallel SCRs from the consideration of di/dt limitations is rarely a determining factor. For some extreme cases, the designer may want to use devices which are designed to have extremely fast turn-on characteristics to minimize the di/dt
suppression necessary. Since triacs now available are not specifically designed for very high inrush rates a pair of fast turn-on SCRs with special gate structures would be the best choice in such cases.

## Dissipation Characteristics

Since the triac is characterized as a bi-directional control device, its ratings are also characterized in this fashion. It is relatively easy, then, for the design engineer to determine the required heat dissipator for a given circuit application. Knowing the required RMS current which the device will be subjected to, one can consult a curve of RMS on-state current vs. maximum allowable case temperature. As in Figure 1-54, this is represented by one curve for all conduction angles. We shall label this maximum allowable case temperature as $\mathrm{T}_{\mathrm{C}}$. The next step is to consult the curves for device dissipation vs. RMS current for the proper conduction angle. Representative curves are shown in Figure 1-55. This dissipation may be called $W_{T}$. Knowing the maximum ambient temperature $\mathrm{T}_{\mathrm{A}}$ and the interface thermal resistance between the heat sink and the device case ( $\mathrm{R}_{\theta \mathrm{CS}}$ ), we can now calculate the necessary heat exchanger efficiency for the application ( $\mathrm{R}_{\theta \mathrm{S}}$ ) using Formula 1-W.
$\mathrm{R}_{\theta \mathrm{S}}=$

$$
\begin{equation*}
\frac{\left[\mathrm{T}_{\mathrm{A}}+\mathrm{R}_{\theta \mathrm{CS}} \times \mathrm{W}_{\mathrm{T}(\mathrm{AV})]}\right.}{\mathrm{W}_{\mathrm{T}(\mathrm{AV})}} \tag{1-W}
\end{equation*}
$$

Where:

| $\mathrm{R}_{\theta \mathrm{S}}$ | $=$Heat exchanger <br> efficiency |
| :--- | :--- |
| $\mathrm{T}_{\mathrm{C}}$ | $=$ Case temperature |
| $\mathrm{T}_{\mathrm{A}}$ | $=$ Ambient temperature |
| $\mathrm{R}_{\theta \mathrm{CS}}$ | $=$ Thermal resistance, |



Figure 1-54. Triac Onstate Current vs. Maximum Allowable Case Temperature
heat exchanger to device

## $\mathrm{W}_{\mathrm{T}(\mathrm{AV})}=$ Device power loss

The dissipation in the triac is considerably greater than that of a single SCR for a given RMS line current. This, of course, is to be expected, since the triac conducts during both half cycles. It is often more practical to use high power triacs when either forced air cooling or liquid cooling is available. These cooling means provide high thermal efficiency and allow the use of relatively small heat exchangers to keep the triac below its maximum allowable case temperature. If natural convection cooling is the only means available, a rather large heat exchanger will generally be required as compared to one needed for each

SCR in an equivalent anti-parallel configuration.

## HOCKEY-PUK SCRs [9]

International Rectifier's Hock-ey-Puks are a natural development in SCR construction to achieve more effective junction cooling and greater flexibility in assembly. The Hockey-Puk is a pressure-assembled device designed to maximize the benefits of double-side cooling using air-cooled or liquid-cooled heat exchangers. This double-side cooling is accomplished by constructing the device so that the anode and cathode connections are large area contacts. These copper pole pieces maximize heat transfer to the heat exchangers while retaining compactness.


Figure 1-55(a). Low-Level On-State Power Loss vs. Current


Figure 1-55(b). High-Level On-State Power Loss vs. Current

The greater thermal efficiency achieved by this construction provides up to $60 \%$ more continuous current-carrying capability over comparable stud-mounted devices. In addition, pressure-assembled construction eliminates all solder joints within the device, thus avoiding the thermal fatigue problem sometimes found in large area semiconductor devices. To further adapt the Hockey-Puk to heavy industrial applications, the package is hermetically sealed. Figure 1-56 shows a cutaway view of a typical IR Hockey-Puk.

Since the Hockey-Puk device is designed for double-side cooling, it presents unique possibilities in mounting and circuit design.

## Mounting the Hockey-Puk

Mounting is an important aspect in applying Hockey-Puk devices. Failure to observe necessary precautions in handling and mounting
can result in impaired operation and reduced reliability.

International Rectifier HockeyPuk devices are supplied with pole surfaces that are flat to 0.0015 TIR and a maximum roughness of 32 microinches. The mating heat exchanger surfaces must have the same quality finish, or better. If the surface finish does not conform to these recommended limits, the pole surfaces will contact the heat exchanger only in a relatively few spots. This will cause the contact thermal resistance to increase to a point that the power losses of the junction may raise the junction temperature above the maximum rated values. To further insure good heat transfer, a thermal interface compound, such as Penetrox "A", (Burndy Corp.), or equivalent, should be used between the pole piece and heat exchanger mounting surfaces.

The clamping force should be applied smoothly, evenly, and per-


Figure 1-56. Typical Hockey-Puk Structure
pendicularly to the Hockey-Puk to insure that there is no deformation of either the pole faces or heat exchanger during mounting. The amount of clamping force is important. The clamping force required on IR Hockey-Puks is listed in Table I-VII. Figures 1-57 and 1-58 show the effect that varying the clamping force (applied force in pounds) has on thermal resistance and on-state voltage on a device rated to have 900 to 1100 pounds applied.

The clamp shown in Figure 1-59 was designed to apply the clamping force in a smooth, even manner, perpendicular to the Hockey-Puk pole face. Figure 1-60 shows the effect of non-perpendicular application of force. Note the resultant
hot spot and pole deformation. This type of mounting drastically reduces device capability.

## Mounting Hockey-Puk Assembly

When the Hockey-Puk is assembled, one more precaution must be taken. If the assembly is mounted with both heat exchangers immovable as shown in Figure 1-61(a), the thermal expansion due to normal operation can place stresses on the assembly, causing catastrophic failure. Figure 1-61(b) shows a better method of mounting a single Hock-ey-Puk assembly. The same principle would apply for two or more devices on a common heat exchanger.

## Versatility

Stud-mounted controlled recti-


Figure 1-57. Hockey-Puk Thermal Resistance vs. Applied Force


Figure 1-58. Hockey-Puk On-State Voltage vs. Applied Force


Table I-VII. Hockey-Puk Mounting Data

| $\begin{gathered} \text { SCR } \\ \text { CASE STYLE } \end{gathered}$ | TO-200AB |  | TO-200AC | A-10 | A-18 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SCR Series | $\begin{aligned} & 115 \mathrm{PA} \\ & 175 \mathrm{PA} \\ & 250 \mathrm{PA} \\ & 300 \mathrm{PA} \end{aligned}$ | 125 PAM, PAL, PALB 140 PAM, PAL | $\begin{aligned} & 350 \mathrm{PBM}, \mathrm{PBL} \\ & 360 \mathrm{PBM}, \mathrm{PBL} \\ & 420 \mathrm{~PB}, \mathrm{PBM} \\ & 430 \mathrm{PBM}, \mathrm{PBL} \\ & 470 \mathrm{~PB} \\ & 500 \mathrm{PBQ} \\ & 550 \mathrm{~PB}, \mathrm{PBQ} \\ & 600 \mathrm{~PB} \\ & 750 \mathrm{~PB} \\ & 900 \mathrm{~PB} \end{aligned}$ | $\begin{aligned} & 700 \mathrm{PK} \\ & 850 \mathrm{PK} \\ & 1000 \mathrm{PK} \end{aligned}$ | $\begin{aligned} & 1200 \mathrm{PN} \\ & 1600 \mathrm{PN} \end{aligned}$ |
| Rectifier Case Style (1) | DO-200AA | - | DO-200AB | B-19 | - |
| Rectifier Series | $\begin{aligned} & 401 \text { PDAL } \\ & 471 \text { PDA } \end{aligned}$ | - | $\begin{aligned} & 651 \text { PDBL } \\ & 801 \text { PDB } \end{aligned}$ | 2001PD | - |
| Mounting Force $\text { (Ib) } \pm 10 \%$ | 1,000 | 800 | 2,750 | 4,500 | 8,000 |
| Pole Face Dia. [inch (mm)] |  | $\begin{aligned} & 752 \\ & 9.10) \end{aligned}$ | $\begin{gathered} 1.302 \\ (33.07) \end{gathered}$ | $\begin{gathered} 1.760 \\ (44.70) \end{gathered}$ | $\begin{gathered} 2.477 \\ (62.92) \end{gathered}$ |
|  |  | $\begin{aligned} & 748 \\ & 9.00) \end{aligned}$ | $\begin{gathered} 1.298 \\ (32.96) \\ \hline \end{gathered}$ | $\begin{gathered} 1.750 \\ (44.45) \\ \hline \end{gathered}$ | $\begin{gathered} 2.473 \\ (62.81) \end{gathered}$ |
| Max. Thickness [inch (mm)] |  | $\begin{aligned} & .555 \\ & 4.10) \end{aligned}$ | $\begin{gathered} 1.06 \\ (26.92) \end{gathered}$ | $\begin{gathered} 1.09 \\ (27.69) \end{gathered}$ | $\begin{gathered} 1.38 \\ (35.05) \end{gathered}$ |
| Clamp Series |  | C-3 | C-4 | C-5 | C-6 |
| Suggested Springs |  | 1 | 3 | 2 | - |

(1) Similar to SCR types, but without gate and auxiliary cathode terminals.


Figure 1-59. Typical Hockey-Puk Mounting Clamp
fiers are not available in the forward polarity configuration (cathode to base). The Hockey-Puk configuration permits overcoming this limitation by merely turning the Hockey-Puk over in the assembly. Having this versatility, the HockeyPuk allows the design engineer much more freedom in parallel and series designs. Some of these possibilities are illustrated in Figure 1-62.

## PASSIVATED ASSEMBLED CIRCUIT ELEMENTS - PACE/paks [10, 11]

IR uses improved passivation techniques for power semiconductors, and has employed some of the technology from the microelectronics industry to manufacture high power thyristor and rectifier hybrid circuits. The circuits generally util-
ize thyristor or diode junctions mounted on an electrically isolating, thermally-conductive substrate, which is, in turn, mounted to a copper or aluminum plate that can be attached to a heat dissipator. The active components of the device are encapsulated with high temperature, moisture-resistant epoxy. The junctions are isolated from the copper plate by means of a beryllium oxide, or, in the case of lower power applications, an alumina substrate. Then, depending upon the amount of current to be handled, the devices are interconnected by a wire frame or by thick film techniques. The power and control leads can then be brought out of the epoxy encapsulation by means of fast-on terminals or lugs.


Figure 1-60. Hockey-Puk with Uneven Force

## Advantages

This construction offers many advantages over the conventional packaging techniques. These advantages include: 1) The user's engineering design time is better utilized because only one device must be specified instead of as many as five for single-phase applications and seven for three-phase applications. 2) Assembly labor costs are reduced, as only one device must be mounted and interconnected for the entire power section. 3) Visual keys by either color coding or mechanical asymmetries can be used to aid in making the assembly installation foolproof. 4) Isolated heat dissipators are eliminated because the single copper plate is isolated from the circuit. 5) Thermal efficiencies are better than with individual devices. 6) In many applications, the smaller size of the power circuit assembly can be utilized to advantage. For example, a single-phase full wave controlled bridge assembly, designed for a 2

(a) NOT RECOMMENDED

(b) RECOMMENDED

Figure 1-61. Mounting a HockeyPuk Assembly
hp dc motor, is only $1.25^{\prime \prime} \times 2.5^{\prime \prime} \mathrm{x}$ 0.9 " ( $31.75 \times 63.5 \times 22.86 \mathrm{~mm}$ ) and could be mounted directly on the bell housing of the motor itself. 7) There is a savings in the parts inventory required for a product using the PACE/pak; this parts count savings can be as high as 7 to 1 , not counting hardware and wire. 8) An increase in rating over the equivalent junction when mounted in the standard junction-soldered-to-stud case is obtained. This was noted during the earliest testing and evaluation of the PACE/pak; there was a large reduction of the thermal impedance, junction-to-case of the thyristors (the "case" being the


Figure 1-62. Hockey-Puk Mechanical Configurations
copper base plate) when compared to the same junction soldered to a copper stud.

From the rating sheets of IR's 25 ampere, standard, stud-mounted SCR series, the thermal impedance of a $16 R \mathrm{C}$ is $1.5^{\circ} \mathrm{C} / \mathrm{W}$. However, referring to Figure 1-63, the SCR
and the diode together in the hybrid assembly have a thermal impedance of $0.9^{\circ} \mathrm{C} / \mathrm{W}$. Mounting the devices on the beryllium substrate directly has increased the heat removal capacity (reduced the thermal impedance) of the hybrid assembly over that of the stud-


Figure 1-63. PACE/pak Estimated Power Loss
mounted device by $40 \%$. The reason is the large contact area of the substrate to the copper plate, while in the stud-mounted device, the interface between the stud type base and the heat dissipator presents a thermal barrier, due to the small contact area between the two. One might speculate that very little might be gained when considering contact areas. However, the shorter the thermal path, the greater the thermal efficiency (considering materials with similar thermal conductivities). The thermal path from the junction to the copper base of the PACE/pak is basically a straight line, while the thermal path of the stud-mounted device is at best a $20^{\circ}$ line around the stud of the device. This principle also holds true for the diodes in these assemblies.

## Construction

The construction of the PACE/ pak is straightforward; however, there are some variations in the techniques used, depending on the power level to be handled by the device.

Diode and/or thyristor junctions are taken directly from the standard (stud mount devices) production line. (This allows a larger variety of circuits and power capabilities without the necessity of starting a new production line.) The junctions are used in two forms, one with connecting wires and a solderable molybdenum disc attached and these wires and dises are used for the interconnections and mounting. In the other form (generally lower power), the junctions are metallized for direct soldering of the interconnections and the junction to the metallized substrate. This latter form of junction is particularly suited, with proper jigging,
to furnace soldering. In many lower power PACE/paks, thick film techniques are used to make the interconnections. The berylliumoxide substrate is then soldered to the copper mounting plate for high power devices or in the case of lower power units a thermalconducting epoxy is used to attach the substrate.

The power hybrid circuits are then directly encapsulated in epoxy resin. In order to prevent interaction between the resin and the junctions, and to increase reliability, the junctions are passivated. This eliminates the need for any intermediate encapsulation of the junctions, with the consequent advantage of better heat flow and less bulk and cost. The method used is the same as that used in the production of some microelectronic circuits.

## Rating and Application

To give more insight into the use of these new encapsulated devices, consider the circuit configuration shown in Figure 1-64. This circuit


Figure 1-64. Common PACE/pak Circuit: Single-Phase Hybrid Bridge with Free-Wheeling Diode
would be used in low power dc motor drives or without the freewheeling diode as a power supply. Further, for purposes of this discussion, let us assume that the devices used are in the 25 ampere RMS rating category.

Figure $1-65$ defines the maximum allowable base plate (case) temperature vs. conduction angle and de output current. Knowing the worst case conditions of the user's application, the maximum allowable base plate (case) temperature can be determined. Then, taking Figure 1-66, which shows power loss vs. conduction angle and output current, and knowing the maximum allowable base plate temperature, it is possible to determine the heat dissipator requirements. Assuming a $1.5^{\prime \prime}(38.1 \mathrm{~mm})$ surface
area, a good thermal compound and smooth contact surface, the thermal resistance of the base plate to dissipator, $\mathrm{R}_{\theta \mathrm{CS}}$, is in the neighborhood of $0.1^{\circ} \mathrm{C} / \mathrm{W}$.

Using these design graphs, it is possible to characterize this power hybrid assembly in a fashion very similar to that used for a discrete device. There are some interesting variations from this rule, because this is a complete circuit, not a single device. Consider working into a highly inductive load with the circuit shown in Figure 1-64. The permissible output current into an inductive load can actually be greater than that permitted for a resistive load, during a phase-back condition. Figure 1-67 shows this for the 25 amp PACE/pak working into a theoretically perfect inductor at a


Figure 1-65. PACE/pak Output Current vs. Base Plate Temperature and SCR Conduction Angle


Figure 1-66. PACE/pak Actual Power Loss vs. Output Current and SCR Conduction Angle
$75^{\circ} \mathrm{C}$ case temperature. The reason is that during the free-wheeling portion of the cycle, the forward voltage drop, hence the power loss, is less than when the SCRs are conducting. For example, when the
bridge is conducting 25 A , the current is going through two devices with a combined forward voltage of 2.55 volts; the power dissipated is $(2.55 \mathrm{~V} \times 25 \mathrm{~A}) 63.75 \mathrm{~W}$, while during free-wheeling, it encounters


Figure 1-67. Maximum Allowable Output Current vs. SCR Conduction Angle
only one diode voltage drop, 0.9 volts, and the power dissipated is $(0.9 \mathrm{~V} \times 25 \mathrm{~A}) 22.5 \mathrm{~W}$. The final downturn in current at about $90^{\circ}$ is caused by having reached the freewheeling diode's current capability.

## Circuits

The use of PACE/paks is similar to using integrated circuits, in that the designer is no longer selecting an individual component, but he selects the circuit which will meet his functional job requirement. However, similarly to the integrated circuit industry, it is expensive to generate an infinite variety of specialized circuits to satisfy each application. As with the integrated circuit industry, it is better for a designer to select a standard circuit, rather than a special design, and take advantage of volume production and the resultant lower costs.

(c) SINGLE PHASE HYBRID BRIDGE WITH COMMON CATHODE CONNECTION

Some of the variations which are available and relatively easy to generate are shown in the following figures.

Several common SCR bridge control circuits can be seen in Figure 1-68 with (c) being the most common. Both circuit (c) and (d) can be supplied with or without a free-wheeling diode. Circuit (a) can be used for generator exciters, dc motor drives and power supplies. It also has the advantage of not requiring a free-wheeling diode. Circuit (b) can be used as a dc motor drive with the added advantage of being able to provide regeneration during braking. Circuits (c) and (d) are commonly used as dc motor drives. The most popular power levels to date have been in the one to five horsepower range. It might be noted that by shorting the positive to negative output of these

(b) SINGLE PHASE, ALL SCR, CONTROLLED BRIDGE

(d) SINGLE PHASE HYBRID BRIDGE WITH COMMON ANODE CONNECTION

Figure 1-68. PACE/pak Bridge Configuration Circuits
circuits, an ac switch configuration is obtained.

Figure $1-69$ shows a miscellany of circuits that have been built using a common substrate. Circuit (a) has been used as a field excited in a generator, a half wave dc power supply, as well as a de relay/contactor driver. Circuit (b) is a universal configuration. It can be used as a positive or negative center tap circuit, pulse charger, doubler, ac switch or with selected devices even an inverter leg. Circuit (c) is an inexpensive pulse charger for leading power factor loads.

A variety of ac switches are shown in Figure 1-70; these can be used for lighting controls, heating controls and motor starters. The triac is especially well-suited to these jobs and has the advantage of being only one control element. However, some caution must be exercised when using it with an inductive load. The triac's commutating $\mathrm{dv} / \mathrm{dt}$ is not especially high and must be considered or a


Figure 1-69. Other PACE/pak Circuits
loss of control may be experienced during a phase-back condition. The circuit using the diode in anti-parallel is used mostly in three-phase circuits; however, it could be used in a limited range single-phase light dimmer application.

A new area where PACE/paks are being applied is three-phase power circuits as shown in Figure 1-71. Three phase diode bridge circuits can be delivered with voltage ratings of up to 600 volts and current levels to 150 amps .

Various other circuit configurations are under development, with new standard building blocks being introduced regularly.

## GENERAL APPLICATION HINTS

One of the most common difficulties in the application of thyristors is a misunderstanding of SCR specifications and ratings, such as critical vs. reapplied dv/dt, the significance of reverse recovery in SCRs and power rectifier diodes, and the meaning of the di/dt rating in terms of circuit performance and design.

Second is a cost related factor that concerns all design engineers. Often, the SCR design engineer attempts to specify a device with very stringent performance requirements and ratings to save money on other components in the circuit, and he forgets that the device may be impossible or uneconomical to produce. This problem is most apparent when a few such special devices have been used in a prototype breadboard. Later, when a large quantity order results, no SCR manufacturer can provide the device in the quantities needed.

[^2](b) AC SWITCHES
(a) TRIAC



Figure 1-70. PACE/pak AC Switch Circuits


Figure 1-71. PACE/pak Three-Phase Rectifier Circuit
trolled bridge rectifier circuits often overlooked is that output voltage cannot be decreased to near zero while maintaining the same average output current. In this case, the device may be kept well within its average current rating, but will be operating many times beyond maximum RMS current rating.

This is true because the different form factors associated with the average and RMS currents cause the RMS value to greatly exceed the average at low conduction angles. The limiting factor is that RMS current (heating) flows through the
resistive portion of the leads and internal assembly parts, and adds heat to the junction rather than carrying it away. Table I-VIII shows the various form factors vs. the conduction angle ( $\theta_{\mathrm{C}}$ ).

Table I-VIII. Form Factor vs. Conduction Angle (Sine Wave)

| $\theta \mathrm{C}$ | IRMS/IAVG |
| :---: | :---: |
| $15^{\circ}$ | 5.653 |
| $30^{\circ}$ | 3.979 |
| $45^{\circ}$ | 3.233 |
| $60^{\circ}$ | 2.780 |
| $90^{\circ}$ | 2.221 |
| $120^{\circ}$ | 1.878 |
| $180^{\circ}$ | 1.571 |

It is important for the designer to keep these concepts in mind, because the average current may look extremely low, yet the RMS currents may be high enough to cause device destruction. It is possible to fall into this trap when selecting a current detection circuit or locating it in the main circuit. The problem exists, for example, when current is detected through
an averaging network, or when a peak current detector is positioned after the filtering in the power circuit.

## Snubbers

All SCR applications must take account of device dv/dt ratings and steps must often be taken to soften anode-cathode waveforms. The standard techniques for limiting applied dv/dt rely on the integrating ability of capacitors. The most primitive snubber of this type is shown in Figure 1-72. The capacitor absorbs excess transient energy, while the resistor defines the applied dv/dt in conjunction with the external system inductance.

An informative analysis studies the response of this snubber to a step function voltage. If an infinitely sharp voltage, of magnitude $E$, is impressed across the entire R,L,C combination, the waveform applied to the protected SCR will be considerably softened, due to the high transient impedance of the inductor. The maximum SCR dv/dt will then be given by Formula 1-X.
Maximum aevice dv/dt =
$2 \propto \omega_{n} E_{\text {in }}=\frac{E R}{L}$

$$
\mathrm{L}_{3}
$$

Where:
$\mathrm{E}_{\text {in }}=$ peak value of applied transient voltage
$\omega_{\mathrm{n}}=$ circuit natural angular frequency $(1 / \sqrt{\text { LC }}$
$\propto$
$=$ damping factor
$\left(\frac{\mathrm{R}}{2 \sqrt{\mathrm{~L} / \mathrm{C}}}\right)$
To prevent excessive magnification of any applied transient voltages, a damping factor in the range of about 0.5 to 1.0 should be chosen for the LRC suppressor network. A damping factor of 0.7 restricts the overswing to 20 percent greater than the peak transient voltage.

A damping factor of 1.0 would restrict the voltage to that of the peak transient with no overswing.

Consequently, standard design requires
$\frac{\mathrm{L}}{\mathrm{R}^{2}}<\mathrm{C}<\frac{4 \mathrm{~L}}{\mathrm{R}^{2}}$
Going over the upper limit overdamps the circuit and requires excessively large capacitors and dissipation.

In practical situations, it is usually necessary to choose $R$ quite
158.


Figure 1-72. SCR Snubber Circuit
small ( 10 to 200 ohm) but even so, for higher frequency operation, the snubber dissipation can be quite significant, increasing system cost and impairing system efficiency.

However, these are the trade-offs that the design engineer must decide for himself.

## Hybrid Bridge

Two systems may be used to provide controllable three-phase bridge rectifiers, one utilizing 6 SCRs (the full converter circuit) and the other 3 SCRs and 3 conventional rectifiers (the hybrid or semi-converter circuit). (See Figures 1-73 and 1-74.)

Figure 1-73 shows the 6 SCR 3 -phase bridge circuit. This circuit provides full control of output power as the thyristors receive independent gate triggering signals and does not lose control of the output voltage. On the other hand, the bridge circuit shown in Figure 1-74 consists of only 3 SCRs together with 3 diodes and requires only 3 gate drive circuits. Consequently it is much less expensive to build.

On inductive loads, in hybrid assemblies, it is important to avoid sudden removal of the gate pulses, as the inductance prevents the output current from immediately dropping to zero and the conducting SCR will not turn-off. Current will be drawn from the supply under these conditions for $240^{\circ}$ of the full cycle, and, providing the inductance of the load is sufficiently high, current will circulate for the remaining $120^{\circ}$ (via the rectifier in series with the conducting thyristor).

The above condition can remain in effect indefinitely, and will generally result in serious overloading of the conducting SCR. Two solutions are available for this difficulty:
A. Never remove gate pulses unless the output current has previously been maintained at a low level for a period of time well in excess of the load time constant. B. Provide a free-wheeling diode across the load.

## Gate Drive

One of the most frequent causes of trouble for a designer is the SCR


Figure 1-73. Three-Phase, All-SCR (Full Converter) Bridge Circuit


Figure 1-74. Three-Phase, Hybrid (Semi-Converter) Bridge Circuit
gate drive. The problem usually involves providing sufficient power gain between the logic and the SCR gate; arriving at the SCR gate with adequate drive and isolation seems to be a stumbling block for many SCR design engineers.

The design engineer would like to trigger a 740 ampere RMS SCR with a unijunction transistor pulse circuit through a 10 volt-microsecond pulse transformer for isolation.

The problem exists because, under the above conditions, many large SCRs will turn on and operate successfully at room temperature and with a low di/dt load, but at $0^{\circ} \mathrm{C}$, the unit will not work at all, and with a high di/dt load it will not work for long even at room temperature. Faced with this problem, the engineer will tighten the specification for the gate trigger current and voltage to obtain easy triggering at low temperatures. To cover the extra cost of this selection, the SCR manufacturer must raise the price of the device. In addition, the designer has removed some much needed noise immunity and performance with a high di/dt load may still be marginal.

The designer, in this case, should reconsider his drive circuits to decide if, in the long run, it would not be less expensive to meet the gate drive conditions specified in the catalog data sheet for a standard device.

There is another problem surrounding a lagging power factor load. In many inverter designs, the power SCR in the circuit may not be forward biased until well into the half-cycle. At the same time, the reactive current is flowing through the free-wheeling diode. In this case, it is clear that a pulse gating scheme cannot be used. A direct current must be supplied to the gate after the initial gate pulse to insure that the device will trigger when it does become forward biased. This current is commonly referred to as the "back porch" of the gate drive signal.

## Reverse Recovery (Diode and SCR)

Many engineers do not fully appreciate the phenomenon of reverse recovery in a semiconductor device. They tend to view them as perfect switches. At low frequency $(60 \mathrm{~Hz})$ and low current, this is a valid
assumption with respect to reverse recovery. However, at high frequency (repetition rates) and large currents, reverse recovery takes on considerable importance.

Consider, for instance, the waveshape for the diode designated as a normal diffused rectifier shown in Figure 1-75. Let us assume the diode is to be applied in a typical inverter power supply (Figure 1-76). Figures 1-75, 1-77, and 1-78 show that the average losses during recovery can be calculated by Formula 1-Y.


NORMAL DIFFUSED RECTIFIER DIODE, 250A
FORWARD CURRENT: 785A PEAK

| $\mathrm{di} / \mathrm{dt}:-25 \mathrm{~A} / \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{a}}: 4.1 \mu \mathrm{sec}$ |
| :--- | :--- |
| $\mathrm{t}_{\mathrm{rr}}: 5.8 \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{b}}: 1.7 \mu \mathrm{sec}$ |
| $\mathrm{I}_{\mathrm{R}}(\mathrm{REC}): 95 \mathrm{~A}$ |  |

IR(REC): 95A

$$
\begin{align*}
W_{R}= & \frac{V_{F} I_{R(R E C)} t_{a} / 2+}{t_{a}+t_{b}}  \tag{1-Y}\\
& \frac{V_{R W M} I_{R}(R E C) t_{b} / 2}{t_{a}+t_{b}}
\end{align*}
$$

Where:
$\mathrm{W}_{\mathrm{R}} \quad=$ Recovery power
$\mathrm{V}_{\mathrm{f}} \quad=$ Diode forward voltage at the proper current level during $t_{a}$.
$I_{R}($ REC $)=95 A$
$\mathrm{t}_{\mathrm{a}} \quad=4.1 \times 10^{-6} \mathrm{sec}$
tb $\quad=1.7 \times 10^{-6} \mathrm{sec}$
$V_{\text {RWM }}=$ Peak reverse voltage applied to rectifier during operation.

Assume:
$\mathrm{V}_{\mathrm{F}}=2 \mathrm{~V}$
Therefore:
the losses, $\mathrm{W}_{\mathrm{R}}=$
$2 \mathrm{~V} \cdot 95 \mathrm{~A} \cdot 4.1 \times 10^{-6} \mathrm{sec} / 2+$
$4.1 \times 10^{-6} \mathrm{sec}+1.7 \times 10^{-6} \mathrm{sec}$
$600 \mathrm{~V} \cdot 95 \mathrm{~A} \cdot 1.7 \times 10^{-6} \mathrm{sec} / \mathrm{w}$
$4.1 \times 10^{-6} \mathrm{sec}+1.7 \times 10^{-6} \mathrm{sec}$

Averaging this dissipation over the full cycle period for the inverter determines the contribution of the recovery losses to the total diode

Figure 1-75. Diode Reverse Recovery


Figure 1-76. High Frequency Inverted Bridge Circuit


Figure 1-77. Output Waveshape of $T_{1}$ Inverter Bridge


Figure 1-78. Inverter Bridge Rectifier Recovery Characteristics
dissipation. This contribution is given in Formula 1-Z.
$W_{a}=\mathrm{fW}_{\mathrm{R}}\left(\mathrm{t}_{\mathrm{a}}+\mathrm{t}_{\mathrm{b}}\right)$
Where:
$\mathrm{W}_{\mathrm{a}}=$ Average recovery power
f $=$ Inverter operating frequency
Assume:
$\mathrm{f}=1 \mathrm{kHz}$

## Therefore:

$\mathrm{W}_{\mathrm{a}}=48.8 \mathrm{~W}$
At 3 KHz , this dissipation would be 146.4 watts. Therefore, high operating frequencies limit the application of normal recovery diodes.

Thus, by using a fast recovery diode at these higher operating frequencies, average power dissipation during recovery is reduced, and rectification efficiency is improved. Furthermore, the diode can handle a larger forward current without overheating.

It has also been found, especially in some of the higher current dif-
fused rectifiers, that the sweep-out characteristic can display a rather dismaying property. The declination rate (time for decay of the bulk recovery current) can be very fast. This sudden decrease of current generates a rather high apparent di/dt in the distributed inductance of the circuit and the resultant voltage ( $e=L \mathrm{di} / \mathrm{dt}$ ), generated by this "snap-off" characteristic, has often attained a peak value several times the circuit voltage. Consequently, it is important not only to provide a high current rectifier with limited apparent stored charge, but that it should exhibit a controlled declination rate of bulk recovery current in order to assure predictable transient voltages.

Figure 1-79 characterizes the four types of recovery characteristics of a rectifier. Figure 1-79(a) depicts a "normal" recovery for a diffused power rectifier. Figure 1-79(b) shows the typical recovery current of a rectifier with a snap-off characteristic. Figure 1-79(c) shows recovery current of a "soft' recovery rectifier, and Figure 1-79(d) shows recovery current of a fast recovery rectifier. The snap-off diode characteristic has been found to be so rapid that some rather unique pulse-forming networks have been designed using the snap characteristics of certain units. It has generally been found less than desirable to generate such pulses in a circuit that contains components which could be punched through by these transients.

Another area where diode recovery characteristics can cause trouble is when the diode is used for reactive energy return in choppers. If the load is reactive enough to conduct during the whole off period


Figure 1-79. Rectifier Recovery Characteristics
for the SCR, when the SCR is again triggered, it sees essentially a short circuit until the diode recovers. Generally, unless some means is used to limit the initial current through the SCR and diode (or a fast recovery diode is used), there will be excessive di/dt through the SCR. This is a particularly insidious problem, because di/dt can manifest itself as a slow deterioration causing the SCR to fail many months later.

The SCR itself also has a reverse recovery interval, which can give rise to similar difficulties if it is not fully appreciated during design.
di/dt
If the current in an SCR is allowed to build up too rapidly at turn-on, there is a current crowding effect in the area where gate current is flowing. The device switches on progressively across the junction, starting at the point where the gate current is injected at about 0.1 $\mathrm{mm} / \mu \mathrm{sec}$. (This turn-on increase in current is called di/dt.) This current crowding causes local overheating, which may or may not destroy the device immediately. There can, however, be a degradation in device characteristics which will eventually lead to a failure. Therefore, it is important that if the basic external circuits will allow the current in the device to rise at above a certain critical rate, then the external circuit has to be modified by the introduction of sufficient inductance, to reduce the maximum possible rate of change of current to within a defined value.

The most obvious area where this can happen is in resistive or capacitive circuits, where the SCR must switch on into such a load. The designer must be cautious when dealing with these loads.

Another trap exists where the load is an incandescent lamp. In this case, the load is not only resistive, but the initial current, when the lamp is cold, can be ten times the rated running current.

Another area that must be considered is the R-C snubber network, where the SCR is expected to discharge the snubber capacitor each time it turns on. This discharge
current increases the di/dt required of the device.

Also, high di/dt in a circuit can lead to higher switching losses, which is especially important at
high frequency, and if the di/dt is allowed to go too high, device degradation takes place and the SCR eventually fails.

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## Parallel Operation

## Important Characteristics

The following characteristics of thyristors are of importance in achieving an optimum design in a large power, high current converter using devices in parallel: 1) Turn-on sensitivity, 2) Delay time, 3) Finger voltage, 4) Turn-on propagation characteristics, 5) Latching and holding current, 6) On-state voltage, 7) Thermal resistance, and 8) Loop Inductance.

The relative importance of these characteristics depends upon the system that is being designed in terms of whether it is a single-phase converter, multiple phase converter, chopper, inverter, etc. This is important because of the theoretical rise time possible of the device currents due to the external circuit limitations. We can discuss some of
the system characteristics and their relation to each other and some of the solutions commonly used to help to control or match the characteristics of the devices. The solutions used by the circuit designer will depend upon his particular application.

Of the eight listed characteristics, turn-on sensitivity, delay time, and turn-on propagation characteristics are interrelated. Turn-on propagation was discussed in detail in Chapter 1 and will not be discussed here. Figure 2-1 shows the delay times of two thyristors manufactured by different methods. Curve A is typical of the characteristic of an alloy diffused SCR. Curve B is typical of either an epitaxial diffused thyristor or a double-diffused thyristor.


Figure 2-1. Turn-On Characteristics of Two Thyristors

Turn-On Sensitivity and Delay Time
In order to understand why these characteristics are inherently different, one must understand a little about the construction of each type of device and how the cathode regions are formed in them. In the case of an alloy diffused thyristor, after the initial diffusion sandwich forming a PNP wafer is achieved, the final junction is formed by alloying a gold antimony dise into the top of the silicon wafer as shown in Figure 2-2. This forms an N -region and forms the final PN junction. Because this
is a relatively imprecise means of forming a junction, this region has a rather feathered boundary and therefore provides somewhat of a nonuniform turn-on characteristic as is seen in Figure 2-1.

Figure 2-3 shows the construction of an epitaxial diffused device which is formed in terms of the PNP sandwich in a similar manner to that of the alloy diffused device, but when the final N region is added, a well-defined window is cut into the silicon and intrinsic silicon is mixed in a gaseous form with an N dopant and deposited into this


Figure 2-2. Cross Section of Alloy Diffused SCR


Figure 2-3. Cross Section of Epitaxial Diffused SCR
window forming a much more sharply defined PN junction. This junction, which can be considered hyperabrupt, exhibits a much more uniform turn-on characteristic and a much more uniform delay time characteristic as is shown in Figure 2-1.

In many applications, this type of characteristic is not important. Where the devices are to be paralleled, the turn-on characteristic of the device, including the triggering sensitivity and the delay time, become important. For example, consider two SCRs to be connected in parallel; first two devices having an alloy diffused structure, and then two devices having an epitaxial diffused structure, and consider their various characteristics and what might happen if these characteristics were not in some way taken into consideration in the circuit design.

Figure 2-4 illustrates one of the sets of conditions for alloy diffused devices that may result in this case. The turn-on characteristic of device A, shown in the top of Figure 2-4, indicates that the anode-to-cathode voltage begins to fall more quickly because the triggering sensitivity of that device, as shown in the second part of Figure 2-4, is slightly greater than that of device B. Since the devices have no well-defined delay time, they begin to turn on as soon as gate current is applied and then the voltage across device A begins to fall more rapidly as both devices go into the regenerative turnon mode.
The anode current as shown in the third part of Figure 2-4 begins to rise sooner in device A than in device $B$, and even if the devices had been matched in forward voltage at some high current, they
would never achieve that current level equally because of the unequal turn-on characteristics. Figure 2-4 is somewhat optimistic in the fact that anode current of device $B$ is shown rising at all. If indeed device A turned on and there were no appreciable inductance in the loop which includes device A, device B might never turn on if the anode-to-cathode voltage of A fell below the finger voltage of $B$ before it triggered.

One of the things that affects the degree of importance of this characteristic is the amount of inductance in each SCR loop. This loop inductance can be built in by the construction of the equipment, or may be inserted in the form of a saturable or a nonsaturating inductance, whichever is more economic and more feasible for the circuit designer in order to force this type of sharing.

One method of equalizing this turn-on characteristic of alloy diffused devices is to choose a resistor to be put in series with each gate of the devices to be paralleled. By adjusting the turn-on sensitivity of the device under a given anode-tocathode voltage and triggering characteristic, this resistor can force better uniformity in the devices. This technique is not necessary if a device with a hyper-abrupt junction is used as in the case of an epitaxial diffused device.

Let's consider a similar idealized example of the turn-on characteristics of the epitaxial diffused device shown in Figure 2-5. Figure 2-5 shows the anode-to-cathode voltage vs. time characteristic, the gate triggering current characteristics, and the anode current resulting from paralleling two epitaxial diffused




Figure 2-4. Alloy Diffused SCR Turn-On Characteristics


Figure 2-5. Epitaxial Diffused SCR Turn-On Characteristics
thyristors in a similar fashion to that used in Figure 2-4 for the alloy diffused devices. Without having matched the delay characteristics of the devices, the delay mismatch shown in the first part of Figure 2-5 would be typical of what one might experience in choosing two devices from the same manufacturing class at random. If the devices also had a mismatched gate current to trigger characteristic as shown in the second part of this figure, then the anode current shown in the third part might result again, assuming some reasonable amount of circuit inductance in each of the thyristor loops.

The resulting mismatch between the two devices would be appreciably lower than with the alloy diffused devices, and the technique of using gate resistors in series with each of the gates may not be necessary in this case. What the circuit designer would want to do then would be to require that the device was made by the process yielding a well defined delay period, as shown in Figure 2-5, and furthermore, that the delay times of the devices were matched within some reasonable figure, say 0.25 to 0.5 microseconds maximum mismatch under a given anode-tocathode voltage and a given gate drive. Then, by inserting an inductance in series with each device, either a saturating inductance or a linear reactance, a minimum mismatch between the two loops could be achieved. The delay time should be specified for the minimum gate drive expected, and the minimum anode-to-cathode voltage to which the devices would be subjected during turn-on for current sharing, because delay time of a device will
lengthen under low anode to cathode forcing voltages and also under low gate current conditions.

In observing the delay time characteristic of the epitaxial diffused device shown in the top of Figure $2-5$, the circuit designer would like to have the gate current rise, with the shortest delay time, well above the triggering sensitivity level of any device that he might use in his circuit before the delay period for the device ends. This technique would help minimize the possible mismatch in gate characteristics and delay times. Generally, if the gate current is designed to supply, under a short circuit, each of the gate circuits a current which rises to about 0.75 ampere in less than 0.5 microsecond, the gate characteristic can be optimized. A rise time to this current level in 0.25 microsecond is even more attractive in terms of reaching an optimum, but this is sometimes impractical due to voltage isolation considerations in the gate circuits.

While on the subject, gate circuit design might be discussed briefly in order to give the circuit designer some tips on ways of achieving the rise times recommended above in a relatively inexpensive manner. The circuit shown in Figure 2-6 serves as a pulse sharpening circuit to give good voltage isolation without requiring the isolation transformer to have high frequency characteristics. In this circuit, the combination of $V_{G}$, and $i_{g}$ for $S C R_{1}$ and $R_{g}$ should be chosen to give a triggering characteristic which is uniform for all combinations of $\mathrm{V}_{\mathrm{G}}, \mathrm{R}_{\mathrm{g}}$ and $\mathrm{SCR}_{1}$ to be used in each of the SCR trigger circuits. Capacitors $\mathrm{C}_{1}$ and resistors $\mathrm{R}_{1}$ act not only as delay circuits to square up the collector


Figure 2-6. Pulse Sharpener Circuit
vs. time characteristic shown, but also as noise suppressors to the gates of the SCRs which are connected in parallel. $\mathrm{R}_{2}$ simply acts as pulse stretchers to stretch out the discharge of capacitors $\mathrm{C}_{1}$ and should be chosen so that there is no discontinuity in the SCR gate triggering characteristic between the discharge of the capacitor and the follow-up of the slower current from the pulse transformer.

Figure 2-7 shows an alternate method of achieving voltage isolation and yet using pulse gating techniques where it may be important, because of a reactive load in the main power circuit, that the gate current be continuous in the SCRs connected in parallel. This can be achieved by supplying a series of gate pulses from two circuits operating alternately and connected through diodes to the same gate. These pulses need not be overlapping or continuous as far as the gate is concerned. A ratio of time-on to time-between-pulses might be about $70 \%$ on, $30 \%$ off for large SCRs, as long as the $30 \%$ off time is well below the turn-off time of the SCR. In the case of devices of 300 ampere rating or more, the off time should probably be kept below about 30 or $40 \mu \mathrm{sec}$. It would not then be normal for the devices to achieve a great deal of recombination during that period of time. If the diodes $\mathrm{RD}_{1}$ are used in the gate circuit for isolation, their turn-on characteristics should be studied by the circuit designer to be sure that they do not effect the gate current rise characteristic. Normally a device doped for fast recovery characteristics will serve well in this type of application.

Figure 2-8 illustrates another means of achieving an additive pulse characteristic and at the same time high voltage isolation. In this case, a simple magnetically coupled multivibrator is used as the pulse generator to provide the power pulsing on the output of a saturating transformer, $\mathrm{t}_{1}$, that is connected to low current SCRs, SCR 1 and $\mathrm{SCR}_{2}$, which are, in turn, pulsed by UJT pulses. The output of these devices, $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ is connected to the high voltage isolation transformer, $\mathrm{t}_{2}$, which, through two squaring networks, is connected to the SCR gates. By controlling the UJT pulses, the pulsing to $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ can be controlled and this provides a relatively high amplification, well isolated means to control the high frequency pulsing to the main SCRs.

If a toroidal transformer is being used, where a square loop material is being employed in the toroid, then it is necessary to provide a reset winding on the transformer; the following type yields the best results in terms of frequency response and isolation in the transformer. In Figure 2-9, the reset winding should be wound on a small section of the toroid, insulated from the metal case, on the opposite side of the toroid from the side where the gate windings are located. The toroid should be wrapped with some insulating material if it is in a metal case, and the first gate winding applied. A second layer of insulation should be wrapped, and then the second gate winding should be wound on top of the first one. The primary winding should then be wound on top of the gate windings with the neces-


Figure 2-7. Multiple Gate Circuits to Achieve Continuous Pulsing




Figure 2-9. Toroidal Transformer with Reset Winding
sary insulation material in-between. This gives an optimum coupling between the gate windings in terms of equalization to the main or primary winding.

## Finger Voltage

Probably the least understood characteristic and certainly one of major importance in high frequency thyristor applications is the finger voltage of the device. The finger voltage characteristic of a thyristor can be seen by observing the trace of the anode-to-cathode voltage vs. time during the operation of the device under a given applied time varying anode voltage and gate drive condition, as in Figure $2-10(\mathrm{~b})$. All thyristors require some minimum anode to cathode voltage (greater than the normal on-state voltage) before they can be triggered into conduction. The reason for this is not fully understood, but it can be explained in terms of the low current, low voltage, saturated gain of the PNP transistor in
the two transistor model which is used to explain the operation of thyristors.

Unless this minimum anode-tocathode voltage (finger voltage) is actually applied to the thyristor, it will not turn on. Figure 2-10(a) shows the V-I characteristic for two thyristors which are perfectly matched except for finger voltage, device A having a lower finger voltage than device B. Forward voltage waveshapes appling to the two devices are shown in Figure 2-10 (b). At time " $\mathrm{t}_{0}$," the thyristors become forward biased and the gate current is applied. However, thyristor A does not begin to conduct until time " $\mathrm{t}_{1}$," and thyristor B conducts later at time " $\mathrm{t}_{2}$." Therefore, if thyristors A and B are connected directly in parallel, thyristor $B$ will never see a high enough voltage to turn on. From this, it can be seen that the specification of finger voltage is a critical requirement in very low voltage applications.


Figure 2-10. Finger Voltage

In higher voltage applications, finger voltage can be an important parameter where parallel thyristors are to be gated just before, or at the time, the thyristor becomes for-ward-biased. It is possible to minimize the effects of finger voltage in two ways. First, by ensuring that gate current is not applied to the thyristors until the supply (anode-to-cathode) voltage has risen above the maximum finger voltage level. Second, by including an inductor in series with each thyristor, with sufficient voltsecond capability to ensure that all thyristors have more than the finger voltage before the inductors saturate.

This finger voltage characteristic is most pronounced in high voltage devices (thyristors processed from high resistivity silicon with wide base regions). If this characteristic were not measured and matched for
a group of thyristors to be connected in parallel, and should one device possess a much higher finger voltage than another, the device with the high finger voltage might never turn on fully.

All major manufacturers of devices understand this characteristic well enough to measure it under given anode-to-cathode voltage and gate drive conditions and to specify a match so that the circuit designer can then include sufficient loop inductance in the individual thyristor loops to equalize the voltage under a worst match condition. Usually any linear or nonlinear inductance used in the individual thyristor loops to help equalize the turn-on characteristics, the mismatch due to delay mismatch, and to minimize the turn-on inrush of anode current differences due to equalization characteristic differences, is suffi-
cient to equalize the finger voltages between devices, so long as this voltage has been tested and reasonably well matched among the individual thyristors.

## Latching and Holding Current

The next characteristic, "Latching and Holding Current," is important to understand, because the two are not the same, and also they are important in terms of successful turn-on of a thyristor with a given gate drive. The "holding current" is that minimum on-state current that sustains the device current conduction following operation at some nominal level of conduction current. The "latching current" is the minimum on-state current needed to keep the device in the onstate after the trigger pulse has been removed. Generally, the latching current is two to four times the holding current for a given device. The holding current is important in an inductive circuit where, after a gate pulse is applied to a device and it has turned on successfully, some disturbance in the load temporarily diminishes the anode current of the thyristor. If this anode current should fall below the holding current the device may turn off. If subsequently the load demands more current, the load current will be found to have been discontinued, unless an additional gate pulse is supplied to the thyristor to turn it on again.

It is important that a thyristor reach the latching current level before the initial gate pulse is removed from the thyristor or else it may turn back off again and never reach full conduction. In a circuit where devices are being paralleled and their gates are being supplied
with gate pulses, this latching current level is important to know for a given set of devices to insure that all of the devices will turn on and stay on, once the gate pulses are removed. This characteristic is also important where an inductance is being inserted with each thyristor in a parallel circuit, so that with a given anode-to-cathode voltage supplied to the device, the required duration of the gate pulse can be obtained by the following simple relationship:

Latching current and holding current decreases with temperature increase, as the gate current increases, and as the applied anode voltage increases. Therefore, the measurements chosen for a given circuit should be chosen carefully to match up with the worst case device characteristics in terms of the circuit conditions to which the device will be subjected.

## Steady-State Conditions

Once all of the transient sharing conditions mentioned to this point are satisfied, the matter of steadystate conditions must be considered in terms of paralleling the devices. The primary consideration is the on-state voltage of the device. In order for devices to equally share load current, the drops across parallel paths must be equal. Even if an inductance is inserted in series with the thyristor, a mismatch in the steady-state equalized on-state voltages of the thyristors could cause a mismatch of current.

It is important to specify the maximum anode current expected in the thyristor under the worst operating condition at which the devices are expected to share equal-
ly and also the maximum temperature at which this current can occur. This, then, will guarantee that once the devices are matched at this level, they will be matched under the worst case condition.

An additional consideration, when considering Hockey-Puk type devices, is the thermal resistance of the device. When Hockey-Puks are connected for parallel operation, they should be mounted using the maximum allowable mounting force in order to minimize the thermal resistance differences from one device to another. If the thermal resistances between the internal pole pieces and the junctions are different, even if the on-state voltages are closely matched at a given junction temperature, the junction temperatures from one device to another could vary because of different abilities to transmit heat and therefore the desired match in onstate characteristics might never be obtained.

## Loop Inductance

With all of these device characteristics taken into consideration, the last item to consider (but by far not the least) is the loop inductance in the thyristor arrangement. Obviously, any time a group of large devices is to be connected in parallel, it is difficult to get the current in and out of the thyristor packages and equalize the inductances in each current carrying loop. Proximity of ferrous materials or other conductors to the bus-bars coming to and from the individual thyristors can affect the magnetic fields and therefore can change the apparent inductance. Differences in spacing between conductors and incoming and outgoing bus-bars can also
change this inductance. Various methods have been used in the past to provide forcing of current in this type of loop. One method is shown in Figure 2-11, and discussed in Reference [1]. In this case, a series of current balancing reactors are connected as shown, in order to force current sharing during the initial period of conduction in each circuit. This method is used infrequently in today's circuit designs, because of the high cost of the core material and the expense involved in paralleling multiple devices.


Figure 2-11. Thyristor Assembly [1]
A second approach is to use a linear reactor in series with each device and to go through the exercise of specifying the devices under the limitations previously discussed in this section and choosing the magnitude of the inductance to satisfy those conditions outlined.

A third system which is used quite effectively is to use a delay reactor in series with each thyristor to provide the same sort of inductive function as mentioned above but to minimize the size of the reactor by minimizing its voltsecond capacity.

Of equal importance with the choice of type of magnetic device used for equalization is the mechanical arrangement of the thyristors in the system. For instance, two possible mechanical configurations are shown in Figures 2-12 and 2-13 with the expected current sharing per leg in each thyristor branch shown on the accompanying graphs [2]. The contrast between a straight-through, bus-bar assembly as shown in Figure 2-12, with the resulting $20 \%$ mismatch between the maximum and nominal current per device and that in Figure 2-13
shows how some slight variations in bus-bar configuration can have significant effect upon the number of devices necessary to carry a given amount of current or on the maximum expected mismatch between parallel connected devices. In this case, the ac bus-bar loops shown in Figure 2-13 change the inductance in the center of the construction, thus varying the amount of mismatch across the assembly.

Another technique that has been used successfully to minimize this mismatch in inductance per diode path is shown in Figure 2-14. If the system can be connected in a cylindrical manner, then, theoretically, the inductance becomes more nearly equalized until finally there would be no apparent mismatch due to construction variations or mismatch in inductive loops from one device to another. The degree


IN-LINE THYRISTOR ASSEMBLY


Figure 2-12. In-Line Thyristor Assembly and Current Curve


Figure 2-13. Improved In-Line Thyristor Assembly and Current Curve
to which these techniques can be applied in a given application depends upon the constraints to which the circuit designer is required to work.

It has been the aim of this chapter to point out the various con-
straints to consider in application of high-current thyristors in a parallel configuration in order to obtain a successful design using a minimum number of devices with the maximum expected reliability.


Figure 2-14. Cylindrical Paralleling Assembly

## References

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4. J.H. Galloway, "Harmonic Line Currents in Large Thyristor Six Pulse Converters," the Udylite Co.
5. "SCR Handbook," Second Edition, International Rectifier.
6. D. Bewley, "Methods of Achieving Balance in Diode Type Rectifiers," AIEE Conference Paper, January, 1963.
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## Series Operation

Although SCRs are available in voltage ratings in thousands of volts, it is often necessary to connect them in series in order to block higher voltages than any available individual SCR can handle. In such cases, there are several requirements to take into account in order to assure proper and safe operation of the semiconductor devices. The general topics to be considered, and which are covered in the following sections are equalization and triggering. Equalization of off-state and reverse (leakage) current of the devices will be taken into account as will equalization of the recovered charge. Reliable triggering of devices connected in series will be discussed. This section will consider the delay time differences in devices and the differences between the various capacitances to ground, or neutral. Also, some general triggering methods will be considered which can lead to an easy solution of series triggering problems.

## Equalization

The two characteristics to take into consideration under this heading are elevated temperature blocking characteristics of the SCRs and their recovery characteristics. In each case, the difference in characteristics from one device to another must be considered.

If we were to examine two oscilloscope traces of anode blocking current vs. anode voltage for two different SCRs of the same family
at a given junction temperature, we might observe traces similar to those shown in Figure 3-1. For either a positive or a negative voltage applied to the SCRs, the leakage currents at a given temperature at that voltage are somewhat different. Obviously, if we were to connect these two devices in series and begin to apply voltage either in the reverse or off-state direction on the series combination, $\mathrm{SCR}_{2}$ would begin to take the majority of the applied voltage, since its leakage at any applied voltage in either direction is lower than that of $\mathrm{SCR}_{1}$. Although the voltage-current characteristics are nonlinear for these devices, they would, at any given condition, divide voltage in inverse proportion to their leakage currents. Therefore, if we were to try to connect these devices in series and at the same time force them to more equally share the applied voltage, a method to force this sharing would be to connect a resistor in parallel with each device as shown in Figure 3-2.

One method for equalization would be to vary the value of the resistance dependent upon whether the SCR was a high or low leakage device. We would, therefore, have unequal resistances down the string of a number of SCRs connected in series. However, this is in general not a practical approach to circuit design, and, therefore, one would like to determine some value of resistance that would be suitable for connection in parallel with any


Figure 3-1. SCR Blocking Characteristics


Figure 3-2. Resistor Equalization of Blocking Voltage

SCR of a given family. In order to do this, it's necessary to know certain characteristics of both the application and the devices to be used.

The first thing to know is what is the maximum voltage to be applied to the circuit; the second is
what is the maximum allowable voltage for any given device; the third is the minimum applied voltage for any given device. In other words, what is the maximum mismatch that the circuit designer wishes to see as he checks voltage across the series string with full voltage applied to it.

For instance, let's say we have a 4000 V supply voltage and we would like to have a $2: 1$ redundancy or safety factor in the voltage rating of the devices. Therefore, we would choose devices whose total voltage capability equaled 8000 V . Let's also say that we have 2200 V SCRs available for the application. We would, therefore, decide that nominally we would want to connect four 2200 V devices in series. Let's also assume we've decided that the maximum voltage we want
any device to see is 2100 V , and the minimum voltage we want any device to see is 1900 V . Therefore, the difference between the maximum and minimum applied voltage on any given cell is 200 V . In addition, we look at leakage current at the maximum allowable operating junction temperature for the devices (in general, this is given as $125^{\circ} \mathrm{C}$ ) and find that the maximum peak blocking current at 2000 V is 20 mA .

The minimum peak blocking current for any given device of this family is not a characteristic generally given by SCR manufacturers. To be safe, one could assume that this value of blocking current was zero; however, this would lead to an extremely conservative design. The best way to determine this value is to contact the manufacturer, describe the application and ask for some minimum blocking current value at the maximum temperature that could be expected or guaranteed by that manufacturer in any devices delivered. Let's assume that this value is 5 mA . The difference then, between the maximum blocking current and the minimum blocking current at a given temperature with approximately the designed applied voltage is 15 mA . We then have enough information to calculate the required equalization resistance.

A derivation of the relationship between this difference in blocking current, allowable difference in voltage, and equalization resistance is given in Formula 3-A and Figure 3-3.
Assume:
$\mathrm{E}_{1}+\mathrm{E}_{2}+\mathrm{E}_{3}=\mathrm{E}_{\mathrm{T}}$
$\mathrm{E}_{1}<\mathrm{EMAX}^{2}$
$\mathrm{E}_{2}=\mathrm{E}_{\text {MAX }}$
$\mathrm{E}_{3}<\mathrm{EMAX}_{\mathrm{MAX}}$
$\triangle E=E_{2}-\mathrm{E}_{1}$


Figure 3-3. Voltage Equalization Network

Therefore:
$\mathrm{I}_{1}-\mathrm{I}_{2}=$ Maximum Leakage Difference $=\Delta I$
$\frac{E_{1}}{R_{E}}+I_{1}=\frac{E_{2}}{R_{E}}+I_{2}=\frac{E_{3}}{R_{E}}+I_{3}$
$\frac{E_{1}}{R_{E}}+I_{1}=\frac{E_{2}}{R_{E}}+I_{2}$
$\frac{\mathrm{E}_{1}}{\mathrm{R}_{\mathrm{E}}}+\Delta \mathrm{I}=\frac{\mathrm{E}_{2}}{\mathrm{R}_{\mathrm{E}}}$
$\Delta I R_{E}=E_{2}-E_{1}$
Therefore:
$R_{E}=\frac{E_{2}-E_{1}}{\Delta_{I}}=\frac{\Delta E}{\Delta_{I}}$
Where:
$\mathrm{E}_{\mathrm{T}} \quad=$ Voltage to be blocked by String
$\mathrm{E}_{\mathrm{MAX}}=$ Maximum Voltage
Allowed per Device
$\mathrm{R}_{\mathrm{E}}=$ Equalization Resistance
Using this derived formula, the equalization resistance for the previous example, with $\triangle \mathrm{E}=200$ volts and $\triangle \mathrm{I}=15 \mathrm{~mA}$, is $200 \div 15 \times 10^{-3}$ or 13.3 thousand ohms. This is unquestionably a conservative figure for equalization resistance. A worst case example for leakage differences has been taken into ac-
count. The maximum allowable operating temperature for the device has been used to calculate or measure the leakage of the worst case SCR, and, therefore, the resistance actually required in the given application can often be larger than that derived by this formula. This is important as a consideration in the circuit design, because dissipation in this resistor in very high voltage applications can be extremely high and, therefore, costly and limiting in the design.

Another point worth noting in considering this simple approach to choosing the equalization resistance is that unidirectional conducting thyristors have a slightly higher blocking current at a given blocking voltage and temperature in the offstate direction than in the reverse direction. Stating it another way, they have a higher blocking capability in the reverse direction than in the off-state direction. In certain applications, this can be taken into account in designing equalizing networks for series SCR strings if the application is such that the reverse voltage applied to the system is higher than the forward voltage applied.

The next consideration is to determine the power dissipated in the equalization resistor. This is given

(a) RECTANGULAR VOLTAGE WAVESHAPE
by the expression shown in Formula 3-B. Although this seems to be a very simple relationship, for some applications it can be misleading.

$$
\begin{equation*}
\mathrm{W}=\frac{\left(\mathrm{E}_{\mathrm{MAX}}^{\mathrm{RMS}}\right)^{2}}{\mathrm{R}_{\mathrm{E}}} \tag{3-B}
\end{equation*}
$$

For single phase applications, the applied voltage vs. time on a given equalizing resistor may be very close to being sinusoidal and, therefore, the maximum RMS voltage is easily determined and the power dissipated in the resistor can be calculated. However, in applications where the reverse voltage is not sinusoidal, the circuit designer should be careful to determine the maximum RMS voltage applied to any of the equalization resistors. For a rectangular voltage waveshape, as shown in Figure 3-4(a), Formula 3-C states that the RMS voltage is equal to the square root of the duty cycle times the peak voltage. This, then, reduces Form ula 3-B to the expression shown as Formula 3-D.
$\mathrm{E}_{\text {RMS }}=\sqrt{\text { Duty Cycle }} \times \mathrm{EMAX}_{\text {(3-C) }}$
Where:
Duty Cycle $=\frac{t_{1}}{t_{1}+t_{2}}$

(b) SAWTOOTH VOLTAGE WAVESHAPE

Figure 3-4. Voltage Waveshapes
$\mathrm{W}=\frac{\text { Duty Cycle } \mathrm{x}\left(\mathrm{E}_{\mathrm{MAX}}\right)^{2}}{\mathrm{R}_{\mathrm{E}}}$
Formulas 3-C and 3-D apply only in the square wave case. Similar expressions can be derived for other waveshapes; for instance, for a sine wave application of varying duty cycle, the dissipation is given by Formula 3-E.
$\mathrm{W}=\frac{\text { Duty Cycle } \mathrm{x}\left(\mathrm{E}_{\mathrm{MAX}}\right)^{2}}{2 \mathrm{R}_{\mathrm{E}}}$
For a sawtooth application as shown in Figure 3-4(b), Formula $3-F$ gives the expression for the dissipation.
$\mathrm{W}=\frac{\text { Duty Cycle } \mathrm{x}\left(\mathrm{EMAX}^{2}\right)^{2}}{3 \mathrm{RE}_{\mathrm{E}}}$
Where:
Duty Cycle $=\frac{t_{1}}{t_{1}+t_{2}}$
Another point in choosing the equalization resistor is to be careful about the type of resistor used. In the case where the voltage applied rises very sharply and the voltage per resistor is rather high, it is often wise to consider the crowding effects that can take place in a resistor. For these applications, bulk type resistors, for instance some of the noninductive bulk types, are advisable for reducing to a minimum difficulties with corona discharge in the resistor or nonlinear resistance characteristics with time. Another type of resistor that can be used here is a film type wound on a stable type of mandrile, such as glass. In most phase control applications, normal wirewound, vitreous enamel, power-type resistors are generally acceptable.

In general, when using an SCR or a triac, the circuit designer will connect a series RC combination in parallel with the SCR or triac to minimize the $\mathrm{dv} / \mathrm{dt}$ applied to the device and therefore to prevent turn-on of the SCR during high rates of rise of applied circuit voltage. In the case of series connected SCRs, however, this network accomplishes a dual purpose. Because of carrier recombination in a semiconductor after on-state (forward) conduction, the semiconductor exhibits a reverse recovery phenomenon. If an SCR has been conducting forward current and then at some period later it is back-biased, it will exhibit a recovery characteristic similar to that shown in Figure 3-5. There is, then, a period of time between the application of the reverse voltage to the SCR and the ability of the SCR to block that reverse voltage. This characteristic varies somewhat as a result of varying the peak current through the


Figure 3-5. SCR Recovery Characteristics
device during conduction, the declination rate of that current (the declination di/dt), and the junction temperature of the device.

The recovery characteristic also varies from one device to another, even in a manufacturing process. Two devices from a given manufacturing lot with the same rating might show recovery characteristics as shown in Figure 3-6. If we were to integrate this recovery current over the recovery time, we would get the expression for recovered charge, Q. Subtracting the integrals for Q for the two devices, we would get an expression for the difference in stored charge of the two SCRs, $\triangle \mathrm{Q}$. This is shown in Formula 3-G.

$$
\begin{aligned}
& \text { QSCR1 }=\mathrm{t}_{0} \int \mathrm{t}_{1} \text { isCR1 } 1 \mathrm{dt} \\
& \text { QSCR2 }=\mathrm{t}_{0} \int{ }^{\mathrm{t}} 2 \text { isCR2 } \mathrm{dt} \\
& \triangle \mathrm{Q}=\text { QSCR } 2 \cdot \text { QSCR1 } \\
& =t_{0} \int \mathrm{t}_{2} \text { iSCR2 } \mathrm{dt} \text {. } \\
& =\mathrm{t}_{0} \int \mathrm{t}_{1} \text { iSCR1 } \mathrm{dt}
\end{aligned}
$$



Figure 3-6. Recovery Characteristics of two Similar SCRs

Shown in Figure $3-1(\mathrm{a})$ is a series connection of the two SCRs used in the derivation of Formula 3-G, together with their steady-state equalization resistances and some series impedance in the circuit shown as "L". If a voltage were applied to this combination, the two devices would share voltage in a fashion similar to that shown in Figure $3-7$ (b). The resultant voltage sharing under these conditions with no external means of forcing equalization of the recovery characteristics may not be acceptable.

A means of forced sharing of the blocking voltage is to connect a series combination of a resistor, $\mathrm{R}_{\mathrm{S}}$, and capacitor, $\mathrm{C}_{S}$, across each device as shown in Figure 3-8. In this way, the recovered charge of the parallel combination of $\mathrm{R}_{\mathrm{S}}, \mathrm{C}_{\mathrm{S}}$, and SCR is equivalent to all other parallel combinations in the series string. The size of $R_{S}$ and $C_{S}$ in this network is generally determined by the amount of $\mathrm{dv} / \mathrm{dt}$ suppression to be accomplished for the device as well as the needed equalization of recovered charge to force voltage sharing. The size of $\mathrm{R}_{\mathrm{S}}$ is also determined by series impedance, the type of application, and the allow able inrush current imposed on the SCR during turn-on. The size of the capacitor, $\mathrm{C}_{\mathrm{S}}$, is determined by the required $\triangle Q$ equalization of the two devices. If additional capacitance is required for $\mathrm{dv} / \mathrm{dt}$ suppression, the capacitor can be increased in size, with no harmful effect on the sharing of blocking voltage.

The relationship between $\triangle Q$, the difference in recovered charge from one device to another, $\Delta V$, the allowable difference in sharing voltage during the reverse recovery of the devices and $\mathrm{C}_{\mathrm{S}}$, the capacitance

(a) CIRCUIT

(b) WAVEFORMS

Figure 3-7. Series Connection with No Equalization Capacitor


Figure 3-8. Series Connection with $R$-C Equalization
needed for equalization, is given in Formula $3-\mathrm{H}$. The capacity selected should be able to operate on alternating voltage without overheating.

Capacitors should also be a type, such as extended foil, having minimum inductance.

$$
\begin{equation*}
C=\frac{\Delta Q}{\Delta V} \tag{3-H}
\end{equation*}
$$

Where:
$\Delta Q=$ Difference in recovered charge $\Delta \mathrm{V}=$ Allowable blocking voltage differences C = Equalization capacitor

Table III-I gives typical recovered charge for a number of types of SCRs. As an example, if the series string of devices used in the previous example had a $\triangle Q$ of 50 microcoulombs and the allowable difference in sharing voltage was given as 200 V , then the capacitance

Table III-I. Range of Recovered Charge for Various IR SCRs
$\left.\begin{array}{|c|c|c|}\hline & \begin{array}{c}\text { TYPICAL RANGE OF } \\ \text { RECOVERED CHARGE, } \\ \text { AT 1250C,25A/ } \mu \mathrm{S}\end{array} & \\ \text { ( } \mu \text { COULOMBS) }\end{array}\right)$
necessary for equalization under these conditions would equal 0.25 microfarads, as shown in Formula 3 -J.
$\mathrm{C}=\frac{50 \times 10^{-6}}{200}=0.25 \mu \mathrm{~F}$
Where:
$\triangle \mathrm{Q}=50$ microcoulombs
$\Delta \mathrm{V}=200 \mathrm{~V}$
In high dv/dt circuits, the resistor should be chosen so that the RC circuit is overdamped. In this way, the capacitor will not charge to a voltage above its proper sharing voltage. Again, the resistor should be chosen to be of a bulk type or of a film type wound on a stable core such as glass. The capacitor should have minimum inductance in this type of circuit and therefore should be of extended foil construction and, since there can be a considerable amount of power dissipation in the capacitor, it should be oil-filled.

## Triggering Series-Operated SCRs

Under series operation, the gates of the various devices will be at considerable potential above neutral or ground in the circuit. Most triggering circuits are low voltage, low energy-level circuitry and the capacitance to ground or to neutral in these circuits may vary widely from one SCR to another.

Another consideration is the variation in delay time from one SCR to another. When using pulse transformers, it should be noted that the insulation between windings must be able to support the voltage from that point in the circuit to the lowest reference potential point, and this is often the peak voltage in the system. Devices connected in series should be chosen to have delay times closely matched so that differences in the turn-on characteristics are minimized. The importance of this is illustrated in Figure $3-9$ where, even though the two delay times are very close in the two SCRs, it is important for the gate signal rise time to be much shorter than the delay time in order to minimize the difference in turnon characteristics of the two devices. In this case, the anode voltage of $\mathrm{SCR}_{1}$, which has a longer delay time than $\mathrm{SCR}_{2}$, increases, since $\mathrm{SCR}_{2}$ begins to turn on sooner. The RC network in the system helps to equalize this if there is series impedance in the circuit, since it tends to minimize the rate-of-rise of applied voltage on any part of the circuit.

The gate circuit of Figure 3-10 can be used to minimize difference in turn-on characteristics of SCRs in a series string. This gate circuit will transform a slow rising square


Figure 3-9. Delay Time Effect on Series SCRs
wave into a trigger signal with both a fast rise time and a current overshoot on the leading edge, both desirable qualities for triggering series SCRs.

It is often necessary, because the load is either an active load or an inductive load, to make the trigger pulse to the SCRs either continuous over a $180^{\circ}$ conduction angle of the supply voltage or a series of pulses which are spaced so no appreciable recovery in the SCR takes place between pulses. A suitable gate circuit for this type of opera-
tion is shown in Figure 3-11. In this gate circuit, a blocking oscillator is triggered by a high frequency clock. The resultant series of pulses is then amplified by a power transistor and used to trigger the series string of SCRs.

The gate circuit of Figure 3-12 combines the qualities of a fast rise time gate current to minimize delay time effects and a wide pulse for inductive loads.

Interwinding capacitance of conventional pulse transformers may be prohibitive for series operation


Figure 3-10. Fast Rise Time Trigger Circuit
of SCRs when high rates of rise of voltage are encountered. High dv/dt can induce currents to flow in the interwinding capacitance, which may falsely trigger an SCR. This problem can be avoided by the use of optical couplers to provide extremely high voltage isolation between trigger circuits of series connected SCRs. The gate circuit of Figure 3-13 uses a light emitting diode (LED) and photo-sensitive SCR to provide optical isolation for each main SCR.

Another method for triggering series-connected SCRs is to trigger one gate and arrange for the other gates to trigger "sympathetically" by use of a slave triggering circuit arrangement.

The slave triggering method eliminates the need for multiple, isolated outputs from a powerful triggering circuit. One such method is shown in Figure 3-14. Resistors $R_{1}$ and $R_{2}$ are voltage equalizing resistors. Capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$, with their damping resistors $\mathrm{R}_{3}$ and $\mathrm{R}_{4}$, provide additional voltage equalizing under ac conditions, and also provide transient suppression.

When the controlled rectifier $\mathrm{SCR}_{2}$ is triggered, its anode-tocathode voltage drops abruptly to a low value. This results in a surge of charging current into capacitor $\mathrm{C}_{3}$ and through the gate of controlled rectifier $\mathrm{SCR}_{1}$, which is turned-on. Resistor $\mathrm{R}_{5}$ should be about ten times the gate-to-cathode resistance of the controlled rectifier.


Figure 3-11. Pulse Train Trigger Circuit

The rectifier diode $\mathrm{RD}_{1}$ acts as a clamp to prevent the gate of its controlled rectifier from being made negative during the negative half cycles when the gate capacitor is charged in the reverse direction. Capacitor, $\mathrm{C}_{3}$, must be large enough to assure reliable triggering, but if it is made too large, it may cause turn-on as a result of its charging current, due to the forward voltage. Hence, the size of this
capacitor must fall between two limits given by Formula $3-\mathrm{K}$.
$\frac{10^{6}}{12.6 \times \mathrm{fx} \mathrm{R}_{\mathrm{S}} \times \mathrm{V}_{\mathrm{pt}}}>\mathrm{C}_{3}$
$>\frac{I_{G T}}{10^{7}}$
Where:
f = frequency of ac supply
$\mathrm{I}_{\mathrm{GT}}=$ maximum gate current required to trigger
$\mathrm{V}_{\mathrm{pt}}=$ maximum peak forward or reverse voltage applied across the series string of two controlled rectifiers
$\mathrm{C}_{3}=$ triggering capacitance (microfarads).

The purpose of capacitor $\mathrm{C}_{4}$ is to provide a low impedance source of voltage during the period required to trigger $\mathrm{SCR}_{1}$. Because of the shunting capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$, this additional capacitor is usually not needed.

An improved slave triggering circuit is shown in Figure 3-15. Here, the triggering capacitors also serve the function of transient suppression; furthermore, the clamping diodes are breakdown diodes, selected to limit the forward voltage applied to the gates, as well as to clamp them to the cathode for reverse voltage. Resistors $\mathrm{R}_{7}$, R8, and Rg are selected to limit gate current during triggering and also to limit the rate at which capacitors $\mathrm{C}_{1}, \mathrm{C}_{2}$, and $\mathrm{C}_{3}$ discharge through each associated SCR (di/dt) when the SCRs trigger on. The gate pulses


Figure 3-12. Combined Fast Rise Time and Wide Pulse Trigger Circuit


Figure 3-13. Optically Coupled Series SCRs
may be applied between any gate and cathode, and all the controlled rectifiers will turn on; usually it is most convenient to apply the pulses in the manner shown.

Another slave triggering circuit is shown in Figure 3-16. This circuit is very simple, but selection of the resistor and capacitor is much more critical, since no protection is pro-
vided against applying excessive voltage, current or power to the gate of the "slave" controlled rectifier. Whereas the circuit of Figure 3-15 operates satisfactorily under many different circumstances, the circuit of Figure 3-16 must be tuned to a narrow range of favorable conditions with the probability of failure when these conditions are not maintained.


Figure 3-14. Slave Triggering Circuit

A wide variety of series SCR assemblies have been manufactured by International Rectifier. The photo of Figure 3-17 shows Hockey-Puk SCRs arranged with six legs in parallel. Each leg consists of two AC switches in series, for a total of 24 SCRs.

Figure 3-18 shows a cylindrical configuration of seven strings of 150 ampere stud SCRs in parallel. Each series string consists of 12 watercooled SCRs in series. Current balancing reactors are included to assure sharing of current among the parallel legs.

The half-wave assembly of Figure 3-19 consists of 13 SCRs in series. Gate and auxiliary cathode wiring is not shown for the sake of clarity.


Figure 3-15. Improved Slave Trigger Circuit


Figure 3-16. Economical Slave Trigger Circuit


Figure 3-17. Series-Connected Hockey-Puk SCRs in Liquid-Cooled Assembly

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Figure 3-18. Series-Connected, Stud-Mounted SCRs in Liquid-Cooled Assembly

\& ฯ'LIdVHD
Figure 3-19. Series-Connected, Hockey-Puk SCRs in Half-Wave Assembly


## AC Phase Control

Solid-state ac controllers take many forms. They may be used simply for on-off switching, in which case triggering the semiconductor device(s) at essentially zero voltage on the ac wave will minimize radio frequency interference (RFI). On the other hand, by employing phase controlled triggering the ac controller may be used to adjust the voltage applied to the load and so perform such functions as ac motor speed control or adjusting the direct voltage output from a rectifier fed by a transformer having a solid-state controller on the primary.

A number of circuit configurations are possible; two popular ones for single-phase applications are two SCRs connected in anti-parallel, or a single triac, which functionally replaces two SCRs.

Mechanical configuration requirements differ greatly for various controller applications. In the smaller current ratings, PACE/pak assemblies which simplify installation and cooling may be considered. For larger ratings, assemblies in which the rectifying devices are mounted on extruded aluminum heat exchangers are popular. For some industries, notably the resistance welding industry, where cooling water is readily available and space and weight limitations are severe, water-cooled assemblies are popular.

## PHASE CONTROL CIRCUITS

A number of circuits are available for controlling alternating volt-
age with thyristors. Reverse blocking thyristors may be connected in anti-parallel, or a single-phase bridge may be used to rectify the ac line current, so that one thyristor can control both halves of the ac wave; this is accomplished by replacing the dc load on the single phase bridge with a short circuit and locating the load in the ac line. In some polyphase circuits, essentially the same control of voltage can be obtained when one thyristor is replaced with a rectifier diode. This arrangement is more economical. A number of possible circuit configurations are shown in Table IV-I.

In addition, the same kind of control can be provided by a triac, since it can be triggered into conduction during either half of the ac wave. In Table IV-I, a triac may be used in place of many of the allthyristor and thyristor-diode control circuits shown, within the current ratings available.

When the load is inductive, current flows as a sine wave which lags the supply voltage by the angle $\theta$, the angle which is a measure of the power factor. If each thyristor is triggered at this angle, load current will be unaffected. If the triggering angle is made to lag behind $\theta$, the load current will flow as a series of nonsinusoidal pulses of less than 180 electrical degrees duration.

As the angle of phase retard is increased, these pulses become increasingly shorter until, at 180 degrees retard, they cease to exist, and the voltage across the load is

Table IV-I. Thyristor Circuit to Control AC Loads

| CIRCUIT | RELATIVE POWER OUTPUT | $\begin{aligned} & \text { TYPE } \\ & \text { OF } \\ & \text { LOAD } \end{aligned}$ | CONTROL RANGE \% | TYPICAL USES | APPLICABLE MODES OF CONTROL | SEE NOTES |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $1 \mathrm{~A}$ | 1 | Resistive only | 50 to 100 | Low Power Heater Loads Lamp Intensity Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{aligned} & 1 \\ & 2 \\ & 3 \\ & 4 \end{aligned}$ |
| 2A | 0.7 | Resistive or with low inductance | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Motor Speed Control (Induction or Universal) | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 2 3 4 |
| 3 A | 1 | Resistive or Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control Motor Speed Control (Induction or Universal) Transformer Primary Control Solenoid Pull Control AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 3 4 |
| 4A | 1 | Resistive or Inductive | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heater Control <br> Lamp Intensity Control Motor Speed Control (Induction or Universal) Solenoid Pull Control AC Magnet Control On Load Tap Changing | SWC <br> PC <br> PBM | 3 4 5 6 |
| 5A | 1 | Resistive or Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control Motor Speed Control (Induction or Universal) Transformer Primary Control Solenoid Pull Control AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 3 |
| 6A | 1 | Resistive or Inductive | $\begin{aligned} & \% \tau_{1} \text { to } \\ & 100 \end{aligned}$ | Heater Control <br> Lamp Intensity Control Motor Speed Control (Induction or Universal) Solenoid Pull Control AC Magnet Control On Load Tap Changing | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 3 4 5 6 |
|  | $1.73$ $1.73$ | Resistive or Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Motor Speed Control (Induction) <br> Transformer Primary Control Solenoid Pull Control AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 3 4 7 |
|  | $1.73$ $1.73$ | Resistive or Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Motor Speed Control <br> (Induction) <br> Transformer Primary Control Solenoid Pull Control AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{aligned} & 2 \\ & 3 \\ & 4 \\ & 7 \\ & 8 \end{aligned}$ |
|  | 3 | Resistive or Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Motor Speed Control <br> (Induction) <br> Transformer Primary Control <br> Solenoid Pull Contral <br> AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | 3 <br> 10 |

Table IV-I. Thyristor Circuits to Control AC Loads (Continued)

| CIRCUIT | RELATIVE POWER OUTPUT | TYPE OF LOAD | CONTROL RANGE \% | TYPICAL USES | APPLICABLE MODES OF CONTROL | $\begin{array}{\|c\|} \text { SEE } \\ \text { NOTES } \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 1.21 | Resistive or Slightly Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Transformer Primary Control (when load has high power factor) <br> Note: If load is connected $\Delta$, a third diode-thyristor control unit is required in the third line. | SWC PC PBM | $\begin{array}{r} 3 \\ 4 \\ 8 \\ 11 \end{array}$ |
| $13 \mathrm{~A}$ | 1.21 | Resistive or Slightly Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control Transformer Primary Control (when load has high power factor) <br> Note: If load is connected $\Delta$, a third diode-thyristor control unit is required in the third line. | SWC PC PBM | $\begin{array}{r} 3 \\ 4 \\ 8 \\ 11 \end{array}$ |
| $14 \mathrm{~A}$ | 2.1 | Resistive or Slightly Inductive | 0 to 100 | Heater Control <br> Lamp Intensity Control Transformer Primary Control (when load has high power factor) | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{array}{r} 3 \\ 4 \\ 10 \end{array}$ |
|  | 2.1 | $\begin{aligned} & \text { Resistive } \\ & \text { or } \\ & \text { Inductive } \end{aligned}$ | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heater Control <br> Motor Speed Control <br> (Induction) <br> On Load Tap Changing | swc PC PBM | $\begin{gathered} 3 \\ 4 \\ 5 \\ 6 \\ 10 \\ \\ \text { for } Y \\ \text { Conn. } \\ \text { Load } \\ 7 \\ 11 \\ 12 \end{gathered}$ |
| $16 A$ | 1 | Resistive or Inductive (Inductance in RA only) | Depends on Ratio $R_{A}: R_{B}$ | Heater Control Lamp Intensity Control Transformer Primary Control (Transf. Winding replaces RA) Induction Motor Speed Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{array}{r} 3 \\ 4 \\ 13 \end{array}$ |
|  | 3 | Resistive or Inductive (Inductance in R $\mathrm{R}_{\text {only }}$ ) | Depends on Ratio $\mathrm{R}_{\mathrm{A}}: \mathrm{R}_{\mathrm{B}}$ | Heater Control <br> Lamp Intensity Control <br> Transformer Primary Control (Transf. Winding replaces $\mathrm{R}_{\mathrm{A}}$ ) Induction Motor Speed Control Wound Rotor Induction Motor Speed Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{array}{r} 3 \\ 4 \\ 11 \\ 13 \end{array}$ |
|  | 1.73 | $\begin{aligned} & \text { Resistive } \\ & \text { or } \\ & \text { orductive } \end{aligned}$ | 0 to 100 | Heater Control <br> Lamp Intensity Control <br> Motor Speed Control (Induction) <br> Transformer Primary Control Solenoid Pull Control AC Magnet Control | $\begin{aligned} & \text { SWC } \\ & \text { PC } \\ & \text { PBM } \end{aligned}$ | $\begin{array}{r} 1 \\ 2 \\ \hline 14 \end{array}$ |

## Table IV-I. Thyristor Circuits to Control AC Loads (Continued)

## 1) All Circuits

Pulse burst modulation is applicable only to the control of heating element loads where substantial thermal inertia exists.
2) All Circuits

Zero voltage switching may be employed advantageously to supplement pulse burst modulation control and eliminate RFI resulting from steep wavefronts common to phase control modes.
3) Circuit 1 A

Used only for low power loads, operating directly from distribution systems where unbalance between positive and negative half cycles is not detrimental.
4) Circuit 1 A

Can be used also to control the speed of small universal motors.
5) Circuits 4A, 6A, 14A

The switching mode between two transformer taps is useful for both phase control and pulse burst modulation control, especially for heating elements. Tap $\mathrm{T}_{1}$ is selected to provide slightly less than the minimum required power input; then, either phase control or pulse burst modulation can be used to add the necessary incremental extra power to obtain fine control and with a minimum fluctuation of heater element temperature, resulting in longer element life. In addition, less waveform distortion is introduced than when either type of control switches from zero to full voltage (as in Circuits 2A, 3A, 4A, and 6A through 12A).
6) Circuits 4A, 6A, 14A

In circuits similar to $4 A$, additional taps between $T_{1}$ and $T_{2}$ also may be used provided that an anti-parallel pair of thyristors is added for each tap. This mode of operation permits tap changing under load, either by switching from tap to tap or, when phase control is also provided, to provide a smooth variation of voltage between each pair of taps.
7) Circuits 7A, 8A

In Circuits 7A and 8A, where an anti-parallel diode-thyristor pair is used, either in each line or between load and neutral of a polyphase $Y$ connected circuit, it is NOT permissible to connect the neutral to a 4-wire system. Where a 4 -wire system is necessary, see Circuits 9A, 10A and 12A.
8) Circuits 9A, 10A, 12A, 13A

In circuits 9A, 10A, 12A, and 13A, the 3-phase $Y$ connected circuits will operate with full control in a 3 -wire system with only two anti-parallel thyristor sets, or bridge-thyristor sets. When 4 -wire systems are necessary, a third set of either type is required in the location indicated by the phantom box.
9) Circuits 9A, 10A

For 3-phase delta connected circuits, it is practical to use circuits 9A, 10A, 12A, and 13A with only two anti-parallel thyristor sets, or two bridge-

## Table IV-I. Thyristor Circuits to Control AC Loads (Continued)

thyristor sets, in two of the three supply lines. The addition of the third set, however, provides added insurance against false triggering due to a voltage transient, since with three sets the transient must trigger two devices before conduction can commence.
10) Circuits 11A, 14A, 15A

Placing the two thyristor sets or the bridge-thyristor sets inside the delta instead of in the line always requires three sets. However, this location of the sets results in the ability to control 73 percent higher line current for the same thyristor rating. It also requires that the semiconductors have a 73 percent higher peak reverse voltage/forward breakover voltage rating as compared to the $Y$ connected circuits with three semiconductor device sets.
11) Circuits 9A, 10A, 12A, 13A

In all $Y$ connected circuits, it is necessary to provide a gate triggering supply which supplies either: a) double pulsing at 60 degree phase displacement, instead of 120 degrees, or b) a square-wave triggering pulse, that is maintained for a time interval which exceeds 60 degrees, to assure that the two thyristors, which are in cascade line-to-line, conduct at the same time.
12) Circuits $4 \mathrm{~A}, 6 \mathrm{~A}$

Where definite maximum and minimum duty cycles are known or are determinable for the circuits which switch from one voltage level to another (as opposed to zero to full voltage switching), it may be practical to utilize devices with lower rated current (thyristors and/or diodes) than where phase control of the thyristors is the only control means.
13) Circuits 16A, 17A

The shunt control circuits 16A and 17A provide a similar mode of control to those of the transformer tap switching control (circuits 4A, 6A, 14A, and 15A), and are useful where transformers with taps are not available, but where taps can be obtained on heater elements, or they are useful to control a resistor in the rotor circuit of a wound-rotor motor.
14) Circuit 18 A

The delta assembly of thyristors connected in the wye of heater loads, transformer primary windings, or induction motor yields results similar to 7A, 8A, 9A, 10A, 12A, and 13A.

## LEGEND OF ABBREVIATIONS:

SCR = Silicon Controlled Rectifier
RD = Rectifier Diode
FWD $=$ Free Wheeling (By-Pass) Diode
SWC $=$ Switching Control
PC = Phase Control
PBM $=$ Pulse Burst Modulation
RFI = Radio Frequency Interference
ZVS = Zero Voltage Switching
zero. Thus, the voltage across the load will be reduced by phase retard in much the same manner as with a resistive load, except that voltage control will take place over a narrower range of triggering angles; from $\theta$ to 180 degrees. At all triggering angles, the power factor of the load does not depart significantly from the value observed with no phase control [2], [3].

The typical transfer characteristics of ac phase control circuits are shown in Figures 4-1, 4-2, and 4-3.

## Triggering Thyristors

When thyristors are used to control resistive loads, almost any of the varied forms of triggering circuits may be used with satisfactory results. Synchronization of the triggering pulses may be accomplished from either the line voltage or the voltage across the thyristor.

However, when the load is inductive, several precautions must be observed in order to achieve optimum performance.


Figure 4-1. Load Current vs. Angle of Phase Retard


Figure 4-2. Load Voltage vs. Angle of Phase Retard
A. If a triggering circuit is used which produces a narrow spike of gate signal, the charge injected into the thyristor may not be sufficient to maintain the thyristor in the conducting state until the load current has built up to a magnitude larger than the latching current. This may result in mistriggering and erratic control, or no load current whatever. One solution is to shunt the inductive load with a small resistive load drawing a current some-
what larger than the maximum value of thyristor latching current. An alternate (and usually more satisfactory) solution is to provide a triggering circuit which produces a square-wave gate signal which lasts from the time at which triggering is initiated until the time when the thyristor conducts a significant amount of current.
B. For inductive loads, it is mandatory to obtain line synchronization for the triggering circuit from

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Figure 4-3. Angle of Phase Retard vs. Power
the line voltage, NOT from the voltage across the thyristor. If the synchronizing signal is obtained from across the thyristor, a large unbalance between the positive and negative half cycles of current is probable. The result may be overloading of one thyristor, saturation of a transformer core (if a transformer is being controlled), and unstable control. (See Figure 4-4.)

For highly inductive loads, triggering the thyristor full on can result in no output if the triggering pulse is so short that it disappears and the thyristor regains its offstate blocking ability before current can flow in the load circuit. To avoid this, it is necessary to make the triggering pulses long enough so that the thyristor will always be able to conduct whenever circuit conditions are right for conduction, once it has been triggered. Figure 4-5 defines the necessary triggering pulse duration as a function of the load power factor, when the pulse is initiated with zero phase retard.

Other Means of AC Voltage Control
There are numerous types of equipment or systems which can be controlled readily and advantageously by the use of thyristors as switches (as opposed to using them in the phase control mode for continuous variability of voltage). Of
course, many of the switching mode circuits may be readily modified so that they incorporate phase control to provide a fine voltage adjustment to supplement the switching mode of control.

Some of the advantages of the switching mode of operation of thyristors for controlling voltage are as follows:
A. Switching of load voltage (either from zero to full voltage or from partial to full voltage) is accomplished without mechanical contacts, thus eliminating common maintenance problems which result from burning, pitting, and welding of contacts. "Contact bounce" is also eliminated, thereby reducing radio frequency interference (RFI) caused by the repetitive shock excitation of reactive circuit elements.
B. "Zero voltage switching" may be used to essentially eliminate radio frequency interference (RFI) often encountered when voltage is controlled by phase control.
C. The use of the switching mode of voltage control eliminates the reduction in power factor which inherently occurs when voltage is reduced by phase control.

Many of these switching control circuits will find use in controlling heating elements for ovens, furnaces, hot plates, crucibles, and space heaters. Of equal importance,

(a) Symmetrical line current when Triggering Circuit Synchronization is taken from line.

(b) Asymmetrical (undesirable) line current which results when Triggering Circuit Synchronization is taken across SCR Assembly.

Figure 4-4. Triggering Circuit Synchronization

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Figure 4-5. Pulse Duration vs. Load Power Factor
they may also be used for speed controls of squirrel cage and wound rotor induction motors where the motor and/or load inertia is high. Still other types of load, for example; 1) resistance welders, 2) stud welders, 3) flashers and flashing beacons, and 4) magnetic hammers or pulsers, demand this type of control as an inherent element in their mode of operation.

Most heating elements have a high thermal inertia and are easily adaptable to control by the switching mode, either by being switched from zero to full voltage (Circuits $1 \mathrm{~A}, 2 \mathrm{~A}, 3 \mathrm{~A}, 5 \mathrm{~A}, 7 \mathrm{~A}, 14 \mathrm{~A}$ and 18 A of Table IV-I) or from a low voltage tap to full voltage (Circuits 4A, 6A, $15 \mathrm{~A})$. Where the heating elements can be tapped at a midpoint, the circuits of 16 A and 17 A are also useful.

When the circuits with a tapped transformer winding are compared to those with a tapped load, it will be seen that the final control result is very similar. However, where the transformer is tapped, the load voltage is initially low and is switched to a higher value. In the tapped load circuit, the initial voltage is high across one section of the load and zero across the other section. After switching, the voltage decreases across one section while increasing across the other. This tapped load "shunt controller" performs equally well for resistive loads (such as heating elements) and for speed control of wound rotor induction motors, by varying the resistance in the rotor circuit.

Phase control is also very effective with circuits 16 A and 17 A (although radio frequency interference filtering may be necessary) using the shunt mode of control.

Figure 4-6(a) and (b) illustrate the control characteristic for both a resistive load and an inductive (70 degree lagging) load. When $R_{B}$ is small compared to $\mathrm{R}_{\mathrm{A}}$, the range of load current variation is small, but precision of adjustment is very good. When $\mathrm{R}_{\mathrm{B}}$ is large compared to $R_{A}$, the swing in load current can be very large, but with a reduction in adjustment precision. In either case, the voltage is smoothly adjustable over the design range, and is readily adaptable to automatic control.

In the cases of flashers and beacons, it often becomes possible to substantially lengthen filament life of the lamps by switching from full voltage to a lower transformer tap (reducing the voltage below the incandescence level), thus minimizing the range of filament temperature excursion. A similar improvement in the life of heating elements may also be expected.

To obtain good temperature regulation, or speed regulation, with the switching mode of control, the control system may employ pulseburst modulation. This mode of control is usually based on a fixed time control period, for example, 20 cycles at power frequency. The number of cycles during this period when the thyristor switch is in conduction is made variable and is adjusted by temperature or speed feedback controls. The switch always conducts for essentially an integral number of cycles, and either is off, or conducts at a reduced voltage level, for the balance of each period (Figures 4-7 and 4-8).

Pulse-burst modulation can be applied to the control of most heating systems and motor drives due to the high thermal or mechanical in-

(a) RESistive load

(b) INDUCTIVE LOAD

Figure 4-6. Thyristor Shunt Mode of AC Control


CONTROL OF AC LOAD
(CIRCUITS 1A, 2A, 3A, 5A AND 7A THROUGH 13A)
Figure 4-7. Pulse Burst Modulation
Voltage Control Full On/Off


CONTROL OF AC LOAD (CIRCUITS 4A, 6A, AND 15A)

Figure 4-8. Pulse Burst Modulation Voltage Control Transformer Tap Switching
ertia of these systems. Systems with very high inertia can tolerate relatively long control periods, whereas systems with lower inertia, or requiring a fine control resolution, will demand a short control period.

As mentioned earlier, the use of pulse burst modulation with thyristor switches will minimize radio frequency interference, but this, by itself, will not completely eliminate it. The fast turn-on of a thyristor when the supply voltage is at any value other than zero, still causes one pulse of shock excitation each time the thyristor is turned on to carry a burst of pulses. However,
with thyristor switches, it is possible and often desirable to incorporate zero voltage switching. When controlled in this mode, the thyristors are always turned on at zero voltage (they turn off at zero current), thus eliminating the interference caused by fast switching of heavy currents.

All of the circuits which switch from one tap to another (either tapped transformer or tapped load) may incorporate phase control to supplement the switching type of control to obtain voltage or current regulation of power supplies. Methods of applying phase control have been discussed earlier in this chapter. It is possible to achieve such regulation by phase control alone and eliminate the taps. However, where only a limited range of adjustability is required, the combination of phase control with switching mode operation greatly reduces the peak-to-RMS current ratio in ac power supplies. For instance, output voltage can be smoothly varied between the voltages obtained from any two transformer taps by first gating a thyristor connected to the lower voltage tap, and then later in the cycle gating a thyristor connected to the higher voltage tap. This type of voltage control reduces the peak-to-average current ratio. It also minimizes the change in powerfactor as voltage is varied.

## Application of Specific Circuits

Circuits to control resistive loads (heater, lighting, etc.) are very tolerant of variable supply conditions, such as waveform distortion, phase unbalance (either magnitude or phase shift distortion) and variations in switching rate, as long as
the switching period is small when compared to the thermal time constant of the load. Any of the Table IV-I circuits may be utilized when properly matched to the application requirements. Triggering synchronization may be taken from either the line, or across the power control device or assembly.

The control of power into the primary of a transformer becomes slightly more critical. The following procedures should be observed to assure good operation:
A. The load is now inductive. Therefore, triggering synchronization must come from the supply line (NOT from across the SCR assembly) to insure equal positive and negative half cycles of power (see Figure 4-4(a) and (b)).
B. If the transformer iron is worked near saturation, or if it has a high residual magnetism, the triggering circuit should be designed to insure that conduction always starts on a positive half cycle and ends on a negative half cycle. If this is not done, a transformer core may become partially saturated and draw excessive magnetizing current on one-half cycle and very little on the opposite polarity half cycle. (This is particularly true of resistance welding transformers.)

1) Polyphase circuits using SCRs to control both half cycles (Circuits 11A, 14A, 15A, 17A and 18 A ) are recommended because both positive and negative half cycles are balanced in both waveform and area. Hybrid circuits (7A, 8 A and 14 A ) and unsymmetrical circuits $(9 \mathrm{~A}, 10 \mathrm{~A}, 12 \mathrm{~A}$ and 13 A ) can result in asymmetrical distortions (see Figures 4-9(a) and (b)).
2) However, where transformers have relatively low residual
magnetism, and are operated at low flux densities, many of these hybrid and unsymmetrical circuits can yield satisfactory performance and lower initial cost.
C. The most critical of the SCR Primary Control applications are probably those involving induction motor control (either squirrel cage or wound rotor). It is highly recommended that "all SCR" control circuits be used for all motor controls (Circuits 11A, 12A, 14A, 15A, 17A or 18A). The reasons for this are as follows:
3) It is important that each phase be triggered by the triggering circuit with exactly the same number of degrees of phase retard. If this is NOT done, a de component will result in one or two phases which causes a braking action during a part of each cycle. This (internal) fighting to accelerate and brake during each cycle can cause damaging overheating of rotor bars or windings.
4) Figure 4-9(b) illustrates an unbalanced voltage waveform typical of hybrid circuits. Since flux is proportional to voltage (below saturation), a rotor voltage and current may be induced which is different for positive and negative half cycles. This can again result in overheating of the rotor, and poor speed control.
5) When thyristors are used to control squirrel cage motor speed (by increasing the slip), selection of the motor and type of load is very important. The motor load should be one for which the load varies approximately as $(\text { speed })^{3}$, i.e., such as a fan, a squirrel cage blower or a centrifugal pump, but never one requiring constant torque. The motor should be of a high torque,


WAVEFORMS FOR CIRCUITS 11A, \& 14A
ALSO FOR 9A, 10A, 12A AND 13A WHEN
RESISTIVE LOAD. NOTE THAT WAVE FORMS ARE SYMMETRICAL EVEN THOUGH SHAPE IS DISTORTED.
(a) Symmetrical SCR Primary Controller


WAVEFORMS FOR CIRCUITS 7A \& 8 A NOTE THAT WAVEFORMS ARE BOTH ASYMMETRICAL AND DISTORTED. (THESE WAVEFORMS PROBABL.Y ARE SOMEWHAT TYPICAL FOR CIRCUITS 9A, 10A, 12A \& 13A WHEN ONLY TWO SCR SETS ARE USED.)
(b) Hybrid SCR Primary Controller

Figure 4-9. Waveforms of SCR Primary Controller
high slip design (similar to NEMA Class D). It is usually found that the slip must be greater than 8 percent. Careful system tests should be made with the motor and load to ensure that operating motor current over the desired control range does not exceed rated current limits or temperature rise limits (cooling efficiency is reduced as the speed is reduced).

## The Triac vs. the SCR [4]

For ac power control, anti-parallel (inverse parallel) connection of a pair of SCRs has been troublesome because SCR anodes are generally grounded to the case. This necessitates insulating the case of at least one of the devices from ground, using an insulator that also is a good thermal conductor, if a grounded heat dissipator is used.

One question facing the circuit designer is whether to use the triac or the SCR. AC power control is usually applied to motor speed control, heating control, and light dimming, the first one may be characterized as having a lagging power factor. Hence in deciding which device to use, the designer must often consider it in terms of controlling an RL circuit.

A simple inductive circuit, containing a pair of anti-parallel SCRs, is shown in Figure $4-10$. If we examine the waveshape of $\mathrm{e}_{\mathrm{S}}$ vs. time, Figure $4-11$, where $e_{S}$ represents the voltage drop across the devices, the control devices are subjected to sudden increases of offstate voltage, because of the inductive nature of the load. Use of an SCR that is incapable of remaining in the nonconducting state while the anode-to-cathode voltage is rising rapidly in a direction which can trigger it will cause loss of control. The measure of the ability of a device to withstand rapid application of off-state voltage without losing its blocking capacity is its $\mathrm{dv} / \mathrm{dt}$ rating.

There are two types of $d v / d t$ ratings for a silicon controlled rectifier. The dv/dt applied to the device during its recovery of blocking capability after conduction is called the reapplied $d v / d t$. The ability to withstand a voltage surge after it has fully recovered is the critical $\mathrm{dv} / \mathrm{dt}$ rating. Most thyristors display critical $\mathrm{dv} / \mathrm{dt}$ capabilities that are superior to their reapplied $\mathrm{dv} / \mathrm{dt}$ ratings because major carrier recombination does not occur under critical dv/dt stress.

Because a triac is a bidirectional device, it may have conducted in one direction just prior to blocking in the other. A dv/dt impressed on a triac after it has been in conduction is called commutation $\mathrm{dv} / \mathrm{dt}$. The choice between a triac and a pair of anti-parallel SCRs is determined by whether triacs are available with sufficiently high commutation $\mathrm{dv} / \mathrm{dt}$ ratings to handle the maximum voltage surges in the circuit. If not, the designer must turn to anti-parallel SCRs.

By using an RC snubber connected across the device, as shown in Figure 4-12, the rate of voltage


Figure 4-10. Single-Phase AC Controller


Figure 4-11. Waveshapes for Triggering Angle a Greater than Phase Angle $\theta$


Figure 4-12. Triac with Snubber Network
rise can be suppressed. Analysis of this circuit leads to the expression in Formula 4-A.

$$
\begin{equation*}
\mathrm{C}=\frac{4\left(\mathrm{~V}_{\mathrm{M}}\right)^{2}}{(\mathrm{dv} / \mathrm{dt} \max .)^{2} \mathrm{~L}} \tag{4-A}
\end{equation*}
$$

Where:
$\mathrm{V}_{\mathrm{M}}=$ Peak applied voltage $\mathrm{L}=$ Total inductance of the circuit

The resistance of the circuit should be chosen so that the capacitor discharge does not damage the device from an inrush current standpoint.

During device turn-on, rapid current buildups in limited areas can cause excessively high temperatures which may damage an SCR or triac. Following initial injection of carriers at the gate, a short period of time is required for current to flow across the whole cross-section of the device. If the carriers cannot disperse rapidly enough, the device will be damaged.

Voltage fall and current rise vs. time are plotted in Figure 4-13. As can be seen by multiplying instantaneous values of current and voltage, a curve of watts dissipated vs. time can be obtained. Note that the power curve reaches a sharp peak during turn-on.

A load having a leading power factor or a nonlinear resistance, such as a bank of incandescent lamps (very low cold resistance and high hot resistance) is prone to high inrush currents. Insertion of a choke in series with this type of load reduces inrush currents. The proper value of this choke can be calculated by considering the relationship in Formula 4-B.
$L=\frac{e}{d i / d t}$

## Where:

$e=$ Choke forcing voltage
$d i / d t=\begin{aligned} & \text { The maximum allowable } \\ & \text { rate of change of current }\end{aligned}$


Figure 4-13. Power Dissipation Curve During High di/dt Turn-On Action
specified for the semiconductor device during switching.

It is useful to consider the use of a self-saturating choke in the circuit, which has an inductance that decreases with increasing current. This would limit current flow during turn-on of the device. Equation 4-C gives the voltage drop across a coil, which serves as the basic equation for the design of this reactor.
edt $=N d \phi$
Where:
e = Circuit forcing voltage
$\mathrm{dt}=$ Delay time
$\mathrm{d} \phi=$ Saturation level of choke
$\mathrm{N}=$ Number of turns
Knowing the delay time (dt) introduced by the choke and the circuit forcing voltage (e), it is possible to equate this to the saturation level of the choke ( $\mathrm{d} \phi$ ) and the number of turns necessary ( N ). By selecting a $\phi$ vs I relationship for the choke, it is possible to design for a nonlinear case (saturating choke) or use an idealized B-H loop for an approximate solution [5],[6].

The choice of triac or antiparallel SCR is rarely determined by di/dt considerations, since in most phase control applications, current can be suppressed by "soft start" driving circuits and added line inductance. Triacs are most generally applied in these cases; however, for certain situations the designer may want to use devices which are especially designed to have extremely fast turn-on characteristics. Since triacs now available are not specifically designed for very high inrush ratings (hundreds of amperes per microsecond), a pair of fast turn-on SCRs would be the best choice. SCRs are available in much higher current and voltage ratings than triacs and so are the natural choice for very high power applications.

Transient voltages well in excess of normal supply potentials are common on commercial power lines. There are SCRs that will break-over nondestructively in the off-state direction but may be damaged by overvoltage in the reverse direction. To protect against such damage, designers have, in the past, incorporated shunting diodes, as shown in Figure 4-14. This is unnecessary when using a triac which will automatically breakover in either direction nondestructively in the event of an overvoltage; however, the designer must be careful not to exceed the inrush current rating of the device when the triac is triggered by a sharp transient.

Since the triac is a bidirectional device, its characteristics are given for both positive and negative excursions. For the designer to determine the heat sinking needed for correct heat dissipation, he must first find the RMS current to which


Figure 4-14. Inverse Voltage Protection Circuits
the device will be subjected. He then consults a curve of RMS current vs. allowable case dissipation for the selected device to obtain the maximum allowable case temperature $\mathrm{T}_{\mathrm{C}}$. The next step is to check the curves for device dissipation vs. RMS current for the proper conduction angle. This dissipation, called average on-state power loss, is designated $\mathrm{W}_{\mathrm{T}}$. Knowing the maximum ambient temperature $\mathrm{T}_{\mathrm{A}}$ and the interface thermal impedance between the heat dissipator and the device case ( $\mathrm{R}_{\theta \mathrm{CS}}$ ), the heat dissipator thermal resistance ( $\mathrm{R}_{\theta \mathrm{SA}}$ ) is calculated using Equation 4-D.

$$
\begin{align*}
& \mathrm{R}_{\theta S A}= \\
& \frac{\mathrm{T}_{\mathrm{C}}-\left(\mathrm{T}_{\mathrm{A}}+\mathrm{R}_{\theta \mathrm{CS}}\left(\mathrm{~W}_{\mathrm{T}}\right)\right)}{\mathrm{W}_{\mathrm{T}}} \tag{4-D}
\end{align*}
$$

Where:
$\mathrm{R}_{\theta \mathrm{SA}}=$ Heat dissipator (sink to ambient) thermal resistance
$\mathrm{T}_{\mathrm{C}}=$ Maximum allowable case temperature
$\mathrm{T}_{\mathrm{A}}=$ Maximum ambient temperature
$\mathrm{R}_{\theta \mathrm{CS}}=$ Interface (case to sink) thermal resistance
$\mathrm{W}_{\mathrm{T}}=$ Average on-state power loss

In the case of anti-parallel SCRs, determination of the allowable case temperature is not as straight forward. Generally, when applying anti-parallel SCRs to an ac controller, the load RMS current is known; however, since most SCR ratings are in terms of full cycle average current, it is necessary to convert the RMS current to the full cycle average current for each device. A list of such conversions for various triggering points is given in Table IV-II. If the load is inductive, one must solve a lengthy transcendental equation [3].

Knowing the full cycle average current in each SCR, the allowable case temperature can be obtained by consulting a curve of allowable case temperature vs. full cycle average current for the appropriate conduction angle. Also, a curve of device dissipation vs. full cycle average current can be used to determine the power dissipated in the device. With this information in hand, the designer can then compute $\mathrm{R}_{\theta \mathrm{SA}}$ for each SCR , using Formula 4-D.

The dissipation in a triac is considerably greater than that of a single SCR. Therefore, it is often advantageous when using high power triacs to employ either forced air or liquid cooling. These cooling means provide high thermal efficiency, yet require relatively small heat sinks.

## HEATER CONTROL CIRCUITS

Perhaps one of the most obvious applications of an ac control device is in heating control. Since a heating load by nature has a long thermal time constant, it is not responsive to instantaneous current changes. This characteristic makes it adapt-

Table IV-II. RMS vs. Average Current

| ACWAVESHAPE | SCR CURRENT <br> WAVESHAPE | CYCR RMS <br> CURRENT <br> CURRENT |
| :--- | :--- | :--- | :--- |

able to zero voltage triggering techniques using pulse burst modulation in conjunction with power triacs. Instead of applying ordinary phase control means with its inherent sharply rising circuit voltages and resulting radio frequency interference, the triggering control for a triac can be arranged to trigger the device only when the supply voltage is going through zero.

The waveshapes of Figure 4-15 are an illustration of this type of control with unity power factor load. With a three-phase 460 V line, using three power triacs at 143 amps RMS each, as illustrated in

Figure 4-16, a heating load capacity of ( $\sqrt{3}$ ) ( 143 amps RMS) ( 460 V RMS) $=114 \mathrm{KW}$ can be controlled.

Examining the steady-state rating of a suitable device as shown in Figure 4-17(a) (curve of RMS current vs case temperature), the maximum allowable case temperature is $70^{\circ} \mathrm{C}$ and the 143 A rating can be achieved, for instance, by using a water-cooled heat dissipator. At 143 amperes, $180^{\circ}$ conduction (bidirectional), the curve of dissipation vs. RMS current (Figure 4-17(b)) shows that the device will dissipate 225 watts. If we use a water-cooled heat exchanger with a


Figure 4-15. Voltage Waveforms for Zero Voltage Control of an AC Load


Figure 4-16. Triac Three-Phase Heater Power Control Circuit
thermal efficiency of $0.0425^{\circ} \mathrm{C} / \mathrm{W}$ at $3.5 \mathrm{gal} / \mathrm{min}$ flow rate as shown in Figure 4-18, we can keep the exchanger rise below $9.6^{\circ} \mathrm{C}$. With a $0.08^{\circ} \mathrm{C} / \mathrm{W}$ efficiency between heat
exchanger and case, the total temperature rise between the cooling water and the triac case is $27.6^{\circ} \mathrm{C}$. Thus, with $42^{\circ} \mathrm{C}$ cooling water, the maximum allowable junction temperature of the triac will not be exceeded and the load of 114 KW can be controlled.

An interesting extension of the application of a triac to this type of load can be achieved by using the gate characteristic of the IR power logic triac. If the triacs controlling an ac heater load were to be triggered with a negative dc gate signal, the full ac supply would be conducted to the heater load. By simply reversing the gate potential, half wave rectification of the supply to the load will take place. Thus, by using a simple gate signal reversal, the supply to the load can be reduced appreciably.


Figure 4-17(a). RMS Current vs Case Temperature

There are many types of triggering circuits which are useful for zero voltage triggering. Three of these are illustrated in Figures $4-19,4-20$, and $4-21$. In addition, there are now a number of integrated circuit zero voltage switches which can be used in zero voltage triggering circuits.

In heating applications, transients tending to cause the triacs to trigger, due to high rates of rise of main terminal voltage ( $\mathrm{dv} / \mathrm{dt}$ ) or by exceeding the break-over voltage rating of the devices ( $\mathrm{V}_{\mathrm{BO}}$ ), are not generally worrisome to the circuit designer. An occasional power pulse to the load not called for by the control circuitry is generally of little consequence. By using a device with known avalanche and breakover capability, considerable circuit
complexity can be avoided by choosing a voltage rating for the device such that "false-triggering" does not occur frequently and thus minimizing the need for overvoltage protection and $\mathrm{dv} / \mathrm{dt}$ suppression. A triac with a 1000 V rating will generally suffice for an application to a 460V RMS line.

An oven control utilizing three power triacs has been constructed with a temperature error of $1^{\circ} \mathrm{C}$. Some typical waveforms are shown in Figure 4-22.

## Zero Voltage TriggeringCircuits

In Figure 4-19, transistor $\mathrm{Q}_{1}$ and zener diode $\mathrm{BD}_{1}$ comprise the reference amplifier which establishes an error signal. If the measured quantity is greater than the reference established by $\mathrm{BD}_{1}, \mathrm{Q}_{2}$ will

(a) LOW-LEVEL ON-STATE POWER LOSS VS CURRENT


Figure 4-17(b). Allowable Power Dissipation


Figure 4-18. Typical Liquid-Cooled Heat Exchanger Thermal Characteristic
turn on pulling the upper base of $\mathrm{UJT}_{1}$ to the regulated dc line voltage. The zener diode across $\mathrm{C}_{1}$ is chosen so that it clamps the emitter of $\mathrm{UJT}_{1}$ to a low enough voltage so that if the $\mathrm{UJT}_{1}$ upper base is at $\mathrm{V}_{1}, \mathrm{UJT}_{1}$ cannot trigger. Thus, regardless of what else is happening in the circuit, if the measured quantity is above the reference, the load current will be cut off by virtue of the cessation of $\mathrm{UJT}_{1}$ pulsing.

Now examining the right-hand side of the circuit, we see that the output of a small transformer $\mathrm{T}_{1}$, ( 12 V output is suitable) is rectified and added to a zener voltage ( $\mathrm{BD}_{4}$ ), the sum of these voltages is compared to a reference zener ( $\mathrm{BD}_{3}$ ). Should this sum exceed the reference level (indicating a line voltage far from cross-over), transistors Q4 and Q3 are turned on, pulling the upper base of UJT $_{1}$ to $\mathrm{V}_{1}$ and
also preventing UJT $_{1}$ from triggering.

We can see then that if either the line voltage is considerably greater than zero, or if the measured quantity exceeds the reference, no triggering can take place.

If, on the other hand, the measured quantity is low and the line voltage is near zero, the UJT will trigger and supply power to the load. Caution should be exercised in choosing the values of $R_{3}$ and $C_{1}$ so that the pulse from the UJT will bridge the cross-over from the declining edge of the sine wave to the increasing edge of the sine wave. This can be somewhat alleviated by connecting a small capacitor from the junction of $R_{11}$ and $R D_{5}$ to the negative of $\mathrm{V}_{1}$.

Notes Relative to Figure 4-22
Operational waveforms of power



## INTERNATIONAL RECTIFIER ISR



Figure 4-20. Zero Voltage Control Circuit [14]
triac control of an electronically heated industrial oven.
A. Line voltage and line current waveforms during the ON period of operation. Even though the heater resistance winding exhibits a small amount of inductance, the waveforms are symmetrically sinusoidal and undistorted by the triac control.
B. On-state voltage and line current during conduction. They are inphase and the peak values of on-state voltage are symmetrical.
C. Gate current and line current. The gate current is phase-shifted to lead the line current such that it will be driving the triac gate hard at the time it starts to conduct current.



Figure 4-22(a). Line Voltage and Line Current Over Control Waveforms


Figure 4-22(b). On-State Voltage and Line Current


Figure 4-22(c). Gate Current and Line Current Waveform


Figure 4-22(d). Gate Voltage


Figure 4-22(e). Gate Current and Line Voltage


Figure 4-22(f). Line Voltage and Line Current
D. Gate voltage across the triac gate. The alternate peaks of the waveform shows the small influence in voltage magnitude that the direction of flow of line current imposes on the gate signal.
E. Gate current and line voltage. Phase shift and the transient in the gate current are obvious as line current changes polarity.
F. Line voltage and line current showing zero-voltage switching.

Note the line voltage is a continuous sine wave, while the line current starts and stops at the zero axis. The triac operating temperature also influences the starting load current at the zero cross-over point.

## Lighting Circuits [7], [8]

A lamp dimmer is an example of one of the basic uses of phase control. There are many different types of triac circuits designed for lamp dimming. However, most of these differ only in the method of triggering the triac. Among the components used for triggers are UJTs, PUTs, neon bulbs, silicon unilateral switches, assymetrical switches, reed switches, and diacs. The diac offers the advantage of needing fewer components for a trigger circuit. Its characteristics also make it an ideal trigger for a triac. The main disadvantage of the diac is that it takes approximately 32 volts to break over, thus limiting the portion of the wave that can be controlled.

One of the more simple circuits using a diac-triac combination to dim incandescent lamps is the single
time constant phase control shown in Figure 4-23. This circuit has as its major disadvantages a limited control range and hysteresis. For a more thorough description of hysteresis see reference [9]. For the single time constant circuit, the voltage on the capacitor charges up to the breakover voltage of the diac and discharges through the diac to trigger the triac. This enables the triac to conduct for the remaining portion of the half cycle of the input wave. When the input goes to zero, the triac turns off and the charge on the capacitor, since the diac has already recovered, begins to build up with the opposite polarity until the same events occur again. Figure $4-24$ shows waveforms for this single time constant circuit when operating with a large phase control angle.

A slightly more complex circuit is the double time constant circuit, shown in Figure 4-25. This circuit was designed and built for both a 3600 and a 7200 watt load.

The double time constant circuit operates in a similar fashion to the single time constant circuit with the exception of capacitor $C_{1}$ recharg-


Figure 4-23. Single Time Constant Lamp Dimmer Circuit


UPPER: VOLTAGE ACROSS TRIAC
LOWER: VOLTAGE ACROSS $C_{2}$
LOWER: VOLTAGE ACROSS C $C_{2}$
Figure 4-24. Waveforms forSingle Time Constant Lamp Dimmer Circuit (Operating with Large Phase-Control Angle)


Figure 4-25. Double Time Constant Lamp Dimmer Circuit
ing $\mathrm{C}_{2}$ after the diac has broken down. The size of the triac controls the size of the capacitors used in the circuit. Figure $4-26$ shows the waveforms with the triac nearly full off for the 3600 watt circuit of

Figure 4-25 operating with the 1200 watt amp load.

Figure 4-27 shows the effect of the diac as a trigger when operating full on. The triac is never on for the full period of the input wave, but


Figure 4-26. Waveforms for Double Time Constant Lamp Dimmer (Near Full On)


UPPER: VOLTAGE ACROSS TRIAC
LOWER: VOLTAGE ACROSS $\mathrm{C}_{2}$
100 V DIV: 10 MSEC DIV
Figure 4-27. Waveforms for Double Time Constant Lamp Dimmer (Full-On Operation)
only after the charge on capacitor $\mathrm{C}_{2}$ has reached 32 volts.

The relative light intensity of the circuit in Figure 4-25 as measured with a light meter held two feet away from a circular concentration of the 1200 watt lamp load is shown in Figure 4-28.


Figure 4-28. Relative Light Intensity from Double Time Constant Triggering Circuit Lamp Dimmer

A configuration for a light flasher is shown in Figure 4-29, requiring two triacs and one heat sink, rather than the four SCRs and three heat sinks previously required.

When motor loads are switched on to an ac line which is also supplying fluorescent lamps there is often a visible flicker in the lamps due to the surge loading of the line. This can often be objectionable, especially when the motor starting is frequent. For example, compressor motors are often required to start frequently and run a relatively short time. One method of minimizing the effect of such flicker is
by automatically correcting the line voltage during high surge currents. This is done by inserting a section of a step-up transformer to boost the line voltage temporarily until the surge disappears.

The triac is an excellent device for this purpose because of the simplicity of the driving function and the ease of heat sinking. A tap changer similar to that shown in Figure 4-30 can be used as a line compensator. Line compensation can also be accomplished by using a triac and an autotransformer as shown in Figure 4-31. As the starting contactor, $\mathrm{K}_{1}$, in series with the motor load, is closed, the motor surge current begins to flow. This current is generally three to six times the running current of the machine. The surge causes a voltage drop on the line inductance and transient inductance of the supply alternator which causes the line voltage, as seen by the fluorescent lamps, to drop. If the surge current is sensed by a current transformer as shown in Figure 4-31 and caused to trigger the triac into a compensating auto-transformer, the flicker resulting from motor starting can be greatly minimized.

The degree of compensation can be adjusted by the resistor in series with the triac, while the surge current at which compensation takes place can be changed by adjusting the resistor divider across the secondary of the current transformer. By utilizing this circuit across each line, a three-phase system can be automatically compensated.

## FERRORESONANT TRANSFORMER REGULATED AC <br> POWER SUPPLY

A ferroresonant voltage regulator may be used for line voltage


Figure 4-29. Light Flasher Circuit


Figure 4-30. Static Tap Changer Circuit
regulation. This is inherent in the device, since it is composed of a high leakage transformer which serves as a saturable reactor and an inductance in series. The half cycle average output voltage of the ferroresonant regulator is given in Formula 4-E.
$\mathrm{V}_{\mathrm{O}}=4 \mathrm{~N} \phi \mathrm{~S} \mathrm{f} \times 10^{-8}$

## Where:

$\mathrm{V}_{\mathrm{O}}=$ Average output voltage $\mathrm{N}=$ Number of turns
$\phi_{S}=$ Saturation flux
$\mathrm{f}=$ Input frequency [10]
Since the saturation flux, $\phi_{\mathrm{S}}$ is fixed as long as the input frequency remains constant, the output voltage will remain the same. This equation points out the main difficulty of the ferroresonant regulator, in that the output voltage is frequency sensitive. Some of the other disadvantages include: (1) Since the core operates in saturation, the core losses are high and the external magnetic field is high; (2) Since the output varies directly with the cross-sectional area of the core, normal core tolerances cause unit-to-unit output voltage differences; (3) Since the core is the regulating element, the output voltage varies with load current changes due to voltage drop in the secondary resistance.

One method of eliminating these disadvantages is to simulate saturation of the transformer. This can be done by using a transformer with additional magnetic shunts and an additional winding, or by adding inductance in series with the primary winding of a transformer with two secondary windings. This in-


Figure 4-31. Line Voltage Compensator Circuit
ductance must be sufficiently large to produce the voltage drop required to regulate the output voltage.

The conventional ferroresonant regulator may be described in several ways. One simplified explanation is to consider it similar to the circuit of Figure 4-32. Assume the input voltage is sufficiently large so that the core of $T_{1}$ is driven from - $\phi$ to $+\phi_{\mathrm{S}}$ in less than a half cycle. Thus, the half cyclic average voltage induced in any winding on $\mathrm{T}_{1}$ is a constant as long as the core saturates and the frequency is fixed. This is true, regardless of the magnitude or waveform of the input voltage. Also, regardless of the number of turns on the primary winding, as long as the core is driven into saturation, the output voltage follows the number of turns on the secondary winding. If a rectifier
and averaging filter follow the output of the transformer, the dc output will be regulated for line voltage changes. This is a fundamental type of line voltage regulator.

A more efficient line voltage regulator would use an inductor, $\mathrm{L}_{1}$, in series with $\mathrm{T}_{1}$, rather than a resistor to eliminate the power losses (see Figure 4-33). This circuit also regulates the half cyclic average of the output voltage, regardless of the magnitude or waveform of the input voltage. If a rectifier and averaging filter follow the output of $\mathrm{T}_{1}$, again the output voltage will be regulated for line voltage variations.

The circuit of Figure 4-34(a), called a ferroresonant regulator, is a more effective and efficient technique of regulating the output voltage. This circuit uses a capacitor $\mathrm{C}_{1}$ in parallel with $\mathrm{T}_{1} . \mathrm{C}_{1}$ and $\mathrm{L}_{1}$ are


Figure 4-32. Saturating Transformer Regulator
tuned near the input frequency. This arrangement provides almost unity power factor and efficient shows transfer. Figure 4-34(b) shows the schematic for a ferroresonant transformer. Here the magnetic functions of $L_{1}$ and $T_{1}$ are combined on a single core structure. The leakage inductance provided by the shunts takes the place of $\mathrm{L}_{1}$. Figure $4-35$ shows a typical output voltage waveform from either arrangement.

Because of the near square waveform of the output voltage, and since for a square wave $V_{P K}=$ $\mathrm{V}_{(\mathrm{AV})}=\mathrm{V}_{\text {RMS }}$, this circuit regulates all three values. Therefore, with this circuit, the filter may be either capacitor input or inductor


Figure 4-33. Improved Saturating Transformer Regulator
input - it does not matter - the dc output will be the same and will be regulated for line voltage changes. In practice, a capacitor terminated rectifier is usually used because the filter capacitance is reflected in parallel with $\mathrm{C}_{1}$, reducing the value of $\mathrm{C}_{1}$ required to resonate with $\mathrm{L}_{1}$.

Another advantage of this circuit is that the tuning of $L_{1}$ and $\mathrm{C}_{1}$ provides a low pass filter between the input and the output. Thus, harmonics in the input waveform are attenuated by ferroresonant regulator circuits.

Shown in Figure 4-36, is a circuit which consists of a ferroresonant regulator, a control circuit, and a rectifier and filter [10]. In the control circuit the $\mathrm{R}_{1} \mathrm{C}_{2}$ combina-


Figure 4-34. Secondary Resonance, Saturating Transformer Regulators


Figure 4-35. Waveshapes of FerroResonant Regulator on Transformer
tion is an integrator used to measure the volt-time area of the output voltage. $\mathrm{L}_{1}$ is an inductor chosen to have a value approximately equal to the value of the saturated inductance of the secondary of the ferroresonant transformer. The triac acts as a switch which closes when there is sufficient gate current flowing
into the device. The control circuit operates as follows: The $R_{1} C_{2}$ combination integrates the output voltage, and therefore the peak voltage across the capacitor $\mathrm{C}_{1}$ at any instant is proportional to the volt-time area of the voltage eout. When the voltage on capacitor $\mathrm{C}_{2}$ reaches a value sufficient to break over the zener diode, $\mathrm{BD}_{1}$ or $\mathrm{BD}_{2}$, on alternate half cycles, gate current flows and the triac conducts current. This causes the capacitor $\mathrm{C}_{1}$ to rapidly discharge and recharge in the opposite direction through the inductor $\mathrm{L}_{1}$. At this time, the voltage across the triac and the current through it are reversed, causing the triac to come out of conduction, thus completing the half cycle. The same action occurs the next half cycle with the opposite polarity. Clearly this ac-


Figure 4-36. Ferroresonant - Triac Regulator
tion cannot occur if the core saturates since the necessary volt-time area to trigger the triac cannot be obtained.

Specifically, the output voltage, $e_{\text {out }}$ in this figure is approximately a square wave. However, in this case, the output voltage is still fre-quency-dependent.

Figure $4-37$ is a schematic of the ferroresonant circuit incorporating feedback. Here the control circuit has been placed across an isolated winding of the transformer. This is necessary to obtain the isolation required for the feedback circuit. The integrating resistor consists of
$R_{4}, R_{5}$, and $R_{0}$, where $R_{O}$ is the impedance seen looking into $a-a$ : The zener diode $\mathrm{BD}_{3}$ is the reference, and the transistor $Q_{1}$ is the error detector and amplifier. The diode bridge, $\mathrm{RB}_{2}$, is added to keep the current flow through $\mathrm{Q}_{1}$ unidirectional. In this arrangement, $\mathrm{R}_{\mathrm{O}}$ is an impedance whose value is decreased by the feedback circuit as edC tries to increase. Thus, the regulating function is taken by sampling the actual filtered de output voltage rather than by monitoring the intermediate square wave voltage. Therefore, the regulator is no longer frequency dependent. As


Figure 4-37. Ferroresonant-Triac Regulator with Isolated Output Regulation
can be seen from Figure 4-37, the output voltage is regulated by controlling the amplitude of the ac voltage feeding the rectifier bridge and filter. Another advantage of this circuit is that $\mathrm{L}_{1}$ can be made very small, causing the voltage across the triac to reverse more rapidly, making $\mathrm{e}(\mathrm{t})$ a squarer wave, and reducing the required filter capacitance. Since the transformer core does not saturate, core losses are reduced and the circuit is more efficient. The half cycle response of the ferroresonant regulator is retained, and the stray magnetic field is reduced.

This system provides a means for marrying the best characteristics of both magnetics and triacs to result in a reliable, well-regulated power supply, which should be relatively inexpensive and extremely reliable.

Figure 4-38 shows the circuit of a feedback controlled simulated ferroresonant regulator where the regulating effect is achieved by adding on inductor, $\mathrm{L}_{1}$, in series with the primary of the supply transformer, $\mathrm{T}_{1}$. This is an excellent means for simulating the action of the ferroresonant regulator. However, for a practical power supply, it is much more economical to design a special input transformer to include the necessary regulating reactance effect.

In the circuit of Figure 4-38, the series inductance $\mathrm{L}_{1}$ produces a reactive voltage drop, which is controlled by the impedance connected across the lower secondary winding of the input transformer. When the triac is off, capacitor $\mathrm{C}_{2}$ draws a leading current through $\mathrm{L}_{1}$ from the ac supply. This leading current produces a voltage across $\mathrm{L}_{1}$, which adds to the source voltage. Thus,
the transformer secondary voltages are highest when the triac is off. If inductor $\mathrm{L}_{2}$ is such that its reactance is one-half that of capacitor $\mathrm{C}_{2}$, a lagging current, equal in magnitude to the leading current drawn by $\mathrm{C}_{2}$ alone, will flow through inductor $\mathrm{L}_{1}$ when the triac is on for the entire cycle. Thus, the triac can be phase controlled to adjust the voltage across $L_{1}$, thereby regulating the transformer secondary voltages. Figure 4-39 includes phasor diagrams to illustrate this regulating principle.

The circuit in Figure $4-39$ is divided into two parts: (1) the output secondary winding circuit, and (2) the control secondary winding circuit of the transformer.

The output winding voltage is rectified and filtered to provide the dc load voltage. This voltage is also used as a supply for the power switch/amplifier. The level detector is used to measure the error between the output voltage and the zener reference voltage. It is a simple bridge consisting of a zener diode, two fixed resistors, and one variable resistor which is used to set the output voltage level. The supply for $\mathrm{IC}_{1}$ comes from a voltage divider which outputs approximately 20 volts. The IC is used in the differential amplifier mode to drive the base of the power transistor. The power transistor acts as a variable resistor to control the rate of charging of capacitor $\mathrm{C}_{3}$. Capacitor $\mathrm{C}_{3}$ charges up, at a rate determined by $\mathrm{T}_{1}$, to the breakdown voltage of the diac and then triggers the triac.

Figure 4-40 shows the triac voltage with a load of 150 ohms and the output adjusted to 75 volts. It can be seen that the triac is on for an appreciable part of each cycle.


Figure 4-38. Ferroresonant Voltage Regulator with Simulated Feedback Control


Figure 4-39. Phasor Diagram of Ferroresonant Voltage Regulator with Simulated Feedback Control

Figure $4-41$ shows the triac voltage with a 30 ohm load on the output winding. This figure indicates that the triac is on for less total time. The continuous variation in the triac triggering angle is believed to be caused by the system attempting to regulate the ripple in the output.

Figure $4-42$ shows the gate signal compared with Figure $4-41$. It is interesting to note the difference in the signals whether positive or negative. Figure $4-43$ compares the voltage on $C_{2}$ with the triac voltage. When the triac goes off the charge on $\mathrm{C}_{2}$, which had started to decrease, begins to build up again. This depends on the point in the cycle where the triac goes off. Figure 4-44 compares load voltage with triac voltage. A larger filter capacitor, $\mathrm{C}_{1}$, would reduce the amount of ripple shown.

All of the previous figures show the effect of the inductor $\mathrm{L}_{2}$ in series with the triac in that instead of the triac going off when the voltage reaches zero, it goes off when the current reaches zero. Table IV-III shows the amount of regulation the circuit provides for variation in the load and also input variation.

Table IV-III. Simulated Ferroresonant Voltage Regulator Load Voltage Variation

| LOAD CURRENT <br> (AMPS) | LOAD VOLTAGE <br> (V dc) |
| :---: | :---: |
| 0.0 | 75.0 |
| 0.5 | 75.0 |
| 1.0 | 74.6 |
| 1.5 | 73.3 |
| 2.0 | 73.3 |
| 2.5 | 73.7 |
| 3.0 | 73.8 |
| INPUT VOLTAGE | LOAD VOLTAGE |
| (V) | (V dc) |
| 75.0 | 75.0 |
| 80.0 | 75.0 |
| 90.0 | 75.0 |
| 110.0 | 75.0 |
| 10.0 | 75.0 |
| 1230.0 | 75.0 |
| 140.0 | 75.4 |



50 V/DIV; 20 MSEC/DIV
Figure 4-40. Ferroresonant Voltage Regulator Triac Voltage with 150 Ohm Load


50 V/DIV: 20 MSEC/DIV
Figure 4-41. Ferroresonant Voltage Regulator Triac Voltage with


Figure 4-42. Ferroresonant Voltage Regulator Gate Signal and Triac Voltage


50 VIDIV: 10 MSECIDIV
Figure 4-43. Ferroresonant Voltage Regulator Capacitor Voltage and Triac Voltage


Figure 4-44. Ferroresonant Voltage Regulator Load Voltage and Triac Voltage

## MOTOR CONTROL

For many years, induction motors were considered to be constant speed machines which provided a cost reduction and improvement in reliability.

These factors, together with the possible simplification of starting controls, have favored the use of induction motors over other types of machines. Wound rotor machines with secondary resistance and shorting means (contactors) have provided limited speed control. However, the disadvantages of finite step speed control, with its inherently poor speed regulation and incompatibility with closed-loop speed regulator operation, have eliminated this drive from consideration in most variable-speed drive applications.

With the availability of the power SCR and power triac, these limitations have been circumvented, providing an expanded field of application for induction machines. For
high performance applications, var-iable-frequency, constant voltsecond supplies have been constructed using cycloconverters and dc link inverters which minimize the power losses in the machine compatible with the greatest possible controllable speed range. However, due to the relative complexity of these drives and the resulting cost, there is an economic lower limit of horsepower when applying them. Consequently, there is a need in the power level below about 25 HP for a reduced cost speed control system. The statically controlled wound rotor induction machine can meet these requirements.

Figure 4-45 illustrates a triac phase controlled system. The control of the triacs is simply a phase control problem and has been discussed for inductive loads.

When the starting duty of a synchronous motor is such that a rotor resistor is required, the circuit

FROM SLIP RINGS


Figure 4-45. Triac Speed Control
of Figure $4-46$ can be used. During starting, $\mathrm{SCR}_{1}$ is blocking and remains so until the exciter field supply is energized and dc flows to the motor field circuit, whereupon current flows in $\mathrm{R}_{2}$ and turns on $\mathrm{SCR}_{1}$. This is similar to low starting torque starters, in which one can eliminate $\mathrm{SCR}_{1}, \mathrm{R}_{1}$, and $\mathrm{R}_{2}$ and simply short the motor field on starting [11].

No discussion of polyphase motor control would be complete without considering static motor starters. For example, a simple static motor starter is shown in Figure 4-47. The current transformer feedback level will reduce until the


Figure 4-46. Triac Synchronous Motor Starter


Figure 4-47. Triac Static Motor Starter
starting winding is de-energized as the motor comes to speed. Perhaps a more straight forward application is shown in Figure $4-48$ which is for a polyphase motor contactor. An interesting by-product of this type of static starter is that the motor can be easily plugged by using a triac with a "logic" gate and simply reversing the gate signal polarity, thereby applying de to the motor ac line terminals.


Figure 4-48. Triac Three-Phase Motor Starter Circuit

## WELDING SERVICE

## CIRCUITS [16]

The basic circuit configuration for an AC resistance welder is shown in Fig. 4-49.

SCRs in anti-parallel (or "back-to-back") configuration are used to control the power applied to the transformer primary. By precisely controlling the phase angle and number of pulses applied to the gates, a very precise control of welding power ("heat") may be obtained.

Water cooling is almost exclusively used in this service. In addition, it has become common also to water-cool the welding transformer and welding electrodes.

The Hockey-Puk method of constructing the power thryistors is the ideal configuration to use in building an assembly of two thyristors in anti-parallel for welding service. Full load on the welding transformer amounts to a virtual short circuit on the secondary. In addition, welding transformers generally have a high leakage reactance which limits' short circuit current. Therefore, if current surges due to transformer


Figure 4-49. Power Circuit for Resistance Welder Using Solid-State Contactor
saturation can be avoided, there is no need to provide a reserve for overloads when determining the current the thyristors may have to handle. Thus, by cooling the Hock-ey-Puks on both sides, they may be operated at a high current density without concern for the possibility of damage due to a current overload. In addition, their pressureassembled construction eliminates the possibility of device degrada
tion due to deterioration of internal solder bonds. This degradation is caused by repeated heating and cooling resulting from the cyclical welding load.

## Hockey-Puk Assembly for Welder Service

A representative water-cooled assembly of two large thyristor Hock-ey-Puks is shown in Fig. 4-50. It will be seen that a water-cooled pad


Figure 4-50. Water-Cooled, Hockey-Puk SCR AC Switch On a Coolant Manifold
is provided next to each HockeyPuk pole piece. These remove the heat and, together with the copper tubing which joins each pair of pads, provide the means to bring the electric current into and out of the assembly. Terminations for electrical cables and inlet and outlet water connections are provided. A sufficient length of non-conductive tubing to permit connecting the water paths of the two pairs of water-cooled pads in series is incorporated in the manifold which also serves as a base for the assembly.

When two 470 ampere average Hockey-Puk SCRs are used in this assembly, the highest ac line current that may be handled continuously is 1200 A RMS. This is under conditions of $40^{\circ} \mathrm{C}$ maximum inlet water temperature at a flow of at least 1.2 gallons per minute.

## Welding Service Rating Curves

In welding service current is required in trains of pulses as shown in Fig. 4-51. Frequently these trains have a longer off than on period. (Duty cycle less than 50 percent.) Advantage can be taken of this operating condition to control greater amounts of current than 1200 A during the on periods. Current carrying capability during such operation is enhanced by the water cooling system, which tends
to rapidly carry heat away from the semi-conductor devices. Thus, the junction cools down rapidly between power applications.

Fig. 4-52 gives the rating of a variety of AC switches shown in Fig. 4-50 for various duty cycles. The conditions covered by the curves in Fig. 4-52 embrace those usually found in welding service. Two variables are considered; percent duty cycle and number of conducting cycles in each pulse train. For example, consider an application requiring a train of 36 cycles for each weld at a rate of ten welds in one minute. This represents a duty cycle of 10 percent ( 36 cycles of current flow out of every 360 cycles of the 60 Hz power source). Reading from Fig. 4-50 (by interpolating between 20 and 50 conducting cycles), it is seen that the solid state contractor can handle up to 2000 amperes RMS, under these conditions.

The curves shown in Figure 4-52 demonstrate that with the variety of Hockey-Puk thyristors available, a wide range of welding applications is suitable for thyristor control.

## Protection Considerations

It was mentioned that current surges due to transformer saturation should be avoided. Some of the steps which can be taken in


Figure 4-51. Typical Welding Current Waveform


Figure 4-25(a) and (b). Welder Service Rating Curves for Thyristor AC Switch (Type 470A95A)



Figure 4-52(c) and (d). Welder Service Rating Curves for Thyristor AC Switch (Type 470A95A)


Figure 4-52(e). Welder Service Rating Curves for Thyristor AC Switch
equipment design to accomplish this are:
A. The thyristors should be triggered so that the initial load current pulse is of opposite polarity to the last one in the previous pulse train.
B. On pulse trains of 5 or more cycles, the initial pulse should be phased back to 90 electrical degrees. All other pulses (positive and negative) should be phased full on. (Advancing the pulses following the initial one in a controlled, repeatable fashion until full advance is reached will further minimize current surges.)
C. On shorter pulse trains, where all current pulses must be phased full on in order to obtain the desired amount of heat
from the welding current, the welding transformer must be designed for a low magnetizing current and the flux density must be held to a maximum of about 70 percent of the saturation level so that inrush current is held to a minimum.
The reverse voltage rating of the thyristors must be sufficiently high to avoid false triggering of the thyristors due to line voltage transients. As a further aid to prevent false triggering, transient voltage suppression devices should be included in the complete system design. Selenium transient overvoltage protectors (KlipSels) are particularly useful. To avoid triggering due to $\mathrm{dv} / \mathrm{dt}$, a series-connected capacitor-resistor, "snubber network" should be connected across anti-parallel thyristors.

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Crydom was the originator of the solid state relay. The product line now includes photo-isolated SSR's ranging from 2 Amp, PC-board mounted units to 40 Amp SSR's. Several series employ integral heat radiators to increase ratings. Newer products include input/output switches (extreme left, and right of picture) which are used to interface microprocessors and microcomputers with the higher power equipment they control.

## Solid State Relays and Contactors

Widespread use of Solid State Relays (SSR's) in standard packages has developed in recent years. Although SSR's are still usually more expensive than the equivalent elec-tro-mechanical relays, they have several distinct operational characteristics which give them overall advantage in difficult applications.

SSR's are used in applications which require long life, smooth (RFI free) switching characteristics, ability to be driven directly from low level integrated circuit signals, or extreme shock and vibration resistance. These applications include both the replacement of electro-mechanical relays and discrete component solid state switch-
ing circuits for control of motors, heaters, lamps, transformers, contactors, valves, and solenoids.

## Solid-State Relays

A solid-state relay, in terms of its function in a circuit, is identical to an electro-mechanical relay. It has input or control terminals and output or power terminals with a certain electrical isolation between input and output circuits. However, this is a superficial similarity. The differences in the principles of operation are shown in Figure 5-1. In the electro-mechanical relay, the coupling is achieved magnetically and in the very common type of


Figure 5-1. Solid-State Relay Block Diagram
solid-state relay shown, the coupling is achieved by light.

In general, solid-state relays provide only single-pole operation, because most of the cost is in the output pole, not in the control, and little economy can be achieved by using extra power semiconductors with a single control. The solidstate relays described here have normally open contacts, but because of the easy interface with low level controls, a normally closed function can easily be achieved in the control circuits by the use of a single inverting stage in the input circuit.

Figure 5-2 shows the RMS surge current rating of three series of solid-state relays, as a function of time. This is very important when the relays are being used to control high inrush current loads such as motors, particularly when the motor has a high inertia load.

The solid-state relay is more complex than the electro-mechanical relay, but this complexity allows the solid-state relay to perform more sophisticated functions, particularly with respect to a welldefined closing angle, delay time, and total closed time. However, before discussing the specific uses of a solid-state relay, the characteristics of this type of device will be reviewed. Typical input and output characteristics are shown in Figures $5-3$ and 5-4. Table V-I lists the specifications for three typical series of solid-state relays.

Solid-state relays are available in a wide combination of output currents and voltages with ac or dc control. The types with dc control can be selected for low ( 3 to 32 V dc) or high ( 80 to 140 V dc ) voltage operation. The low voltage types can be operated directly from low level logic circuits without an intermediate amplifying stage.


Figure 5-2. Solid-State Relay Surge Current Ratings



Figure 5-3. Solid-State Relay Signal Current Drain


Figure 5-4. Solid-State Relay Load Current Rating

Table V-I. Typical Solid-State Relay Electrical Specifications

| Characteristics |  | Package Style |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | Series 1 | Series 2 | Series 3 |
| OUTPUT CHARACTERISTICS |  |  |  |  |
| AC Line Voltage Range | VAC | 90-480 | 20-240 | 20-240 |
| Max. Load Current Ratings | Amps | 40 | 8 | 2 |
| One-Cycle Capability | Amps Peak | 630 | 120 | 55 |
| Overload Capability: 1 Sec | Amps Peak | 112 | 42 | 14 |
| Max. Contact Voltage Drop @ Rated Current |  | 1.6 | 1.6 | 1.2 |
| "Off-state" Leakage Current | milliamps | 8 | 4 | 1 |
| Min. Current | milliamps | 20 | 20 | 5 |
| Response Time: DC Signal |  | Max. 1/2 cycle (next zero cross) : no bounce |  |  |
| Isolation: Output-to-Input | VAC | 1500 or 2500 | 1500 | 1500 |
| dv/dt |  | $100 \mathrm{~V} / \mu$ Sec. min. |  |  |
| CONTROL SIGNAL DC Models |  |  |  |  |
|  |  |  |  |  |
| Control Signal Range |  | $0 \pm 32 \mathrm{VDC}$ | $0 \pm 8 \mathrm{VDC}$ |  |
| Pick-Up $\left(-30^{\circ} \mathrm{C}\right.$ to $\left.+80^{\circ} \mathrm{C}\right)$ | max. VDC | 3.0 | 3.5 |  |
| Drop-Out ( $-30^{\circ} \mathrm{C}$ to $+80^{\circ} \mathrm{C}$ ) | min. VDC | 1.0 |  |  |
| Input Impedance | Ohms | 1500 | 225 |  |
| AC Models |  |  |  |  |
| Control Signal Range | VAC | 0 to 280 | not available |  |
| Pick-Up ( $-30^{\circ} \mathrm{C}$ to $+80^{\circ} \mathrm{C}$ ) |  |  | not available |  |
| Drop-Out ( $-30^{\circ} \mathrm{C}$ to $+80^{\circ} \mathrm{C}$ ) |  |  | not available |  |
| Input Impedance |  |  | not available |  |
| Isolation: Input-to-Output; Input-to-Base |  | Opto-isolated, 1500 VAC, $10^{10}$ ohms DC |  |  |
| Capacitance: Input-to-Output |  | 8.0 pF, max. |  |  |
| Dimensions (see p. 211) | inches | $2.2 \times 1.7 \times 0.9$ | $1.7 \times 0.8 \times 0.8$ | $1.2 \times 0.8 \times 0.4$ |
| Weight | OZ. | 4 | 1.3 | 0.6 |
| Operating Temperature Range |  | $-30^{\circ} \mathrm{C}$ to $+80^{\circ} \mathrm{C}$ |  |  |

All solid-state, SPST-N.O. line power applied to the load only at zero-voltage crossover, and interrupted only at zero-current crossover.

The solid-state relays described are suitable for ac contact operation only. This is because of the nature of the semiconductor switches used in the output circuit. These switches are thyristors which have to be reverse-biased for a finite time to regain their blocking capability; in an ac circuit, this occurs naturally every half cycle, but in a dc circuit, the reverse bias for the output switch, has to be generated by special circuit configurations.

Figures 5-3 and 5-4 describe the input characteristics and the tem-
perature limitations on the output current of a relay rated 25 A . Because the output switch is a semiconductor, special precautions have to be taken to ensure that the maximum junction temperature of the semiconductors is not exceeded.

The control provided by solidstate relays can be very much more precise than when an electro-mechanical relay is used. This is mainly because there are no mechanical lags in the solid-state relay. Also, because there is no movement of contacts, there is absolutely no con-
tact bounce. In addition, because semiconductor switches react instantaneously to a trigger signal, there need be no significant delay between the application of a trigger signal and the operation of the output switch.

On the other hand, by the proper configuration of internal control circuits, the application of a trigger signal to the output switch, can be delayed relative to the application of an input signal. In the solid-state relays discussed here, this feature has been included so there is a variable delay between the input and trigger signals which ensures that the output switch always closes at voltage zero (zero voltage switching control). This is a very important and desirable feature. Not only is the closing angle totally defined, but by switching on at voltage zero, radio frequency interference (RFI) is eliminated. This is a very important consideration
when the relay is associated with equipment such as computers and on-line process controls, which can be very sensitive to electrical noise. This feature is shown in Figure 5-5.

The control signal is applied, but the load voltage does not appear until the next voltage crossover. When the control signal is removed, the output switch remains closed until the next current zero. For this example, the load is resistive, and the switch opens at voltage zero because the current and voltage are in phase. However, if the load is reactive, then the switch (because the semiconductors remain on until the current reverses) remains closed until current zero, as shown in Figure 5-6, once again eliminating RFI caused by rapidly changing currents. Examination of the contact voltage waveshapes shows that when the contacts open, with reactive load, the contact voltage steps up to the supply voltage very


Figure 5-5. Solid-State Relay DC Control Signal and Resulting AC Load Voltage

## INTERNATIONAL RECTIFIER <br> ISR



Figure 5-6. Waveforms for Solid-State Relay Controlling Inductive Load
rapidly, imposing a high $\mathrm{dv} / \mathrm{dt}$ on the output switch.

The output switch is rated for a critical $\mathrm{dv} / \mathrm{dt}$ of $100 \mathrm{~V} / \mu \mathrm{sec}$ minimum to rated voltage at maximum junction temperature. For the majority of applications with the power factors normally encountered, the voltage switched to will be less than half the peak of the supply voltage and the output switch will be operating at less than rated junction temperature. Under these conditions, the dv/dt capability will generally be in excess of $400 \mathrm{~V} / \mu \mathrm{sec}$. In very few applications will the circuit $\mathrm{dv} / \mathrm{dt}$ be this high. In those applications where $\mathrm{dv} / \mathrm{dt}$ is a problem, a snubber network can be connected across the output terminals as shown in Figure 5-7.

One application for the solidstate relay is energy control for heating loads such as furnaces and commercial heating. To control this
type of load, which has a fairly high thermal inertia, the pulse burst modulation technique is used. In pulse burst modulation when the output switch is closed full supply voltage is applied to the load until the switch is opened. By varying either the duration of the 'burst' of energy or the time between 'bursts' or a combination of the two, the average amount of energy can be controlled. The solid-state relay with its zero voltage switching and precise control makes an ideal element for this type of control. Typical pulse burst modulation control waveshapes are shown in Figure 5-8.

A very simple control technique would be to allow the load temperature to fluctuate between an upper and lower limit by closing the output switch at the lower limit and opening it at the upper limit. The absolute limits would be a function


Figure 5-7. Solid-State Relay with Snubber Network
of the heating and cooling rates of the load relative to the possible nearly half cycle delay and extension of the conduction period (if the load is inductive) due to the zero voltage turn on and zero current turn off of the solid-state relay.

Fig. 5-9a shows 3 package styles which form an SSR product line suitable for a vast range of applications.

Solid-state relays are being widely used in traffic signal controls, where the reliability of the relays and the zero voltage turn-on makes them ideal. A typical three-relay module for traffic signal control is shown in Figure $5-9 \mathrm{~b}$, with the relays mounted directly to a heat dissipator. This is possible because the relay base plate is isolated from the internal control and power circuits.

These relays are very well suited to computer, machine control, and process applications. The compatibility of the relays with logic circuit outputs allows them to be driven
directly from low level circuits and the absence of RFI generation eliminates the possibility of cross-talk between power and control circuits. Along with the precise control of output voltage duration, sophisticated timing and sequencing of power switching can be achieved, taking the guesswork out of the operation of many machine tool and process control systems.

Because they do not create ares, solid-state relays are especially well suited for application in explosive environments and hospital operating rooms, although in this particular case, it must be recognized that in the off condition, the solid-state relay can have leakage currents of 4 or 5 mA (depending on the voltage classification). If necessary, relays can be selected to have significantly lower leakage currents, particularly if the junction temperature is limited to some level below its rated value.


Figure 5-8. Waveforms for Pulse Burst Modulation Operation of Solid-State Relays

## Solid-State Contactors

Basically a solid-state contactor can be described as an extension of a solid-state relay. However, due to the higher ratings provided, contactors are constructed with discrete components rather than junctions contained in a single package. In one type the main power switching components are electrically isolated from the frame of the contactor. The insulating material used to accomplish this has excellent thermal properties ensuring good heat transfer to the main heat dissi-
pators. The construction of a typical solid-state contactor is shown in Figure 5-10.

The solid-state contactor has excellent surge capability for those types of loads which require high starting currents (e.g., induction motor starters which draw high currents until the machine is running close to its normal speed). The rated surge current/time characteristics of a range of solid-state contactors are shown in Figure 5-11.

Like the solid-state relay, the solid-state contactor is designed to


Figure 5-9a. Solid-State Relay Product Line


Figure 5-9b. Typical Three Solid-State Relay Assembly.


Figure 5-10. Typical Solid-State Contactor


Figure 5-11. Solid-State Contactor Surge Current Ratings
close at a voltage crossover and, because of the output thyristors, to open at a current zero. An excellent example of the difference in operation between solid-state and elec-tro-mechanical contactors is shown by the oscillograms in Figure 5-12.

The general specifications for a range of solid-state contactors are shown in Table V-II. Three typical applications of solid-state contactors are shown in Figures 5-13, 5-14 and 5-15.

There are many other applications for solid-state contactors, but most of these are extensions of the three described in Figures 5-13, $5-14$ and $5-15$. In many systems, where the source impedance is sufficient to limit the available fault current to within the capabilities of the contactor, it can be used with no back-up protection (fuses or
mechanical contacts). In this instance, a detection system is provided which consists of a di/dt detector and an absolute current amplitude detector. This combination allows the system to anticipate a fault without reacting to sudden load changes (as a di/dt detector alone might). The control signal to the contactor is removed only when the detector recognizes that both the di/dt and the current amplitude have exceeded allowable limits. When this condition is reached, the control signal is removed and at the next current zero, the switch opens allowing just the initial half cycle of fault current to flow. A typical sequence is shown in Figure 5-16.

## Solid-State Switches

One application for solid-state switches is in a system for vehicle

(a) SOLID STATE CONTACTOR OPERATION. NOTE ZERO CROSSING TURN ON AND OFF BOUNCE FREE OPERATION, AND FAST RESPONSE.

(b) ELECTROMECHANICAL CONTACT CLOSURE. NOTE NON-ZERO CLOSURE AND EXTENSIVE CONTACT BOUNCE.

Figure 5-12. Solid-State Contactor Operation
Table V-II. Typical Solid-State Contactor Specifications



THE CONTACTOR PROVIDES ELECTRICALLY AND ACOUSTICALLY NOISE-FREE OPERATION IN AN ON-OFF OR TIME PROPORTIONING MANNER WITH A TIME BASE AS SHORT AS ONE SECOND.

Figure 5-13. Solid-State Contactor Temperature Control System


THE TWO-POLE CONTACTOR SERVES AS A LONG LIFE MOTOR STARTER CONTROLLED FROM ANY LOW POWER, REMOTE SOURCE. A MECHANICAL DISCONNECT IS NORMALLY USED IN ALL THREE LINES AS A SAFETY DISCONNECT. TWO LEG SWITCHING IN THE CONTACTOR WORKS WELL FOR ALL DELTA AND FLOATING NEUTRAL WYE LOADS. THREE SINGLE POLES MUST BE USED FOR A GROUNDED NEUTRAL WYE LOAD.

Figure 5-14. Solid-State Contactor Three-Phase Motor Starter Circuit


Figure 5-15. Solid-State Contactor with Pushbutton Control


Figure 5-16. Waveforms of Solid-State Contactor Fault Detection Circuit Operation
propulsion and material handling. A special type of linear induction motor is used in which the windings are located in 18 -inch sections between the tracks on which the vehicle moves. On the underside of the vehicle, a metal plate acts as the member in which current can be induced to provide linear induction motor action between an excited
winding and the vehicle. The windings located between the tracks are spaced several feet apart. Thus, the vehicle can be propelled by impulse propulsion simply by sequentially energizing the linear induction motor windings in a fashion similar to that shown in Figure 5-17.

The advantage of this type of switching is the minimizing of


Figure 5-17. Linear Induction Motor System
power demand from the ac source, since the majority of the induction motors need not be energized simultaneously. This tends to average out the power demand and reduce the overall installation cost and operating cost of the system. The requirements for the static switch needed to energize the system are interesting.
A. It must be capable of being operated remotely from a centralized computer which senses the position and the destination of the cars and dispatches them by energizing the proper motors.
$B$. The signaling must be isolated from the power circuit to prevent transients.
C. The switch must be low cost because of the considerable number of switches required in a large system. For instance, when using the system in a large airport baggage handling unit, up to 50,000 switches might be required.
D. The switch must employ a zero voltage triggering system to minimize radio interference and the filtering cost of the system.
E. The switch must be small to enable it to be located remotely with the motor winding.
F. It must be completely sealed, since it will not be packaged in an electronic rack or equipment cabinet.
G. This switch must be able to operate in a high ambient temperature, because it will be located thermally close to the motor winding.

A typical single-phase switch, which meets the above requirements, is shown in Figure 5-18. The simple solid-state power switch consists of a triac, $\mathrm{TRIAC}_{1}$, a gate drive source, $\mathrm{R}_{1}, \mathrm{C}_{1}$, and an on-off switch, $\mathrm{S}_{1}$. With $\mathrm{S}_{1}$ closed, the triac gate is shorted to main terminal 1 , and the solid-state switch is off. With $S_{1}$ open, power line voltage is applied through $\mathrm{R}_{1}$ and $\mathrm{C}_{1}$ to the triac gate, triggering TRIAC 1 into conduction. $\mathrm{S}_{1}$ may be any bidirectional switch, mechanical or solid-state, with an on-state voltage drop less than the minimum gate-voltage-to-trigger of TRIAC 1 .

An additional requirement of the single-phase switch is that it must have its power components electrically isolated from the heat sink. For instance, it might be possible to package the linear induction motor winding and the switch in a common heavy metal case to be imbedded between the rails, the


Figure 5-18. Solid-State AC Switch Circuit
case acting as the heat sink for the electronic switch. It would not be allowable from a safety standpoint to have the case electrically hot.

These requirements suggest the applicability of the PACE/pak hybrid circuit techniques for this type of application. Certainly alumina, beryllium oxide, and boron nitride substrates are economically feasible in large quantities for hybrid circuits of a given type. Also passivation techniques for SCR junctions make their applicability to such hybrid circuit constructions quite feasible. Since these substrates are readily available with moly-manganese metallization for connection purposes, and since the moly-manganese provides the proper thermal co-efficient of expansion to interface with the silicon of the semiconductor, thermal fatigue difficulties can easily be overcome. The requirements for this type of application are not far from the requirements for electric heating control. The applicability of triacs in this type of control is also evident. Other applications of the same techniques take advantage of the common circuitry capability and the large volume, low cost of such a hybrid approach.

## Aircraft Power System

The trend in advanced high performance aircraft is toward more sophisticated missions which require much more complex electrical and electronic systems. Complex digital avionic systems require clean (transient free) electric power, thus adding emphasis to electromagnetic compatibility and interface compatibility between all signal systems and digital computers.

The approach must simplify circuitry, combine functions, separate signal and power switching requirements, and eliminate any unreliable features of switching control and protective devices used in circuit techniques. The application of semiconductor technology to aircraft electrical distribution systems, however, has been slow to catch on. Some of this can be attributed to the application approach that has generally been made. A number of solid-state devices have been placed on the market with the idea of providing a solid-state device to replace an electro-mechanical device on a part-for-part basis. This approach has some obvious drawbacks since in most aircraft electric control circuits the switching logic is performed at the power level. Because of the voltage drop and power dissipation characteristics of semiconductor devices, this approach results in a very inefficient system and makes it impossible to meet the voltage drop requirements of Military Specification MIL-W5088 for Aircraft Electric Distribution Systems. However, semiconductor devices have advantages such as high reliability, long life, and small size, which, if properly applied, can provide the urgently needed improvements in aircraft electrical distribution systems.

Work was initiated specifically toward the development of an advanced electrical system for aircraft. This type of system has been given several names: "Contactless Switching," "Solid-State Switching," and "SOSTEL" (Solid-State Electric Logic), but they all represent an application of semiconductor technology to the management and control of aircraft electric
systems. Figure 5-19 is a block diagram of an aircraft electrical system. Figure $5-20$ is representative of conventional aircraft electrical circuits and is presented to highlight the fact that logic functions are performed at the power level. In the advanced system, emphasis is placed on separating power switching from signal switching and on switching power through a minimum number of semiconductor devices (see Figure 5-21). This not only minimizes the voltage drop between the source of power and utilization equipment, but also provides efficient power control, since power dissipation is held to a minimum. Lower power dissipation means that less heat sinking is required, and therefore size and weight are reduced.

A concept is required which separates power and signal switching
and utilizes solid-state devices to perform all of the switching and circuit protection functions normally performed by electro-mechanical switches, relays, and circuit breakers. The system is composed of three basic building blocks: 1) signal sources, 2) control logic, including bus monitoring and built-in testing, and 3) power controllers. Signal sources are transducers which provide a digital output. They are used to sense controlling functions such as temperature, pressure, mechanical motion, etc. Their output signals are fed into the control logic unit where they are correlated in a prescribed manner to provide signals to control the power controllers. The logic switching is performed by standard integrated circuit NAND/NOR gates to provide maximum reliability with minimum space and weight. The fan-out cap-


Figure 5-19. Aircraft Electrical System Block Diagram


Figure 5-20. Portion of a Conventional Aircraft Electrical System


Figure 5-21. Portion of a Solid-State Aircraft Electrical System
ability provided by multiple-phase switches and relays is provided by the integrated circuit and is performed at the signal level instead of at the power level. This reduces considerably the number and size of wires needed to gather intelligence from the various controlling functions.

The flow of power from the power sources to the bus and from the bus to the loads is controlled by power controllers. Separation of power switching and signal switching provides high system efficiency and makes it possible to meet the voltage drop requirements of the MIL Specs. The flexibility of the system permits the incorporation of an automatic bus monitoring system which permits optimum loading on the source supplying power. By assigning priorities to various loads in the airplane, it becomes possible to operate the emergency source at its optimum capacity. A technique is included to perform preflight go-no-go tests on the low level portions of the system which are made up of signal sources and data handling equipment. Bus controllers and power controllers are not checked by the built-in test circuitry and are actually inhibited while the built-in test feature is in operation. However, they are checked as part of subsystem functional checks. A digital indicator indicates a faulty signal source during the short and open test and a faulty input buffer card during the input buffer test. A typical solidstate electrical system of this type is shown in Figure 5-21.

An alternative and even more advanced solid-state electrical system is shown in Figure 5-22. In this system, the control signal sensing
and the power switching approach remain essentially unchanged. The change occurs in the method of handling and processing the control data which is by remote multiplexing the input terminals located in close vicinity to large groups of signal sources, thus allowing a significant reduction in the length of wires required to gather control information. These terminals monitor each signal source and upon command from the Master Control Unit (MCU), code and serially transmit the status of each signal source through the multiplex transmission data line. The MCU decodes the data from the input terminals, solves the switching equations, and according to instructions permanently stored within its memory, transmits coded output data over the multiplex data transmission line to the properly addressed output terminal. The MCU contains a nondestructable read only memory in which are stored all control instructions and the switching equation associated with the control of power to each individual load. Changes in control logic can be accomplished by reprogramming the MCU with a paper or magnetic tape, thereby eliminating the need to make any wiring changes in the aircraft. Upon malfunctioning of the operating unit, the standby MCU is automatically switched into operation. The two MCUs are interchangeable. The power controllers for these systems must be capable of switching electric power in a system exhibiting characteristics described below and controlled by a $5 \mathrm{~V}, 10 \mathrm{~mA}$ de signal supplied by the control logic unit.

The load switching power controllers are used between the bus


Figure 5-22. Portion of an Advanced Solid-State Aircraft Electrical System
and the utilization equipment to provide control current limiting and circuit protection, while the bus switching controllers are used only to connect power sources to the bus. The requirements for these power controllers are isolation be-
tween the control and the power circuits, operating efficiency of $95 \%$ minimum, voltage drop of 0.5 V max dc ( 1.5 V max ac), leakage current of less than $10^{-4} \mathrm{amp}$ eres at maximum temperature, operating ambient temperature
range of $-54^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$, and no external power supply to be required. The ac voltage is allowed to swing between 60 V RMS and 180 V RMS. The ac units must also control loads exhibiting a power factor between 0 lagging and 0.4 leading. In the dc power switches, the power switching element is an N-P-N silicon power transistor. The ac power controller contains a thyris tor power switch, power supply, driver, circuitry for zero-cross-over turn-on, current sensing, and circuit protection. This is shown in block diagram form in Figure 5-23 and in more detail in Figure 5-24. The anti-parallel connected SCRs could also be a triac with the proper electrical characteristics.

The bus switching controller performs the function of a relay only. The ac bus switching power controller block diagram is identical to
that shown in Figure 5-24, except it does not contain the current limiting and the circuit protection circuitry, but it does include a lockout feature that is not included in the ac load controller.

In either case, the overload requirement for the ac controllers can be high compared to the steadystate rating. As an example, in a typical 20 KVA system, fault currents of 350 amperes per phase have been recorded. Therefore, very large semiconductor chips must be used in the units. The required ac power controller trip characteristics are shown in Figure 5-25

Although packaging efficiency is an important factor in determining the size of the power controller module, the power dissipated within the module is of utmost importance. To prevent the junction temperature of the devices within the


Figure 5-23. Aircraft AC Power Switch and Control Circuit


Figure 5-24. Aircraft AC Load Controller
module from exceeding their maximum ratings, the heat generated within the module must be removed. Devices with low current ratings will present no problem, but the high current devices must be attached to an external heat dissipator. Since the junction tempera-
ture of the main switching devices (triacs or power SCRs) is most critical, the thermal resistance between these devices and the module surface must be low.

To obtain a small package size, integrated circuits, transistor, SCR and triac wafers, and thin film tech-


Figure 5-25. Aircraft AC Power Controller Characteristics
niques must be used, as shown in Figure 5-26. In this package, the logic elements are located toward the top of the package, and the large, vertical internal connection posts are available to support and connect the logic to the power functions. A more detailed outline of the internal assemblies is shown in Figure 5-27. A function requiring both isolation and current sensing for the desired trip characteristics can be rather space-limiting. The overall outside dimension of this cube (Figure 5-28) is approximately one inch ( 25.4 mm ) square. The thermal considerations and the effect of the temperatures on the power chip can be limiting in the design. Table V-III lists required thermal resistances for various current ratings of controllers. In examining this data, it should be apparent that one of the assumptions for determining the required thermal
resistances is a maximum allowable junction temperature approaching $170^{\circ} \mathrm{C}$. But many logic-triacs are advertised at a maximum allowable junction temperature of $125^{\circ} \mathrm{C}$. However, by modifying the process and geometry of the junction assembly devices have been made which actually will operate quite reliably and satisfactorily at $175^{\circ} \mathrm{C}$ junction temperature with an allowable reapplied dv/dt up to 100 volts $/ \mu \mathrm{s}$. This not only permits the small size of the package as seen in the previous figures, but also permits operation under the extreme power factor conditions described. An extreme case for this design in terms of power rating might require a power device even larger than the 200 ampere power logic triac chip size - in this case, two power SCRs are used.

Since reliability was so heavily stressed in the earlier discussion of


Figure 5-26. Aircraft AC Power Controller Module
the system requirements, it is certainly of interest to show a reliability study of a typical ac controller with estimated failure rates (see Table V-IV). The inordinately high failure rate of the SCRs shown is estimated on a very conservative basis because no transient suppression was involved or associated with the circuitry, and also because of the many unknowns associated with a very new type of packaging. However, even with these conservative figures, it can be seen that the failure rate of the devices and of the overall system is very low.

The marriage of power devices and low level solid-state logic elements in hybrid circuitry for reliable, small, efficient power control opens a new era in the field of power control development. Where circuits can be designed for high volume usage or common circuits can be used for several smaller volume applications, the cost of present systems can be greatly reduced. Where low level logic hybrid circuitry is marginally economically feasible, high power level hybrid circuitry is, without question, economically feasible.


Figure 5-27. Aircraft AC Power Controller-Internal Details


Figure 5-28. Aircraft AC Power Controller - Dimensions

Table V-III. Aircraft AC Power Controller Thermal Resistance Requirements

| POWER CONTROLLER TYPE | JUNCTION TO CASE THERMAL RESISTANCES REQUIRED FOR VAD CONTROLLERS, ASSUMING $150-170^{\circ} \mathrm{C}$ CHIP TEMP. ${ }^{\circ} \mathrm{C} / \mathrm{W}$ | PRESENT THERMAL RESISTANCES ( $\mathrm{R}_{\mathrm{Gjc}}$ ) ACHIEVABLE BY <br> INTERNATIONAL RECTIFIER (NO ELECTRICALISOLATION) ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| :---: | :---: | :---: |
| 75 AMP AC <br> BUS CONTROLLER | 0.16 TO 0.34 | 0.095 TO 0.115 |
| 35 AMP AC LOAD CONTROLLER | 0.32 TO 0.70 | 0.3 TO 0.4 |
| 10 AMP AC LOAD CONTROLLER | 1.5 TO 2.8 | 1.0 TO 1.5 |

Table V-IV. Aircraft AC Power Controller Failure Rate Data

| QTY | COMPONENT | FAILURE RATE SOURCE | FAILURE RATE |
| :---: | :---: | :---: | :---: |
| 3 | INTEGRATED CIRCUITS @ 0.020 | 1 | 0.060 |
| 14 | RESISTOR, FILM @ 0.007 | 2 | 0.098 |
| 2 | CAPACITOR, CERAMIC@ 0.038 | 2 | 0.076 |
| 2 | SCR @ 0.102 | 2 | 0.204 |
| 2 | DIODES, GP@ 0.005 | 2 | 0.010 |
| 6 | TRANSISTOR@ 0.010 | 2 | 0.060 |
| 2 | SCR @ 1.3 | 6 | 2.600 |
| 4 | TRANSFORMERS@ 0.2 | 2 | 0.800 |
| 1 | RECTIFIER (BRIDGE)@ 0.020 | 2 | 0.020 |
| 100 | LEAD BOND@ 0.00007 | 3 | 0.007 |
|  | SUBSTRATE, FRAME \& COVER | 4 | 0.0035 |
| 24 | EXTERNAL LEADS @ 0.00005 | 5 | 0.0012 |
| TOTAL FAILURERATE 4.886 |  |  |  |

SEE DISCUSSION
NORMALIZED MIL-HDBK-217A MINUTEMAN LEVEL, FAILURE RATES.
ULTRASONIC LEAD BOND ESTIMATE BASED ON TELEDYNE INDUSTRY DATA
BEST ENGINEERING ESTIMATE,
WELDED TERMINATION ESTIMATE BASED ON TELEDYNE AND INDUSTRY DATA
. INTERNATIONAL RECTIFIER NORMALIZED LIFE TEST DATA.

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International Rectifier PACE/pak (Passivated Assembled Circuit Elements) are packaged circuit functions which replace discrete devices. For example, the unit above (center) is a 42.5 Amp single phase hybrid bridge with free wheeling diode. It is used in place of a separate assembly requiring the three SCR's and three diodes shown, plus additional heat sinking.

## DC Power Conversion

Probably the most common method of adjusting direct voltage by phase control is by using reverse blocking thyristors in a conventional rectifier circuit and delaying the start of current conduction through them. By this means, the direct voltage can be reduced from the value obtained without phase control to some other desired value. If the start of conduction is delayed sufficiently, the average output voltage will be reduced to zero.

The average voltage which will appear across the load for a given phase control angle depends upon the rectifier circuit and the type of load. Performance with a purely resistive and also with a highly inductive load can easily be analyzed, and in this way, insight is provided with respect to circuit performance when the load is partly resistive and partly inductive. It is also useful to consider performance when the load is capacitative, has a large counter-EMF, or is provided with a free-wheeling diode. Table VI-I shows a number of typical circuits.

In some circuits, half of the thyristors are replaced by rectifier diodes which cannot be phase controlled. In these hybrid or half-controlled circuits, the voltage reduction for a given phase control angle, or angle of retard, will be different than in conventional circuits where all the rectifying devices are thyristors [1].

## Biphase Circuits

As a simple example of a phase controlled rectifier circuit, consider
the single-phase, full-wave, centertap circuit (more correctly known as the biphase circuit) shown in Figure 6-1. Output direct voltage waveforms for several angles of delay, or phase retard, $a$, are shown in Figure 6-2 for the cases of resistive load and highly inductive load. Angle of phase retard $a$ is measured from the point where current conduction through the rectifying device would naturally begin if a device with no forward blocking capability (i.e., a rectifier diode) were being used. A thyristor may be made to operate in the same manner as a diode by pulsing the gate so that the thyristor conducts the instant that anode voltage becomes positive with respect to the cathode (anode is forward biased). By delaying the triggering pulse, the thyristor blocks the more positive ac phase so that the preceeding phase, although it is at a lower potential, remains connected to the load. When the delayed triggering pulse finally appears, load current is commutated (or switched) to the thyristor triggered, and this connects the load to the ac phase having the highest voltage at that instant. However, during the time when the triggering pulse is delayed by the angle $a$, the voltage across the load is less than if conduction had occurred at the earliest possible moment. In this way, the average voltage across the load is reduced by phase control.

When the load is purely resistive, load current will be a faithful reproduction of load voltage, as illus-

Table VI-I. Circuits for DC Loads


Table VI-I. Circuits for DC Loads (Continued)

| CIRCUIT | RELATIVE POWER OUTPUT | $\begin{aligned} & \text { TYPE } \\ & \text { OF } \\ & \text { LOAD } \end{aligned}$ | CONTROL RANGE \% | TYPICAL USES |
| :---: | :---: | :---: | :---: | :---: |
|  | 2 | All | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heating Elements Lamp Intensity Control Adjustable \& Regulated Power Supplies <br> Motor Speed Controls Magnet Strength Control |
|  | 2 | All | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heating Elements Lamp Intensity Control Adjustable \& Regulated Power Supplies <br> Motor Speed Controls Magnet Strength Control |
|  | 2.7 | All | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heating Elements Lamp Intensity Control Adjustable \& Regulated Power Supplies <br> Motor Speed Controls Magnet Strength Control |
|  | 2.7 | All | $\begin{aligned} & \% T_{1} \text { to } \\ & 100 \end{aligned}$ | Heating Elements <br> Lamp Intensity Control <br> Adjustable \& Regulated <br> Power Supplies <br> Motor Speed Controls <br> Magnet Strength Control |

NOTE: FWD = FREE WHEELING DIODE (BYPASS DIODE).


Figure 6-1. Biphase Circuit
trated in Figure 6-2(a). When phase control is introduced, the voltage across the load is seen to be discontinuous, and current flows through the thyristor for some interval less than the full 180 electrical degrees that it flows when there is no phase control. The time current flows under these conditions is
known as the conduction angle. Energy is stored in the inductance of the transformer each time current increases and is returned to the load as current decreases, so there is essentially no reactive voltage drop with a purely resistive load, as long as load current is discontinuous.

On the other hand, when the load is highly inductive, the load current remains continuous for all angles of phase retard. In this case, the duration of current flow through the rectifying devices remains the same as the phase retard angle is varied, but it is displaced with respect to the alternating supply voltage wave by the phase retard angle $a$ as shown in Figure 6-2(b). With an inductive load, the angle of conduction is determined by the circuit used and not by the angle of phase retard, and is often referred to as the conduction period.

(a) RESISTIVE LOAD

(b) INDUCTIVE LOAD

Figure 6-2. Biphase Circuit Waveforms

With an inductive load, the flow of current through each thyristor is essentially rectangular, assuming negligible ripple in the load current. Inductance in the ac supply (due to transformer leakage reactance, ac supply reactance, etc.) prevents the load current from commutating instantaneously from one thyristor to the next thyristor when the latter is triggered. For a brief interval, both thyristors conduct, one dropping current and the other picking it up. This interval is known as the angle of overlap, $\mu$.

The currents through two thyristors which are under-going commutation are shown in Figure 6-3. It can be seen that the total current remains constant, due to the inductive nature of the load. The length of the angle of overlap $\mu$ depends upon the magnitude of the ac supply voltage, the load current, and the inductive reactance of the circuit which carries that commutating current (the circuit comprising the two diodes and the transformer windings which feed them).

The inductive reactance of this circuit is known as the commutating reactance.

During the angle of overlap, the direct output voltage of the rectifier is the average of the voltage applied to each thyristor by the transformer windings which feed them. This is a lower voltage than would be present if the angle of overlap were zero, and so the overlap phenomenon introduces a voltage drop $\mathrm{E}_{\mathrm{X}}$, which is a function of the angle of overlap. Hence, in a given rectifier unit, it is a function of load current, proportional to $\mathrm{I}_{\mathbf{C}} \mathrm{X}_{\mathbf{C}}$, the product of current commutated and commutating reactance.

In a thyristor feeding an inductive load and operated with phase retard, the angle of overlap will be present immediately following the angle of phase retard. As phase retard is increased, the angle of overlap $\mu$ will decrease, because there is a greater voltage difference between phases when commutation begins, and this speeds up the trans-


CONDITIONS: INDUCTIVE LOAD WITH COMMUTATING REACTANCE PRESENT

Figure 6-3. Biphase Circuit Output Waveforms
fer of current from one phase to the next. However, the voltage drop due to overlap remains the same whether phase control is present or not.

In the inductive load case, although the alternating component of voltage appears across the load at large angles of phase retard, the average voltage can be reduced to zero. Zero average output voltage is obtained when $a$ is 90 degrees. In order to obtain zero voltage across the load when it is resistive, the angle of phase retard must be 180 degrees.

Expressions that give the output voltage at no load for any angle of phase retard are:
For resistive loads:
$E_{D}=E_{D O} \frac{1-\sin \left(a-90^{\circ}\right)}{2}$
For inductive loads:

$$
\begin{equation*}
E_{D}=E_{D O} \cos a \tag{6-B}
\end{equation*}
$$

In these expressions, $\mathrm{E}_{\mathrm{D}}$ is the direct output voltage, $E_{D O}$ is the output voltage without phase control (rectifying devices operated without constraint), and $a$ is the angle of phase retard in electrical degrees.

It is often convenient to express the above relationships in terms of $\mathrm{E}_{\mathrm{DO}}$ and the voltage reduction $\mathrm{E}_{a}$. For resistive loads:
$\frac{E_{D O}-E_{a}}{E_{D O}}=\frac{1-\sin \left(a-90^{\circ}\right)}{2}$

For inductive loads:

$$
\begin{equation*}
\frac{E_{D O}-E_{a}}{E_{D O}} \tag{6-D}
\end{equation*}
$$

These two expressions are plotted on linear coordinates in Figure 6-4 as curves D and A, respectively.

## Single-Phase, Half-Wave Circuits

The single-phase, center-tap circuit is actually a biphase circuit, since it is two single-phase circuits displaced by 180 degrees. The sin-gle-phase, half-wave circuit, where the number of phases is one, was not considered in the previous discussion. Where it is used to feed a resistive load (equations 6-A and 6-B apply), recognizing that for a given alternating supply voltage, the direct voltage will be one-half of that obtained with the biphase circuit, since load current flows only during every other half cycle. The halí-wave circuit is not suitable for feeding an inductive load, because the inductance demands a continuous current source; the halfwave circuit can be used successfully with an inductive load shunted by a free-wheeling diode, in which case its performance with phase control is the same as when the load is resistive.

A half-wave phase control circuit for use as a very simple battery charger is shown in Figure 6-5[2]. Transformer $\mathrm{T}_{2}$ is used to step down the input voltage. The output of transformer $\mathrm{T}_{2}$ feeds $\mathrm{SCR}_{1}$ acting as a half wave rectifier. Transformer $\mathrm{T}_{2}$ determines the rated current that can be delivered to the battery by the rating of its windings. It partially offsets the other advantages of this circuit since, although the control portion is small and consists of fairly inexpensive components, the transformer size and cost increase with the amount of current delivered. Resistor $\mathrm{R}_{4}$ is used to limit the current which can be delivered by the circuit.

The trigger circuit consists of a voltage sensor, a relaxation oscillator, and a pulse transformer. The


Per-unit no-load output voltage vs. angle of phase retard $\alpha$. (A) Average values for all rectifier circuits when all rectifying devices are phase controlled and load is inductive. (B) Average values for 6 -phase ectifier circuits when all rectifying devices are phase controlled and load is resistive or is provided with free wheeling diodes. (C) Average values for 3 -phase rectifier circuits under same conditions as in (B). (D) Average values for biphase rectifier circuits under same conditions as in (B) and (C). Also for single-phase and 3-phase hybrid bridge circuits, resistive or inductive load. (E) The RMS values for phase control of alternating voltage

Figure 6-4. Output Voltage Vs. Angle of Phase Retard


Figure 6-5. Half-Wave Battery Charger Circuit
power for the circuit is obtained from the output which is connected to the battery. Since the ability of a unijunction transistor to oscillate is controlled by the base-to-base voltage, the higher this voltage the higher the voltage required to trigger $\mathrm{UJT}_{1}$. If this voltage is sufficiently high, the period of oscillation is approximately $\left(\mathrm{R}_{1}\right)\left(\mathrm{C}_{1}\right)$. However, the zener voltage regulator, $\mathrm{BD}_{1}$, limits the voltage to which the emitter of $\mathrm{UJT}_{1}$ can rise. When the required triggering voltage of $\mathrm{UJT}_{1}$ exceeds that of the zener breakdown voltage, $\mathrm{UJT}_{1}$ can no longer oscillate and no longer produces a pulse through the pulse transformer to the gate of SCR1.

This circuit cannot oscillate unless a voltage between three volts and the cutoff voltage is present between the output terminals. Thus, it prevents $\mathrm{SCR}_{1}$ from triggering into a short circuit, an open circuit, and the presence of reverse polarity. Figure 6-6 shows waveforms for the operating circuit.

## Polyphase Rectifier Circuits

The above discussion described the performance of single phase circuits. The same principles apply to the common polyphase rectifier circuits where all rectifying devices are thyristors. For inductive loads, the Equations 6-B and 6-D for voltage output vs. phase retard angle apply to all polyphase circuits. When a polyphase rectifier circuit feeds a resistive load, less than 180 degrees of phase retard is needed to obtain zero output voltage. The generalized form of Equation 6-A is used to arrive at Equations 6-E and 6-F which calculate output voltage from polyphase rectifier circuits feeding a purely resistive load as phase retard angle $a$ is varied.

$$
\begin{aligned}
E_{D} & =E_{D O} \frac{1-\sin (a-\pi / \mathrm{p})}{a \sin \pi / \mathrm{p}} \\
& =E_{D} \frac{1-\cos [\pi / 2+(\pi-2) / \mathrm{p}]}{2 \sin \pi / \mathrm{p}}
\end{aligned}
$$



Figure 6-6. Oscillogram of Half-Wave Battery Charger Circuit

$$
\begin{align*}
& \frac{E_{D O}-E_{a}}{E_{D O}}=\frac{1-\sin \left(a-\frac{\pi}{\mathrm{p}}\right)}{2 \sin \frac{\pi}{\mathrm{p}}}  \tag{6-F}\\
& \frac{1-\cos \left(\frac{\pi}{2}+\frac{\pi-a}{\mathrm{p}}\right)}{2 \sin \frac{\pi}{\mathrm{p}}}
\end{align*}
$$

In these expressions $p$ is the number of rectifier phases. (For the biphase circuit previously discussed, $p=2$, since the circuit is actually two single-phase circuits 180 degrees out-of-phase.)

Curves B and C of Figure 6-4 show equation $6-\mathrm{F}$ plotted for all 6 -phase and 3-phase rectifier circuits, respectively. In each case, the curves are seen initially to follow the inductive load curve. The angle at which they depart from this curve, $a_{1}$, is given in Formula 6-G.

$$
\begin{equation*}
a_{1}=\frac{\pi}{2}-\frac{\pi}{\mathrm{p}} \tag{6-G}
\end{equation*}
$$

At this angle, the load current becomes discontinuous. The output voltage $E_{D}$ becomes zero at $\varphi_{2}$ in each case, as shown in Formula 6-H.

$$
\begin{equation*}
a_{2}=\frac{\pi}{2}+\frac{\pi}{p} \tag{6-H}
\end{equation*}
$$

Table VI-II gives $a_{1}$ and $a_{2}$ for various numbers of phases $p$ :

| Table VI-II. Values for Angles of |  |  |  |  |  |  |
| :---: | ---: | :---: | :---: | :---: | :---: | :---: |
| Phase Retard |  |  |  |  |  |  |

If the load includes both resistance and inductance, load current
will become discontinuous at some angle of phase retard greater than $a_{1}$ (from Table VI-II) and at this angle the voltage characteristic will no longer follow the inductive load $(\cos a)$ curve, but will follow a line which goes through zero output voltage at $a_{2}$. If the inductance of the circuit is fairly high, the change in slope of the output can be quite pronounced. This can lead to instability when the rectifier is provided with an automatic regulating system [3].

Operation With Free-Wheeling Diode
Where the load is inductive, and the large amount of ripple obtained in the usual circuits with a large angle of phase retard is not desired, one or more rectifier diodes may be used as free-wheeling diodes and placed across the load in the direction to block the flow of current from the rectifier, but to provide a path for the current flowing in the load inductance during the intervals when the rectifier output voltage is negative, as shown in Figure 6-7. This occurs at angles of $a$ between $a_{1}$ and $a_{2}$; the values for these are given for several rectifier circuits in Table VI-II. The action of the freewheeling diode reduces the ripple voltage across the load; it also causes the rectifier output current to become discontinuous although the load current is continuous.

When a free-wheeling diode is present, a rectifier behaves very much as if it were supplying a resistive load, and the curve of output voltage vs. angle of phase retard is the one shown in Figure 6-4 for the same rectifier circuit when it is feeding a resistive load.


Figure 6-7. Six-Phase Double-Y Rectifier Circuit

## Operation with Capacitive or Coun-

 ter-EMF LoadA rectifier, when supplying either a capacitive or a counter-EMF load, will tend to deliver output current in a discontinuous manner, because current can flow only near the peak of each ac wave. For current to flow, the rectifier output voltage must exceed the voltage across the capacitor, which will be more or less fully charged, depending upon the magnitude of the resistive component of the load. Other loads presenting a counterEMF, such as electrolytic cells, batteries, and lightly loaded de motors, will cause the same circuit action.

If the load includes some inductance, which is usually the case, this inductance will store energy while the current is rising to its peak value, and current will continue to flow until this stored energy is de-
livered to the load. This means that the rectifier output current will persist for a longer time than just the interval when rectifier voltage exceeds the counter-EMF, which is the case when there is no inductance. Waveforms to illustrate current flow with and without load circuit inductance are shown in Figure 6-8.

When phase control is applied, the output voltage will be reduced if the thyristors are triggered at some instant later than when the rectifier phase voltage exceeds the counter-EMF. At the same time, the energy absorbed in the inductance of the load will be less, so that the conduction angle is further reduced, causing the additional loss in voltage output. Because of this interaction, there is no simple relationship between angle of phase retard and reduction of output voltage.


Figure 6-8. Waveforms of Biphase Circuit Feeding Counter-EMF Load

When the load exhibits a coun-ter-EMF, the earliest instant a given rectifying device can be triggered depends upon the ratio of the load voltage to the peak voltage supplied by the transformer. This ratio will vary with changes in load current, which could be caused by changes in load resistance; or it will vary because of changes in the alternating supply voltage. In the designing of the triggering circuit, this effect must be recognized; long triggering pulses are desirable, so that if the thyristor is triggered before load current can flow, it will remain turned ON by the triggering pulse until some instant later when current can flow to the load. If this is not done, the rectifier may fail to deliver any power to the load when it is phased ahead in an effort to obtain maximum output.

## Hybrid Circuits

In the single-phase and polyphase bridge circuits, half the rectifying devices can be made rectifier diodes, the others remaining thyristors, and the output voltage can be controlled by phase shifting the triggering pulses for the thyristors.

The performance of these hybrid or half-controlled circuits, where the thyristors have a common cathode (or common anode) connection, can be analyzed by considering them as a phase-controlled rectifier in series with one which is not. In this group of bridge circuits (including all hybrid circuits except one of the single-phase bridge circuits), when the angle of retard at which the thyristors are operated exceeds 90 degrees, the thyristors must invert or pump back some of the power delivered by the rectifier diodes. It is theoretically possible for this action to take place all the way down to zero voltage output, at which point the angle of phase retard required is 180 degrees. In practice, it will be found that with a large amount of phase retard, the current may not completely commutate to the next phase before the phase which is commutating out becomes positive again. In this event, the thyristor which was supposed to commutate to the next phase will instead conduct full ON, and control of output by phase control will be lost. This is sometimes referred to as the "mouse
trap" effect, or as "half-waving." [2].

All hybrid circuits can be thought of as having an action similar to that provided by a freewheeling diode. For this reason, the control characteristic shown by curve D in Figure 6-4 applies.

## Single-Phase Hybrid Bridges

In the case of the single-phase hybrid bridge, two circuit configurations are possible; in one, the two thyristors are connected with the cathodes (or anodes) tied to a common point, as in the center-tap rectifier circuit, and in the other configuration, the two thyristors are connected in series, as in the doubler rectifier circuit, (see Figure $6-9$ ). Circuit action is similar, but not the same, in both cases.

With the common cathode configuration (Figure 6-9(a)), the conduction angle through all the rectifying devices remains the same as the angle of phase retard is increased. With the doubler circuit (Figure 6-9(b)), the conduction angle through the rectifier diodes increases with increasing phase re-

tard. The rectifier diodes used must be large enough to handle this increased current flow.

A disadvantage of the common cathode configuration is that, for large angles of phase retard, "halfwaving" may occur. Where the thyristors are connected in the doubler configuration, this effect is not present.

## Ripple from Hybrid Circuits

Because hybrid circuits behave as if a free-wheeling diode were present, the ripple voltage they exhibit, as output voltage is reduced by phase control, is less than in a bridge circuit using four thyristors. four. This can be illustrated by comparing the action of the singlephase bridge having four thyristors with that of the hybrid single-phase bridge. In the first circuit, with an inductive load, zero output voltage will be obtained with a phase retard angle of 90 degrees. Under this condition, the peak of the alternating input voltage will appear across the load (see Figure 6-2(b), waveforms for $a_{3}$,) although the average voltage across the load will be zero.


Figure 6-9. Single-Phase Hybrid Bridge Circuits

On the other hand, with the hybrid circuit phased back 180 degrees, the average and peak voltage both will be essentially zero. This difference in ripple voltage can be significant if part of the load is purely resistive, since with the hybrid circuit there will be less power dissipated in the resistive part of the load when the voltage is reduced by phase retard. For instance, with the hybrid circuit, an indicating lamp across the load will give a measure of the average voltage across the load; with the regular circuit having four thyristors, the lamp intensity will hardly change over the full range of average output voltage.

On the other hand, in the polyphase hybrid bridge circuits, the ripple frequency will assume a lower value as phase retard is introduced. For instance, in the regular 3 -phase bridge circuit, the fundamental ripple frequency is six times the supply frequency for all values of phase retard. In the hybrid 3 -phase bridge circuit, a ripple frequency component three times the line frequency appears when phase retard is introduced. This action must be considered when the load is adversely affected by lower ripple frequencies; for example, in some dc motors.

## Inversion of Inductive Energy

If it is desired to quickly reduce the voltage across an inductive load, this can be done by operating the rectifier as an inverter and pumping the energy stored in the load inductance back into the ac system. This is done by adjusting the angle of phase retard to be greater than 90 degrees. When a hybrid rectifier circuit is used, this mode of voltage control cannot be used, since the
half of the rectifier circuit which is made up of diodes cannot be made to function as an inverter.

## Triggering Pulses for Bridge Circuits

In certain bridge rectifier circuits, precautions must be taken when designing the thyristor triggering circuit to be certain that the desired rectifier circuit action can take place. For example, in the conventional 3 -phase bridge circuit having six thyristors, current flow through the load will not start if each thyristor is simply given a short gate pulse at the instant when current flow in each thyristor normally would start, since this eircuit behaves as two 3 -phase circuits in cascade and displaced by 30 degrees. To initiate current flow, thyristors in both halves of the circuit must be pulsed simultaneously. Under operating conditions where current flow becomes discontinuous, the simultaneous pulsing must occur six times a cycle.

Two solutions are possible. One is to provide each thyristor with a long gate pulse, more than 60 degrees in duration. The other solution is to double pulse each thyristor; one, when initiation of current flow is desired, and once again 60 degrees later.

In hybrid bridge circuits, where circuit action similar to that provided by a free-wheeling diode is obtained (and also in all-thyristor circuits which feed a load having a free-wheeling diode), the discontinuous nature of the current through the thyristors must be considered when designing the triggering circuit. Since the interval of current discontinuity varies with load current and also with angle of phase retard, a triggering circuit
which provides a long triggering pulse is desirable to assure proper action from the thyristors.

## Full-Wave Control of Output of Single-Phase Diode Bridge

A circuit of particular interest for use with thyristors is the singlephase bridge rectifier with a thyristor in series in the dc output. If the thyristor can regain forward blocking ability at the end of each voltage pulse on the output of the bridge rectifier, phase control may be applied to the thyristor and it will control the average voltage applied to the load. This circuit is most successful when the load has a counter-EMF, as with a storage battery. It also can be made to work successfully with a resistive load and with a dc motor armature as the load when a free-wheeling diode is connected across the armature.

In this circuit, the diodes in the single-phase bridge help to provide a short interval at the end of each half-cycle when flow is zero and during which the thyristor can turn off. Nevertheless, when feeding a resistive load or a de motor, thyristors which have fast turn-off times are needed. This is the major reason this circuit has never been used
with thyratron tubes. Conventional mercury vapor thyratrons simply do not turn off (deionize) fast enough to operate in this circuit at supply frequencies of 50 or 60 Hz .

If the load is resistive or is provided with a free-wheeling diode, the voltage output will follow curve D of Figure 6-4 as $a$ is varied. It should be understood that $a$ in this case is the angle of retard of each pulse applied to the thyristor in series with the load.

## DC Motor Drives

The circuit in Figure 6-10 is a full-wave bridge, feeding the armature of a dc motor through a single controlled rectifier. The speed of the motor is controlled by appropriate triggering of the controlled rectifier at various angles with respect to the applied voltage which results in phase control of forward current through the controlled rectifier. [4],[5]

After every half cycle of forward current, the controlled rectifier must recover its forward blocking state. This means that the device must turn off during the time interval between the cessation of for-


Figure 6-10. DC Motor Control Circuit
ward current and reapplication of forward voltage. A quick analysis of the applied voltage waveshapes would lead one to believe that the time interval between forward current cessation and reapplication of forward voltage is zero. However, in analyzing the circuit, one can see that the time required for the voltage to overcome the threshold voltage of two diodes and the controlled rectifier in series, is the time during which the device can recover to its blocking state. Threshold voltage is that voltage required across the diode or controlled rectifier to cause substantial forward current to flow. Threshold voltage is approximately 0.5 volts.

With an input of 230 volts, it would appear that the time interval provided by the threshold voltages
should be approximately 23 microseconds, as seen in Figure 6-11. There are three semiconductor devices in series with the motor when current is flowing so that the total threshold voltage is approximately 1.5 volts.

Voltages and waveshapes observed in laboratory tests of this circuit, as illustrated in Figure 612 , show that in one case, from the time the forward current dropped to zero (indicated by zero forward voltage drop) to the time of the voltage transient, there is approximately 17 microseconds. This time interval is less than the anticipated 23 microseconds. We can see that with this circuit, one critical SCR parameter requiring careful definition is turn-off time.


Figure 6-11. Interval of Zero Current Flow



Figure 6-12. DC Motor Control Circuit Voltage Waveforms

The voltage transient (in Figure $6-12(b))$ is $30 \%$ of the peak supply voltage, is five microseconds wide, and the rate-of-rise of the leading edge is 40 volts per microsecond. This particular voltage transient was seen for both resistive and inductive loads. It is caused by the recovery transient of the free-wheeling diode.

Thus, we see that instead of 23 microseconds allowed for turn-off, we have only 17 microseconds, a much more stringent requirement on the controlled rectifier. To select devices which will work reliably in the circuit of Figure 6-10, they should be tested for reverse recovery time with no reverse voltage, and also for circuit commutated turn-off time. A practical way to do this on many turn-off time testers is to select units which turn off fast, even when essentially zero reverse voltage is applied during the turn-off time interval.

Another approach which has been used successfully is the testing of devices by operating them in the circuit shown in Figure 6-10. Testing time can be minimized by providing the device under test with a very small heat exchanger, so that an elevated junction temperature (where turn-off and recovery times are the longest) will be reached in seconds. Torque is applied to the motor so that a specified motor current is drawn, and the device under test must not lose control of the motor at the end of a specified time period.

Another characteristic which devices should have in order to work well in this circuit is relatively high holding current. However, it is more important to have fast turnoff characteristics under the condi-
tions described above, than to have relatively high holding current, since the additional time during which the controlled rectifier may turn off that is gained by having a high holding current is only a few microseconds.

The controlled rectifier will be aided in turning off if one or more rectifier diodes are connected in series with it. Doing this will increase the threshold voltage mentioned earlier. In many cases, it may be found more economical to do this than to attempt to select extremely fast units, or to use another circuit configuration where turn-off time is not critical. For instance, the turn-off time of the controlled rectifiers in Figure 6-13 is not critical. However, it is quite possible that it would be more economical to add one or two diodes in series with the controlled rectifier in the circuit of Figure 6-10 than to use a completely different circuit.

A physical arrangement illustrating how two diodes may be connected in series with the controlled rectifier, at the same time mounting all the rectifying devices on three heat exchangers, is shown in Figure 6-14.

The single phase dc motor drive circuit using one controlled rectifier is an attiactive and practical circuit to use with fractional and small integral horsepower rated motors when operation is from a 115 volt line. The required silicon controlled rectifier must be selected for maximum turn-off time under the special test condition of essentially no reverse voltage during the turn-off interval. The maximum permissible value of turn-off time under these conditions is long enough so there


Figure 6-13. Single-Phase DC Motor Drive
usually is no great difficulty in selecting satisfactory parts from normal production. Selection of parts for operation from a 230 -volt line is more difficult because of the shorter turn-off time required. The circuit can be modified to enable parts with longer turn-off times to operate satisfactorily. If this circuit is to be operated from a 460 -volt line, circuit modifications are, in general, mandatory. In addition, consideration should be given to using a completely different motor drive
circuit, such as a hybrid singlephase bridge, having two diodes and two controlled rectifiers.

## Triac Reversing Drives [6] [7]

An application which lends itself ideally to use of the triac is a full-wave reversing drive for a dc motor. The basic power circuit is shown in Figure 6-15. If the gates of the triacs are synchronized as shown, the motor will have the polarity as shown in the diagram. If the phase relationships of the triac


* REVERSE POLARITY RECTIFIERS

Figure 6-14. Physical Arrangement for DC Motor Control Circuit


Figure 6-15. Full Wave Triac Reversing Drive Circuit
gate signals are reversed, the opposite polarity will be impressed on the motor. Figure $6-16$ shows the waveforms for this circuit. The $\mathrm{dv} / \mathrm{dt}$ as seen by the triac in this circuit can be reduced by placing an R-C snubber across the device. In some cases, it may also be necessary to place an inductance in series with the triac to reduce di/dt.


Figure 6-16. Waveforms for Triac Reversing Drive

A full-wave drive can be accomplished without a center-tapped transformer using the circuit shown in Figure 6-17. By properly phasing the signals to the gates of TRIACS $1,2,3$, and 4 , the motor can be made to run in either direction. We
can also plug the motor by gating the opposite pair of triacs.


Figure 6-17. Circuit for Full-Wave Triac Reversing Drive Without Transformer

This dynamic braking action can also be achieved by simply providing positive gate bias on all the triacs. This will prevent the power supply from being connected to the motor, but will allow dynamic braking action of the machine. Of course, to limit the armature current, an impedance should be supplied in the armature circuit and/or field weakening should be incorporated.

A three-phase version of the full-wave reversing drive circuit is presented in Figure 6-18.

## PACE/pak Power Controls [17]

PACE/paks are packaged power circuits with no internal control circuitry. They are designed to provide a particular power circuit function in a single isolated package. These units are compatible with existing electrical designs as the power control semiconductors have just been combined in a single package. PACE/paks are available in current ratings from 10 to 42.5 amps at 115 or 230 volt ratings.

The circuits generally utilize thyristor or diode junctions mounted on an electrically isolating, thermally-conductive substrate, which is, in turn, mounted to a copper or aluminum plate that can be mounted to a heat sink. The junctions are isolated from the copper plate by means of a beryllium oxide or Alumina substrate. Then, depending upon the amount of current to be handled, the devices are interconnected by means of a lead frame or by thick film techniques.

This construction offers many advantages over the conventional packaging techniques. These advantages include:
A. Engineering design time is better utilized because only one device must be specified instead of as many as five for single-phase applications and seven for threephase applications.
B. Assembly labor costs are reduced, as only one device must be mounted and interconnected for the entire power section.
C. Visual keys by either color coding or mechanical asymmetrics can be used to aid in making the assembly operation foolproof.
D. Isolated heat sinks are eliminated because the single copper plate is isolated from the circuit. Thermal efficiencies are better than with individual devices.
E. In many applications, the smaller size of the power circuit assembly can be utilized. For example, the single-phase full-wave controlled bridge assembly, when used as a motor drive, could be mounted directly on the bell housing of the motor itself.


Figure 6-18. Three-Phase Triac Reversing Drive Circuit

One very useful circuit configuration is shown in Figure 6-19. This circuit would be used in low power dc motor drives or without the free-wheeling diode as a power supply. For purposes of this discussion, it is assumed that the devices used are in the 25 ampere RMS rating category.


Figure 6-20 defines the maximum allowable base plate temperature vs. conduction angle and dc output current. Knowing the worst case application conditions, the maximum allowable base plate (case) temperature can be determined. Then, with Figure 6-21, which is for watts loss vs. conduction angle and output current, and knowing the maximum allowable base plate temperature, it is possible to determine the heat dissipator requirements. The thermal resistance of the base plate to sink, $\mathrm{R}_{\theta \mathrm{CS}}$, assuming a 1.5 -inch (38.1 mm ) square surface area, a good thermal compound and smooth contact surface, is in the neighborhood of $0.1^{\circ} \mathrm{C} / \mathrm{W}$. It can be seen that using these design graphs, it is possible to characterize this power hybrid assembly in a fashion very similar to that used for a discrete device.

Figure 6-19. PACE/pak Hybrid Bridge


Figure 6-20. Typical PACE/pak Temperature Vs. Current Curve


Figure 6-21. Typical PACE/pak Power Loss Curve

Several common SCR bridge control circuits are shown in Figure $6-22$, with $6-22$ (c) being the most common.

Circuit 6-22(a) can be used for generator exciters, dc motor drives and power supplies. It also has the advantage of not requiring a freewheeling diode.

Circuit 6-22(b) can be used as a de motor drive with the added advantage of regeneration during braking.

Circuits 6-22(c) and 6-22(d) are commonly used as de motor drives. The most popular power levels to date have been in the one to five horsepower range.

Although this chapter is primarily concerned with DC circuits, it might be noted that by shorting the positive to negative output of these circuits, an ac switch configuration is obtained. Figure 6-23 shows
three of the many circuits that have been built using a common substrate.

A variety of ac switches is shown in Figure 6-24. These can be used for lighting controls, heating controls and motor starters.

The triac is especially well suited to these jobs and has the advantage of only one control element. However, some caution must be exercised when using it with an inductive load. The triac's commutating $\mathrm{dv} / \mathrm{dt}$ is not especially high and must be considered or a loss of control may be experienced during a phase-back condition.

The circuit using the diode in anti-parallel is used mostly in three-phase circuits; however, it could be used in a single-phase light dimmer application.

A new area where PACE/paks are being applied is three-phase


Figure 6-22. Popular PACE/pak Circuits


Figure 6-23. Other PACE/pak Circuits
power circuits as shown in Figure $6-25$. Circuits can be delivered with voltages up to 1200 volts and current levels to 150 amps . Circuits 6-25(a) and 6-25(b) are standard three-phase controlled bridges.

Circuit 6-25(a) requires fewer gate control circuits and is excellent
for resistive and capacitive loads; however, some caution must be exercised on inductive loads. Unless some provision is made to handle the reactive current at phased-back conditions (a free-wheeling diode is one method), the bridge can lose control.


Figure 6-24. PACE/pak AC Switch Circuits


Figure 6-25. PACE/pak Three-Phase Circuits

Circuit 6-25(b) does not suffer from the above problem, but requires six gate control circuits.

The circuits shown in Figure 6-25(c) are usable as half-wave, three-phase circuits or can be combined to make various full-wave configurations.

Finally, an inverter module is shown in Figure 6-26. This array of devices can be interconnected with inductors and capacitors to form many of the basic force-commutated inverter circuits. These modules are very useful in many applications where size, weight and thermal considerations are important.


Figure 6-26. PACE/pak Inverter Circuit

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## Line Commutated Inverters

Most phase-controlled rectifier circuits, comprised entirely of SCRs, can be operated as ac line voltage commutated inverters [1]. With a gradual variation in the thyristor triggering angle, a circuit will change from rectifier to inverter operation with a corresponding reversal of power flow. Inverter commutation is accomplished automatically by the instantaneous relationships existing between the applied ac line voltages. Thus, no added components are required to achieve reliable commutation. However, as commutation is provided by the line voltage, this type of inverter can only operate into an ac system where the ac voltage is maintained relatively independent of the circuit operation. Of course, it is also necessary to have a source of dc power on the dc side of the circuit to deliver power to the ac system.

Regenerative braking of dc motor drives is one common application of phase-controlled rectifiers as line commutated inverters. The cycloconverter is a second important type of line commutated inverter. Work is just beginning in a third very large application area - high voltage dc (HVDC) power transmission systems.

## REGENERATIVE PHASE- <br> CONTROLLED RECTIFIERS

In systems using solid-state power control, the load often stores a significant amount of energy [2]. Preferably, the control circuit should be designed to recover this
energy rather than leaving it to be dissipated unproductively. Energy recovery, of course, improves circuit efficiency and reduces the dissipation requirements of the equipment.

A regenerative technique, to return power from the load to the source, can recover the stored energy. This technique may or may not prove worthwhile, depending on the specific application. The design decision will depend on the following factors:
A. The efficiency of the load when acting as a generator.
B. The over-all system efficiency improvement that can be obtained, compared with the increased cost and complexity of the system.
C. The ability of the source to accept energy.

Once the decision is made to use regeneration, the simplest energyrecovery scheme compatible with the type of control circuit should be chosen.

## Four Possible Operating Quadrants <br> Any electrical control system

 can operate in any of the four quadrants. The number of quadrants in a design depends on the circuit configuration and the control elements. There is a forward power flow from source to load, if the equipment is operating in quadrants I or III (voltage and current are of the same polarity). If in quadrants II or IV (voltage and current are of opposite polarity), there is a reverse power flow from load to source. In many systems the equipment operatespartly in quadrants I or III and partly in quadrants II or IV; the net power flow in this case depends on the relative magnitudes of the "positive" and "negative" flow.

One of the simplest power-conversion systems is the three-phase, full-wave-bridge rectifier in Figure $7-1$. This circuit operates in quadrant I - power can flow only from the source to the load. Thus a simple diode-rectifier system cannot be used to recover energy.

As an example of operation in more than one quadrant, consider
the controlled rectifier circuit of Figure 7-2. This circuit differs from the simple diode rectifier in one important aspect: the SCR can support voltage in both directions. Now, if the load and source characteristics are suitable, the circuit can operate in quadrant II and return energy to the source.

Typical waveforms for the SCR circuit are shown in Figure 7-3. The load in this case could be a dc electromagnet, which needs a large amount of charging energy. After charging is complete, the converter


Figure 7-1. Three-phase Full-Wave Bridge Rectifier Circuit


Figure 7-2. Three-phase Full-Wave, All-SCR Bridge Circuit


Figure 7-3. Waveforms for SCR Bridge during Regeneration
output is readjusted to supply just enough energy to overcome the circuit losses. Then, to discharge the magnet, the control circuit selects a triggering sequence that will cause energy to return to the supply. This involves delaying the gate pulse until near the end of the forwardbiased period.

At the start of regeneration, at time $\mathrm{t}_{0}, \mathrm{SCR}_{4}$ turns on (Figure 7-3(e)), and the trigger pulses for all other SCRs ( $\mathrm{SCR}_{5}$ is already conducting) are inhibited until later, at time t2. But, as seen in Figure $7-3(\mathrm{a})$, the output voltage of the converter changes sign at $\mathrm{t}_{1}$ : After $\mathrm{t}_{2}$, the converter operates in quadrant II, and energy is returned to the supply.

Examination of the remainder of the waveshapes of Figure $7-3$ shows that, after $t_{2}$, the normal trigger sequence is re-established. But because of the delay introduced by inhibiting the gate pulses until time $t_{2}$, the converter returns energy to the supply. Note that in the regenerating mode the phase angle between the line-to-line voltage, $\mathrm{V}_{\mathrm{ac}}$ and line current is almost $180^{\circ}$.

Note the absence, in the regenerative mode, of the free-wheeling diode, often used in SCR circuits to carry the inductive current of the load when the SCRs are off.

In the regenerative technique, free-wheeling is accomplished by phasing the converter to produce an average output of zero. This is illustrated in the waveforms of Figure 7-4, which show a phase retard of about $90^{\circ}$. The output voltage rises to half the positive peak line-voltage. Then, because there is an inductive current holding on the SCRs, the output follows the ac line down to half the negative peak. At this
point, the next SCR is turned on. Current thus continues to flow through the bridge, with zero average voltage at the output, and the current level remains constant.


Figure 7-4. Free-wheeling with inductive loads

## SCRs Should Turn Off Fast

An important consideration is SCR turn-off time. The anode-tocathode waveshapes of the SCRs (Figure 7-3(b) through 7-3(f)) show that, while regenerating, the SCRs are reverse-biased for a relatively short time. As a result, the SCRs should be suitable for inverter applications - with the necessary fast turn-off characteristics.

Normally, in phase-control applications where the SCRs are not used in the regenerative mode, there is ample time for the SCRs to be commutated. But in the regenerative application, the time available for turn-off is controlled by the triggering circuit; the further you phase back, the less time the SCR has to be off; the greater the phase back angle, the closer you are to turning the SCR on before it becomes reverse-biased. This also
means that you are much closer to commutating off, under forward biased conditions, the SCR that is about to become forward-biased. But an SCR will not turn off when it is forward-biased; it will keep conducting. The turn-off time therefore defines the maximum "reverse" voltage applied to the load by fixing the minimum time before zero crossing at which the SCRs can be gated; also called, "margin angle."

The dual converter in Figure 7-5 is an example of a circuit that can be operated in all four quadrants. By selection of the $R$ or F bank of SCRs, the direction of the load current can be chosen. The extra cost of this circuit is justified only where regeneration is economically advantageous and voltage reversal is not feasible - that is, load current alone must be reversed to recover the stored energy.

An example of this is a shunt motor that, for some reason, cannot have its field winding voltage reversed. Thus, the machine-generated emf does not change polarity, but current flows out of the machine during regeneration. The amplitude of the generated current is controlled by field strength up to the maximum and then by armature voltage control as the speed is reduced.

Once again, it must be recognized that the power factor of the system varies as a function of triggering angle. Figure 7-6 shows how both output voltage and input power factor vary as a function of triggering angle.

It is important to note that triac de motor drives may all be operated in regenerative modes, provided the proper gating signals are applied.


Figure 7-5. Dual Converter Circuit


Figure 7-6. Power Factor us. Triggering Angle

BRUSHLESS MOTOR DRIVES [3]
The brushless self-synchronous motor developed for propulsion applications has characteristics which approximate those of dc traction motors. By providing high torque at low speed and having very highspeed capability, it makes an ideal traction machine. This machine also may be easily cooled (for instance, by oil cooling) since all windings, both field and armature, may be made stationary on the stator. The basic motor system is shown in the block diagram of Figure 7-7. It consists of a polyphase synchronous machine, a switching matrix composed of silicon controlled rectifiers (or triacs) and a triggering system coupled to the output shaft of the motor. The solid state switching matrix performs the power switching function normally accomplished by the commutator of a
dc machine. The triggering system relates the switching to the rotor position so as to apply power to the motor winding at the proper time to develop maximum torque. This function in a conventional de machine is accomplished by means of the rotating commutator and brushes.

Figure $7-8$ shows schematically what the motor and the thyristor connections look like. Essentially, the normal motor configuration has been turned inside out without changing any of the basic characteristics. The normally rotating armature and commutator are on the outside of the machine, while the field winding rotates. Obviously another version of such a machine, rather than having a de supply to the rotor, could use alternate bars of magnetic material and non-magnetic material to produce the same

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Figure 7-7. Basic Brushless Motor Drive System


Figure 7-8. Motor and Thyristor Connections
effect. However, the motor input windings are now stationary, and the rotor or rotating field is the torque producing member. This motor configuration is not strictly brushless until the rotor excitation is supplied without using sliprings. There are many ways to accomplish this. To list a few: 1) the previously described magnetic material rotors; 2) several types of brushless Lundel machines; 3) many types of inductor machines; and, 4) the rotating rectifier machine.

As mentioned previously, the triggering system relates the switching of the power thyristors to the rotor position. Rotor position is sensed by means of magnetic coupling in six small cup core transformers. The primaries of these transformers are energized by a 170 kHz oscillator. A slotted disc at-
tached to the rotor rotates in such a way as to make and break the magnetic coupling in the primary and secondary of each of these small cup core transformers. As the slots in the disc uncover the transformers, permitting coupling to the secondary, signals corresponding to thyristor on-time are generated. The output of the transformer secondary is rectified and filtered to give the waveshape shown in Figure 7-9. The output of the amplifier and shaper provides a one ampere signal with 0.1 microsecond rise time providing a hard gate drive signal for the thyristors.

A similar system operating from an ac power source is also possible. This system is shown in Figure 7-10. Notice that in the ac system, there is essentially a full wave bridge connected to each motor


Figure 7-9. Position Sensor and Triggering Circuits

line. The thyristors, therefore, rectify the alternator high frequency as well as switch power into the motor windings. The advantage in ac power source systems is that the thyristors can be line commutated. To accomplish thyristor turn-off in the dc system requires separate commutation systems at starting, as noted in Figure 7-11.

Some of the major advantages of the brushless synchronous motor are the capability of voltage control, field control and commutation angle control. By properly coordinating the field control and commutation angle control, the voltage range required for propulsion applications can be minimized. For example, to obtain a constant horsepower output from the motor over a $16: 1$ speed range, a voltage
change of only $3.5: 1$ is required. Constant horsepower lines which tend to correspond with the constant voltage lines on a torque vs. motor RPM set of characteristics, are obtained by using both field weakening and commutation angle advance to extend the motor speed range and to maximize efficiency. There is no relationship between volts and motor frequency as in the case of some induction motor systems. Dynamic braking can be obtained from the motor by turning off the thyristor gates and connecting the stator windings to a resistive grid. Dynamic braking control is obtained simply by raising or lowering the motor field excitation. In this mode, the motor is acting as a synchronous generator.


Figure 7-11. DC Input Brushless Motor

## CYCLOCONVERTERS

## Basic Systems

For years, cycloconverters were built with grid-controlled mercury are rectifiers. The use of cycloconverters to transform a higher frequency to a lower frequency gradually fell from popularity because of the limited power inversion capability of mercury are rectifiers at that time and because of the bulk and relative complexity of the cycloconverter systems. With the advent of thyristors, interest in the circuit sprang forth again. The first use of the system to any degree was for VSCF applications - variable speed, constant frequency supplies for aircraft. Closed loop, controlled slip, variable frequency induction motor drives were the next important application although, of course, the VSCF system also required the unit to drive induction motors. A
number of manufacturers began to develop circulating current-free reversing dc armature supplies which were essentially three-phase to sin-gle-phase cycloconverters. Three basic cycloconverter circuits are shown in Figure 7-12.

The advent of integrated circuits for the solid state control circuitry has made the use of the cycloconverter much more practical. The basic bias shift method of phase control is used to obtain a linear transfer characteristic between input control voltage and average cycloconverter output voltage. This method basically consists, for any given thyristor, of electronically summing a cosine wave voltage of line frequency and the dc control or bias voltage. A level detector is used to trigger a single shot multivibrator at the instant of the positive going zero-crossing of the out-


Figure 7-12(a). Cycloconverter Circuit: Single Way with Single Phase Input and Three-Phase Output


Figure 7-12(b). Cycloconverter Circuit: Single Way with Three-Phase Input and Three-Phase Output

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Figure 7-12(c). Cycloconverter Circuit: Double Way, with Three-Phase Input and Three-Phase Output
put voltage of the inverted summing operational amplifier. The single shot multivibrator output is amplified, passed through an isolating pulse transformer, and used to gate the thyristor.

Figure $7-13$ is a simplified diagram of the triggering circuitry and two anti-parallel connected thyristor converters. The linearity of the bias shift technique, combined with the anti-parallel connection of the converters, balances their average output voltage. This minimizes the 360 Hz pulsating circulating current that will flow between them, even though the average output voltages are equal and opposite.

To prevent turn-on due to nonsinusoidal waveforms in the power line, each cosine voltage is filtered by a low pass LCR filter contributing negligible phase shift at 60 Hz . If it had been required, increased filtering could have been obtained by permitting a phase lag of 30 or $60^{\circ}$ in the filters and appropriately reconnecting the reference transformers to compensate for the lag. It is necessary to have phase-forward limit pulses and phase-back limit pulses guaranteed to provide sufficient volt/second margin to insure successful commutation under inverting conditions. Failure to do this is one of the most common faults in designing a cycloconverter driving system.

Another approach to the system would be to supply multiple gate pulses to the SCRs rather than a continuous gate pulse. Short triggering pulses have several advantages over long ones. The volt/second capabilities of the pulse transformers can be minimized. The danger of overlap of gating can be minimized. If two thyristors con-
nected to the same input phase in one converter are gated simultaneously because of overlapping in time or spurious pulses, then an inversion shoot-through will occur through the two thyristors. Such a shoot-through fault can be very severe in a three-phase or singlephase cycloconverter used for dc armature supplies, just as it can be for normal three-phase dc conversion schemes for reversing action.

In three-phase to three-phase cycloconverters supplying induction motors, the reactance of the induction motor will limit the magnitude of the fault. However, it can still be severe, and it is desirable to prevent this type of fault. In this case, it is necessary to provide a blanking signal which will blank any gate pulses in the range that can cause such a shoot-through. Reference [4] deals with this subject at some length and in considerable detail.

## Design Considerations

The power circuit of a simple single-phase circuit is shown in Figure $7-14 . \mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ comprise the positive going converter, and $\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$, the negative going converter. Thus if SCR 1 and $\mathrm{SCR}_{2}$ are activated for one cycle of the input voltage, and $\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$ activated for the next cycle, a $2 / 1$ frequency reduction can be realized as illustrated in Figure 7-15. In a similar fashion, it is possible to obtain an output which is $1 / 3,1 / 4$, $1 / 5$, etc. of the input frequency. This method of operation results in simpler gating circuits than are necessary with more complex control schemes involving modulation of triggering angles. With large frequency ratios, the advantage of the



Figure 7-14. Single-Phase Cycloconverter Power Circuit


Figure 7-15. Waveforms for 2/1 Frequency Reduction
more complex schemes is that less filtering is required for a given harmonic distortion in the output waveform.

The logic necessary to produce the correct pulse sequence to each SCR gate for each operating frequency is easy to define. It is clear that all gate signal trains must be exactly synchronized to the input signal and also that each gate signal should appear at approximately the zero crossing of the input signal. Thus, a natural starting point for the
logic is the output of a zero voltage switch, a completely integrated package. A block diagram of the system is shown in Figure 7-16.

The necessary gate signals for a $2 /$ 1 frequency reduction are shown in Figure 7-17. All gate signals are repeated after four input half-cycles (or after four pulses from the zero voltage switch). The logic for this frequency should be driven by a synchronous divide-by-four counter using the zero voltage switch as the clock signal. The logic for this frequency follows:


Figure 7-16. System Block Diagram


Figure 7-17. Gate Signals for 2/1 Frequency Reduction

$$
\begin{aligned}
& \mathrm{SCR}_{1}=\overline{\mathrm{Y}} \overline{\mathrm{Z}} \\
& \mathrm{SCR}_{2}=\overline{\mathrm{Y}} \mathrm{Z} \\
& \mathrm{SCR}_{3}=\mathrm{Y} \bar{Z} \\
& \mathrm{SCR}_{4}=\mathrm{Y} \bar{Z}
\end{aligned}
$$

## Where:

$Z=$ least significant digit of the counter
$\mathrm{Y}=$ next least significant digit.
The gate signals necessary for a $3 / 1$ frequency reduction are shown in Figure 7-18. In similar manner to the $2 / 1$ case, these signals are repetitive after six pulses from the zero voltage switch. Thus, if X, Y, and Z are the outputs of a divide-by-six counter:

$$
\begin{aligned}
& \mathrm{SCR}_{1}=\overline{\mathrm{X}} \overline{\mathrm{Z}} \\
& \mathrm{SCR}_{2}=\overline{\mathrm{X}} \overline{\mathrm{Y}} \mathrm{Z} \\
& \mathrm{SCR}_{3}=\mathrm{Y} \bar{Z}+\mathrm{XZ} \\
& \mathrm{SCR}_{4}=\mathrm{X} \overline{\mathrm{Z}}
\end{aligned}
$$

Where:
$\mathrm{X}=$ third least significant digit.
For the $4 / 1$ case, the required gate signals are shown in Figure 7-19. This case is analogous to the first two cases; a divide-by-eight counter is required here:

$$
\begin{aligned}
& \mathrm{SCR}_{1}=\overline{\mathrm{X}} \overline{\mathrm{Z}} \\
& \mathrm{SCR}_{2}=\overline{\mathrm{X}} \mathrm{Z} \\
& \mathrm{SCR}_{3}=\mathrm{X} \bar{Z} \\
& \mathrm{SCR}_{4}=\mathrm{X} \overline{\mathrm{Z}}
\end{aligned}
$$

A variable modulus counter is needed in order to control the output frequency of the cycloconverter. The counter should be able to divide by four, six, and eight on command. Such a counter is shown in Figure 7-20. Its functions are listed in Table VII-I.

As can be seen from the power circuit, all four SCRs do not have


Figure 7-18. Gate Signals for 3/1 Frequency Reduction


Figure 7-19. Gate Signals for 4/1 Frequency Reduction


Figure 7-20. Variable Modulus Counter

Table VII-I. Functions of Modulus Counter

|  |  |  | FREQUENCY |
| :---: | :---: | :---: | :---: |
| A | B | MODULUS | REDUCTION |
| 0 | 0 | 4 | $2 / 1$ |
| 0 | 1 | 6 | $3 / 1$ |
| 1 | 0 | 8 | $4 / 1$ |

common cathodes, making electrical isolation between the digital circuit and the power circuit necessary. Pulse transformers were usually employed as the coupling means whenever complete isolation was required. However, optical isolation techniques have gained prominence as an effective method of triggering thyristors where isolation is required. Optical couplers have several advantages over transformers, the main one being that it is often necessary that the triggering signal remains at the gate for a significant amount of time, in which case a transformer design is extremely difficult. Optical couplers also have a higher frequency response, no inductance, and no feedback from output to input. Their main disadvantages are their limited current rating and time delay from input to output. Maximum output currents are in the order of 100 mA and time delays range from around 1 $\mu \mathrm{sec}$ to $150 \mu \mathrm{sec}$ and are a function of output current.

The coupler for this particular circuit consists of a light emitting diode at the input and a photoDarlington transistor at the output. This device has a maximum output current of 100 mA and a dc current transfer ratio of 5 minimum. When operated at maximum output current, it has a time delay of approximately $10 \mu \mathrm{sec}$. A coupler is placed at the gate of each SCR yielding the
power and triggering circuits shown in Figure 7-21.

The voltage sources $\mathrm{V}_{1}, \mathrm{~V}_{2}$, and $\mathrm{V}_{3}$ are simple power supplies consisting only of a 6.3 volt transformer , a diode bridge, and a $220 \mu \mathrm{~F}$ filter capacitor. These produce about 9 volts dc available to drive each SCR gate. This design takes advantage of $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ having a common cathode. The 330 ohm resistors limit the input diode current to approximately 10 mA . This produces a gate current of at least 50 mA which is quite sufficient for the SCRs used in this circuit. The three diodes at the input of each coupler serve as a logical OR gate to keep separate the three signals that go to each gate (one for each frequency of operation). For any given output frequency, two of the three signals at each gate will be kept at zero level by inhibiting gates in the logic circuit. The complete logic circuit is shown in Figure 7-22.

The circuit was operated from a 120 volt, 60 Hz input, a two-to-one step-down power transformer, and with a 14 ohm power resistor as the load. The circuit waveforms are shown in Figures 7-23, 7-24, and $7-25$. These are traces of the unfiltered load voltage for each frequency of operation: $30 \mathrm{~Hz}, 20 \mathrm{~Hz}$, and 15 Hz .

The logic scheme previously described operates reliably with a resistive load. When an inductive load is present, it is necessary to incorporate considerable additional logic and/or a load current detection scheme. A simple current detector is shown in Figure 7-26.

With an inductive load, the current through the positive SCR con-


Figure 7-21. Cycloconverter Circuit Showing Optical Isolation


Figure 7-22. Complete Cycloconverter Logic Circuit for Resistive Load

30 Hz OUTPUT (20v/div) AND SCR 1 GATE SIGNAL ( $2 \mathrm{v} / \mathrm{div}$ ). FOR RESISTIVE LOAD


Figure 7-23. 30 Hz Output Cycloconverter Waveform

20 Hz OUTPUT (20v/div) AND SCR 2 GATE SIGNAL (2v/div) FOR RESISTIVE LOAD


Figure 7-24. 20 Hz Output Cycloconverter Waveform

15 Hz OUTPUT (20v/div) AND SCR GATE SIGNAL (2v/div) FOR RESISTIVE LOAD


Figure 7-25. 15 Hz Output Cycloconverter Waveform


Figure 7-26. Power Circuit Showing Current Detector
verter may not go to zero for some time after the negative bank of SCRs is to begin conducting. This will cause a type of commutation failure which results in momentarily shorting the ac source voltage and which also produces distortion in the cycloconverter output waveform. Such a commutation failure can be avoided if the gate signals are inhibited until the load current goes to zero. It is also possible to operate with a circulating current using a reactor between the positive and negative SCR converters in the cycloconverter. In this mode of operation, gating signals are always applied to both the positive and negative banks of SCRs. The gate signals are such as to produce the same average load voltage regardless of which converter is conducting.

Three-Phase Cycloconverter
The gating logic is very similar for the three-phase and single-phase cycloconverters. Of course, many more SCRs are involved in polyphase systems, and the proper phase relationship must be maintained for all SCRs in a given converter. Several typical gating schemes are illustrated in reference [4].

The SCR voltage ratings should be determined in the same fashion as for a phase controlled rectifier. However, the RMS current ratings may be reduced by $\sqrt{2}$, since each converter in a cycloconverter is conducting for only half the time. If the cycloconverter is operated at a very low frequency, the SCR current ratings should be the same as that for a simple phase controlled rectifier of the same configuration.

## References

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A vacuum evaporator used during the epitaxial growth of SCR junctions.

## Forced Commutated Inverters

Modern thyristors make it feasible to produce power conversion systems with a variety of outputs, greater efficiency, higher reliability, and extremely fast response to control signals. Although all areas of the power conversion technology have been enhanced, dc-ac inverters have received the greatest boost from the application of power semiconductors. The solid-state inverter is one of the most sophisticated thyristor application areas. It is most demanding in terms of device characteristics, including short turn-off time, low switching loss, high dv/dt capability, and the ability to withstand rapid increases in on-state current. A great variety of circuit techniques are now available for the design of inversion equipment.

## BASIC CIRCUITS

## Parallel Inverter

The parallel capacitor-commutated inverter is one of the oldest
forced commutated inverters. It is described at length in reference [1] and in the additional literature cited in [1]. It is briefly described here to illustrate its important features compared with other forced commutated inverters. A basic circuit is shown in Figure 8-1.
$\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ are alternately turned on to connect the de source voltage to one-half of the transformer primary and then the other, producing a square wave voltage on the load. Assuming that $\mathrm{SCR}_{1}$ is on, the commutating capacitor $\mathrm{C}_{1}$ is also charged to a voltage which would equal twice the source voltage $E_{D C}$, neglecting the influence of inductor $\mathrm{L}_{1} . \mathrm{SCR}_{1}$ is commutated when $\mathrm{SCR}_{2}$ is triggered as this connects the charged commutating capacitor $\mathrm{C}_{1}$ across $\mathrm{SCR}_{1}$ to reverse bias this SCR causing it to turn off. During the $\mathrm{SCR}_{2}$ conducting period, the capacitor is charged to the opposite polarity, ready to commutate off $\mathrm{SCR}_{2}$ when $\mathrm{SCR}_{1}$ is


Figure 8-1. Parallel Inverter Circuit
triggered. The major purpose of $\mathrm{L}_{1}$ is to limit the commutating capacitor charging current during switching. In fact, often a relatively large $\mathrm{L}_{1}$ is used such that the dc source current is almost constant. This ensures commutation over a reasonable load range and minimizes oscillations in the commutating capacitor voltage.

There are many variations in the basic circuit shown in Figure 8-1 for single phase and polyphase systems. However, it does illustrate the important features of this class of forced commutated inverters. Summarizing the advantages and disadvantages of the parallel capaci-tor-commutated inverter:
A. It is one of the simplest forced commutated inverters and it is a feasible approach where the load power factor is near unity and where the magnitude of the load is relatively constant.
B. A reasonably sinusoidal load voltage can be produced with the use of an output filter.
C. Gradually, the dc inductor $\mathrm{L}_{1}$, and the commutating capacitor $\mathrm{C}_{1}$ are relatively large for circuits operating at normal power frequencies.
D. The load voltage waveform changes quite drastically over wide load current ranges and with different power factor loads.
E. Reliable starting and stopping is a fairly difficult design problem to avoid commutation failure and/or excessive currents due to transformer saturation.
F. The basic circuit does not allow for voltage control. Excellent control can be achieved with the
addition of phase controlled SCRs on the transformer secondary.

## Series Inverter

Another forced commutated circuit is the series capacitor-commutated inverter. This inverter was developed using mercury are valves. Figure 8-2 illustrates a series inverter. Assuming $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ are of equal magnitude and that the inductors $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$ are also equivalent, $\mathrm{SCR}_{1}$ switches on, resonantly discharging $\mathrm{C}_{1}$ through $\mathrm{L}_{1}$ and through the load which is transformer coupled to the main inverter circuit. At the same time, $\mathrm{C}_{2}$ will charge resonantly towards the dc line potential. At the end of this conduction period then, $\mathrm{SCR}_{1}$ will shut off when the current tries to reverse in this half of the circuit. $\mathrm{SCR}_{2}$ is then turned on, discharging $\mathrm{C}_{2}$ resonantly through the load and also through $\mathrm{L}_{2}$. During this time $\mathrm{C}_{1}$ will resonantly charge toward the dc line potential as $\mathrm{C}_{2}$ discharges. This will result in a peak current through the SCR given by equation $8-\mathrm{A}$ and a half period of time in the circuit given by equation 8-B.

$$
\begin{align*}
& I_{P K}=E_{D C} \sqrt{\frac{C}{L}}  \tag{8-A}\\
& \frac{\tau}{2}=\pi \sqrt{\mathrm{LC}} \tag{8-B}
\end{align*}
$$

The various waveshapes for SCR current and voltage, load current and voltage, capacitor current and voltage, and inductor current and voltage are shown in Figure 8-2(b). These waveshapes, of course, will vary with the Q of the circuit. As


Figure 8-2. Series Inverter
the load increases, especially if it is of unity power factor, the waveshapes will vary somewhat from these ideal conditions. If the load is purely inductive, it can be lumped in the analysis into $L_{1}$ and $L_{2}$ and the waveshapes will be identical with those depicted. If it is capacitive in nature, it can be lumped into $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ and then again the waveshapes will be of this ideal nature.

If the period of oscillation of this type of inverter is long, the $\mathrm{dv} / \mathrm{dt}$ on the SCR is low and the characteristics generally available in thyristors intended primarily for 60 Hz operation are satisfactory; however, if the unit is used for very high frequency applications, in the order of 5 to 10 kHz , the turn-on characteristics of the device becomes important in rating it proper-
ly so as to maintain junction temperatures below the maximum allowable value. Thus, the turn-on losses of the device become important. An ACE-type inverter SCR offers low turn-on losses and high frequency capability.

Although the series inverter has most of the disadvantages of the parallel inverter, it does not require a large dc reactor. Thus, it is quite widely used in high frequency applications where the commutating L and C are small and the load is relatively constant. [2],[3].

## McMurray Inverter[4]

One of the simplest configurations of the McMurray auxiliary impulse commutated inverter is shown in Figure 8-3. This arrange ment is also the basic building block


Figure 8-3. McMurray Inverter Circuit
in the single phase bridge and three phase versions of the McMurray inverter.

The basic operation of the circuit in Figure 8-3 is relatively uncomplicated. Assuming the correct initial capacitor voltage, a main SCR is commutated by gating the appropriate auxiliary SCR. When $\mathrm{SCR}_{1 \mathrm{~A}}$ or $\mathrm{SCR}_{2 \mathrm{~A}}$ are triggered, they cause a resonant pulse of current to flow in opposition to that being carried by the conducting main SCR. When the main SCR current has been reduced to zero, the commutating current pulse will continue to flow in the appropriate feedback or free-wheeling diode, thus providing a small reverse voltage on the main SCR for the time interval necessary for it to regain its off-state blocking capability.

Possibly the most advantageous feature of this inverter is that after a given main SCR is commutated, the capacitor voltage is left at the polarity required to commutate the next main SCR. This feature, combined with the pulsating nature of the commutating action, provides a highly efficient inverter for operation at normal power frequencies. In fact, an efficiency of over $90 \%$ can be attained, with SCR turn-off times in the 20 microsecond range, for circuit operating frequencies up to several kilohertz.

Another very advantageous feature of this inverter approach is that with the proper SCR triggering sequence, sufficient commutating capacitor voltage is assured for a wide range of load conditions.

Possibly the two most important additional configurations of the McMurray inverter are shown in Figure 8-4 and Figure 8-5. Figure $8-4$ is the single phase bridge ar-
rangement. This is essentially two circuits of the type shown in Figure $8-3$. By using two half bridge circuits, it is not necessary to return the load to a center tap on the dc supply. The opposite leg of the bridge provides the load return path.

Figure 8-5 shows the basic three phase McMurray inverter. This contains three half bridge circuits. Thus, the circuit of Figure 8-3, is the basic building block for both the single phase bridge and the three phase McMurray inverter.

The commutating action in Figures 8-4 and 8-5 is the same as for the circuit of Figure 8-3. However, the load voltage waveforms are somewhat more involved. Possibly the simplest way to derive the load voltage waveforms is to first sketch the waveforms of the voltages of Figure 8-3. The voltages in Figure $8-5$ may then be obtained by subtracting the appropriate half bridge output voltages.

## Modified McMurray - Bedford Inverter [1],[5]

This circuit can best be analyzed by examining a single-phase version of this type of inverter, which is shown in Figure 8-6(a). Under steady-state conditions, assume that $\mathrm{SCR}_{1}$ is conducting current to the load and that the capacitor $\mathrm{C}_{1}$ is charged with a voltage equivalent to one half the supply voltage, with terminal A positive with respect to terminal B. In order to commutate $\mathrm{SCR}_{1}$, a gate signal is applied to $\mathrm{SCR}_{2}$, turning it on. At the same instant that $\mathrm{SCR}_{2}$ is gated on, the gating signal is removed from $\mathrm{SCR}_{1}$, but because $\mathrm{SCR}_{1}$ is conducting load current, it does not turn off at that instant. Thus, im-


Figure 8-4. Single Phase Bridge McMurray Inverter Circuit


Figure 8-5. Three-Phase McMurray Inverter Circuit


Figure 8-6(a). Single Phase Half Bridge Modified McMurray-Bedford Inverter Circuit
mediately after $\mathrm{SCR}_{2}$ is turned on, both SCRs are conducting and the full de supply voltage is impressed across the primary turns, $N_{p}$, of the reactor $L_{2}$. Since the voltage across $\mathrm{N}_{\mathrm{p}}$ is the supply voltage, $\mathrm{E}_{\mathrm{DC}}$, the center-tap point at this instant of time must be one half EDC. Thus, the load voltage between A and B must be zero, since $A$ is also at one half EDC voltage. Hence, no current flows to a resistive load while both SCRs are conducting.

Just prior to the turn-on of SCR 2, a current was flowing through the upper winding of the $\mathrm{L}_{2}$ reactor. Immediately after turnon of $\mathrm{SCR}_{2}$, the load current in $\mathrm{SCR}_{1}$ drops to one half the load current and the current through $\mathrm{SCR}_{2}$ jumps to one half the load current to satisfy the ampere turns of the $L_{2}$ reactor. The capacitor $\mathrm{C}_{1}$ then begins to discharge through $\mathrm{L}_{1}$
into the center-tap of $\mathrm{L}_{2}$ where it divides. One half of the commutating current flows up through the upper windings of $\mathrm{L}_{2}$, decreasing the load current through $\mathrm{SCR}_{1}$, then flows back into capacitor $\mathrm{C}_{1}$ through $\mathrm{C}_{2}$. The other half of the commutating current flows down through the lower half of $L_{2}$, then back into $\mathrm{C}_{1}$, through $\mathrm{C}_{3}$. The commutating current builds up sinusoidally at a rate determined by the natural frequency of $\mathrm{C}_{1}$ and $\mathrm{L}_{1}$. The current in the upper winding will build up and exceed the current to $\mathrm{SCR}_{1}$ with the excess current flowing through diode $\mathrm{RD}_{1}$, back biasing $\mathrm{SCR}_{1}$ and turning it off. The lower commutating current adds to the original lower winding current, thus maintaining the ampere turns in the $\mathrm{L}_{2}$ reactor.

This type of circuit imposes considerably different reapplied dv/dt


Figure 8-6(b). Three-Phase Bridge Modified McMurray-Bedford Inverter Circuit
conditions on the SCRs than was seen in a series inverter. It should also be noted that in this circuit, during turn-off of an SCR, the reverse bias on the device is simply
the forward drop of the diode which is connected in anti-parallel with it. This also imposes a different turn-off duty than was seen by the SCRs used in the previously mentioned series inverter case.

## Current Source Inverter [6],[7]

A single phase version of the current source inverter circuit is shown in Figure 8-7. It is quite similar to the parallel inverter, except that the commutating capacitor is divided into two parts and diodes $\mathrm{RD}_{1}$ and $\mathrm{RD}_{4}$ are added. In a practical application, the circuit is driven from a rectified voltage with a large series reactor to provide low ripple in the dc bus current.

The waveforms shown in Figure 8-8 illustrate the operation with a purely resistive load $R$, and assuming ideal semiconductor components. At time $\mathrm{t}_{0}$ it is assumed that $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{4}$ are triggered with some initial voltage on the capacitors.

A three phase version of the current source inverter circuit of Figure 8-7 is shown in Figure 8-9.

The most significant features of the current source inverter are:
A. No commutating reactors are required.
B. With a phase controlled rectifier supply to the dc bus and a large dc reactor in series to provide relatively constant dc current, the inverter can feed power back to the ac system since EDC can have an average value of either polarity.
C. The constant current dc provides an automatic current limit for the inverter output into a low impedance load. However, with a high impedance load, the capacitor voltage becomes large.
D. The constant current system can provide very fast response to demanded speed changes when the inverter is supplying an ac motor. The change in speed is initiated by changing the frequency of the SCR gating oscillator and full torque is very quickly available to produce the required speed change.


Figure 8-7. Single Phase Current Source Inverter Circuit


Figure 8-8. Single Phase Current Source Inverter Waveforms


Figure 8-9. Three-Phase Current Source Inverter Circuit

Table VIII-I is a summary of forced commutated inverters. It lists the circuits discussed and compares their more important features.

FREQUENCY MULTIPLIER
[8]
Thyristors are also used in frequency conversion equipment to provide power supplies for induction heating and melting applications. This system, known as a frequency multiplier, is shown in Figure $8-10$. This cycloinverter uses a type of forced commutation. It has the capability of maintaining relatively constant power in the load independently of resistance changes during the work cycle. These changes can be as much as 5 per unit.

In the past, the low power factor of the loaded coil was compensated for by using series or parallel capacitance. For an output frequency
higher than 60 Hz the power supply generally used a magnetic frequency multiplier or motor generator set. The thyristor system does not have the limitations of the magnetic frequency multiplier and the $\mathrm{m}-\mathrm{g}$ set systems.

The static system has high efficiency, high input power factor, small size, low maintenance, and the output frequency is variable; thus no variation in load compensating capacitance is required. A low-pass input filter provides a path for higher harmonics generated by the frequency converter, thus keeping the higher harmonics to a low level in the input lines.

A thyristor block consisting of two thyristors in an AC switch configuration is connected to each phase. The appropriate one of these thyristors can be rendered conductive when a positive or negative output voltage is desired. The posi-


Figure 8-10. Frequency Multiplier or Cycloinverter Circuit

Table VIII-I. Comparison of Forced Commutated Inverters

|  | Parallel | Series | McMurray | Modified <br> McMurray-Bedford | Current <br> Source |
| :--- | :---: | :---: | :---: | :---: | :---: |
| Output Waveforms | Load dependent | Sinusoidal | Square | Square | Load <br> dependent |
| Voltage Control <br> Capability | No | No | Yes | No | No |
| Voltage Regulation | High | High | Low | Low | High |
| Load Range | Limited | Limited | Large | Large | Limited |
| Reactor Size | Large | Large | Small | Small | Large |
| Capacitor Size | Large | Large | Small | Small | Large |
| Auxiliary SCRs | No | No | Yes | No | No |
| Complex Control | No | No | Yes | No | No |
| Efficiency | Low | Low | Highest | Next Highest | Low |
| SCR dv/dt <br> Requirements | Low | Low | Highest | Next Highest | Low |
| SCR di/dt <br> Requirements | Low | Low | Highest | Next Highest | Low |

tive and negative thyristor can be rendered conductive alternately at the desired output frequency. The parallel compensated induction heating melting load is shown connected to a ringing inductor-capacitance to achieve commutation of the thyristors. The ringing capacitors are wye connected and the wye point voltage varies at the output frequency with respect to the input supply neutral. These capacitors provide a path for the output frequency current preventing its appearance in the input lines.

The SCRs used in this type of application are, in general, required to be high voltage, fast turn-off devices, and considering the possible operating frequency for load compensation, should have extremely good turn-on capabilities and maintain high current capability at high frequency. For higher power systems, paralleling of devices might be advantageous for very large melting loads.

## DC POWER SUPPLIES

Figure $8-11$ is a circuit for conversion from 1,500 volt dc to 37.5 and 75 volt regulated dc for auxiliary power on a moving vehicle [9]. If it is assumed that all capacitors are charged initially, $\mathrm{SCR}_{1}$ is turned-on, discharging $\mathrm{C}_{2}$ through $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$, and $\mathrm{C}_{3}$ through $\mathrm{L}_{2}$ at the same time that power is supplied to transformer $\mathrm{T}_{1}$ through $\mathrm{SCR}_{1}$. Both capacitors will charge negatively, thus shutting off $\mathrm{SCR}_{1}$. $\mathrm{C}_{5}$ and $\mathrm{C}_{6}$ will, of course, reflect this charge in the opposite direction. $\mathrm{R}_{1}$ is simply to suppress parasitic oscillations in the circuit. The bottom half of the converter will operate exactly as the top half.

It should be noted that $\mathrm{C}_{2}$ and $\mathrm{RD}_{3}$, and also $\mathrm{RD}_{4}$ and $\mathrm{C}_{5}$, act as $\mathrm{dv} / \mathrm{dt}$ suppressors across $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ at the same time they form part of the commutation circuitry. Should the system be operated on a supply with high transient voltages, the gate and regulating circuitry can be equipped with a static high voltage interlock to stop trigger pulses during the transient condition, thus allowing $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ to form a series SCR pair to hold off the excess line voltage.

Figure 8-12 shows a high voltage inverter power supply. Triggering $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{4}$ simultaneously applies the input voltage EDC to the load transformer $\mathrm{T}_{1}$ and the commutation capacitor $\mathrm{C}_{5}$. Turning on $\mathrm{SCR}_{2}$ and $\mathrm{SCR}_{3}$ on the opposite sides of the inverter causes the charge on $\mathrm{C}_{5}$ to reverse bias $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{4}$, turning them off. Figure 8-12(b) shows the resulting trapezoidal voltage waveshape applied to the diode bridge RB1. Figure $8-12(c)$ shows the current during the recovery period.

Since a square wave is applied to the diode bridge, the diodes will see a fast rising reverse voltage during their commutation interval. A high value of recovery current will result in a high instantaneous power dissipation. Therefore, fast recovery diodes should be utilized in the output bridge.

Figure $8-13$ is an inverter dc power supply using soft commutation techniques [9]. This type of circuit has the capability of being designed, using high frequency SCRs, for extremely high repetition rates while maintaining relatively low dynamic stress on the devices and emitting low electrical noise.


Figure 8-11. Vehicle Auxiliary Power DC Supply Circuit

The circuit waveforms are shown in Figure 8-14.

When $\mathrm{SCR}_{1}$ is triggered on, at the beginning of time interval $\mathrm{t}_{1}$, with $\mathrm{SCR}_{2}$ off, a series-resonant circuit is connected to the dc supply. The voltage across windings $\mathrm{L}_{2}$ and $\mathrm{L}_{3}$ will initially back bias SCR 2 and $R D_{1}$ respectively. The capacitor voltage sinusoidally charges up towards twice EDC minus the ini-
tial voltage on the capacitor. The voltage across the transformer winding $L_{1}$ is the difference between the input voltage $\mathrm{E}_{\mathrm{DC}}$ and the capacitor voltage. As the capacitor charges up to a value greater than the input voltage, the voltage across $L_{1}$ reverses polarity.

At some time after $\mathrm{SCR}_{1}$ is triggered on and the magnitude of the voltage on the capacitor is larger


Figure 8-12. High Voltage Inverter Power Supply
than $\mathrm{E}_{\mathrm{DC}}$, the voltage across winding $L_{3}$ is of sufficient magnitude to forward bias RD1. At $t_{2}$, when $R D_{1}$ conducts, the voltage of the windings will be clamped to the output voltage $\mathrm{E}_{\mathrm{O}}$ assuming that first $\mathrm{L}_{1}=\mathrm{L}_{2}$; second, $\mathrm{L}_{3}=\mathrm{n}^{2} \mathrm{~L}$; third, $\mathrm{C}_{2}$ is much greater than $\mathrm{C}_{1}$; and lastly, effects of leakage react-
ances are neglected. The current through $\mathrm{SCR}_{1}$ will decrease to zero since any further current flow through SCR 1 will continue to charge capacitor $\mathrm{C}_{1}$ and increase the reverse bias appearing across $\mathrm{SCR}_{1} . \mathrm{SCR}_{1}$ then commutates off. The energy that has been stored in $\mathrm{L}_{1}$ is now discharged to the load through $\mathrm{RD}_{1}$.


Figure 8-13. Self-Commutated DC to DC Converter Circuit

As was noted above, the voltage across $\mathrm{L}_{1}, \mathrm{~L}_{2}$, and $\mathrm{L}_{3}$ windings is constant and equal to V . The voltage across these windings is assumed constant since it is possible to increase the value of $\mathrm{C}_{2}$ arbitrarily until this condition is met at with precision desired. The current through $\mathrm{RD}_{1}$ will be a ramp of current with a negative slope. This current is allowed to relax to zero before $\mathrm{SCR}_{2}$ is triggered on. $\mathrm{SCR}_{2}$ is triggered at t3 to repeat the cycle and reverse the voltage across $\mathrm{C}_{1}$. Energy is stored in $\mathrm{L}_{2} ; \mathrm{SCR}_{2}$ commutates off and a ramp of current is discharged through $\mathrm{RD}_{1}$. The voltage across $\mathrm{C}_{1}$ is now at its initial value. After the current through $\mathrm{RD}_{1}$ has relaxed to zero, $\mathrm{SCR}_{1}$ can now be retriggered.

The output voltage $\mathrm{E}_{\mathrm{O}}$ can be regulated by controlling the trigger-
ing of the thyristors. This type of control system is shown in Figure $8-15$. The output voltage $\mathrm{E}_{\mathrm{O}}$ is compared to a reference voltage $\mathrm{E}_{\mathrm{R}}$ by means of a comparator circuit. Whenever the output voltage is above a threshold level established by the reference, the comparator output biases the gate circuit in a manner to inhibit the free-running pulse generator. In addition, a signal is derived from the voltage appearing across $\mathrm{L}_{3}$, such that at any time $R D_{1}$ is conducting the gate circuit is biased to inhibit the blocking oscillator. The maximum frequency of the free-running pulse generator is equal to the maximum frequency of operation of the system. When the system is operating in a voltage regulated mode, the system frequency is less than maximum. Thus the output voltage is


Figure 8-14. Circuit Waveforms for DC to DC Converter


Figure 8-15. Diagram of DC to DC Converter
regulated at a value proportional to $\mathrm{E}_{\mathrm{R}}$.

In order for the converter system to regulate over a load range from zero to full load, the switching frequency will range from a very low value to the maximum designed frequency, $\mathrm{f}_{\mathrm{o}}$. As a result, the converter will operate in the audible range for at least some load conditions. This condition could limit the usefulness of this style of converter in some sensitive areas since the resulting noise can be offensive or damaging to the human ear.

Up to the early 1970 s, the alternatives available to the circuit designer were less than pleasant. He had either to use bulky enclosures, thus inhibiting air flow in general, operate magnetic devices at reduced flux densities, or operate well above the audible spectrum. In general, each of these alternatives increased the cost of the system. A random noise generator can be added to this type of circuitry, in order to circumvent these problems.

A source of random noise, $\mathrm{N}_{\mathrm{G}}$, is connected in series with the reference voltage $\mathrm{E}_{\mathrm{R}}$ as shown in Figure 8 -16. The long-term average voltage of this source is zero, therefore the long-term average output voltage will not differ if the source is shorted out. The effect of putting this
noise source in series with the reference is to cause the inverter operating frequency to be randomly distributed about some center value. Therefore, at loads less than full load, the converter will emit a hissing sound. This sound has a quality similar to air escaping from a radiator or an air hose. The quality of this sound remains constant over nearly the full load range. At extremely light loads the sound reduces to ticking sounds when the switching period becomes very long.

With this new type of noise emission it was also found much easier to effectively baffle the noise of the converter. This effect is to be expected since the acoustical energy is now randomly distributed over a wide range of frequencies. The sound is no longer periodic and the reinforcing effect of standing waves is not present.

Thus, with this type of soft commutation system, with a random noise generator inserted in the reference loop, the following power supply characteristics are achievable:
A. The rate of reapplied forward $\mathrm{dv} / \mathrm{dt}$ and the rate of current rise during the tturn-on di/dt, for the thyristor devices, are a function of $L$ and $C$ only and are independent of the load.


Figure 8-16. Diagram of DC to DC Converter with Random Noise Source
B. The minimum turn-off time is independent of the load.
C. The RF energy developed across the diode $\mathrm{RD}_{1}$ can be minimized.
D. The load impedance, $R_{L}$, can be varied from zero to infinity.
E. High di/dt in the thyristors is avoided by permitting the current in the commutating inductances $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$ to relax to zero, before triggering the thyristors.
F. By decoupling the load from the main charging thyristors, the system results in being short circuit stable.
G. Single frequency tones have been eliminated from the acoustical spectrum of the converter. The audible sound emitted by the converter is considerably altered by this procedure and results in a converter which produces less acoustical annoyance.

## 

## Induction Heating Supply Design Example [3],[11],[12]

Figure 8-17 shows the block diagram for a high frequency inverter for induction cooking. The main design constraints are the upper operating frequency, which is limited by present device technology, and the lower operating frequency which is set by the acoustic noise generated in the circuit. The present frequency limit on power semiconductor switching is approximately 50 kHz , and acoustic noise is obtained below 20 kHz . One other important constraint when considering a consumer product is cost. For this reason the minimum number of components must be selected while meeting the circuit requirements. Also, the system should be well shielded to prevent undesirable RFI.

The cooking unit uses induction heating principles. Thermal energy


Figure 8-17. Induction Heating Cooking Unit Block Diagram
is generated within the metal of the cooking vessel by means of a strong high frequency magnetic field. The magnetic field sets up eddy currents that circulate within the vessel, heating its surface but not the circuit components. The magnetic field is produced by varying an electric current in a coil. This is accomplished by means of a series, single SCR inverter, which operates at a fixed resonant frequency. The amount of current flowing in the load coil is varied by changing the input dc voltage supplied to the series resonant circuit. This is accomplished using a half wave phase controlled rectifier circuit. The half wầve circuit is sufficient to meet the necessary voltage requirements; thus it is used because of its simplicity and relatively low cost. However, half-wave loading of the power line may be undesirable.

The series inverter is triggered by a basic UJT relaxation oscillator with a frequency fixed just above the audio range, thus keeping acoustic noise to a minimum. The schematic diagram is shown in Figure 8-18.

The load coil is constructed from a spirally wound coil of copper tubing. The copper tubing provides a low resistance to the ac current and remains relatively cool while providing the required magnetic field. The power delivered to the load is controlled by varying the phase angle at which $\mathrm{SCR}_{1}$ triggers. Once triggered, $\mathrm{SCR}_{1}$ remains on for the rest of the applied half cycle.

The trigger circuit for $\mathrm{SCR}_{1}$ is a double time constant arrangement. Using two RC networks extends the range of gating control to something greater than $90^{\circ}$. This allows
the voltage applied to the inverter to be reduced effectively to zero. Triggering capacitor $\mathrm{C}_{1}$ is recharged by capacitor $\mathrm{C}_{2}$ after every trigger pulse. The voltage on $C_{1}$ builds up to a value slightly less than the breakdown voltage of DIAC $_{1}$, resulting in a relatively constant positive reference voltage, from which $\mathrm{C}_{1}$ is recharged again to the diac triggering point. The circuit components are chosen to produce a phase shift as close to $180^{\circ}$ as possible while simultaneously maintaining the voltage across $\mathrm{C}_{1}$ above the 32 volts required to trigger the diac. This output is then filtered by capacitor $\mathrm{C}_{3}$ to obtain a usable dc. Wave forms for the half-wave, phase controlled rectifier are shown in Figure 8-19.

The series, single SCR inverter was chosen for its simplicity and relatively low cost. Its principle of operation is quite old but it works exceptionally well with today's power semiconductors.

A series resonant circuit, consisting of capacitor $\mathrm{C}_{4}$, and inductors $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$, is connected across the dc supply each time $\mathrm{SCR}_{2}$ is triggered. Considering no loss in the system, the capacitor voltage sinusoidally builds up to twice the supply voltage during the first half-cycle of oscillation. On the second halfcycle of oscillation, current tries to reverse through $\mathrm{SCR}_{2}$ thus turning it off. The negative cycle of current must then flow through diode $\mathrm{RD}_{2}$ reversing the current in the load coil $\mathrm{L}_{1}$. Upon the start of the next half cycle, $\mathrm{SCR}_{2}$ is off and current is blocked. At this time the voltage on capacitor $\mathrm{C}_{4}$ is zero. To repeat the cycle, $\mathrm{SCR}_{2}$ must receive another trigger pulse from the trigger circuit. Therefore, for each pulse


Figure 8-18. Induction Heating Cooking Unit Circuit


Figure 8-19. Induction Heating Phase Controlled Rectifier Waveforms
from the UJT oscillator, there is one complete cycle of current through the load coil.

With no cooking vessel near the load coil, the diode half-cycle average current IRD2 is nearly equal to $\mathrm{SCR}_{2}$ 's half-cycle average current ISCR2. The total current is IDC $=$ ISCR2 - IRD2. When a load is placed on the load coil the SCR current, ISCR 2, increases while the diode current, IRD2, decreases and the total current from the de supply increases.

The basic design parameters are:
$f_{O}=$ resonant frequency of capacitor $\mathrm{C}_{4}$ with inductor $\mathrm{L}_{1}$.
$\mathrm{E}_{\mathrm{DC}}=$ dc supply voltage
$\mathrm{I}_{\mathrm{M}}=$ peak current through $\mathrm{L}_{1}$
$\mathrm{f}_{\mathrm{t}}=$ frequency of the triggering circuit
The resonant frequency $f_{0}$ was chosen equal to 35 kHz for which, from formula $8-C$, time on equals $28.6 \mu \mathrm{sec}$.

$$
\begin{equation*}
\tau=\frac{1}{\mathrm{f}_{\mathrm{O}}}=28.6 \mu \mathrm{sec} \tag{8-C}
\end{equation*}
$$

The circuit will only operate properly when the current is less than zero for at least the turn-off time of the SCR. This is required for $\mathrm{SCR}_{2}$ to regain its off-state blocking capability at the end of every other half-cycle. Therefore, the maximum turn-off time for $\mathrm{SCR}_{2}$ has to be less than $\tau / 2$ or approximately $14 \mu \mathrm{sec}$.

The peak value of the SCR current is given in formula 8-D:

$$
\mathrm{I}_{\mathrm{M}}=\sqrt{\frac{\mathrm{E}_{\mathrm{DC}}}{\frac{\mathrm{~L} 1}{\mathrm{C} 4}}}
$$

The circuit was designed to produce a peak current of 100 A . Thus, the greatest required value of the de supply voltage is $\mathrm{E}_{\mathrm{DC}}=$ $100 \sqrt{\mathrm{~L} / \mathrm{C}}$.

The resonant frequency determines the LC product as shown in formula 8-E:

$$
\begin{align*}
& \mathrm{f}_{\mathrm{O}}=\frac{1}{2 \pi \sqrt{\mathrm{LC}}}  \tag{8-E}\\
& \mathrm{LC}=\left(\frac{0.159}{35 \times 10^{3}}\right)^{2}
\end{align*}
$$

With the heating coil $\mathrm{L}_{1}$ equal to $6 \mu \mathrm{H}$ and thus $\mathrm{C}_{4}=3.45 \mu \mathrm{~F}$, the greatest value of the dc supply voltage is $\mathrm{E}_{\mathrm{DC}}=100[1.32]=132$ volts. These values are assuming that the resistance of the circuit is approximately zero.

The choice of $\mathrm{L} 2 / \mathrm{L} 1$ depends on several factors. If L2/L1 is low then the cost of L2 will be low but the turn off time for SCR2 will be reduced. An increase in L2/L1 will result in an increase in cost plus an increase in size. Therefore L2/L1 is selected at about 50 . This is large enough so that L2 does not affect the resonance of L1 and C4 at the present operating frequency.

Waveforms for the inverter are shown in Figure 8-20.

Many different triggering circuits could be used to produce the necessary 20 kHz pulse, capable of triggering $\mathrm{SCR}_{2}$. The relaxation UJT oscillator has been selected here for its reliability and simplicity. Q1 is used as a current amplifier to drive the SCR gate circuit. Capacitor $\mathrm{C}_{7}$ is charged through $R_{7}$ and $R_{8}$ until the emitter voltage of the UJT reaches $V_{P}$, at which time it turns on and discharges $\mathrm{C}_{7}$ through $\mathrm{R}_{6}$. When the emitter voltage drops be-


Figure 8-20. Induction Heating SCR Series Inverter Waveforms
low the holding value of the UJT emitter, it ceases to conduct and the cycle repeats. The period of oscillation, T, is given by Formula 8-F:
$\mathrm{T}=\frac{1}{\mathrm{f}}=\left(\mathrm{R}_{7}+\mathrm{R}_{8}\right)\left(\mathrm{C}_{7} \ln \frac{1}{1-\eta}\right)$
Where:
$\eta=$ the intrinsic standoff ratio of the UJT.

The pulsed output, developed across $R_{6}$, is coupled directly to the base of $Q_{1}$. Q1 turns on and $\mathrm{C}_{6}$ then discharges through the gate of $\mathrm{SCR}_{2}$, providing a greater pulse of current for $\mathrm{SCR}_{2}$ than that from UJT $_{1}$. The dc that supplies the UJT oscillator is furnished from a 25 volt filament transformer, rectified through $\mathrm{RD}_{3}$ and filtered by $\mathrm{C}_{8}$. $\mathrm{BD}_{1}$, a 25 volt zener voltage regulator, provides the necessary regulation for the UJT. Resistor Rg limits the zener current.

## Variable Frequency Motor Drives

The curve shown in Figure 8-21 is a comparison of cost of ac motors versus de motors in various
horsepower sizes. With even a premium price for the ac system required to drive an ac motor, the overall ac drive should be less costly than the similar horsepower size using a de motor.

The heart of the ac drive is the silicon controlled rectifier. Production of SCRs suitable for ac drives has historically been a matter of parameter trade-offs leading to the production of limited numbers (due to low yield factors) of suitable devices at relatively high prices. These problems have been solved so that SCR devices are now available with all of the parameters required by an ac drive system. Figure $8-22$ shows curves of weight, inertia and efficiency, versus horsepower for dc and ac motors. With the inertia of the ac machine lower than that of a comparable dc machine, the response time of the control system can be reduced, thus increasing the achievable accuracy with a high gain, stable system. Moreover, the inherent weight savings (decreasing the necessary support structure in an installation) further reduces the initial system cost. The slightly bet-


Figure 8-21. Horsepower versus Cost
ter efficiency of the ac machine proves to be an advantage over extended periods of operation in terms of power savings. In addition to these advantages there are savings in maintenance. The ac ma-
chine has no commutator and brushes, while in the dc machine these must be periodically replaced or overhauled, causing downtime in the installation. It is also possible to obtain an ac machine in an ex-


Figure 8-22. Motor Horsepower versus Pertinent Parameters
plosion-proof enclosure which is required in some volatile environments.

Using a pulse width modulated inverter it is possible to produce an ac motor drive system that can develop the full torque characteristics of de machines. The phase shifted, fixed dc voltage inverter circuit approach found in the pulse width modulated inverter requires more sophisticated semiconductor devices than the variable voltage dc link inverter approach. Nevertheless, with an economical, high performance, high power SCR, the cost of the more advantageous (in terms of performance) pulse width modulated inverter becomes competitive to the de system.

In the circuit arrangement shown in Figure 8-23(b), both voltage and frequency are controlled by a single set of SCRs, simplifying the necessary control and power circuitry and thus increasing the inherent reliability of the system. The triggering cir-
cuits needed to control the dc are completely eliminated, and the circuitry necessary to interlock these triggering circuits with the pulse system of the inverter is also eliminated (see Figure 8-23). If this drive system were applied to a moving vehicle, for instance, it would be possible to use a gas turbine prime mover directly coupled to a high speed alternator which in turn would supply the variable frequency inverter drive to power inductor motors coupled to the wheels. This system produces the ultimate in a high efficiency, high performance, light weight, and low operating cost electric transmission for large vehicle drives, with the added feature of making ac power available for auxiliary systems with a single power generating unit. The application of this concept to military vehicles, high speed rapid transit cars and large earth moving equipment is a technical reality. With the availability of low cost, sophisticated power thyristors it is an economic practicality.


Figure 8-23. Block Diagram of DC Link Inverter Circuits

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Automatic scribing systems employ a laser beam to cut chips from large SCR wafers in a "scribe and break technique." Computer programmed, the lasers provide high production capacity with accuracy. The chips, or junctions, are used for low power SCR's.

## Choppers

## Switching Principles [1]

If a switch is connected between a source of direct current and a load as in Figure 9-1(a), it is possible to energize or de-energize the load by simply closing or opening the switch. The voltage at the load terminals appears as in Figure $9-1$ (b) if the switch is opened and closed periodically.

The average voltage to the load is $\mathrm{E}_{\mathrm{DC}} / 2$, if in Figure 9-1(b), $\mathrm{t}_{1}$ is made equal to $t_{2}$. This voltage can be varied by maintaining $\mathrm{t}_{1}$ constant and varying $t_{2}$ (sometimes called pulsed rate modulation), by holding $\mathrm{t}_{2}$ constant and varying $\mathrm{t}_{1}$

(a) BASIC CHOPPER CIRCUIT

$t_{1}$ SWITCH CLOSED, $t_{2}$ SWITCH OPEN
(b) LOAD VOLTAGE WAVEFORM

Figure 9-1. Basic Chopper Circuit and Output Voltage Waveform
(sometimes called pulse width modulation), or by varying both $\mathrm{t}_{1}$ and $t_{2}$.

It is easy to see how this system can be used to decrease the average voltage to the load, thus serving the purpose of a de step-down transformer. Two basic techniques are available to provide a means of increasing the voltage from the supply to the load. The first of these, as shown in Figure 9-2, utilizes a transformer between the chopping switch $\mathrm{S}_{1}$ and the load. Theoretically, as the switch is opened and closed in a periodic manner, the voltage to the load is again described by a chain of rectangular pulses, as in Figure 9-1(b), except that the maximum load voltage is now described in Formula 9-A and the maximum average load voltage is described in Formula 9-B:

ELOAD, MAX. $=\operatorname{EDC}_{\mathrm{DC}} \frac{\mathrm{N}_{2}}{\mathrm{~N}_{1}}$
Where:

$\mathrm{N}_{1}=$ primary turns
$\mathrm{N}_{2}=$ secondary turns
$\mathrm{E}_{(\mathrm{AV})} \mathrm{LOAD}$, MAX. $=$
$E_{D C} \frac{N_{2}}{N_{1}} \cdot \frac{t_{1}}{t_{1}+t_{2}}$
Where:
$\mathrm{t}_{1}=$ time switch is closed $\mathrm{t}_{2}=$ time switch is open

Although this system acts as a step-up transformer, the average


Figure 9-2. Transformer Load Switch
voltage to the load can still be varied by the means described for the basic Chopper Circuit (Figure 9-1(a)). When the switch is closed, the transformer and the load are energized. Then, as the switch is opened, the load is de-energized. The reactive nature of the transformer causes a voltage to be generated whose magnitude can be derived by Lenz' law, formula 9-C.

$$
\begin{equation*}
e=-N \frac{d \phi}{d t} \tag{9-C}
\end{equation*}
$$

Where:
e = generated or induced voltage
$\mathrm{N} \quad=$ number of turns
$\mathrm{d} \phi / \mathrm{dt}=$ rate of change of flux
If the switch were infinitely fast, the current in the transformer would try to cease instantaneously and the change in flux would also tend to be instantaneous.

This would result in a theoretically infinite voltage being generated by the transformer in a direction to continue the flow of current. The voltage measured across the switch would be $\mathrm{E}+\infty$ and the diode would be required to block an infinite voltage.

Obviously, no physically realizable switch can operate (either open or closed) in zero time. However, the time can be sufficiently short to cause inordinately high


Figure 9-3. Transformer Load Switch with Free-wheeling Diode
voltages to be generated. One way to substantially reduce these voltages and yet continue the current in the transformer without continuing the load current is to connect diode $\mathrm{RD}_{1}$ as shown in Figure 9-3. A diode in a configuration such as this is sometimes known as a "freewheeling" or "by-pass" diode. This technique of obtaining slow flux decrease requires that the energy stored in the transformer be dissipated by means of the free-wheeling current.

Since this process takes time, it is necessary that the switch remain open during this decay period so that the transformer flux can be returned to remanence. Anothermeans of accomplishing the same result would be to provide a second winding on the transformer and to connect this winding in one of two ways, as shown in Figure 9-4 and 9-5.


Figure 9-4. Transformer Load Switch with Reset Winding


Figure 9-5. Transformer Load Switch with Clamped Reset Winding

In the case of Figure 9-4, the transformer flux is reset by means of the extra transformer winding being connected to the supply through limiting resistor $R_{1}$. The resetting action in Figure 9-5 is provided by clamping the resetting winding through diode $\mathrm{RD}_{1}$ to the supply. With the exception of the configuration in Figure 9-4, the transformer must be provided with an air gap in all of these schemes in order to avoid saturation.

Another method of constructing a step-up de transformer is by means of the circuit shown in Figure $9-6$. In this case, the reactive "kick" of an inductor, $\mathrm{L}_{1}$ is used to generate very high voltages by means of a fast acting switch. While the switch is closed, energy is stored in the inductor $\mathrm{L}_{1}$. When the switch is open a voltage is generated across $\mathrm{L}_{1}$ to keep the current flowing in the reactor. This voltage causes current to be conducted to the load and to charge capacitor $\mathrm{C}_{1}$. The diode, $\mathrm{RD}_{1}$, serves to block the capacitor from discharging into the switch while it is closed.

Each of these techniques is made practical by using thyristors, such


Figure 9-6. Step-Up Chopper
as SCRs or triacs, as the switch. However, since a thyristor is basically a latching device, a means must be provided to cause conduction to cease (open the switch). A circuit designed to accomplish this is called a commutating circuit. The function of the commutating circuit is to switch (or commutate) the load current away from the thyristor for a period sufficiently long for the thyristor to recover its blocking capability.

A discussion of various types of commutation circuits is appropriate in order to indicate some of the many techniques available to the circuit designer. These various methods of commutation are useful, not only for choppers, but also for inverters.

## Commutation Circuits

The first type of commutation to be used is called the "Morgan" circuit, as shown in Figure 9-7, using a form of self-saturating choke, $\mathrm{L}_{1}$, in series with the commutation capacitor, $\mathrm{C}_{1}$, connected in parallel with the $\mathrm{SCR}, \mathrm{SCR}_{1}$, to be commutated. The choke $\mathrm{L}_{1}$ in this circuit is a self-saturating type using a square loop core material. The volt-second capacity of this
core and the half period of oscillation between the choke's aftersaturation inductance and the capacitor $\mathrm{C}_{1}$ set the on time of the chopper. Thus, this type of chopper is naturally a pulse rate modulation circuit.

If a second winding were added to $\mathrm{L}_{1}$ and connected to a dc source, the apparent volt-second capacity of $L_{1}$ could be varied by varying the resulting flux setting current in the second winding. This then would make the circuit suitable for pulse width modulation. Recharging the commutation capacitor $\mathrm{C}_{1}$, in this circuit, takes place during the off time of $\mathrm{SCR}_{1}$. The discharge of $\mathrm{C}_{1}$ through $\mathrm{SCR}_{1}$ is limited by the after-saturation inductance of $\mathrm{L}_{1}$ and thus is the determining factor (other than the load) of di/dt in the SCR.

This circuit was developed in the days when SCRs with guaranteed dynamic properties (turn-off time, $\mathrm{dv} / \mathrm{dt}$, di/dt, turn-on dissipation) were expensive and sometimes impossible to obtain. The advantages of this type of commutation are obvious in the light of these early drawbacks as compared to using a separate SCR to activate the commutation circuitry. Some of the early choppers for control of small


Figure 9-7. Morgan Circuit
dc motors used this principle successfully.

As the cost of SCRs began to decrease and more became known about $\mathrm{dv} / \mathrm{dt}$ limitations of the devices (but before much work had been done in establishing device turn-on dissipation limitations), other types of commutation became attractive. An example of one of these configurations is shown in Figure 9-8.

As $\mathrm{SCR}_{1}$ is turned on, it not only supplies the load, but also supplies energy to charge $\mathrm{C}_{1}$ resonantly through $\mathrm{RD}_{1}$ and $\mathrm{L}_{1}$. When $\mathrm{C}_{1}$ is fully charged, $\mathrm{RD}_{1}$ suddenly becomes back-biased. This then forward biases the gate to cathode junction of $\mathrm{SCR}_{2}$, turning $\mathrm{SCR}_{2}$ on. The capacitor voltage is then impressed across the load (the capacitor in a high $Q$ circuit can be charged nearly to 2 E ) back biasing $\mathrm{SCR}_{1}$ and supplying the load energy while SCR $_{1}$ turns off. The circuit as shown then is suitable for pulse rate modulation. If, however, the gate of $\mathrm{SCR}_{2}$ were not connected as shown, but instead was supplied by a separate pulsing circuit with a varying, controllable pulse rate, the circuit could be used in the pulse width modulation mode.


Figure 9-8. Pulse Rate Modulation Circuit

This circuit (Figure 9-8) has several disadvantages. First, the commutation charging current must be carried by $\mathrm{SCR}_{1}$, thus decreasing its useful rating with respect to the load. Secondly, the di/dt through $\mathrm{SCR}_{2}$ is inherently high and must be suppressed by added circuit reactance. And finally, the rise of commutation voltage at the beginning of the commutation interval is quite abrupt and can cause corona in the load, as well as extending the reverse recovery interval of SCR 1 . This circuit has been used successfully on de to de converters for battery charging with and without transformer isolated loads on both low and high voltages. However, the disadvantages are considerable, and, in general, there are modern techniques which better suit the SCRs available today.

As has been seen, most commutation techniques have depended upon a resonant circuit to charge the commutation capacitor. The Morgan circuit was unique in that it combined the functions of the resonant circuit inductance, commutation switch and the pulse width timing device all into one component, the reactor. (Attributable to the clever use of magnetics usually in evidence in Morgan's work.) An analog for this circuit is shown in Figure 9-9.


Figure 9-9. Modified Morgan Circuit

The operation of this circuit can be very similar to that of the Morgan chopper. $\mathrm{SCR}_{2}$ is first turned on allowing capacitor $\mathrm{C}_{1}$ to charge through the load and inductance $\mathrm{L}_{1}$. When capacitor $\mathrm{C}_{1}$ is fully charged, $\mathrm{SCR}_{2}$ turns off from lack of anode current (assuming its gate signal has been removed). $\mathrm{SCR}_{1}$ can then be turned on, energizing the load. Since $\mathrm{SCR}_{3}$ is in a blocking state, capacitor $\mathrm{C}_{1}$ remains charged. When $\mathrm{SCR}_{3}$ is turned on, the capacitor will discharge resonantly with $\mathrm{L}_{1}$ through $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{3}$ and the voltage on the capacitor will reverse polarity. When $\mathrm{SCR}_{2}$ is once more turned on, capacitor $\mathrm{C}_{1}$ will be discharged resonantly through $\mathrm{L}_{1}$ and $\mathrm{SCR}_{2}$ through the load. This will apply a back-bias to $\mathrm{SCR}_{1}$ and allow it to turn off and regain its blocking capabilities. Thus, by controlling the triggering rates of $\mathrm{SCR}_{1}, \mathrm{SCR}_{2}$ and $\mathrm{SCR}_{3}$, as well as the time relationships among their gating signals, either pulse width or pulse rate modulation or a combination of the two is possible with this circuit. The advantages of this type of circuit are obvious. The commutation pulse application can be made gradual, and the di/dt or switching losses in the various SCRs due to the commutation, are minimized by judiciously choosing the choke ( $\mathrm{L}_{1}$ ).

The disadvantages of the circuit are, of course, that $\mathrm{SCR}_{1}$ is required to carry the commutation charging current and three SCRs are used to accomplish the logic. Of course, $\mathrm{SCR}_{3}$ could be replaced by a diode (as shown in Figure 9-10). This eliminates the ability to control the timing between the inversion of voltage on $\mathrm{C}_{1}$ and the triggering on $\mathrm{SCR}_{1}$. Otherwise, the


Figure 9-10. Modified Morgan Circuit-Diode
Replacing one SCR
operation of the circuit is the same.

An interesting extension of this type of commutation is achieved by what is termed "delay line" commutation. By replacing the simple LC of Figure $9-10$ with a "delay line" or pulse-forming network, some interesting effects can be achieved. A sample of this type of circuit is shown in Figure 9-11. The interesting characteristic of this type of commutation is that it concentrates the commutation energy in a trapezoidal current wave, thus providing excellent conditions for turning off $\mathrm{SCR}_{1}$. For large power levels the commutation capacitor can be divided into several separate capacitors so that load sharing by the capacitors can be assured, due to the insertion of the network inductances. The waveshape of current through $\mathrm{SCR}_{2}$ also tends to be trapezoidal, thus allowing it to be operated under more ideal conditions, especially for low frequency applications.

This type of commutation is especially useful in conjunction with the type of step-up chopper shown in Figure 9-6. The combination of the two circuits can be seen


Figure 9-11. Modified Morgan
Circuit - Delay
Line Added
in Figure 9-12, the operation of this circuit being the same as described for Figure 9-6.

In order to minimize the probability of an SCR being triggered falsely by high rates of rise of line voltages or disturbances in the load, it has become common practice to use an R-C circuit (snubber) in parallel with the SCR to reduce the rates of rise of these voltages. It is possible, by arranging the commutation components properly, as shown in Figure $9-13$, to combine the functions of the "snubber" and the commutation circuits. With a given load impedance, the $\mathrm{dv} / \mathrm{dt}$ to which $\mathrm{SCR}_{1}$ is subjected can be predicted by choosing $\mathrm{C}_{1}$ properly. However, the size of $\mathrm{C}_{1}$ as dictated by the turn-off time of $\mathrm{SCR}_{1}$, is generally larger than the values dictated by the $\mathrm{dv} / \mathrm{dt}$ rating of $\mathrm{SCR}_{1}$. Thus, the R-C snubber can be eliminated with no loss of performance. The function of $\mathrm{RD}_{2}$ in this circuit is simply to allow excess charge in $\mathrm{C}_{1}$ (charge in addition to that necessary to supply the load during the turning off of $\mathrm{SCR}_{1}$ ) to be used to recharge the capacitor, rather than dissipating it uselessly in the load.


Figure 9-12. Step-Up Chopper With Delay Line


Figure 9-13. Chopper with Commutation Capacitor Functioning also as a Snubber Capacitor

An extension of this principle is shown in Figure 9-14. This circuit combines the functions of the snubber network with the delay line commutation circuit into a single set of components. In this case, $\mathrm{RD}_{1}$ and $\mathrm{C}_{1}$ act to suppress $\mathrm{dv} / \mathrm{dt}$ across $\mathrm{SCR}_{1}$. $\mathrm{C}_{1}$ also acts with $\mathrm{L}_{1}$, $\mathrm{L}_{2}$, and $\mathrm{C}_{2}$, as the commutation circuit tending to form a trapezoidal commutation current waveform. A diode in anti-parallel with $\mathrm{SCR}_{1}$, to recapture excess commutation energy, can also be added to this circuit.


Figure 9-14. Chopper with Delay Line Type Commutation Capacitor Functioning also as a Snubber Capacitor

Each of these combinations has advantages and disadvantages as outlined, and, of course, there are an infinite number of combinations possible to achieve desired circuit characteristics. However, certain characteristics of such circuits, from the standpoint of properly commutating the SCR, must be considered by the design engineer. These are:
A. High inrush current in the SCR
B. Provide reverse bias to the SCR during commutation
C. High voltage transients imposed on the SCR
D. High rates of rise of reverse current causing increased SCR dissipation
E. Re-applied rate of voltage rise on the SCR after the commutation period
F. High rates of rise of forward voltage imposed on the SCR during its off-state
By observing these characteristics of the circuit carefully, and by properly coordinating with the SCR manufacturer, the designer can be
sure of choosing the optimum arrangement for his particular application. At the same time, the designer can be confident of a reproducible system with a high degree of reliability. A summary of the main advantages and disadvantages of three of the more basic chopper circuits is included in Table IX-I.

## DC Motor Drives

A dc chopper type propulsion speed control is required to operate over a relatively wide range of speed, using a solid-state switch. The variable on-off duty cycle transfers a quantity of pulsed energy into the dc motor. The pulsed battery current is stored and expended within the motor and its series inductance during each period of SCR conduction and also during period when the free-wheeling diode is conducting. By this
means, a dc transformer essentially is created with the choke and motor acting as energy storage components. However, the instantaneous battery current amplitude, which equals the motor current demand during the "on" period of the switch, results in very large peak power demands from the battery. This is less than desirable from the standpoint of battery charge life. This may be corrected by one of two means, 1) inserting a means of energy storage between the battery source and the chopper, and 2) of sequentially switching a multi-phase chopper containing individual de reactors and free-wheeling diode current paths. A combination of the two methods results in an optimum design in terms of system efficiency, weight, and cost.

Regardless of the type of chopper employed, the basic de chopper

Table IX-I. Advantages and Disadvantages of Three Basic Chopper Circuits

|  | Advantages | Disadvantages |
| :---: | :---: | :---: |
| Morgan Circuit (Figure 9-7) | 1. Simplicity - only one SCR needed | 1. Approximately fixed on time so only useful for pulse rate modulation. <br> 2. Requires saturable reactor <br> 3. Current to reverse commutation capacitor charge increases rating required of SCR |
| Modified Morgan Circuit <br> (Figure 9-9) | 1. All types of pulse modulation control are possible | 1. Requires three SCRs (or two if SCR3 replaced by diode) <br> 2. Main SCR must carry current to reverse charge or commutation capacitor |
| Chopper with Snubber (Figures 9-13 and 9-14) | 1. Includes dv/dt and di/dt limiting | 1. Commutating reactor carries dc load current <br> 2. Main SCR carries current to reverse charge on commutation capacitor |

circuit can be represented as in Figure 9-15. The waveforms shown in the same figure assume negligible change in the motor back EMF. After interrupting the current flow in the switch, voltage is induced across the inductor which attempts to maintain the flow of current in the inductor. This current flows in the same direction but in decreasing magnitude through the motor and the free-wheeling diode, $\mathrm{RD}_{1}$.

Low speed motor operation for large drives requires large current amplitudes. Figure $9-16$ shows a typical motor drive characteristic where maximum acceleration performance or torque capability is required to half speed, typically at about $50 \%$ chopper duty cycle. Using this, then, as a typical vehicle propulsion profile, and since this exhibits a low speed dc motor cur-
rent requirement of twice the full speed current to provide an acceptable acceleration characteristic or torque capability, it can be seen that low speed, high torque operation will result in the least efficient source power utilization. A typical battery bank, consisting of 110 cells delivering 142 volts no-load voltage and 34 ampere-hours capacity when fully charged, exhibits a source resistance of 135 milliohms. In terms of 500 ampere current pulses, this results in a $52 \%$ battery source utilization. This is poor performance, not only in terms of source efficiency, but also in RMS heating loss. Implementation of a two-phase sequentially switched chopper will increase battery efficiency to $75 \%$ by decreasing the battery surge pulse current to $50 \%$ of the current amplitude for the

(a) BASIC DC MOTOR CHOPPER CIRCUIT

(b) LOAD VOLTAGE AND CURRENT WAVEFORMS

Figure 9-15. Basic Chopper Type DC Motor Drive


Figure 9-16. Typical Chopper Motor Drive Characteristics
single-phase chopper when operating at low duty cycle. Although additional sequentially phase switches would further reduce the battery losses for identical motor current demand, added system complexity may not warrant the additional cost. The required operating load and converter size will play a strong part in determining the feasibility of using more than two sequentially phase switches [17].

The addition of a filter between the source and the chopper may also come into the study as a strong primary determining factor. A typical schematic for a two-phase sequentially switched dc motor drive with L-C filter buffering is shown in Figure 9-17. Thus, by using this type of system and alternately storing energy in one of the chokes, while the opposite choke is discharging, the peak amplitude of the current drain from the motor is reduced by $50 \%$, resulting in the
battery efficiency while discharging shown in Figure 9-18.

It is interesting to note that should additional powered axles beyond a two-wheel motor drive be required, a corresponding decrease in the peak ripple current can be obtained if these additional axles are also switched in sequence to the others. The control frequency can be regulated in terms of minimum battery ripple current, while the individual wheel speeds are still controlled by means of the chopper duty cycle or pulse width modulation. This, in turn, reduces the size of the battery capacitor filter required.

A very simple system utilizing the chopper as a resistance modulator to control the speed of a dc motor is shown in Figure 9-19. In this circuit the chopper is located across a section of current limiting resistance which is in series with the series motor. The method of operation is simply to increase the duty


Figure 9-17. Sequentially Switched Two-Phase Chopper
cycle of the SCR until it is essentially full on, thus reducing the effective resistance in series with the dc motor by the amount of resistance across which the SCR is located. Then, by closing one of the mechanical contactors located across an equal segment of resistance in the propulsion circuit and by stopping the chopping action of the SCR circuit, the shunting action is transferred to the contactor. The chopper can then be increased in
duty cycle again until essentially a second section of the resistor has been shunted by it, at which time the second contactor can be closed, the chopper again reduced to zero duty cycle and the chopping action then repeated. By this means smooth acceleration can be obtained. It might be mentioned also that a similar means can be utilized for performing solid-state type motor field shunting, again using the chopper.


Figure 9-18. Discharge Characteristics of Two-Phase Chopper

DC Motor Step-Down Choppers
To control the power to a dc motor by means of a series chopper, it is preferable to provide a commutation system which is independent of the condition of the motor, to provide for stopping, and for reliable commutation. In the circuit in Figure $9-20, \operatorname{SCR}_{1}$ is the main power SCR supplying power directly from the source to the motor. $\mathrm{C}_{1}$ is a large bank of capaci-
tors necessary to provide a low impedance source from which the chopper will operate. The action of the circuit is described as follows: $\mathrm{SCR}_{2}$ is turned on, charging $\mathrm{C}_{2}$ through $\mathrm{L}_{1}, \mathrm{RD}_{1}$; and $\mathrm{SCR}_{2}$ through the smoothing reactance L3 located in series with motor, MA and MF. Once capacitor $\mathrm{C}_{2}$ becomes charged, $\mathrm{SCR}_{2}$ turns off due to the cessation of current, at which time $\mathrm{SCR}_{1}$ may be turned


Figure 9-19. Resistance Modulator Chopper Circuit
on. $\mathrm{C}_{2}$ remains charged in the polarity shown. After $\mathrm{SCR}_{1}$ is turned on, $\mathrm{SCR}_{3}$ may be turned on, which discharges $\mathrm{C}_{2}$ through $\mathrm{SCR}_{3}, \mathrm{~L}_{2}$, $\mathrm{L}_{1}$, and $\mathrm{SCR}_{1} . \mathrm{C}_{2}$ then charges in the opposite direction to the polarity shown.

Reactor $\mathrm{L}_{2}$ limits the additional peak current that $\mathrm{SCR}_{1}$ is subjected to during the reversal of charge on $\mathrm{C}_{2}$ when $\mathrm{SCR}_{3}$ is triggered. This optimizes the utilization of $\mathrm{SCR}_{1}$ for controling the motor speed. Both $\mathrm{RD}_{1}$ and $\mathrm{RD}_{2}$ should be fast recovery diodes in order to minimize the transients caused by stored energy during the reverse recovery of these devices. $\mathrm{RD}_{2}$ is simply to provide a by-pass for current from $\mathrm{L}_{3}$ through the motor and helps smooth the motor cur-
rent. With this type of commutation scheme, as the motor builds in speed and the counter EMF rises, the available voltage to charge $\mathrm{C}_{2}$ from the source, which is the source voltage minus the armature voltage of the motor, decreases. This in itself is not a limiting factor since any voltage on the capacitor in the order of ten or twenty volts would be sufficient to commutate $\mathrm{SCR}_{1}$ in terms of providing negative bias, since this commutation scheme through $\mathrm{SCR}_{3}$ provides a means for reversing the charge on the capacitor. However, it is required under those conditions for the capacitor to store enough energy to provide the required current by the motor during this commutation period. The need for the


Figure 9-20. DC Motor Step-down Chopper
capacitor to operate from a wide range of operating voltages increases the energy storage requirement of the capacitor significantly.

Another characteristic with this type of commutation means is that should commutation not be achieved sucessfully, there is no longer any control over $\mathrm{SCR}_{1}$. A method of correcting both these faults of the circuit is to provide an auxiliary charging source by which capacitor $\mathrm{C}_{2}$ can be charged through $\mathrm{SCR}_{2}$ even during the period that $\mathrm{SCR}_{1}$ has been turned on. This is the reason for incorporating diode $R D_{1}$ in the circuit. $\mathrm{RD}_{1}$ serves to block the auxiliary charging current from flowing through $\mathrm{L}_{1}$ and $\mathrm{SCR}_{1}$, thus isolating the auxiliary charging circuit from the main power circuit. Using this scheme it is now possible to have a mis-commutation of the system, recharge capacitor $\mathrm{C}_{2}$ from the aux-
iliary charging circuit and retrigger the commutation system. This permits commutation of $\mathrm{SCR}_{1}$ regardless of an intermittent fault in the system. Once $\mathrm{C}_{2}$ has been charged negatively, (opposite to the polarity shown in Figure 9-20) $\mathrm{SCR}_{2}$ can be triggered on at any time in order to cause commutation of $\mathrm{SCR}_{1}$.

Reliable commutation without the necessity of an auxiliary voltage source is achieved by the practical chopper shown in Figure 9-21. The important current and voltage waveforms for this circuit are shown in Figure 9-22. These waveforms assume steady-state operation with a chopping frequency high enough so there is negligible ripple in the motor current. In addition to providing reliable commutation without the addition of an auxiliary commutating voltage source, the circuit of Figure 9-21 has several other advantages:


Figure 9-21. Modified Series DC Motor Chopper
A. The di/dt is limited in each SCR due to the inductors $\mathrm{L}_{1}$ and $\mathrm{L}_{2}$ and the motor field inductance.
B. The dv/dt reapplied to each SCR is limited.
C. The commutating capacitor $\mathrm{C}_{1}$ is reset to zero volts by discharging into the load after the end of each commutation. Assuming sufficient load for this to occur, the commutating voltage is then load independent.

## Analysis of a Step-Up Chopper [15.16] <br> Figure 9-23 shows a diagram of a

 step-up chopper circuit. MF is the field winding of the motor and ${ }^{e} \mathrm{C} 1$ is the voltage across the armature taking into account the drop due to armature resistance; it is also the voltage across capacitor $\mathrm{C}_{1} . \mathrm{SCR}_{1}$is the main SCR and $\mathrm{SCR}_{2}, 3,4$, and 5 are the commutating SCRs. $\mathrm{C}_{2}$ is the commutating capacitor and $\mathrm{C}_{1}$ is a filter capacitor.

Ideally $\mathrm{SCR}_{1}, 2,3,4$, and 5 and $\mathrm{C}_{2}$ act together as a switch. This is represented in Figure 9-24. When the switch is closed, the supply voltage EDC is impressed across the field winding and current iF builds up linearly. When the switch is open, the current flows through diode $\mathrm{RD}_{1}$ and into capacitor $\mathrm{C}_{1}$ and the motor armature, MA.

When the circuit has reached steady-state operation, the average voltage across the inductor is zero, and the relationships in equation $9-\mathrm{D}$ and $9-\mathrm{E}$ hold true:
$\frac{E_{D C} \cdot t_{\text {on }}+\left(E_{D C} \cdot e_{C 1}\right) t_{\text {off }}}{t_{\text {on }}+t_{\text {off }}}=0(9-D)$


Figure 9-22. Waveforms for Modified Series DC Motor Chopper


Figure 9-23. Step-Up Chopper Power Circuit


Figure 9-24. Equivalent Step-Up Chopper Power Circuit

Where:

| $E_{D C}$ | $=$ supply voltage |
| ---: | :--- |
| $\mathrm{t}_{\text {On }}$ | $=$ time on |
| $\mathrm{e}_{\mathrm{C} 1}$ | $=$ voltage across armature |
| $\mathrm{t}_{\text {off }}$ | $=$ time off |
| OR |  |
| $\mathrm{e}_{\mathrm{C} 1}$ | $=\frac{\mathrm{t}_{\text {on }}+\mathrm{t}_{\text {off }}}{\mathrm{t}_{\text {off }}}$ |
|  | $=\frac{\mathrm{E}_{\text {DC }}}{1-\text { Duty Cycle }}$ |

Where:
Duty Cycle $=\frac{t_{\text {on }}}{t_{\text {on }}+t_{\text {off }}}$

Equation 9-E indicates the stepup feature of the circuit. When $t_{\text {on }}$ is small compared to $t_{\text {off }} e^{e} 1$ is nearly equal the supply voltage $E_{D C}$. As $t_{\text {on }}$ increases relative to $t_{\text {off }}$ the voltage $e^{e} 1$ becomes greater.

In order for SCR 1, 2, 3, 4, and 5 to act as the switch, they must be triggered in the proper sequence. The following is an analysis of the circuit at each step of its operation. A sketch of the voltage across the motor field at each time interval is shown in Figure 9-25. Note that the average voltage is ZERO.


Figure 9-25. Voltage Across Motor Field in Step-Up Chopper Power Circuit

Assume that the circuit is in steady-state, and initially all SCRs are turned off and voltage eC2 across $\mathrm{C}_{2}$ is equal to eC1.

Trigger $\mathrm{SCR}_{1}\left(\mathrm{t}_{1}>\mathrm{t}>\mathrm{t}_{0}\right)$. When $\mathrm{SCR}_{1}$ is triggered, diode $\mathrm{RD}_{1}$ is reversed biased. Voltage $\mathrm{E}_{\mathrm{dc}}$ appears across inductor MF (see Figures 9-25 and 9-26) and the current $i_{F}$ builds up linearly.

Trigger $\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}\left(\mathrm{t}_{3}>\mathrm{t}\right.$ $>\mathrm{t}_{1}$ ). $\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$ are one pair of commutation SCRs. When they are triggered, capacitor $\mathrm{C}_{2}$ is placed in parallel with $\mathrm{SCR}_{1}$. From $\mathrm{t}_{1}$ to $t_{2}, \mathrm{SCR}_{1}$ is reverse biased and cur-
rent $\mathrm{i}_{\mathrm{F}}$ flows through $\mathrm{SCR}_{3}, \mathrm{C}_{2}$, and $\mathrm{SCR}_{4}$ (See Figure 9-27).

As the current $\mathrm{i}_{\mathrm{F}}$ flows into $\mathrm{C}_{2}$, the voltage reverses. At t2, voltage ${ }^{e}$ C2 reaches the same magnitude as ${ }^{e} \mathrm{C} 1$ and diode $\mathrm{RD}_{1}$ again conducts (See Figure 9-28).

Trigger $\mathrm{SCR}_{1}\left(\mathrm{t}_{4}>\mathrm{t}>\mathrm{t}_{3}\right)$. $\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$ turn off when $\mathrm{SCR}_{1}$ is gated. The circuit is again the same as in Figure 9-26.

Trigger $\mathrm{SCR}_{2}$ and $\mathrm{SCR}_{5}\left(\mathrm{t}_{6}>\mathrm{t}\right.$ $\left.>\mathrm{t}_{4}\right) . \mathrm{SCR}_{2}$ and $\mathrm{SCR}_{5}$ make up the other pair of commutation SCRs. Note that when $\mathrm{SCR}_{3}$ and SCR4 were on, the capacitor volt-


Figure 9-26. Step-Up Chopper Power Circuit $-\mathrm{SCR}_{1}$ On


Figure 9-27. Step-Up Chopper Power Circuit $-\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$ Gated


Figure 9-28. Step-Up Chopper Power Circuit $-\mathrm{SCR}_{3}$ and $\mathrm{SCR}_{4}$ On and $R D_{1}$ Conducting
age eC2 had reversed. When SCR 2 and $\mathrm{SCR}_{5}$ are triggered, the polarity is such that $\mathrm{SCR}_{1}$ is again reverse biased and current iF flows into capacitor $\mathrm{C}_{2}$ (See Figure 9-29). Again when e${ }^{\mathrm{C}} 2$ reverses and builds up to ${ }^{e} \mathrm{C} 1$ (at $\mathrm{t}=\mathrm{t}_{5}$ ), diode $\mathrm{RD}_{1}$ conducts (See Figure 9-30). At this point the cycle begins again.

$$
\begin{equation*}
T=\frac{K_{t}}{(1-D)} \frac{E_{D C}}{(1-D)^{2}\left(R_{A}\right)^{2}+2(1-D) K V R_{A} W+\left(K_{V}\right)^{2} W^{2}} \tag{9-F}
\end{equation*}
$$



Figure 9-29. Step-Up Chopper Power Circuit $-\mathrm{SCR}_{2}$ and $\mathrm{SCR}_{5}$ Gated


Figure 9-30. Step-Up Chopper Power Circuit $-\mathrm{SCR}_{2}$ and $\mathrm{SCR}_{5}$ on and $R D_{1}$ Conducting
Where:
$R D_{1}$ Cond
$\mathrm{K}_{\mathrm{t}}=$ torque constant
$1-\mathrm{D}=$ fraction of time off $=$

$$
\frac{t_{\text {off }}}{t_{\text {off }}+t_{\text {on }}}
$$

$$
\begin{aligned}
& \mathrm{E}_{\mathrm{DC}} \\
& \mathrm{R}_{\mathrm{A}}
\end{aligned}
$$

$\mathrm{E}_{\mathrm{DC}}=$ dc supply voltage
$\mathrm{R}_{\mathrm{A}}=$ motor armature resistance.
$\mathrm{K}_{\mathrm{V}}=$ counter EMF constant
$\mathrm{W}=$ speed in radians/second
It is very interesting to note that the torque-speed characteristic for this modified series motor control is essentially the same as for a conventional de series motor. Figure 9-32 shows the time relationships among the gate trigger pulses applied to $\mathrm{SCR}_{1}, 2,3,4$ and 5 .

The voltage waveform across $\mathrm{SCR}_{1}$ appears as shown in Figures 9-33 and 9-34 along with the gating pulses to $\mathrm{SCR}_{1}$. When $\mathrm{SCR}_{1}$ is triggered, the voltage drops to zero and current builds up in the field. When a pair of commutating SCRs is gated, the negative voltage on the commutating capacitor instantly appears and the capacitor charges up fairly linearly to the output voltage on the filter capacitor. The waveform is very similar to the ideal waveform shown in Figure 9-25.

Figure $9-33$ is with $\tau \approx 3 / 4$ where the output voltage should be


Figure 9-31. Step-Up Chopper - Torque Vs. Speed


Figure 9-32. Step-Up Chopper - Gating Pulse Timing


UPPER TRACE: SCR 1 VOLTAGE $10 \mathrm{~V} /$ div
LOWER TRACE: GATE TO CATHODE VOLTAGE OF SCR $11 \mathrm{~V} / \mathrm{div}$ TIME BASE: $0.1 \mathrm{msec} / \mathrm{div}$

Figure 9-33. Step-Up Chopper-SCR 1 Anode and Gate Voltage Waveforms for $\tau \approx 3 / 4$


UPPER TRACE: $S C R_{1}$ VOLTAGE $20 \mathrm{~V} / \mathrm{div}$
LOWER TRACE: GATE TO CATHODE VOLTAGE OF SCR $12 \mathrm{~V} / \mathrm{div}$
TIME BASE: $0.1 \mathrm{msec} / \mathrm{div}$
Figure 9-34. Step-Up Chopper - SCR 1 Anode and Gate Voltage Waveforms for $\tau \approx 1 / 3$

16 volts. The measured value was 15 volts. Figure $9-34$ was taken with $\tau \approx 1 / 3$ and the measured output voltage was 40 volts. The theoretical voltage is 36 volts.

The motor armature voltage is quite smooth, as shown in Figure 9-35.

The current drawn from the source contains considerable ripple as shown in Figures 9-36 and 9-37. The voltage across $\mathrm{SCR}_{1}$ appears in these figures as the top trace. When $\mathrm{SCR}_{1}$ is triggered, the current builds up rapidly. At the point where a pair of commutating SCRs is triggered, the current rises sharply until the voltage on the commutating capacitor reverses to equal 12 volts. During the off time, the current decays as it is fed into the filter capacitor and motor armature.

Figure 9-36 was taken with minimum output voltage of about 15 volts. The current changes from 1 to 9 amps .

Figure 9-37 was taken with an output voltage of 50 volts. The current in this picture changes from about 20 amps to 50 amps .

The current supplied to the motor armature is very smooth as seen in Figure 9-38.

In summary, this rather novel modified series dc motor control has torque-speed characteristics essentially the same as a conventional series de motor. The main advantage of the circuit is that it is possible to use reasonably standard motor armature voltage ratings even though the de supply voltage is low. For the system discussed, the rated motor armature voltage is 100 volts with a de source voltage of 12 volts. At least a $10: 1$ control range of motor speed and current is possible for a wide range of motor loads. However, the minimum current at low speed is limited by the nature of the motor load and the minimum on-time that is possible for $\mathrm{SCR}_{1}$. A step-up ratio of at least

$20 \mathrm{~V} / \mathrm{div}, 0.1 \mathrm{msec} / \mathrm{div}$
Figure 9-35. Step-Up Chopper - Armature Voltage Waveform


UPPER TRACE: SCR ${ }_{1}$ VOLTAGE $10 \mathrm{~V} / \mathrm{div}$
LOWER TRACE: GATE TO CATHODE $5 \mathrm{AMP} / \mathrm{div}$
TIME BASE: $0.2 \mathrm{msec} / \mathrm{div}$
Figure 9-36. Step-Up Chopper - Source Current Waveform $\left(E_{D C}=15 \mathrm{~V}\right)$


Figure 9-37. Step-Up Chopper - Source Current Waveform ( $E_{D C}=50 \mathrm{~V}$ )


Figure 9-38. Step-Up Chopper - Waveform of Current into Armature
$10: 1$ is easily attainable from rated load to a few percent of rated motor load.

With a 12 volt de supply, the circuit efficiency is limited to about $70 \%$. Also, nearly 100 amperes source current is required to deliver 10 amperes to the motor armature with a 10:1 voltage step-up ratio. Thus, with a 12 volt source, this motor control is most appropriate for motor ratings of 10 HP or less. The di/dt imposed on SCR $_{1}$ may be quite high, limited only by the inductance in the $\mathrm{SCR}_{1}, \mathrm{RD}_{1}$ and $\mathrm{C}_{1}$ loop. However, the dv/dt on SCR 1 is limited by the commutating capacitor $\mathrm{C}_{2}$ charging rate.

## Wound Rotor Induction Motor Speed Control

One means of obtaining a vari-able-speed ac motor is to vary the rotor resistance of an induction motor [2]. This method of speed control provides speed-torque char-
acteristics similar to those of a dc shunt motor speed controlled by means of resistance in series with the armature.

Figure $9-39$ is an interesting circuit which functions as a type of resistance modulator. The purpose of this circuit is to vary the average load on the filter $\mathrm{L}_{1}$, $\mathrm{C}_{1}$ and, therefore modulate the effective value of $R_{2}$ reflected to the rotor. The circuit operates as follows: with $\mathrm{C}_{2}$ charged, $\mathrm{SCR}_{1}$ is turned on, drawing current through $R_{1}$. At the same time, the charge on $\mathrm{C}_{2}$ is reversed by the current flow through $\mathrm{RD}_{1}$. Sometime later $\mathrm{SCR}_{2}$ is turned on, back biasing and shutting off $\mathrm{SCR}_{1}$ and recharging $\mathrm{C}_{2}$ positive.

Figure $9-40$ shows an equivalent circuit and theoretical waveforms. The relationships between the battery voltage (EDC) and current (IDC) to the motor parameters are shown in Formula 9-G.


Figure 9-39. Wound Rotor Motor Chopper Speed Control

(c) TYPICAL CHOPPER WAVE SHAPES

Figure 9-40. Wound Rotor Motor Chopper Speed Control Waveforms
$\mathrm{E}_{\mathrm{DC}}=1.35 \mathrm{E}_{\text {line-to-line }}$ (rotor)
$\mathrm{I}_{\mathrm{DC}}=1.22 \mathrm{I}_{\text {rotor }}$
When the synchronous switch is turned on, IDC will rise sharply to $\mathrm{E}_{\mathrm{DC}} / \mathrm{R}_{\mathrm{o}}$. The current will fall to zero when the switch is shut off. If we examine an idealized waveshape of IDC shown in Figure 9-40, it is seen that Formula 9-H applies:
$I_{D C}=\frac{\left(t_{1}\right)}{t_{1}+t_{2}} \frac{E_{D C}}{R_{O}}$
Resistor $\mathrm{R}_{2}$ in Figure $9-39$ is chosen to provide the minimum speed-torque characteristic. Resistor $\mathrm{R}_{1}$ simply limits the current peaks to SCR $_{1}$; however, the relationship results in Formula 9-J.
$\mathrm{S}_{\text {min }}=\frac{\mathrm{R}_{1}}{2 \nu(100 \% \text { ohms })}$
Where:
$\nu=$ maximum possible duty cycle of chopper
By using a pulse width modulated, pulse rate modulated chopper as in Figure 9-39, a duty cycle very close to 1 can be achieved giving the widest possible controllable speed range.

The importance of the filter approach shown in Figure 9-39 can be illustrated by understanding that excessive rotor ripple in the motor can obviously have a profound influence on machine temperature (therefore insulation life) and also perhaps less obviously on bearing life, due to sympathetic vibration.

High efficiency under normal running conditions requires a low rotor resistance; but a high resistance results in a high starting torque and low starting current at low starting power factor.

The motor control of Figure 9-39 provides a simple means of controlling the effective rotor resistance of a wound rotor motor. It also could be readily adapted to closed loop speed control systems, since the rotor resistance is controllable in response to the electrical signal for gating $\mathrm{SCR}_{1}$.

## Battery Charger Design Example [16]

Figure 9-41 shows a chopper battery charging circuit. The main circuit is a series resonant dc-dc chopper; the input is half-wave rectified and filtered. When $\mathrm{SCR}_{1}$ is triggered, the de voltage is applied to the load through series inductor $\mathrm{L}_{1}$; this also starts resonant charging of $\mathrm{C}_{1}$. This charges to a voltage approximately twice the applied dc voltage in the first half-cycle of the resonant interval, and the current returns to zero. In the second halfcycle, the current through $\mathrm{L}_{2}-\mathrm{C}_{1}$ reverses. When it reaches the same magnitude as the load current, $\mathrm{SCR}_{1}$ goes off and diode $\mathrm{RD}_{2}$ conducts to permit current to flow back into the positive side of the dc source. When the current oscillates back to the load current value, the SCR $_{1}-\mathrm{RD}_{2}$ branch opens. Now $\mathrm{C}_{1}$ discharges through the load. If $\mathrm{L}_{1}$ is large compared to $\mathrm{L}_{2}$ and the chopper frequency is relatively high, there is little decay in the load current during this interval; therefore, the voltage on $\mathrm{C}_{1}$ decreases at an almost constant rate. When the voltage on $\mathrm{C}_{1}$ reaches zero, diode $\mathrm{RD}_{3}$ conducts and the load current decreases linearly with the battery load, until $\mathrm{SCR}_{1}$ is triggered again. Capacitor $\mathrm{C}_{1}$ and inductor $\mathrm{L}_{2}$ start each cycle off from zero initial conditions due to the circuit configuration.


Figure 9-41. Chopper-Type Battery Charger

The triggering circuit utilizes a rectified center-tap transformer and a filter capacitor to provide a 20 volt dc power supply to drive $\mathrm{IC}_{1}$ and $\mathrm{UJT}_{1}$. The zener diode, $\mathrm{BD}_{1}$, is used as a reference level for the differential amplifier; $R_{1}$ is a current limiter. The other input to the amplifier is connected to the positive terminal of the battery and is applied through a switch-controlled voltage divider to provide either a 6 - or 12 -volt charge. The output of the amplifier provides a variable voltage to trigger the emitter of UJT $_{1}$. UJT 1 is used to deliver a pulse through pulse transformer $\mathrm{T}_{2}$ which triggers $\mathrm{SCR}_{1}$.

Design factors for the de-dc chopper battery charger are the amount of current desired, the frequency of the chopper, and the frequency of $\mathrm{UJT}_{1}$.

To determine the value of the L-C series circuit, assume the amount of current desired and, depending on whether the circuit is half or full wave rectified, find the approximate dc voltage.
$\mathrm{E}_{\mathrm{DC}}=\frac{\mathrm{E}_{\text {IN }}}{\pi} \approx 50$ volts
With an assumed current of 25 amps,
$\frac{\mathrm{E}_{\mathrm{DC}}}{\sqrt{\mathrm{L} 2 / \mathrm{C} 1}}=2 \times(\max$. load current $)$

$$
\begin{equation*}
=2 \times 25=50 \mathrm{amps} \tag{9-L}
\end{equation*}
$$

This implies that

$$
\begin{equation*}
\frac{\mathrm{L} 2}{\mathrm{C} 1}=1 \tag{9-M}
\end{equation*}
$$

Assume the turn-off time is 50 $\mu \mathrm{sec}$, which is approximately $1 / 3$
the period. Thus, a period is 150 $\mu \mathrm{sec}$.

$$
\begin{align*}
2 \pi \sqrt{(\mathrm{~L} 2)(\mathrm{C} 1)} & =150 \times 10^{-6} \\
\sqrt{(\mathrm{~L} 2)(\mathrm{C} 1)} & =24 \times 10^{-6} \tag{9-N}
\end{align*}
$$

From equations 9-M and 9-L,

$$
\begin{aligned}
& \mathrm{L} 2=\mathrm{C} 1 \\
& (\mathrm{~L} 2)(\mathrm{C} 1)=576 \times 10^{-12} \\
& (\mathrm{C} 1)^{2}=576 \times 10-12 \\
& \mathrm{C} 1=24 \mu \mathrm{~F} \text { and } \mathrm{L} 2=24 \mu \mathrm{H}
\end{aligned}
$$

To determine the oscillation frequency of $\mathrm{UJT}_{1}$

$$
\begin{aligned}
& \frac{50 \mathrm{~V} \times \mathrm{t}_{\mathrm{on}}}{\tau}=12 \mathrm{~V} \\
& \tau=625 \mu \mathrm{sec}
\end{aligned}
$$

This indicates that the chopper frequency will be approximately 1.6 kHz to produce 12 volts output from the 50 volt de source. The
maximum chopper frequency is approximately 6 kHz . Therefore, the UJT frequency range should be from 1 to 6 kHz .

A rough calculation of the ripple current through the battery is provided by



Figures 9-42, 9-43 and 9-44 show waveforms for the operating circuit.

The battery charger circuit of Figure $9-41$ is considerably more complicated than a simple phase control type circuit. However, it provides an apprecable step-down voltage ratio without the need for a transformer. In addition, the filtering required is much smaller to


UPPER TRACE: VOLTAGE FROM SCR CATHODE TO NEGATIVE BUS 50 V /div
LOWER TRACE: LINE VOLTAGE $100 \mathrm{~V} /$ div
TIME BASE: $2 \mathrm{msec} / \mathrm{div}$
Figure 9-42. Waveforms for Chopper-Type Battery Charger


UPPER TRACE: VOLTAGE FROM SCR CATHODE TO
NEGATIVE BUS $100 \mathrm{~V} / \mathrm{div}$
LOWER TRACE: BATTERY VOLTAGE $10 \mathrm{~V} / \mathrm{div}$
TIME BASE: $2 \mathrm{msec} / \mathrm{div}$
Figure 9-43. Waveforms for Chopper-Type Battery Charger
achieve ripple-free charging current. Thus, where a power transformer is not desired or where a more com-
pact and lightweight charger may be required, this chopper charger is a feasible approach.


UPPER: VOLTAGE FROM SCR CATHODE TO NEGATIVE BUS $100 \mathrm{~V} /$ div LOWER: FILTER CAPACITOR VOLTAGE $100 \mathrm{~V} /$ div TIME BASE : $2 \mathrm{msec} / \mathrm{div}$

Figure 9-44. Waveforms for Chopper-Type Battery Charger

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## Fast Recovery Rectifiers

The need for fast recovery diodes has been considerably increased by the development of power control systems using SCRs. Proper use of fast recovery diodes reduces di/dt and accompanying stress levels on SCRs, thereby increasing reliability without necessitating additional complex circuitry.

With fast recovery diodes, power levels may be increased and costly power losses reduced. The primary advantage is that junction heating caused by recovery action is minimized.

Rectifier diodes with fast-recovery characteristics are becoming increasingly important in the design of high-power semiconductor equipment. Circuit designers are showing an increasing interest in these devices for such applications as free-wheeling diodes (also called by-pass diodes), high-frequency inverters, and high-frequency power rectifiers.

Fast-recovery diodes are available today with ratings upwards of 650 A average, and 1300 PRV and higher. Specific devices in these higher current ratings may be obtained with recovery times as short as $1.5 \mu \mathrm{sec}$ maximum when rated 1000 V or less, and $2.0 \mu \mathrm{sec}$ when rated 1100 through 1300 V .

While rectifier diodes with higher voltage and current ratings and shorter recovery times are available, the general rule is that the higher the voltage rating, the longer the shortest recovery time that is available.

High-Frequency Power Rectification
The most obvious application for fast-recovery diodes is in converting high-frequency ac to dc. The upper frequency for efficient rectification with conventional alloy or diffused 250A diodes is about 1 kHz . By contrast, the upper frequency limit for efficient operation of the 100 to 650 A fastrecovery diodes is about 10 kHz .

At any operating frequency, fast-recovery characteristics result in less power dissipation in the diode during recovery, thus more power may be dissipated during the passage of forward current without overheating the diode. The result is a more efficient circuit and a reduction in spurious diode heating.

## Free-Wheeling Diodes in Rectifier Circuits

Large fast-recovery diodes function well as free-wheeling diodes or by-pass diodes, on the output of any single or three-phase SCR rectifier unit when the load is both resistive and inductive, and when the rectifier-unit output voltage is to be reduced by phase-controlling the SCRs. Failure to use freewheeling diodes in rectifier units can result in problems when there is an inductive component to the applied load.

If the load is $100 \%$ inductive, and there is no free-wheeling diode, the inductance will cause current to flow continuously in the SCRs, and zero output voltage is obtained with $90^{\circ}$ phase retard. When the
load includes a resistive as well as an inductive component, and large angles of phase-retard are employed, the load current becomes discontinuous. To obtain zero output voltage with this load, it is necessary to use a larger amount of phase retard; therefore, an abrupt change in the relationship between output voltage and phase retard occurs (at the phase retard angle where the output current becomes discontinuous). Essentially, there is a change in the transfer function of the rectifier unit when viewed as a part of a feedback-regulating system.

The change in operating mode experienced without the free-wheeling diode may therefore create severe instabilities in the operation of a closed-loop voltage or currentregulating system. With or without the free-wheeling diode, the same larger range of phase control is needed to obtain zero output voltage, but the abrupt change in transfer function, and the consequent system instability, are eliminated when the free-wheeling diode is used.

Another advantage of the freewheeling diode is that at reduced output voltage from the rectifier unit current is carried only intermittently by the SCRs. This reduces heating in the SCRs and increases their reliability.

If a hybrid-bridge (semiconverter) circuit is used to feed a partially inductive load, a free-wheeling diode is recommended when nearzero output voltage from the bridge is desired. With the free-wheeling diode, the bridge circuit will feed an apparently resistive load and behave accordingly. Without it, the SCRs may fail to turn off (commutate) when operating with large an-
gles of phase control. This is similar to a failure in an inverter. The SCRs in a hybrid bridge actually function like inverters at very low output voltages, feeding energy from the diode portion of the bridge back into the ac line. A commutation failure in this inverter results in loss of control of output voltage from the hybrid-bridge rectifier unit.

Any rectifier diode can function as a free-wheeling diode; however, the advantages of using a type with fast-recovery characteristics include lower diode junction heating during recovery and reduced di/dt duty imposed on SCRs in the rectifier unit during diode recovery.

If a free-wheeling diode is conducting when an SCR begins to turn on, a high inrush current will flow during the recovery period of the diode; that is, during the flow of recombination current in the diode junction. If this happens, the SCR turns on into a virtual short circuit, resulting in a high di/dt in the SCR. Damage to both the SCR and the free-wheeling diode could result from this effect.

This circuit action is illustrated in Figure 10-1, where an SCR feeds half-wave power to an inductive load with a free-wheeling diode. A high spike of current is carried by the SCR when it is first triggered on, and this same current pulse passes in the reverse direction through the free-wheeling diode. To avoid overheating of the free-wheeling diode during recovery, a snubber network consisting of a resistor and capacitor in series could be placed across the free-wheeling diode. This will limit the rate-of-rise of reverse voltage across the diode while it is recovering, and reduce the heating of the junction during
the recovery period; however, this snubber network will increase the di/dt on the SCR in the rectifier circuit.

At 60 Hz , the di/dt stress level may not be inordinately high, but at higher-power frequencies, the SCR may be damaged by high localized junction temperatures during turn-on. To reduce the rate of current rise during turn-on, a limiting inductance could be placed in the circuit; however, when current ceases, this inductance induces a voltage in the circuit that could damage the free-wheeling diode or break over the SCR.

A better solution is an RC snubber network, placed across each SCR to provide a current path, and thereby reduce the voltage transients during recovery.

The large apparent stored charge of a conventional diode, which must be removed during recombination, is the basic problem in these




Figure 10-1. Free-wheeling Diode in Half-Wave PhaseControlled Rectifier Circuit
cases. By using a fast-recovery diode, and thus minimizing the stored charge, snubber networks might be eliminated altogether. Or, if they are required, snubber-network capacitance may be minimized.

## Free-Wheeling Diodes in DC Choppers

As SCR manufacturers have developed more controlled dynamic characteristics of thyristors, greater attention has been focused on inverter and de chopper applications.

Figure 10-2 illustrates a typical early chopper circuit with some pertinent waveshapes. The circuit through which current flows while $\mathrm{RD}_{1}$ is recovering, stores enough energy in lead inductances and elsewhere to cause a considerable voltage transient when $R D_{1}$ recovers. To suppress this transient, an RC


Figure 10-2. Time-Ratio Control with "Hard" Commutation
network could be inserted across both $\mathrm{SCR}_{1}$ and $\mathrm{RD}_{1}$; however, this causes higher circuit losses and more complexity. A far better solution is to use a fast-recovery diode for $\mathrm{RD}_{1}$.

Free-Wheeling Diodes in Inverters An inverter using free-wheeling diodes connected in anti-parallel with the SCRs is shown in Figure 10-3. With minor modifications, this type of inverter can be made to generate either a sine or square wave. Similar circuits have been operated up to 25 kHz with an output power of 400 W . The trace in Figure $10-3$ is the voltage across one SCR.

Examining Figure 10-4, which shows a circuit equivalent to part of the circuit shown in Figure 10-3, it can be seen that fast-recovery devices are required for $\mathrm{RD}_{1}$ and $\mathrm{RD}_{2}$. While the sweepout current of $\mathrm{RD}_{1}$ flows, the distributed wire inductances ( $\mathrm{L}_{3}$ and $\mathrm{L}_{4}$ ) of the circuit assume the polarity shown. After recombination is completed, the current ceases in $\mathrm{RD}_{1}$ and in $\mathrm{L}_{3}$ and $\mathrm{L}_{4}$. Thus, both induced voltages across the leakage reactances reverse polarity and tend to generate transients.

The transients generated in $\mathrm{L}_{3}$ will be in a direction to cause high $\mathrm{dv} / \mathrm{dt}$ in $\mathrm{SCR}_{1}$, while transients generated in $\mathrm{L}_{4}$ will be in a direction to cause high-reverse voltage across $\mathrm{RD}_{1}$. The resulting transients in a 100 V system can be many hundreds of volts, rising almost instantaneously.

As illustrated in Figure 10-4, operating conditions are considerably improved with a fast-recovery rectifier. The voltage generated
across $\mathrm{SCR}_{1}$ when $\mathrm{RD}_{1}$ recovers is typically 20 V in a 125 V circuit. A fast-recovery diode is also appropriate here to minimize the energy drawn from the dc supply when the diode is recovery, and to minimize junction heating caused by the recovery action.


Figure 10-3. Inverter with Free-Wheeling Diodes


Figure 10-4. Equivalent Circuit During Rectifier Recovery

SCRs as Free-Wheeling Diodes in Inverters

The free-wheeling diodes of Figure $10-3$ have the undesirable characteristic of clamping the reverse voltage applied to the companion controlled rectifiers, causing increased turn-off time. Hence SCRs with shorter turn-off time must be used. Where it is not possible to obtain an SCR fast enough to counteract the presence of the freewheeling diode, it is possible to use an SCR in place of the diode.

The free-wheeling SCR should be triggered by connecting the gate to the anode via an appropriate resistor. When the voltage across the inverter SCR first starts to reverse, the clamping action of the free-wheeling SCR will not be felt until the free-wheeling SCR turns on. During the delay time of the free-wheeling SCR, the main SCR can be turning off with full available reverse voltage applied, thereby assuring fast turn-off action.

## Soft Commutation

High-voltage, inverter-type power thyristors (e.g., VDRM of 1200 V ) are being used in large installations, such as process control and vehicle drives. In these higher ratings, some of the early quick fixes for sweepout transients are not acceptable. Neither are the sharply rising waveshapes generated by the early types of inverters and choppers (because of the resultant low corona threshold of many components).

At operating frequencies of 5 to 10 kHz , losses in the snubber networks in these inverters, sometimes amounting to $10 \%$ of the load, became unacceptable. Therefore, as SCR applications have developed
and operating frequencies of thyristors have increased, the sharply rising waveshape circuits have become less popular, and "soft" waveshape circuits have gained favor.

Figure 10-5 illustrates a cushioned waveshape circuit that reduces the necessity for a fastrecovery rectifier for $\mathrm{RD}_{1}$. However, as the frequency of circuit operation increases, this circuit requires fast-recovery characteristics in the free-wheeling diode to hold the SCR stress to a minimum.


Figure 10-5. Time-Ratio Control with "Soft" Commutation

## Recovery Characteristics

Figure 10-6 characterizes the four types of recovery characteristics of a rectifier. Figure 10-6(a) depicts a "normal" recovery for a diffused power rectifier. Figures $10-6$ (b) and 10-6(c) show recovery current of a snap-off rectifier. Figure $10-6(\mathrm{~d})$ shows recovery current of a "soft" recovery rectifier. The snap-off diode characteristic has been found to be so rapid that some rather unique pulse-forming networks have been designed using the snap characteristics of certain rectifier diodes. It is generally found less than desirable to generate such pulses in a circuit that contains components which can be punched through by these transients.


Figure 10-6. Rectifier Recovery Characteristics

With soft recovery, the reverse current trace gradually approaches normal leakage current. With abrupt recovery, the reverse current suddenly drops to zero, and inductance/capacitance current oscillates violently. More rapid minority carrier recombination in the silicon crystal can reduce recovery time (often accomplished by doping the crystal, creating dislocation centers in the lattice structure).

## Measurement of Reverse Recovery Time

Several years ago, a circuit was devised for measuring reverse recovery time of a small rectifier diode rated about 5 amperes. It consists of a forward current supply which delivers one ampere, and a transistor to abruptly switch on a reverse voltage of 30 volts. This voltage causes the device under test to block the one ampere of forward
current. Later, the transistor was replaced by a mercury-wetted contact relay. These same circuit conditions were subsequently used when measuring the reverse recovery time of rectifier diodes rated as much as 35 amperes average.

Reverse recovery time is a strong function of the forward current, prior to the application of reverse voltage. A forward current of one ampere in a rectifier diode rated tens or hundreds of amperes is not a representative operating condition. Recovery times of the order of 200 nanoseconds, measured under this condition, are gratifyingly low, and perhaps can form a basis of comparison of one diode with another. However, these ratings are not indicative of the recovery time that will be observed when the diode is operated at its normal current level.

Recognizing the shortcomings of this early test method, JEDEC Committee JC-22 on Power Rectifiers, diodes, and thyristors has adopted a different circuit for recovery time measurements on power rectifier diodes. This circuit is shown in Figure 10-7.

The two most important test conditions are the rate of forward current reversal, di/dt, and the magnitude of the forward current. If the resistance of the power loop is kept very small; e.g., $2 \sqrt{\mathrm{~L} 1 / \mathrm{C} 1} \geqslant \mathrm{R}$, then the forward current trace is essentially sinusoidal. Typical waveforms are shown in Figures 10-6(b) and 10-6(d). Called IFM, the peak forward test current is specified as $\pi$ times the full cycle average (half sine wave) rated current of the device under test. The di/dt of this current should be linear as it crosses the zero axis. The slope of the current trace is to be measured
from $1 / 2 I_{F M}$ to $I_{F M}=0$ and the JEDEC registration procedure states that this di/dt be 25 amp eres/microseconds. Since the time for this measurement is 30 electrical degrees or $1 / 6$ of the pulse width ( $\mathrm{t}_{\mathrm{p}}$ ) (assuming a true half sine wave), we can express pulse width in microseconds as $\mathrm{t}_{\mathrm{p}}=0.12$ $I_{F M}$ when $\mathrm{di} / \mathrm{dt}=25$. If high voltage oscillations above the peak reverse voltage rating of the diode under test (DUT) occur, adjust the value of $\mathrm{C}_{1}$, $\mathrm{L}_{1}$, or V (increase the value of $\mathrm{C}_{1}$ for instance).

If this is not effective, apply the clamping circuit, shown in Figure 10-7, by closing $\mathrm{SW}_{1}$. Typical values for this circuit are $\mathrm{R} 2 \approx 250 \Omega$, $\mathrm{C}_{2} \approx 4 \mathrm{mf}$.

Rectifier diode $\mathrm{RD}_{2}$ and its circuit branch, should provide a very low inductance path around $\mathrm{SCR}_{1}$. If the reverse recovery time of $\mathrm{SCR}_{1}$ is shorter than that of the


Figure 10-7. JEDEC Reverse Recovery Test Circuit

DUT, $\mathrm{RD}_{2}$ will provide an alternate path for the reverse recovery current of the DUT. An external triggering source is to be connected to the primary of $\mathrm{T}_{3}$.

It is believed these test parameters represent typical operation of power rectifier diodes under commutating conditions. The earlier test method paid little heed to the commutating rate (-di/dt) and the measurements were considerably influenced by stray circuit inductance.

From the typical waveforms shown, it can be seen that two types of recovery action can occur: Figure 10-6(b) is abrupt recovery, and Figure $10-6(\mathrm{~d})$ is soft recovery. Reverse recovery time, $\mathrm{t}_{\mathrm{rr}}$, is divided into two parts, $\mathrm{t}_{\mathrm{a}}$ and $\mathrm{t}_{\mathrm{b}}$, the sum of these equals $\mathrm{t}_{\mathrm{rr}}$. The JEDEC committee did not name these parts, but it is suggested that $t_{a}$ may aptly be named Junction Recovery Time and $t_{b}$ named Bulk Recovery Time.

The "abrupt recovery" reverse current trace swiftly returns to zero, and the circuit inductance sets up a ringing which causes the reverse current to cross the zero axis, establishing the end of the period $\mathrm{t}_{\mathrm{b}}$. On the other hand, the "soft recovery" reverse current trace gradually approaches steady-state leakage current without crossing the axis. Figure 10-6(d) shows the geometric construction used to determine the end of the recovery period. The oscillogram in Figure 10-8 also shows soft recovery, which is characteristic of most alloy rectifier diodes.

Tests performed per JEDEC recommendations are described in terms of reverse recovery time in microseconds. However, some en-
gineers prefer to think of the recovery phenomenon in terms of recovered charge, called $\mathrm{QR}_{\mathrm{R}}$, and measured in microcoulombs. This recovered charge is proportional to the area of the approximate triangle formed as the reverse recovery current, IRM(REC), increases from zero to its maximum, then recedes to steady-state leakage.


Figure 10-8. Recovery Current Trace-Enlarged

The oscilloscope trace in Figure $10-8$ shows that $I_{\text {RM }}($ REC $)=29$ amperes and $\mathrm{t}_{\mathrm{rr}}=1.75$ microseconds, the total time required for recovery to steady-state leakage. The area enclosed by the trace may be considered a triangle with altitude $=\mathrm{IRM}($ REC $)$ and base, formed by the zero axis line, equal to $\mathrm{t}_{\mathrm{rr}}$. The area of this triangle can be expressed as in Formula 10-A.

$$
\begin{equation*}
\left(\frac{\mathrm{I}_{\mathrm{RM}(\mathrm{REC})}}{2}\right)\left(\mathrm{t}_{\mathrm{rr}}\right)=\mathrm{Q}_{\mathrm{R}} \tag{10-A}
\end{equation*}
$$

Since the units used are amperes and microseconds, the result is in microcoulombs. This example has a recovered charge of $29 \times 1.75 / 2=$ 25.4 microcoulombs.

The slope of the current trace remains approximately constant as the current goes through zero and reverses, until the current nearly reaches IRM(REC). It is possible to write equations which approximately describe the relationship of reverse recovery time, recovered charge, and peak reverse recovery current to each other.

For IR's fast recovery rectifiers, the ratio of the recovery time periods $\mathrm{t}_{\mathrm{a}}$ and $\mathrm{t}_{\mathrm{b}}$ is approximately $3: 1$. Making this assumption, Formulas $10-\mathrm{B}, 10-\mathrm{C}$ and $10-\mathrm{D}$ approximate these relationships:
$\mathrm{Q}_{\mathrm{R}} \approx \frac{\left[\mathrm{I}_{\mathrm{RM}}(\mathrm{REC})\right]\left[\mathrm{t}_{\mathrm{rr}}\right]}{2}$
$\mathrm{t}_{\mathrm{rr}} \approx \sqrt{\frac{2.67 \mathrm{QR}_{\mathrm{R}}}{\mathrm{di} / \mathrm{dt}}}$
$I_{R M}(R E C) \approx \sqrt{1.5 Q_{R}(\mathrm{di} / \mathrm{dt})}(10-\mathrm{D})$

The JEDEC registration procedure includes specifying maximum IRM(REC), as well as IFM, $\mathrm{di} / \mathrm{dt}$, and maximum $\mathrm{t}_{\mathrm{rr}}$, so a comparison may be made between recovered charge and recovery time.

Most tests have been made at a specified slope of 25 amperes/microseconds as the test current reverses from the conducting to blocking mode. However, there is value in observing the relationship of the other variables when the test current slope is changed, but the peak forward current, IFM, is maintained constant at the device rating. Figure $10-9$ shows how the slope of the test current affects IRM(REC), $\mathrm{t}_{\mathrm{rr}}$ and $\mathrm{QR}_{\mathrm{R}}$. This stresses the importance of defining test parameters when assigning a recovery time rating to any rectifier diode with
the fast recovery feature. These relationships are also of value when it is desired to estimate device performance under conditions which are not the same as the standard test conditions.


Figure 10-9. Effects of Slope of Test Current

## A 250 ampere, Fast Recovery Rec-

 tifier DiodeReverse recovery time can be reduced by speeding up the recombination of minority carriers in the silicon crystal; in other words, by reducing the minority carrier lifetime. This can be done by creating dislocation centers in the crystal lattice structure.

Diffused junctions respond to physical changes used to speed up the recombination of minority carriers, which results in a decrease of recovery time. Several oscillograms
display the waveforms of a 250 ampere diode with various types of junction structure to produce changes in recovery type.

Figure $10-10$ shows the forward and reverse current waveforms observed during recovery time tests on a normal diffused rectifier diode. Forward current is essentially a half


REVERSE RECOVERY TIME TEST CURRENT PULSE

Forward Current: 785 A Peak
Pulse Width: $\quad 94 \mu \mathrm{sec}$
$V=200 \mathrm{~A} / \mathrm{div} \quad \mathrm{H}=10 \mu \mathrm{sec} / \mathrm{div}$

Figure 10-10. Normal Diffused Rectifier Current Waveform


REVERSE RECOVERY TIME TEST CURRENT PULSE

| Forward Current: | 785 A Peak |
| :--- | :--- |
| Pulse Width: | $94 \mu \mathrm{sec}$ |
| $\mathrm{V}=200 \mathrm{~A} / \mathrm{div}$ | $\mathrm{H}=10 \mu \mathrm{sec} / \mathrm{div}$ |

Figure 10-11. Fast-Recovery Diffused Rectifier Current Waveform
sine wave with a peak value of $\pi$ times 250 amperes (785A). The reverse recovery current trace is quite evident in the lower right-hand corner. Figure 10-11 shows the waveform when the same test conditions are applied to a similar diode which has been treated to provide fast recovery. The reverse recovery current trace is noticeably smaller.

The next four figures show only the reverse recovery traces, but with scales enlarged. All have identical oscilloscope sensitivity. Figure 10-12 shows the normal diffused rectifier. It is interesting to compare this with Figure $10-13$, the characteristics of an alloy rectifier of similar current rating. The recovery time and charge of the alloy rectifier are seen to be less than that of the diffused, also the recovery action is more gradual. Figures $10-14$ and $10-15$ are for diffused rectifiers of the same size


REVERSE RECOVERY CHARACTERISTICS

| Forward Current: | 785 A Peak |
| :--- | :--- |
| $\mathrm{di} / \mathrm{dt}:$ | $-25 \mathrm{~A} / \mu \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{rr}}=5.8 \mu \mathrm{sec}$ | $\mathrm{I}_{\mathrm{RM}(\mathrm{REC})}=95 \mathrm{~A}$ |
| $\mathrm{t}_{\mathrm{a}}=4.1 \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{b}}=1.7 \mu \mathrm{sec}$ |
| $\mathrm{V}=20 \mathrm{~A} /$ div | $\mathrm{H}=1 \mu \mathrm{sec} /$ div |

Figure 10-12. Normal Diffused Rectifier Reverse Recovery Detail


REVERSE RECOVERY CHARACTERISTICS

| Forward Current: | 785 A Peak |
| :--- | :--- |
| $\mathrm{di} / \mathrm{dt}:$ | $-25 \mathrm{~A} / \mu \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{rr}}=5.5 \mu \mathrm{sec}$ | ${ }^{\mathrm{L}} \mathrm{RM}(\mathrm{REC})=74 \mathrm{~A}$ |
| $\mathrm{t}_{\mathrm{a}}=3.5 \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{b}}=2.0 \mu \mathrm{sec}$ |
| $\mathrm{V}=20 \mathrm{~A} /$ div | $\mathrm{H}=1 \mu \mathrm{sec} / \mathrm{div}$ |

Figure 10-13. Alloy Rectifier
Reverse Recovery
Detail


REVERSE RECOVERY CHARACTERISTICS

| Forward Current: | 785 A Peak |
| :--- | :--- |
| di/dt: | $25 \mathrm{~A} / \mu \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{rr}}=1.75 \mu \mathrm{sec}$ | I $_{\mathrm{RM}}(\mathrm{REC})=29 \mathrm{~A}$ |
| $\mathrm{t}_{\mathrm{a}}=1.3 \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{b}}=.45 \mu \mathrm{sec}$ |

$V=20 \mathrm{~A} / \mathrm{div} \quad \mathrm{H}=1 \mu \mathrm{sec} / \mathrm{div}$

## Figure 10-14. Moderate Recovery Rectifier Reverse Recovery Detail

which have been modified to give different values of recovery time.

The reductions in recovery time and charge are seen to be considerable. Table X-I summarizes the range of reverse recovery times observed in these four types of 250 ampere rectifier diodes. Similar
data is available for IR's other fast recovery diodes.


REVERSE RECOVERY CHARACTERISTICS

| Forward Current: | 785 A Peak |
| :--- | :--- |
| di/dt: | $-25 \mathrm{~A} / \mu \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{rr}}=1.1 \mu \mathrm{sec}$ | $\mathrm{I}_{\mathrm{RM}} \mathrm{I}_{\mathrm{R}(\mathrm{REC})}=18 \mathrm{~A}$ |
| $\mathrm{t}_{\mathrm{a}}=0.8 \mu \mathrm{sec}$ | $\mathrm{t}_{\mathrm{b}}=0.3 \mu \mathrm{sec}$ |
| $\mathrm{V}=20 \mathrm{~A} /$ div | $\mathrm{H}=1 \mu \mathrm{sec} /$ div |

Figure 10-15. Very Fast Recovery Diffused Rectifier Reverse Recovery Detail

Table X-I. Rectifier Diode Recovery
Times

|  | $\mu \mathrm{sec}$ |
| :--- | :---: |
| Alloy | $4.3-5.0$ |
| Normal Diffused | $4.8-6.5$ |
| Moderate Recovery Diffused | $1.5-2.2$ |
| Very Fast Recovery Diffused | $1.1-1.9$ |
| Test Conditions: |  |
| IFM $=785 \mathrm{~A}, \mathrm{di} / \mathrm{dt}=-25 \mathrm{~A} /$ |  |
| $\mu \mathrm{sec}, \mathrm{tp}=94 \mu \mathrm{sec}$ |  |

Relationships as Recovery Time Change

Peak reverse voltage and avalanche voltage are closely related. Both vary directly with silicon resistivity. Forward voltage varies directly with silicon thickness and inversely with carrier lifetime, but is not appreciably affected by resistivity. Recovery time varies directly
with silicon thickness and directly with carrier lifetime. Usually reducing the recovery time results in an increase of forward voltage. The junction modification to obtain shorter carrier lifetime must be properly balanced with junction resistivity and thickness to achieve an optimum relationship between recovery time, forward voltage, and peak reverse voltage. Reducing recovery time by changing carrier lifetime results in increasing the diode's reverse leakage current, which becomes especially significant at elevated temperatures as shown in Figure 10-16.

The initial, or saturation leakage current at $150^{\circ} \mathrm{C}$ for the 900 volt avalanche normal diffused diode shown in Figure $10-16$ is 0.6 mA . For the fast recovery diode, the saturation leakage current is 6 mA , and it is 9 mA for the very fast recovery diode. Normal diodes,
made from high resistivity silicon and which avalanche above 2,000 volts, show a saturation leakage current at $150^{\circ} \mathrm{C}$ of only about 2 mA . The greater leakage current and the higher forward voltage observed in the fast recovery diode make it necessary to limit the maximum operating junction temperature to $175^{\circ} \mathrm{C}$ in order to avoid excessive reverse power dissipation and resulting thermal run-away.

## Calculation of Recovery Losses in Power Rectification

Converting high frequency ac power to de is the most obvious application for a fast recovery diode in power circuitry. By using recovery waveshapes, shown in Figures $10-11$ through $10-15$, one can calculate the upper frequency for efficient rectification for a conventional alloy or conventional diffused diode.


Figure 10-16. Reverse Leakage Current

Consider, for instance, the waveshape for the diode shown as a normal diffused rectifier in Figure $10-12$. Let us assume we wish to apply the diode in a typical inverter power supply (Figure 10-17(a)). Triggering $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{4}$ simultaneously, applies the input voltage $\mathrm{E}_{\mathrm{DC}}$ to the load transformer $\mathrm{T}_{1}$ and the commutating capacitor $\mathrm{C}_{5}$. Turning on $\mathrm{SCR}_{2}$ and $\mathrm{SCR}_{3}$ on the opposite sides of the inverter causes the charge on $\mathrm{C}_{5}$ to reverse bias $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{4}$, turning them off. Figure $10-17$ (b) shows the resulting trapezoidal voltage waveshape applied to the diode bridge $\mathrm{RD}_{5}$, $\mathrm{RD}_{6}, \mathrm{RD}_{7}$, and $\mathrm{RD}_{8}$. The current and voltage waveforms pertaining to one of the diodes in this bridge during reverse recovery are shown in Figure 10-17(c). From these figures it can be shown that the average losses during recovery can be calculated using Formula 10-E.

Averaging this dissipation over the full cycle period for the inverter determines the contribution of the recovery losses to the total diode dissipation. This contribution is shown in Formula 10-F.
$\mathrm{P}_{\mathrm{R}(\mathrm{AV})(\mathrm{REC})}=\mathrm{f} \mathrm{P}_{\mathrm{R}} \mathrm{t}_{\mathrm{rr}}$

Where:

| $\mathrm{P}_{\mathrm{R}(\mathrm{AV})(\mathrm{REC})}=$ | Average Recovery <br> Power |
| ---: | :--- |
|  | $=$Inverter operating |
| f | frequency |
|  | $=4.1 \times 10^{-6} \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{a}}$ | $=1.7 \times 10^{-6} \mathrm{sec}$ |
| $\mathrm{t}_{\mathrm{b}}$ | $=t_{\mathrm{a}}+\mathrm{t}_{\mathrm{b}}$ |
| $\mathrm{t}_{\mathrm{rr}}=\mathrm{t}_{\mathrm{a}}$ | $=5.8 \times 10^{-6} \mathrm{sec}$ |

Assume: $\mathrm{f}=1 \mathrm{kHz}$
Therefore: the average recovery losses,

$$
\begin{aligned}
\mathrm{P}_{\mathrm{R}(\mathrm{AV})(\mathrm{REC})=}= & 1 \mathrm{kHz} \cdot 28,500 \mathrm{~W} \\
& \left(4.1 \times 10^{-6} \mathrm{sec}+\right. \\
& \left.1.7 \times 10^{-6} \mathrm{sec}\right) \\
= & 165.3 \mathrm{~W}
\end{aligned}
$$

At 3 kHz , this dissipation would be 495.9 watts. Therefore, high operating frequencies limit the application of normal recovery diodes.

Consider now the performance of a fast recovery diode, the waveform for which is shown in Figure 10-14. Since $\operatorname{IRM}($ REC ) for this diode is only 29 A , the losses, $\mathrm{P}_{\mathrm{R}}$, are only 8700 W . At 1 kHz , since $\mathrm{t}_{\mathrm{a}}$ is only $1.3 \times 10^{-6} \mathrm{sec}$ and $\mathrm{t}_{\mathrm{b}}$ is only $0.45 \times 10^{-6} \mathrm{sec}$, this becomes an average dissipation of 15.23 watts.

Before the dissipation during recovery becomes as much as that, at 1 kHz , of the previously discussed
$P_{R(R E C)}=\frac{\mathrm{V}_{\mathrm{RWM}} \cdot \mathrm{QR}_{\mathrm{R}}(\mathrm{REC})}{\mathrm{t}_{\mathrm{rr}}}=\frac{\mathrm{V}_{\mathrm{RWM}} \cdot \mathrm{I}_{R M}(\mathrm{REC})}{2}$
Where:
$\mathrm{P}_{\mathrm{R}(\text { REC })}=$ Recovery power
$\operatorname{IRM}($ REC $)=95 \mathrm{~A}$
VRWM $=$ Peak reverse voltage applied to rectifier during operation
therefore, the losses, $\mathrm{P}_{\mathrm{R}(\mathrm{REC})}=\frac{600 \cdot 95}{2}=28,500 \mathrm{~W}$

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Figure 10-17. High Frequency Inverter with Fast Recovery Rectifiers
diode, the operating frequency would have to be increased to 10.85 kHz .

Thus, by using a fast recovery diode at these higher operating frequencies, average power dissipation during recovery is reduced and rectification efficiency is improved. Furthermore, the diode can handle a larger forward current without overheating.

## Schottky Barrier Diodes

The crystal rectifier or Schottky diode was used for many years as a laboratory detector for high frequencies, and as detector for radio broadcasts in the early days of radio.

Today, many uses have been found for Schottky diodes. One, in particular, is for power rectification using large area metal contacts.

In Figure 10-18, a large barrier exists for electron flow from the metal into the semiconductor; however, when the device is forwardbiased, the energy level of the conduction band in the semiconductor is raised so that electrons can flow into the metal.

Since no holes (mobile positive charges) are present in the metal, none can be injected into the semiconductor. Thus, we have the concept of a "majority carrier device." That is, only electrons participate in the conduction mechanism which eliminates the minority carrier storage which slows down the recovery action of P-N junction devices.

The reverse voltage of the Schottky is limited by its structure, which is designed to minimize forward voltage drops. Figure 10-19 illustrates the Schottky diode structure. Extremely low contact resistance is required, and since the Schottky is a majority carrier device, the higher resistivity epitaxial layer must be very thin in order to reduce series resistance. The metal overlapping the insulator at the edge of the barrier region acts as a "guard-ring" and helps reduce the surface electric field and improves the reverse characteristics of the device.

## Applications of Schottky Diodes

The diodes discussed in this sec-


Figure 10-18. Schottky Barrier Band Diagram


Figure 10-19. Schottky Barrier Structure
tion are classed as power Schottkys with a 50 ampere average rating and a repetitive peak reverse voltage rating of 20 volts. Devices rated up to 40 V are available, also 25 A devices over the same voltage range.

When the reverse voltage rating of 20 volts is first considered, it may seem to be too low to be practical; however, when this is considered in conjunction with the very low forward voltage ( 0.65 volts at 100 amps , it becomes obvious that this type of device will have very wide application in low voltage rectifier circuits. Furthermore, as has been mentioned previously, this type of diode is a majority carrier device and does not have the relative slow reverse recovery characteristic associated with $\mathrm{P}-\mathrm{N}$ junction diodes. This feature is extremely important in high frequency systems. Whereas the switching losses even in specially processed high current P-N junctions become significant at frequencies above 10 kHz , a Schottky diode can be used at frequencies in excess of 100 kHz .

Figure $10-20$ shows the basic electrical characteristics of a typical
power Schottky. This figure shows that the reverse characteristic is noticeably different from the standard P-N junction diode reverse characteristic. The Schottky diode has a flat reverse characteristic until the reverse voltage reaches 8 to 10 volts and then it takes a more resistive form.

The significance of the reverse recovery characteristic has been mentioned and oscillographs of this characteristic are shown in Figure 10-21. When these are compared with similar characteristics of fast recovery P-N junction diodes, as tabulated in Table X-II, the advantage of Schottky barrier diodes for high frequency applications can be recognized. A comparison of the Schottky and a fast recovery diode shows that the recovered charge of the Schottky is 75 nanocoulombs as against 12.6 microcoulombs for the fast recovery diode.

Reverse recovery current flows while the load current is transferred from one diode to another, and effectively short circuits the source until the diode recovers. If it is assumed that the source voltage is fixed at some voltage, V , then every


Figure 10-20. Schottky Diode Characteristics

Table X-II. Recovery Characteristics for Different Types of Diodes
Rated Approximately 50 Amperes

|  | RECOVERY TIME | PEAK REVERSE RECOVERY CURRENT | RECOVERED CHANGE |
| :---: | :---: | :---: | :---: |
| Schottky Diode Alloyed PN Junction Diffused PN Junction Fast Recovery PN Junction | 150 nsec | 1A | 75 nCoulombs |
|  | $5 \mu \mathrm{sec}$ | 50A | $125 \mu$ Coulombs |
|  | $3 \mu \mathrm{sec}$ | 40A | $60 \mu$ Coulombs |
|  | $1 \mu \mathrm{sec}$ | 25A | $12.5 \mu$ Coulombs |
| Test conditions, forw | d current = 1 | A peak, half sine | wave |



APPLIED CURRENT PULSE
VERTICAL SCALE

- $50 \mathrm{~A} / \mathrm{div}$

HORIZ. SCALE
$-10 \mu \mathrm{sec} / \mathrm{div}$


APPLIED CURRENT PULSE
VERTICAL SCALE

- 0.5 A/div

HORIZ. SCALE

- 100 nsec/div


APPLIED CURRENT PULSE
VERTICAL SCALE
$-20 \mathrm{~A} / \mathrm{div}$
HORIZ. SCALE
$-0.5 \mu \mathrm{sec} / \mathrm{div}$


RECOVERY CHARACTERISTIC VERTICAL SCALE - 20 A/div

HORIZ. SCALE
$-2 \mu \mathrm{sec} / \mathrm{div}$


RECOVERY CHARACTERISTIC
VERTICAL SCALE - 0.5 A/div

HORIZ. SCALE

- $100 \mathrm{nsec} / \mathrm{div}$


RECOVERY CHARACTERISTIC VERTICAL SCALE -0.5 A/div
HORIZ. SCALE

- $100 \mathrm{nsec} / \mathrm{div}$

Figure 10-21. Recovery Characteristics
time the supply reverses a certain amount of energy is lost, partly in the diode, and also in the wiring, the transformer, and the switching elements. The amount of energy lost is given by Formula 10-G.
Energy $=\int V$ idt

$$
\begin{equation*}
=\frac{\mathrm{V} \cdot \mathrm{i}_{\mathrm{rr}} \cdot \mathrm{t}_{\mathrm{rr}}}{2} \tag{10-G}
\end{equation*}
$$

(Assuming the waveshape of the reverse recovery current is triangular),

## but

$\underline{\mathrm{i}_{\mathrm{rr}} \cdot \mathrm{t}_{\mathrm{rr}}}$ Is equal to the recovered charge

Power lost = Energy x Frequency
As an example of the power savings which can be obtained using a Schottky diode, compared with a fast recovery diode, consider a system with a 20 volt source, an average output voltage of 5 volts (obtained by pulse width modulation) and an output current of 100 amps.

The energy dissipated in a fast recovery diode is, from Equation $10-\mathrm{G}, 20 \times 12.5 \times 10^{-6}$ watt seconds/pulse for each diode; for the Schottky diode, the energy lost is $20 \times 75 \times 10^{-9}$ watt seconds/pulse for each diode. The fast recovery diode will exhibit a forward voltage of approximately 1.15 volts at 100 amps whereas the Schottky diode will have a forward voltage of approximately 0.65 volts resulting in less power being lost in the Schottky during forward conduction also.

This comparison is shown in tabular form in Table X-III. Table X-

III(a) shows how the losses associated with the two types of diodes vary with frequency when operated under the circuit conditions shown. The static losses are simply the diode current multiplied by the diode voltage, assuming a square wave of current through each diode; one or the other diode is conducting at all times.

The switching losses per cycle are twice the losses per pulse derived from Formula 10-G, because one or the other diode conducts (and therefore recovers) once each half cycle.

Table X-III(b) shows how the efficiency of a system can be improved, even at low frequencies, by the use of a Schottky diode. At 1 kHz , the Schottky diode saves 50 watts, and at 100 kHz , the efficiency of the system, using Schottky diodes, changes by only 0.1 percent, whereas using fast recovery diodes, this change in system efficiency is 6 percent ( 49.7 watts more power required).

These data are shown in graphical form in Figure 10-22; here the Schottky diode losses below 1 kHz have been taken as a per unit base to compare the efficiency of Schottky diodes with fast recovery P-N junction diodes over a wide frequency range.
Circuit current $=100 \mathrm{amps}$

Base Losses $=$| 65 watts (dc |
| :--- |
| losses of the |
| Schottky diode) |

| Per Unit |
| :--- |
| Efficiency |$=$| Losses at specified |
| :--- |
| conditions |

The high frequency efficiency of Schottky diodes has been verified by the operation of an experimental inverter at International Recti-

Table X-III. Schottky Diode and Fast Recovery Diode Rectification Losses

| FREQUENCY OF OPERATION | FAST RECOVERY DIODE LOSSES (FOR 2 DIODES IN CENTER TAP CIRCUIT) |  |  |  | SCHOTTKY DIODE LOSSES (FOR 2 DIODES IN CENTER TAP CIRCUIT) |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | STATIC <br> (W) | SWITCHING LOSSES |  | TOTAL LOSSES <br> (W) | STATIC <br> (W) | SWITCHING LOSSES |  | TOTAL LOSSES (W) |
|  |  | PER CYCLE <br> (W-SEC) | TOTAL (W) |  |  | PER CYCLE (W-SEC) | TOTAL <br> (W) |  |
| 1 kHz | 115 | $0.5 \times 10^{-3}$ | 0.5 | 115.5 | 65 | $3 \times 10^{-6}$ | 0.003 | 65.003 |
| 5 kHz | 115 | $0.5 \times 10^{-3}$ | 2.5 | 117.5 | 65 | $3 \times 10^{-6}$ | 0.015 | 65.015 |
| 10 kHz | 115 | $0.5 \times 10^{-3}$ | 5 | 120 | 65 | $3 \times 10^{-6}$ | 0.03 | 65.03 |
| 20 kHz | 115 | $0.5 \times 10^{-3}$ | 10 | 125 | 65 | $3 \times 10^{-6}$ | 0.06 | 65.06 |
| 40 kHz | 115 | $0.5 \times 10^{-3}$ | 20 | 135 | 65 | $3 \times 10^{-6}$ | 0.12 | 65.12 |
| 100 kHz | 115 | $0.5 \times 10^{-3}$ | 50 | 165 | 65 | $3 \times 10^{-6}$ | 0.3 | 65.3 |

Circuit conditions - source voltage 20 volts, output voltage 5 volts, output current 100 amps .
(b)

| FREQUENCY | OUTPUT POWER (WATTS) | RECTIFIER ASSOCIATED <br> LOSSES (WATTS) |  | RECTIFICATION EFFICIENCY (\%) |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} \text { FAST } \\ \text { RECOVERY } \end{gathered}$ | SCHOTTKY | $\begin{gathered} \text { FAST } \\ \text { RECOVERY } \end{gathered}$ | SCHOTTKY |
| 1 kHz | 500 | 115.5 | 65.003 | 81.2 | 88.5 |
| 5 kHz | 500 | 117.5 | 65.015 | 81.0 | 88.5 |
| 10 kHz | 500 | 120 | 65.03 | 80.6 | 88.5 |
| 20 kHz | 500 | 125 | 65.06 | 80.0 | 88.5 |
| 40 kHz | 500 | 135 | 65.12 | 78.4 | 88.5 |
| 100 kHz | 500 | 165 | 65.3 | 75.2 | 88.4 |



Figure 10-22. Diode Rectification Efficiency
fier. This inverter has been operated over a frequency range of 1.5 kHz to 20 kHz . When using Schottky diodes, no change in efficiency could be measured over the entire frequency range, whereas with standard and fast recovery diodes, a noticeable increase in the diode losses was measured.

The power loss measurements were made by carefully calibrating a particular heat dissipator in terms of temperature rise vs. power loss. The diode under test was then installed in this dissipator and the temperature rise of the dissipator was measured while maintaining a constant output (load) power at
several discrete switching frequencies. From the dissipator calibration curve, the actual power dissipated in the diode could be determined.

The advantages of power Schottky diodes over conventional P-N junction diodes can be summarized as being (1) lower forward voltage and (2) greatly reduced switching losses. Although the Schottky diode is only applicable in low voltage circuits, this is the area where the low forward voltage is most significant. In fact, the lower the circuit voltage, the more important becomes the rectifying element forward voltage characteristic.

## References

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## Protection

## PROTECTING WITH FUSES

Fault currents in controlled rectifier applications may result from short circuits, either in the rectifier devices or in the external connections.

Silicon diodes and thyristors, due to their small mass, have a very limited overload capacity as compared to motors and transformers. This can be represented by an overload curve similar to the operating time/current characteristic curve of a fuse. Figures 11-1 and 11-2 indicate diagrammatically two alternative methods of using fuses alone or in combination with other protective devices to protect diodes or thyristors over the full range of
overloads. Figure $11-1$ indicates how a fuse alone could be used to provide complete protection, but such applications are usually limited to low power installations, or installations where an excess of rectifying capacity is available. Figure 11-2 indicates the more commonly used system in which the fuse is used for short circuit protection only; normal overload protection is provided by a circuit breaker or other means, depending on the application.

In general, the elements employed in protective systems can be split into two groups:

1. Means to interrupt short circuits, such as:


Figure 11-1. Complete Overload Protection by Fuse


Figure 11-2. Fuse Used for Short Circuit Protection Only
A. fuses and/or circuit breaker on the ac side
B. fuses and/or circuit breaker on the dc side
C. fuses in series with the semiconductors
2. Means to limit the amplitude and/or the rate of the rise of the short circuit currents by:
A. adding line reactances
B. increasing transformer impedances
C. adding inductance and resistance in the de circuit.
D. providing a current-limiting by-pass switch (crowbar)
In practice, it is common to use one or more of the above methods. Consequently, many aspects of the fuse, semiconductor devices and other associated protective equipment have to be coordinated or matched to give reliable and economic protection for any scheme.

The various factors to be considered are listed in Table XI-I. Since there are, as yet, no national or international specifications dealing with fuses for the protection of semiconductor devices, fuse manufacturers have used their own methods for assigning ratings and obtaining performance data. This sometimes makes it difficult to carry out direct comparisons. In view of this, we have stated clearly how the ratings are devised for the International Rectifier Semiconductor Fuses. The problems of protection are outlined further with typical applications and clarified by practical examples.

## I ${ }^{2}$ t Ratings

During the clearing time of a fuse (melting time plus arcing time), the energy produced by the power source and the energy stored in the inductive portion of the cir-

Table XI-I. Factors to Consider During Fuse Selection

| PARAMETER | FACTORS AFFECTING PARAMETER |  | DATA PROVIDED |  |
| :---: | :---: | :---: | :---: | :---: |
|  | FUSE | DIODE OR THYRISTOR | FUSE | DIODE OR THYRISTOR |
| Steady State RMS Current | Ambient, attachment, proximity of other apparatus and other fuses, cooling employed | Ambient, type of circuit, parallel operation, cooling employed, heat sink | Maximum rated current under specified conditions, factors for ambient uprating for forced cooling attachments | Comprehensive curves (average currents generally quoted) |
| Watts Dissipated for Steady State | As for current | As for current | Maximum quoted for specified conditions | Comprehensive data |
| Overload Curves | Pre-loading cyclic loading surges, manufacturing tolerances | Preloading, cyclic loading surges | Nominal time/current curves for initially cold fuse, preloaded fuse | Overload curves, also transient thermal impedances |
| Interrupting Voltages | ac or dc | Voltage rating | Maximum voltage specified | Voltage rating quoted |
| 12 t Ratings | Pre-loading; total 12 t dependent on: circuit impedance ( $\mathrm{X} / \mathrm{R}$ ), applied voltage, point of initiation of short circuit, fault current, frequency | Pre-loading | For initially cold fuses; total $1{ }^{2}$ t curves for worst case conditions, variation with frequency, fault current, voltage, $X / R$, pre-arcing $12{ }_{\mathrm{t}}$ constant | Quoted value (minimum) |

Table XI－I．Factors to Consider During Fuse Selection（Continued）

|  | FACTORS AFFECTING PARAMETER |  | DATA PROVIDED |  |
| :---: | :---: | :---: | :---: | :---: |
| PARAMETER | FUSE | DIODE OR THYRISTOR | FUSE | DIODE OR THYRISTOR |
| Peak Current | Pre－loading；fault current（voltage second order （effect），frequency | Pre－loading | Curves for worst con－ ditions for initially cold fuses | Half cycle surge current |
| Arc Voltage | Peak value depend－ ent on：applied volt－ age，circuit imped－ ance point of initia－ tion of short circuit | PR V voltage ratings， peak non－repetitive voltage ratings | Maximum peak arc voltages plotted against reapplied voltages | PRV voltage rating and／ or peak non－repetitive voltage rating |

cuit $(1 / 2 \mathrm{Li} 2)$ are transformed into heat within the system. The total energy dissipated in the system is $\int \mathrm{i}^{2} \mathrm{Rdt}$, where R is the total circuit resistance. The $\int \mathrm{i}^{2} \mathrm{dt}$ is identical for all elements in a series system. And so the comparing of fuses to semiconductor devices is done on the basis of $\mathrm{I}^{2} \mathrm{t}$. The fuse will "letthrough" an amount of $-12 t$ based upon fuse design and circuit conditions. The semiconductor device has an ability to withstand an $\mathrm{I}^{2} \mathrm{t}$, usually stated for a specific subcycle time. To properly match a fuse with a semiconductor device requires that the let-through $I^{2}$ t of the fuse never exceeds the $I^{2} t$ capability of the semiconductor device under any set of operating circumstances.

Operation of the fuse is split into the melting (or prearcing) and arcing regions. The melting $\mathrm{I}^{2} \mathrm{t}$ is basically a function of the element dimensions. For a given melting time, the melting $\mathrm{I}^{2} \mathrm{t}$ is affected only by preloading. For subcycle operation, the fuse melting time is inversely proportional to the available symmetrical fault current.

There is considerable change in melting $\mathrm{I}^{2} \mathrm{t}$ from 1.0 to 8.3 milliseconds because the condition of no heat loss from the restricted portion, required for $\mathrm{I}^{2} \mathrm{t}$ to remain constant, is only achieved at very short melting times.

Figure 11-3 illustrates the variation in melting I 2 t vs. melting time for a typical semiconductor fuse. For pre-arcing times less than approximately 5 milliseconds, the melting I 2 t tends toward a definite minimum value. In this period there is insufficient time for the heat to be dissipated from the restricted portions of the fuse elements.


Figure 11-3. Typical Variation of Melting (Pre-Arcing) $I^{2} t$ with Melting Time

During fuse operation over a number of cycles due to a heavy overload, and where the fuse melting time/current characteristic curves are utilized, the melting $I^{2} t$ is essentially the total let-through I 2 t of the fuse. During sub-cycle operation, however, the melting $\mathrm{I}^{2} \mathrm{t}$ becomes a much smaller part of the total let-through $\mathrm{I}^{2} \mathrm{t}$. The remaining $I^{2}$ t let-through is known as the arcing $\mathrm{I}^{2} \mathrm{t}$ and this is a function of the circuit parameters, being greatly affected by the $X / R$ ratio and the applied voltage.

The arcing $\mathrm{I}^{2} \mathrm{t}$ varies with applied voltage, fault current level, power factor and the point on the voltage wave for the initiation of the short circuit. The total $\mathrm{I}^{2} \mathrm{t}$ letthrough figures quoted on fuse data sheets are for the worst of the above conditions with a given voltage and available prospective fault current. There will be a reduction in $I^{2} t$ when the fuse carries load current prior to the fault (pre-loading), but it is better to use maxi-
mum values to insure complete protection.

The majority of manufacturers give $I^{2} t$ ratings for their power diodes and thyristors which should not be exceeded during fusing for all total clearing times below 8.3 milliseconds. This maximum $I^{2} t$ rating is usually given for a device previously carrying maximum rated current at maximum junction temperature; thus an inherent safety factor is introduced into such fuse protection where the semiconductor is operated at less than maximum junction temperature.

International Rectifier data sheets on diodes and thyristors show a value of $\mathrm{I}^{2} \mathrm{t}$ for 5 milliseconds through 8.3 milliseconds and a lower value based on a derating factor of 55 to $60 \%$ for a time of 1.5 milliseconds.

The value of let-through $\mathrm{I}^{2} \mathrm{t}$ of a particular fuse is dependent on available fault current and various other circuit operating conditions, as discussed in Reference [1]. Knowing this a circuit designer can determine the let-through $\mathrm{I}^{2} \mathrm{t}$ of a particular fuse under his operating conditions.

To complete the analysis, the designer also should ascertain the clearing time of the fuse under the anticipated fault conditions. The $I^{2} \mathrm{t}$ capability of the semiconductor device being protected can then be determined for a current pulse of duration equal to the clearing time of the fuse. Interpolation between the published 5 msec and 1.5 msec $\mathrm{I}^{2} \mathrm{t}$ values is generally required to obtain this value. The designer should be sure it is greater than the $\mathrm{I}^{2}$ let-through by the fuse.

To assist the designer in ascertaining fuse clearing time, the
curves for maximum $\mathrm{I}^{2} \mathrm{t}$ let-through by International Rectifier fuses include lines which indicate total clearing times of 5,2 and 1.5 msec . In addition, the curves begin at the left-hand end at approximately 8.3 msec clearing time. By entering these curves at the magnitude of the available fault current, the designer can estimate the clearing time of the fuse he is considering, as well as determine the let-through $\mathrm{I}^{2} \mathrm{t}$ under the same conditions.

## Isolating Fuses

In large rectifier equipment, where a number of SCRs are operated in parallel in each arm of the rectifier circuit, a fuse may be connected in series with each thyristor simply to remove it from the circuit in the event it fails to properly block in the reverse direction. In this instance, the fuse characteristic is generally coordinated with other prospective devices so that the fuse only operates when there is a reverse breakdown of its associated SCR. Thus the fuse provides protection, not to its associated SCR, but to the other elements of the circuit which are subjected to the fault current caused by a reverse blocking failure of one SCR.

## Operation of Fuses on DC

Current limiting fuses intended for the protection of semiconductor rectifying devices may be used in both ac and de circuits. On the other hand, most of the published information for such fuses pertains to their performance in alternating current applications; very little published information pertains to operation on direct current. Yet, in an inverter or de chopper, each SCR is in a de circuit, and information on
fuse performance with dc applied is needed to make it possible to select a fuse which will adequately protect the semiconductor device and at the same time permit it to be operated at the highest possible current level.

DC operation of a fuse is different from ac operation because the applied voltage is at all times of one polarity. This in general makes it more difficult for the fuse to perform its intended function of current interruption following a current of sufficient magnitude to melt the fuse element because the current through the fuse is not inherently reduced to zero as it is when the applied voltage is ac. Whenever the voltage across the fuse reverses repetitively, the fuse can be considered to be operating on ac (except with very low frequency waveforms) even though the voltage waveform does not follow some regular pattern, such as a sinusoidal wave.

A special circumstance is met in the case of dc where the voltage drops to zero, or nearly to zero, in a cyclical manner. An example would be the output of a single phase, full-wave rectifier, where the load is non-inductive. In this instance, a fuse will perform as though connected to an ac source, because the current through the fuse will cease when the voltage reaches zero.

The major factor which determines how a fuse will operate in a dc circuit is the time constant $(L / R)$ of the de circuit. If the time constant is small, fault current will build up through the fuse rapidly, and this will cause a multiple arcing condition, one arc at each element restriction, giving essentially the
same type of fuse performance as occurs when the fuse clears a fault on an ac system. With a high rate-of-rise of current through the fuse, the peak current and also the energy let-through by the fuse (or $\mathrm{I}^{2} \mathrm{t}$ let-through) during the melting and clearing periods will be much the same as for the same fuse when clearing a fault on an ac circuit.

The maximum voltage that can be applied to the fuse and still enable it to clear will be less in the case of de operation; with many current limiting fuses designed for the protection of semiconductors, the dc voltage rating will be about 75 percent of the ac RMS voltage rating when the rate of rise of current through the fuse is high.

For low rates of rise of direct current ( $\mathrm{L} / \mathrm{R}$ of 20 msec or more), the maximum voltage the fuse can interrupt is less, and furthermore, the $I^{2} t$ let-through becomes greater as $L / R$ is made longer. This effect is brought about because the melting time of the fuse increases when the rate-of-rise of current through the fuse is low. If the rate-of-rise of current is low, it is possible for arcing to occur at only one point along the fuse element, thus reducing the dc voltage which the fuse can clear.

The maximum voltage rating that a given current limiting fuse can be given when operated in a dc circuit is therefore not a fixed value, but depends upon the $L / R$ characteristic of the circuit to which the fuse is connected. This relationship, for one make of fuse rated 500 volts ac, is shown in Figure 11-4. The curves pertaining to fuses of other voltage ratings are similar.

The instantaneous peak letthrough current for dc operation


Figure 11-4. DC Voltage Rating of 500V Semiconductor Fuse
can be related to the value published for ac operation in a low power factor circuit and is dependent upon the de circuit $L / R$ as shown in Figure 11-5. This curve was calculated on the basis that the direct current pulse rises in an exponential manner. The let-through $\mathrm{I}^{2} \mathrm{t}$ for dc operation can also be related to the value published for ac operation, and again shows a dependency upon the dc circuit $L / R$ as shown in Figure 11-6, which is representative of the performance of many current limiting fuses.

From Figure 11-5, it can be seen that for dc circuits with values of $\mathrm{L} / \mathrm{R}$ above 2.5 milliseconds, the peak let-through current is less than the peak current anticipated in an ac circuit. As an illustration of this, refer to Figure 11-7, where two circuits with similar voltages and currents are shown. In the case of the dc fault, the rate of current rise is much slower, and the melting time is far longer, as shown in Figure 11-8. The fuse requires a certain energy input (related to the melting $\mathrm{I}^{2} \mathrm{t}$ ) to melt the element. As the melting time is far greater on the dc fault, it follows that the


Figure 11-5. Instantaneous Peak Let-Through Current of AC Fuse in DC Circuit
current in the circuit at the time of melting will be less than the current at melting in the ac circuit. The reduction in melting current in the dc circuit is not as great as it would appear it should be, however, because during the long melting period, the element has time to lose considerable heat from the restricted portions and hence more energy is needed to melt the restrictions.

The simple case involving the interruption of a purely dc load,


Figure 11-6. Let-Through $I^{2} t$ in DC Circuit vs. AC Circuit


Figure 11-7. AC and DC Circuits under Short Circuit Conditions
such as on the output of a rectifier where the output is heavily filtered by a series inductance, generally results in a very long time constant for the short circuit current. In this case, the melting time of the fuse becomes very long, because of the very slow rate-of-rise of current.

When the fuse melts and begins arcing, the rate-of-rise of current is still very low, and hence the arc voltage produced by the fuse is low. This, in turn, makes the extinguishing of the arc very difficult. A further difficulty is the absence of any natural voltage zeros which


Figure 11-8. Waveshapes of Short Circuits in AC and DC Circuits
would make the extinguishing of the arc easier.

The maximum available fault current is not a problem for dc circuits. With an increase in available fault current, at a given value of $L / R$, the rate-of-rise of current increases and allows the fuse to clear in a more positive manner. In general, the higher the di/dt during fault conditions, the easier it is for the fuse to clear under dc operation. The interrupting capacity of a fuse when operated on dc can be exceedingly high and beyond the values likely to be encountered in normal operation.

Determination of Circuit L/R
From this discussion, it can be seen that the time constant ( $L / R$ ) of the dc circuit in which the fuse is located is of major importance when selecting the fuse. At first glance, it may seem that values of $\mathrm{L} / \mathrm{R}$ are not readily available for dc circuits, but, in fact, they can be learned from facts at the disposal of the circuit designer.

In inverter applications, the dc supply is usually obtained from one of two basic sources: from a battery, as shown in Figure 11-9; or from a rectifier, with a choke input filter to the dc output, as shown in


Figure 11-9. DC Circuit with Battery as a Source

Figure 11-10. A charger is often found connected to the battery in Figure 11-9, but current delivered by this charger will generally be limited to some relatively low level and therefore, is not a factor in fuse selection.

Referring to Figure 11-9, the battery voltage is known and the internal impedance of the battery, $R_{B}$, can be obtained either from the battery specification or by measurement. The circuit resistance, $R_{1}$ is more difficult to measure but can be calculated from the known parameters of the length and hence the resistance of the conductors in the power circuit, and also should include the effective on-state resistance of the thyristor at high current levels and the resistance of the fuse. The winding resistance of the di/dt choke, $\mathrm{R}_{2}$, should also be included. The maximum available fault current can then be calculated as shown in Formula 11-A.
$\mathrm{E}_{\mathrm{B} / \mathrm{R}}=\mathrm{E}_{\mathrm{B}} /\left(\mathrm{R}_{\mathrm{B}}+\mathrm{R}_{1}+\mathrm{R}_{2}\right)$ (11-A)
The total circuit inductance, $\mathrm{L}_{1}$ $+\mathrm{L}_{2}$, is a circuit parameter which the designer has to know for di/dt
protection of the thyristor. However, it must not be assumed that the di/dt choke inductance, $\mathrm{L}_{2}$, swamps the circuit lumped stray inductance, $\mathrm{L}_{1}$. In general, the only way to obtain an accurate indication of circuit inductance is to measure it. This measurement can be made very easily by measuring the $\mathrm{di} / \mathrm{dt}$ of the thyristor current and from this measurement, the inductance is obtained from Formula 11-B.

$$
\begin{equation*}
\mathrm{L}=\frac{\mathrm{E}_{\mathrm{B}}}{\mathrm{di} / \mathrm{dt}} \tag{11-B}
\end{equation*}
$$

Therefore, if $E_{B}=100$ volts and $\mathrm{di} / \mathrm{dt}$ is measured to be $20 \mathrm{~A} / \mu \mathrm{sec}$, then,

$$
L=\frac{100}{20}=5 \mu \mathrm{H}
$$

With these inductance and resistance values, the circuit $L / R$ can be calculated under load short circuit conditions.

We now have all the basic information necessary for proper fuse selection; $\mathrm{E}_{\mathrm{B}}$, the supply voltage, $L / R$, the circuit time constant, and $E_{B} / R$, the prospective (available) current through the fuse.


Figure 11-10. DC Circuit with Rectifier as a Source

The parameters of the circuit of Figure 11-10 are obtained in the same way; however, the source is now capacitor $\mathrm{C}_{\mathrm{F}}$, as under very short time conditions the rectifier supply is effectively decoupled from the thyristor circuit by the filter inductor LF. If the natural period of $\mathrm{C}_{\mathrm{F}}$ and $\mathrm{L}_{1}+\mathrm{L}_{2}$ is very long compared with the clearing time of the fuse, then this circuit may be treated in the same manner as the circuit of Figure 11-9. However, if the natural period of $\mathrm{C}_{\mathrm{F}}$ and $\mathrm{L}_{1}+\mathrm{L}_{2}$ is comparable to the clearing time of the fuse, it must be recognized that the prospective (available) current will be greater than $\mathrm{E}_{\mathrm{C}} / \mathrm{R}$ because of the oscillatory nature of the current. The actual amplitude of the prospective current will depend on the damping factor of the circuit. The formula for calculating the peak prospective fault current is given as:
$I_{P}=E_{o} \sqrt{ } C / L$ e $-\frac{125}{f / L R}$
Where:

| $\mathrm{L} / \mathrm{R}$ | $=$ time constant of circuit |
| ---: | :--- |
| $(\mu \mathrm{sec})$ |  |

## Location of Protective Fuses

The best position for protective fuses will depend on the actual circuit configuration being used. A general rule is that it is easier to match the fuse to the semiconductor if the fuse is directly in series with the device to be protected. On the other hand, for reasons of economy, sev-
$\mathrm{f}=\frac{1}{2 \pi} \sqrt{\frac{1}{\mathrm{LC}}=\frac{\mathrm{R}^{2}}{4 \mathrm{~L}^{2}}}$
$\mathrm{f}=\frac{1}{2 \pi} \sqrt{\frac{1}{(3 \mu \mathrm{H}+3 \mu \mathrm{H}+3 \mu \mathrm{H}) 29,000 \mu \mathrm{~F}}}$
$=\frac{\left[2\left(7 \times 10^{-4} \Omega\right)+7.8 \times 10^{-3} \Omega+8 \times 10^{-4} \Omega\right]^{2}}{4(3 \mu \mathrm{H}+3 \mu \mathrm{H}+3 \mu \mathrm{H})^{2}}=299 \mathrm{~Hz}$


Figure 11-11. Three-Phase Inverter Circuit

The circuit $L / R$ is seen from the data in Figure 11-11 to be:

$$
\frac{1}{2 \pi} \sqrt{\frac{1}{\mathrm{LC}}-\frac{\mathrm{R}^{2}}{4 \mathrm{~L}^{2}}}
$$

The peak prospective fault current is the peak of the first half cycle of oscillatory current and can be calcalculated from Formula 11-E.
$I_{P}=E_{B} \sqrt{\frac{C}{L}} e-\frac{125}{f L / R}$
Note that $L / R$ is to be given in milliseconds. Using the values from Figure 11-11, the peak current can be calculated:
$I_{P}=300 \sqrt{\frac{29,000}{9}} e-\frac{125}{299 \times 9 \times 10^{-1}}$
$=17,029 \mathrm{e}^{-0.465}=17,029 \times 0.63$
$=10,745 \mathrm{~A}$
An approximate calculation for the $\mathrm{I}^{2} \mathrm{t}$ in the first half cycle of fault current is shown in Formula 11-F.

$$
\begin{equation*}
\mathrm{I}^{2} \mathrm{t}=\frac{\mathrm{I}_{\mathrm{p}} 2}{2} \times \frac{\tau}{2} \tag{11-F}
\end{equation*}
$$

Using the parameters given in Figure $11-11$, the $I^{2} \mathrm{t}$ is found to be:

$$
\begin{aligned}
& \frac{(10,745)^{2}}{2} \times \frac{1}{299.5 \times 2} \\
& =9.65 \times 10^{4} \mathrm{~A}^{2} \mathrm{sec}
\end{aligned}
$$

This calculation is based on the assumption that the current is a half sine wave and does not take into account the effect of offset on the current waveform. The $I^{2} t$ is actually greater, and a more exact calculation shows it to be about 20 percent greater. Thus, the $I^{2} t$ of the current during the first half cycle is close to $11.6 \times 10^{4} \mathrm{~A}^{2}$ sec.

It is now possible to select a particular fuse and determine how its performance compares with the capabilities of the main thyristors. From Figure 11-4, it is seen that this particular type of 500 V fuse can be used; for a circuit $L / R$ of 0.9 , it is seen to have a dc voltage rating of nearly 500 V .

Since the main thyristors are rated 710 A RMS, it is desirable to select a fuse of nearly equal current rating. From the fuse product data sheet, it is found that a 700A fuse is not available, but 600A and 800 A units are. In addition, it is seen that in a $35^{\circ} \mathrm{C}$ ambient, the 600 A fuse can carry 500 A , and the 800 A unit is good for 700 A .

The published curves for peak let-through current and maximum let-through $\mathrm{I}^{2} \mathrm{t}$ for 60 Hz operation can be used to determine these same parameters under dc operation, provided correction factors are employed. Figures $11-5$ and 11-6 give factors which could be considered for making these corrections, but a more accurate approach is to recognize that in this example, the conditions approximate those for ac operation at 299 Hz . Figures $11-12$ and 11-13, which relate peak let-through current and let-through $I^{2} t$ to supply frequency, are therefore more applicable and will be used.

When using Figure 11-12, the curve for "Theoretical Maximum" should be used, even if it is found the fuse clears close to the peak of the current wave, and therefore, the curve marked "for limit of current limiting condition" would appear to be the one to use. This is, again, the result of the effect of offset of the current waveform.

To use the published curves for peak let-through current and maximum let-through I 2 t , it is necessary to convert the peak prospective fault current to the equivalent symmetrical RMS amperes; this relationship is shown in Formula 11-G.
Max. Symmetrical RMS Fault Current $=$
Max. Peak Prospective Fault Current 2.35

In the example discussed here, this becomes:
Max. Symmetrical RMS Fault Current $=\underline{10,745}=4572 \mathrm{~A}$
2.35


Figure 11-12. Typical Variation of Peak Let-Through Current with Frequency

Calculated values of peak letthrough current and maximum letthrough $\mathrm{I}^{2} \mathrm{t}$ are found in Table XIIIA.

The final column in Table XIIIA is an interpolated value obtained from:
$\mathrm{I}^{2} \mathrm{t} @ 300 \mathrm{~V}=\left(\mathrm{I}^{2} \mathrm{t} @ 500 \mathrm{~V}-\mathrm{I}^{2} \mathrm{t}\right.$ @ 240 V )
$\frac{300 \mathrm{~V}-240 \mathrm{~V}}{500 \mathrm{~V}-240 \mathrm{~V}}+\mathrm{I} 2 \mathrm{t} @ 240 \mathrm{~V}$

The preliminary values in Table XI-II can be corrected for operation at 299 Hz instead of 60 Hz by using Figures 11-12 (reading from "Curve for Theoretical Maximum") and 11-13, respectively, and are shown in Table IX-IIB.

Table XI-IIB also lists the melting $I^{2} t$ of these fuses as given in IR's product data sheet, PD-8.003A.

From the previous calculations, the following additional conclusions can be drawn:


Figure 11-13. Typical Variations of Maximum Fuse Let-Through $I^{2} t$ with Frequency

Table XI-II. Let-Through Current and Let-Through I ${ }^{2}$ t
A. Preliminary Data

| FUSE | LET-THRK | LET-THROUGH 2 t t |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | CURRENT |  |  | $@ 500 \mathrm{~V}$ |
|  | $@ 300 \mathrm{~V}$ |  |  |  |
| 600 A | $6,300 \mathrm{~A}$ | $2.8 \times 10^{5}$ | $1.25 \times 10^{5}$ | $1.60 \times 10^{5} \mathrm{~A} 2 \mathrm{sec}$ |
| 800 A | $7,900 \mathrm{~A}$ | $5.0 \times 10^{5}$ | $2.6 \times 10^{5}$ | $3.15 \times 10^{5} \mathrm{~A}^{2} \mathrm{sec}$ |

B. Detailed Data

| FUSE | FUSE RATING | CORRECTED PEAK LET-THROUGH CURRENT | CORRECTED LET-THROUGH 12t @ 300V | MELTING 12 t |
| :---: | :---: | :---: | :---: | :---: |
| SF50P600 | 600A | $\begin{gathered} 6,300 \times 1.71 \\ 10,770 \mathrm{~A} \end{gathered}$ | $\begin{gathered} 1.6 \times 10^{5} x \\ .53=8.5 \\ \times 10^{4} \mathrm{~A}^{2} \mathrm{sec} \\ \hline \end{gathered}$ | $\begin{gathered} 4.3 \times 10^{4} \\ A^{2} \mathrm{sec} \end{gathered}$ |
| SF50P800 | 800A | $\begin{gathered} 7,900 \times 1.71 \\ =13,510 \mathrm{~A} \end{gathered}$ | $\begin{array}{r} 3.15 \times 10^{5} \\ \times .53=16.7 \\ \times 10^{4} \mathrm{~A}^{2} \mathrm{sec} \end{array}$ | $\begin{gathered} 8.3 \times 10^{4} \\ A^{2} \mathrm{sec} \end{gathered}$ |

A. For the 800 A fuse, the peak let-through current of $13,510 \mathrm{~A}$ is greater than the peak prospective fault current of $10,745 \mathrm{~A}$. On the other hand, the $\mathrm{I}^{2} \mathrm{t}$ in the first half cycle of fault current (11.6 x $10^{4} \mathrm{~A}^{2} \mathrm{sec}$ ) is greater than the melting $\mathrm{I}^{2} \mathrm{t}$ for the fuse ( 8.3 x $10^{4} \mathrm{~A}^{2} \mathrm{sec}$ ). Thus, the fuse will open during the first half cycle and the fault will be interrupted in $\tau / 2$ or 1.67 msec.
Note that the fuse will not "current limit"; the $\mathrm{I}^{2} \mathrm{t}$ letthrough will be $11.6 \times 10^{4}$ $\mathrm{A}^{2}$ sec, the total $\mathrm{I}^{2} \mathrm{t}$ available from the circuit. However, this is less than the $\mathrm{I}^{2}{ }_{\mathrm{t}}$ rating of the main thyristors at 1.5 $\operatorname{msec}\left(16 \times 10^{4} \mathrm{~A}^{2} \mathrm{sec}\right)$ and so the fuse will protect the main thyristors.
B. For the 600A fuse, the peak let-through current of $10,770 \mathrm{~A}$ is the same as the $10,745 \mathrm{~A}$ peak prospective current. The $8.5 \times 10^{4} \mathrm{I}^{2} \mathrm{t}$ let-through is less than 11.6 x $10^{4} \mathrm{I}^{2} \mathrm{t}$ available from the circuit. The fuse will just barely current limit and therefore interrupt the current in less than 1.67 msec . However, the fuse is seen to be not much faster than $\tau / 2$ and so the $1.5 \mathrm{msec} \mathrm{I}^{2} \mathrm{t}$ rating of the semiconductor can be used to coordinate with the $8.5 \times 10^{4} \mathrm{~A}^{2}$ sec let-through by the fuse. There is an even greater margin in this case between the semiconductor $\mathrm{I}^{2} \mathrm{t}$ rating and the $\mathrm{I}^{2} \mathrm{t}$ letthrough by the fuse than for the 800 A unit. If, because of other considerations, such as
the cooling conditions found in the inverter, the main SCRs will be operated at less than 500 A RMS, the 600 A fuse should be selected, since it offers a greater $\mathrm{I}^{2} \mathrm{t}$ margin.
It is instructive to consider the consequences if the fuse fails to clear the fault within a few milliseconds after it occurs. As previously explained, a shoot-through results in a pulse of current (as the capacitor discharges through the relatively low circuit inductance) often of high magnitude and short duration. This is followed by a slower rising dc fault current from the rectifier, which may have a long time constant. The usual practice is to choose a fuse such that the $I^{2}$ t in the current pulse causes the fuse to operate before the peak of the current is reached. This is usually a relatively easy task for the fuse, since the high di/dt has the same effect as a high frequency alternating current with a low associated circuit inductance.

If the fuse does not operate before the peak, current then flows around through the free-wheeling diodes $R D_{1}$ and $R D_{2}$, while the fuse continues to carry only a slowly rising direct current from the supply. This is a more serious fault condition than the initial one, since it normally has a long time constant. If any possibility exists of the discharge current pulse not causing fuse operation, the fuse voltage rating must be chosen to be capable of clearing a fault on the dc supply. In this respect, it is important that stray circuit inductance and resistance, which have the effect of reducing the value of $\mathrm{I}^{2} \mathrm{t}$ in the pulse, are taken into account.

In addition to protecting the main thyristors, the fuse, $\mathrm{F}_{1}$, in Figure 11-11 operates in the event of a blocking failure of a commutating thyristor, $\mathrm{SCR}_{1}$ or $\mathrm{SCR}_{2}$, or of a free-wheeling diode, $\mathrm{RD}_{1}$ or $R D_{2}$. The current rating of $F_{1}$ is too large to enable it to operate at a low enough current level to protect these devices in the event of an injurious overload. But in the event of a blocking failure of any one of these devices, the fuse will operate during the ensuing short circuit, preventing damage to the main thyristors and also protecting the de supply to the inverter section from a sustained fault which could damage it.

## Discussion of Preceding Example

The preceding example presents a method of analysis which can be used with many different types of inverters and dc choppers. From this example, it is evident that a key factor in determining fuse performance is the $L / R$ of the inverter power circuit under fault conditions. If some of the circuit inductance is found in an inductor which saturates during a fault, the calculation of peak prospective fault current may have to be done in two steps. The first step would be to obtain the initial fault current waveform based on full capacitor voltage and the $L / R$ with maximum (unsaturated) circuit inductance. The second step is to determine the current waveform based on the voltage across the capacitor at the instant the inductor saturates and on a new (lower) L/R based on the minimum (saturated) circuit inductance. The waveform of the fault current is the composite of these two calculated waveforms.

## PROTECTING BY LIMITING PEAK JUNCTION TEMPERATURES

To extend the life of semiconductor power rectifier diodes and thyristors, limit the junction temperature when designing the circuit.

Most engineers worry more about the maximum current ratings. Because power rectifiers and thyristors are not usually built to withstand moderate-to-severe current overloads, the average designer relies on control devices alone for protection. And, to some extent, this tactic is successful. You can prevent catastrophic damage with fuses and circuit breakers, true. But with every overload, there is some deterioration in the life of the devices.

If the circuit design limits device junction temperatures to the maximum specified by the manufacturer, most overloads can be accommodated safely without the clearing of fuses or tripping of circuit breakers. Moreover, overloads need not be limited in frequency of occurrence. The only restriction: allow the device temperature to return to the initial value before another overload is applied. Fortunately, since the thermal storage capacity of SCRs is small, they cool quickly following an overload condition.

Limiting temperatures to maximum ratings requires that the anticipated overloads be defined (in terms of duration and current magnitude) and that the peak junction temperature at the end of the overload be calculated. The peak temperature is determined by calculating the junction temperature rise caused by the load (or overload) current and adding this to the initial or ambient temperature.

## Calculate Junction Temperature Above Case

The load current carried by rectifying devices usually has essentially a rectangular waveform (Figure 11-14). Some load inductance almost always present - prevents the current from varying in direct proportion to the variations in output voltage. Hence, each device carries a current pulse equal in magnitude to the dc output of the rectifier unit. The pulse lasts one-third of a cycle ( 120 electrical degrees) in a three-phase bridge circuit (Figure

11-14(a)). In a double-wye circuit, the duration of the current pulses is the same, but the amplitude is only one-half the dc output of the rectifier unit.

When the rectifying devices are SCRs and phase retard is used to control output voltage, the current waveform remains essentially the same; it is shifted in time, however, by an amount that depends on the angle of retard, $a$ (Figure 11-14(c)).

Because of the rectangular waveform, calculating junction-temperature rise is not difficult. The data

(c) ANODE CURRENT WAVEFORM WITH PHASE RETARD

Figure 11-14. Three-Phase Bridge Rectifier Waveforms and Circuit
required are the following: the onstate (forward) voltage curve at maximum rated junction temperature, the transient thermal impedance curve for times between 1 and 10 msec (the time range for one current pulse) and the rated thermal resistance of the device from junction to case. If a curve of instantaneous on-state power loss vs. current is available, the calculation can be somewhat simplified: on-state power loss may then be read directly rather than calculated from the forward voltage curve.

With these data, junction-temperature rise above case temperature under steady load conditions, $\Delta \mathrm{T}_{\mathrm{J}(\mathrm{JC})}$, can be calculated from Formula 11-H.
$\Delta \mathrm{T}_{\mathrm{J}(\mathrm{JC})}=\left[\frac{\mathrm{t}_{\mathrm{p}} \mathrm{R}_{\theta \mathrm{JC}}}{\tau}+\frac{(1-\mathrm{tp})}{\tau}\right.$
$\left.\mathrm{Z}_{\theta \mathrm{JC}(\mathrm{tp})}\right]_{\mathrm{P}}^{\mathrm{TM}}$
Where;
$\mathrm{P}_{\mathrm{TM}} \quad=\begin{gathered}\text { peak on-state or for- } \\ \text { ward power loss }\end{gathered}$
$t_{p} \quad=$ duration of one current pulse
$\tau \quad=$ period (reciprocal of supply frequency)
$\mathrm{R}_{\theta \mathrm{JC}}=$ thermal resistance
$\mathrm{Z}_{\theta \mathrm{JC}}(\mathrm{tp})=$ transient thermal impedance for one currentpulse duration.

The first expression in Formula 11-H (tp/ $\tau$ ) $\mathrm{R}_{\theta \text { JC }} \mathrm{P}_{\mathrm{TM}}$ - represents the average junction-temperature rise (average power dissipated times thermal resistance). To this is added an expression for the temperature response of the junction to the final pulse of load current. This increment contains a factor for the amount of power above the average power that is dissipated during the
final pulse: - (1-tp/ $\tau) \mathrm{P}_{\mathrm{TM}}$ multiplied by the transient thermal impedance.

For a more accurate version of Formula 11-H, the small heating effect of losses during the reverse and off-state (forward) periods should be included. However, in power semiconductors, these losses are only a few watts and are generally neglected. They cause only a small temperature rise of 1 or $2^{\circ} \mathrm{C}$.

## Include Case-to-Ambient Temperature Rise

The case-to-ambient temperature, which must be added to the junction temperature rise, represents the additional rise of the case above the cooling fluid (air, water or oil). It is calculated by multiplying the total average on-state, offstate, and reverse blocking losses by the thermal resistance from case to fluid. This thermal resistance usually results from two series resistances: case to heat dissipator (or case to heat sink) and heat dissipator to cooling fluid (Figure 11-15).

The thermal resistance from case to heat dissipator depends on the size of the thyristor base and presence or absence of thermal compound on the mating surfaces. The thermal resistance from heat dissipator to cooling fluid must be determined from such factors as the configuration, size and surface finish of the heat dissipator. Both resistances can be obtained from measurements or possibly from the manufacturer of the heat dissipator.

The formula for the junction temperature rise above the cooling fluid temperature, $\triangle \mathrm{T}_{\mathrm{J}(\mathrm{JA})}$, is given in Formula 11-J.


Figure 11-15. Thermal Interfaces of $S C R$
$\Delta T_{J(J A)}=\left(\frac{t_{p}}{\tau} P_{T M}+P_{B}\right)$
$\left(\mathrm{R}_{\theta J C}+\mathrm{R}_{\theta \mathrm{CS}}+\mathrm{R}_{\theta \mathrm{SA}}\right)+$ (11-J) (1- $\frac{\mathrm{t}_{\mathrm{p}}}{\tau}$ ) $\mathrm{P}_{\mathrm{TM}} \mathrm{Z}_{\theta \mathrm{JC}(\mathrm{tp})}$.

## Where: <br> $\mathrm{R}_{\theta \mathrm{CS}}=$ case-to-heat dissipator thermal resistance;

$\mathrm{R}_{\theta \mathrm{SA}}=$ heat-dissipator-to-fluid thermal resistance;
$\mathrm{P}_{\mathrm{B}(\mathrm{AV})}=$ average power losses during reverse blocking and forward off-state periods.

Note that the heating caused by blocking losses $\mathrm{P}_{\mathrm{B}}(\mathrm{AV})$ (neglected in Formula 11-H) is included in Formula 11-J. For the calculation of
$\triangle \mathrm{T}_{\mathrm{J}(\mathrm{JA})}$, this heating becomes significant.

Finally the RMS value of the current found by the above procedure should not exceed the RMS current rating of the device.

## Short Overload: <br> The Most Common Case

One of the most common overload conditions is a short overload following continuous loading. Form ula 11-K (an extension of Formula 11-J) may be used to calculate the junction temperature rise at the end of such an overload.

In determining the transient thermal impedance for relatively short overload periods, it is possible to use the transient thermal impedance curve for the idealized case of a thyristor mounted on an infinite heat sink. This yields valid results when the transient thermal impedance does not exceed $90 \%$ of the maximum value on the curve. For longer overloads, where the thermal impedance is found to be greater than $90 \%$ of the maximum value on the curve, use a curve for the actual heat dissipator and SCR together.

Such a curve can be drawn by forming a composite of the published transient thermal impedance curves for the rectifier device and the actual heat dissipator. Make certain to include the effect of the thermal resistance at the interface between the SCR and the heat dissipator.

To prevent excessive junction temperature at the end of an overload, reduce the continuous loading to allow for a possible additional temperature rise that may occur during the overload. The amount of reduction depends on the severity and duration of the overload. If a temperature rise margin, $\triangle \mathrm{T} J(\mathrm{OL})$, is provided (when determining the steady-state current loading), the recurrent overload, $\mathrm{P}_{\mathrm{TM}}(\mathrm{OL})$, that can be imposed for any duration, t (OL), can be found from Formula 11-L (derived from the final term of Equation 11-K.

The average current that can be carried during the overload period is calculated from the on-state voltage vs. current curve, or it can be read from the appropriate on-state power loss vs. current curve.
$\Delta \mathrm{T}_{\mathrm{J}(\mathrm{JA})}=\left(\frac{{ }^{t_{p}}}{\tau} \mathrm{P}_{\mathrm{TM}(\mathrm{SS})}+\mathrm{P}_{\mathrm{B}(\mathrm{AV})}\right)\left(\mathrm{R}_{\theta \mathrm{JC}}+\mathrm{R}_{\theta \mathrm{CS}}+\mathrm{R}_{\theta \mathrm{SA}}\right)+$
$\left(1-\frac{t_{p}}{\tau}\right) \mathrm{P}_{\mathrm{TM}(\mathrm{SS})} \mathrm{Z}_{\theta \mathrm{JC}\left(\mathrm{t}_{\mathrm{p}}\right)}+\left(\mathrm{P}_{\mathrm{TM}(\mathrm{OL})}-\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}\right)$
$\left.\left[\frac{t_{p}}{\tau} Z_{\theta J A(t O L}\right)+\left(1-\frac{t_{p}}{\tau}\right) Z_{\theta J C}\left(t_{p}\right)\right]$
Where:
$\mathrm{P}_{\mathrm{TM}} \mathrm{SS}$ ) $=$ peak steady on-state power loss (prior to overload)
$\mathrm{P}_{\mathrm{TM}}(\mathrm{OL})=$ peak on-state power loss during overload
$\mathrm{Z}_{\theta \mathrm{JA}}(\mathrm{tOL})=$ transient thermal impedance, junction to fluid, for the overload period.
$\mathrm{P}_{\mathrm{t}}(\mathrm{OL})=\frac{\Delta \mathrm{T}_{\mathrm{J}(\mathrm{OL})}+\mathrm{P}_{\mathrm{TM}(\mathrm{SS})}\left[\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{Z}_{\theta \mathrm{JA}(\mathrm{tOL})}+\left(1-\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{Z}_{\theta \mathrm{JC}(\mathrm{tp})}\right](11-\mathrm{L})\right.}{\frac{\mathrm{t}_{\mathrm{p}}}{\tau} \mathrm{Z}_{\theta J A}(\mathrm{tOL})+\left(1-\frac{\mathrm{t}_{\mathrm{p}}}{\tau}\right) \mathrm{Z}_{\theta J C(\mathrm{tp})}}$

## Severe Overloads

Sometimes rectifying devices must accommodate severe overloads. In this case, operate the devices on a continuous basis well below their published continuous ratings. The penalty is particularly severe for controlled rectifiers, which usually have a maximum junction operating temperature of only $125^{\circ} \mathrm{C}$.

Because of this limitation, some equipment designers permit the controlled rectifier junction temperature to exceed the maximum rated operating temperature during a severe overload. At the same time, steps are taken to make sure the SCR does not lose control when voltage is applied in the off-state direction during and immediately following such an overload. Two factors make such operation feasible:
A. The repetitive peak off-state and reverse voltages impressed on an SCR during normal operating conditions are usually considerably lower than the maximum rated values for the part. These margins exist because the designer has provided for transients.
B. When an SCR is supplied from a conventional 60 Hz power system, there is a time interval of about 8.3 msec between off-state voltage applications. During this time, the SCR junction is cooling, and since the junction has a short thermal time constant, it cools rapidly. Its temperature will approach, and may even drop to, less than the maximum rated operating temperature.

Of course, each SCR should be tested to ensure that it will perform in the manner expected. Some SCRs lose their off-state blocking capability rapidly as junction temperature increases above $125^{\circ} \mathrm{C}$. Conversely, epitaxial SCRs exhibit a more gradual blocking capability degradation with temperature, and they have been found appropriate for this application.

The curve in Figure 11-16(a) shows the off-state blocking performance of epitaxial Hockey-Puk SCRs rated 550 A average (860A RMS) in the range from 800 to 1300 V. A second curve, Figure 11-16(b), shows the observed junction temperature rise for the same devices 8.3 msec after a half-sinewave current surge. The curve is plotted for half sine waves up to 7000A peak.

The temperature increase caused by an overload, as read from the graph, should be added to the calculated junction temperature prior to the overload (as calculated by Formula 11-H). The peak junction temperature obtained is then used to determine the greatest off-state voltage that the SCR will block at that temperature.

## Example: AC Power Control Assembly

These principles were used in the design of a high voltage ac power controller, installed in the primary of a rectifier transformer (Figure 11-17). Two SCR string assemblies connected in anti-parallel were used in each conductor to control power from a $4160 \mathrm{~V}, 60 \mathrm{~Hz}, 3$-phase line. Each pair of assemblies was rated to carry 233A RMS continuously at an air flow rate of 350 cubic feet per minute in a maximum ambient

(a) BREAKOVER VOLTAGE ABOVE $100^{\circ} \mathrm{C}$

(b) JUNCTION TEMPERATURE RISE VS SURGE CURRENT

Figure 11-16. Performance Above $125^{\circ} \mathrm{C}$ and Following Current Surge


Figure 11-17. High Voltage Power Control Circuit
temperature of $75^{\circ} \mathrm{C}$. The overload current rating of each assembly was 5200 A peak for 0.2 second and 7000 A peak for 0.0083 second. Following either overload, each string of SCRs in the controller was required to immediately block 4160 V RMS.

The working peak reverse voltage that can be applied can be as much as 6500 V under high-line voltage conditions. The string assembly consisted of ten 860A RMS Hock-ey-Puk SCRs in series, each device having a repetitive peak off-state and reverse voltage rating of 1300 V .

Each device in Figure 11-17 was tested to be sure it did not selftrigger when a $1550 \mathrm{~V}, 60 \mathrm{~Hz}$ half
sine wave was applied in the offstate direction at a junction temperature of $125^{\circ} \mathrm{C}$. The aggregate repetitive peak off-state and reverse voltage rating was therefore $13,000 \mathrm{~V}$, two times the maximum working value, and the aggregate nonrepetitive peak reverse voltage rating was $15,500 \mathrm{~V}, 2.38$ times the maximum working value. These margins provided for nonuniform distribution of blocking voltage across the 10 devices and in addition for line voltage transients up to 2.5 times the normal working peak reverse voltage of 5883 V . Tests showed that the power controller gave the required control under fault conditions.

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## Cooling

## Thermal Considerations for StudMounted Devices

Silicon rectifier devices (rectifier diodes, controlled rectifiers and triacs) have ratings which are based upon thermal considerations. Since it is inherent in the construction of silicon devices that the major losses must occur internally and within a very small volume of the device and that the heat generated by these losses must flow outward to some form of heat dissipator, the optimum cooling for silicon devices may be somewhat more critical than for some other electrical devices.

All three modes of heat transfer - conduction, radiation and convection - are always present and should be considered in all cases of cooling silicon devices. However, under some modes of operation, one or more of these heat transfer methods may be predominant to such an extent as to make the contribution of the other types negligible. For example, if the device is mounted directly on a liquid-cooled heat exchanger, the percentage of losses by natural convection and by radiation may be so small by comparison to the heat transfer by conduction as to be considered negligible. In extremely high altitude applications, conduction or convection heat transfer methods are much too inefficient, so that the major part of the cooling must come from radiation. However, for most industrial applications, either natural or forced convection cool-
ing in air will be used much more frequently than the other two methods.

## General Cooling Theory

The losses within a silicon device occur in the thin wafer of silicon inside the primary component. The heat thus generated must first flow out through the case and/or the lead(s) of the device. By far the greatest proportion of this heat flows out through the case into some form of heat exchanger, and then through the heat exchanger into the cooling ambient, which may be air or a liquid. This thermal path, therefore, may be thought of as a group of thermal resistances all connected in series; analogous to a group of electrical resistors connected in series.

There will be a value of thermal resistance assigned to each resistor in series, the first of which is the internal thermal resistance from junction to case. This is given in the individual device specifications. The next resistance, in series, is the contact thermal resistance from the case to the heat exchanger. Following this is the thermal resistance of the heat exchanger, between the point where the device is mounted and the cooling medium. In normal practice, the heat exchanger internal thermal impedance and the surface to air thermal impedance are combined and experimentally determined as a composite value. Each of these thermal resistances must be considered in detail in or-
der to assure proper cooling of the device, since a temperature drop is associated with each of them.

The above-mentioned thermal resistances are steady-state values only, and are used to calculate the average temperature rise of the junction above the ambient of the cooling medium under steady-state operation.

In addition to continuous operation, there usually are transient heating conditions which may occur in a system and which must also be accounted for; e.g., there may be thermal overloads from rapid changes in the ambient temperature of the cooling medium, or electrical overloads due to varying current requirements which the device must supply. These electrical overloads may be either momentary process load variations or fault conditions, and each must also be considered as a function of its maximum time duration. The individual device specifications also contain curves of transient thermal resistance by which the electrical overload conditions can be translated into transient temperature changes occurring within the device. Only the system designer, however, can account for the transient thermal conditions of the ambient cooling medium.

In almost all systems there will be electrical transients which will create varying amounts of heat. Probably the one notable exception to this is when a unit must supply a large inductive load, such as a large electromagnet, and is coupled directly to the load in such manner that there is no switching between the device and the load. Under these conditions, only moderate variations in load current can occur, due to varying temperatures of the
windings in the electromagnet, or to variations in supply voltage. These are usually small, compared to the transient loading which can occur in most other applications.

## Detailed Requirements

There are several items which should be carefully observed and considered when applying silicon devices in order to obtain optimum cooling conditions:

The device itself should be inspected to insure that the contact surface of the case is clean, smooth, flat, and specifically, that it has no projections from the case which would impair uniform total contact with the heat exchanger.

The heat exchanger for use with either the stud or Hockey-Puk package should be prepared to receive the device, and the contact area should be smooth, with no burrs, no projections, and preferably with no depressions in the surface. It should be flat, such that it can mate with the contact surface of the device case and achieve a maximum uniform contact between the two surfaces, and it should be clean, with no dirt, corrosion, and a minimum of surface oxides. The hole in the heat exchanger for the stud SCR should be accurately drilled perpendicularly to the mounting surface, and be no more than $0.015 \pm 0.010 \mathrm{in} .(0.38 \pm 0.25$ mm ) larger in diameter than the nominal diameter of the stud. Buffing of mating surfaces to remove oxides prior to assembly will assure a low interface thermal resistance.

The two mating surfaces should be lubricated with a substance to improve the thermal heat transfer from the case of the device to the
heat exchanger, by filling any air spaces, and which will remain stable under wide variations of temperature and environmental conditions. In this way, the formation of corrosion products, galvanic products, or oxides between the two surfaces, will be prevented. For this purpose, a Dow Corning silicone grease (number DC-200) has been widely and effectively used. Another product, called "Penetrox A," which was developed for use on the contact surfaces of overlapping aluminum busbars, has also been successfully used in many places. This contains a heat conductive metal oxides to improve heat transfer. Thermal compounds containing filler particles have the disadvantage of indenting the mounting surface slightly, requiring a refinishing of the surfaces should reassembly become necessary. (See later sections of this chapter for mounting precaution for rotating members.)

It is very important to mount the device to the heat exchanger using the proper amount of torque, to obtain optimum pressure between the two mating surfaces. Individual device specifications list the correct torque to be used in these instance, and a torque wrench, accurate in the specified range, should be used in mounting all such devices in order to achieve optimum results.

Two notes of caution should also be added: (1) Excessive torque can damage the threads of the soft copper stud of the device and, in some cases, even mechanically stress the junction, causing a change in the electrical characteristics, and (2) The threads of the stud and nut should not be lubricated, since actual tensile stress on the stud can
double for the same measured torque with lubricated threads.

Care must also be exercised in the use of dissimilar metals in contact with each other when mounting devices to heat exchangers. Thyristors come with various plated metallic finishes to protect them from environmental conditions and to provide an acceptable material to be in contact with heat exchanger finishes. Some of the finishes applied to thyristors are: tin plating, cadmium plating, or nickel plating. When mounting devices with one or more of these finishes against a heat exchanger, care should be exercised either to choose a heat exchanger material which is compatible with the plated finish (which means near to this material in the galvanic series of metals), or to use a lubricating substance between the two metals which will inhibit galvanic action.

For a more comprehensive discussion of and listing of metal surfaces which are compatible with each other, refer to Military Specifications, MIL-F-14072 (Sig. C) and MIL-E-16400E (Navy). Both of these specifications offer excellent guidance in the selection of compatible metallic surfaces. When an aluminum heat exchanger is used, any anodizing should be removed from the contact surface, as it presents substantial thermal and electrical resistance. A light chromate treatment is often acceptable instead of anodizing, and it need not be removed.

Occasionally it is necessary to electrically insulate the case of the device from the surface of the heat exchanger. Under these conditions, usually a thin washer of mica or silicone rubber is placed between
the device and the heat exchanger surface (after lubricating all four mating surfaces with a thermal lubricant, as mentioned above). This practice is acceptable, when necessary, for small devices. It should rarely, or never, be used with high power devices, since the thermal resistance from the base, through the insulating washer, to the heat exchanger increases very rapidly and, in most cases, becomes prohibitively high for large power devices.

## Rotating Rectifiers

Rotating fixtures mounting rectifier devices, such as found in ac motor and alternator exciters, demand special consideration to mounting techniques, thermal conditions, and potentially damaging centrifugal forces.

Special mounting techniques are needed with the large Hockey-Puk packages to avoid an increase in case-to-sink thermal impedance. Preferably, the total force will be greatest at whatever rotational speed demands the highest current. Care must be taken that mounting force plus centrifugal force at the highest rotational speed is uniform and does not result in damage to the silicon.

Thermal compound made with filler particles, such as ZnO , is not recommended for rotating applications, since lubricant will tend to be forced outward with filler particles left behind.

The top terminal of a stud device must have sufficient strength to withstand the high centrifugal forces. Special packages are available from IR for such applications. The 300 ampere diodes, 305 U and 307 U , are equipped with a stress
relief cone for use on rotating members.

## Electrical Contact Resistance

For good (low) electrical contact resistance, the heat exchanger surfaces should be flat, smooth, and of low and stable resistivity. Clean base aluminum has a low surface resistivity but tends to oxidize easily and will have an increasing surface resistance with time unless it is suitably protected. An anodized finish is not conductive and therefore, where an electrical connection between the heat exchanger and semiconductor or where an external electrical connection is made, the affected areas must be masked before anodizing or spot faced after anodizing. Since the contact surface then will be bare aluminum, it is again necessary to be careful to avoid oxidation. A surface finish of thin chromate conversion, per MIL-C-5541, Type II, Class 3, offers a stable and low contact resistance only slightly higher than ox-ide-free bare aluminum.

## Thermal Contact Resistance

For good heat exchanger contact thermal resistance surface finish over the areas where a semiconductor device is mounted should be flat ( 0.001 inches TIR) and very smooth. When a good thermal lubricant (plain or filled) is used on the mounting surface, acceptable results can be achieved with a surface finish of 64 microinches or less. In any event, a thermal lubricant should be used, since it results in substantial improvement of contact thermal resistance, and it provides long-term electrical and thermal resistance stability.

## Thermal Resistance

Thermal resistance of a semiconductor device is defined as "the temperature difference between two specified points or regions divided by the power dissipated under conditions of thermal equilibrium." Thermal resistance values, as shown in Formula 12-A, are expressed in the units degrees $C$ per watt.

$$
\begin{equation*}
\mathrm{R}_{\theta}=\frac{\Delta \mathrm{T}}{\mathrm{~W}} \tag{12-A}
\end{equation*}
$$

Where:
$\Delta T$ is temperature difference between particular points, for example,
A. Junction and case ( $\mathrm{TJ}-\mathrm{T}_{\mathrm{C}}$ )
B. Case and heat exchanger (heat sink) ( $\mathrm{T}_{\mathrm{C}}-\mathrm{T}_{\mathrm{S}}$ )
C. Heat exchanger and ambient $\left(\mathrm{T}_{\mathrm{S}}-\mathrm{T}_{\mathrm{A}}\right)$
$\mathrm{R}_{\theta}=$ Thermal resistance between two particular points.
$\mathrm{W}=$ Power Dissipation

## Thermal Considerations for Hockey

 Puk DevicesIn order to calculate the current rating of a Hockey-Puk device in a given mechanical assembly, it is necessary to know the thermal resistance from the Hockey-Puk case to ambient. This can be determined by referring to the published data for the heat exchangers (heat sinks) used in the assembly, or by measurement.

Analysis of the thermal resistance paths of the Hockey-Puk, shown in Figure 12-1, results in the thermal resistance schematic shown in Figure 12-2.

Using the junction as a starting point, it is obvious that two substantial thermal paths exist: an-ode-to-air and cathode-to-air. The thermal resistance, junction-to-air of each path, anode and cathode, is the sum of the series connected thermal resistances, as shown in Formulas $12-\mathrm{B}$ and $12-\mathrm{C}$


Figure 12-1. Typical Hockey-Puk Construction

## INTERNATIONAL RECTIFIER IRR

\%


Figure 12-2. Thermal Resistance Schematic
$\mathrm{R}_{\theta \mathrm{JA}(\mathrm{K})}=\mathrm{R}_{\theta \mathrm{JC}(\mathrm{K})}+\mathrm{R}_{\theta \mathrm{CS}(\mathrm{K})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{K})}$
$\mathrm{R}_{\theta \mathrm{JA}(\mathrm{A})}=\mathrm{R}_{\theta \mathrm{JC}(\mathrm{A})}+\mathrm{R}_{\theta \mathrm{CS}(\mathrm{A})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{A})}$
Where:
Cathode Anode
Path
$\mathrm{R}_{\theta \mathrm{JC}}(\mathrm{K}) \quad \mathrm{R}_{\theta \mathrm{JA}}(\mathrm{A})=$ Thermal resistance, junction-to-air
$\mathrm{R}_{\theta \mathrm{JC}}(\mathrm{K}) \quad \mathrm{R}_{\theta \mathrm{JC}}(\mathrm{A})=$ Thermal resistance, junction-to-case
$\mathrm{R}_{\theta \operatorname{CS}(\mathrm{K})} \quad \mathrm{R}_{\theta \mathrm{CS}(\mathrm{A})} \quad=$ Thermal resistance, case-to-sink
$\mathrm{R}_{\theta \mathrm{SA}(\mathrm{K})} \quad \mathrm{R}_{\theta \mathrm{SA}(\mathrm{A})}=$ Thermal resistance, sink-to-air

The net thermal resistance in each path ( $\mathrm{R}_{\theta} \mathrm{JA}$ ) may then be represented as in Figure 12-3.

The composite thermal resistance of both paths is given in Formula 12-D.

$$
\begin{aligned}
& \mathrm{R}_{\theta \mathrm{JA}(\text { comp })}= \\
& \frac{\left[\mathrm{R}_{\theta \mathrm{JA}(\mathrm{~K})}\right]\left[\mathrm{R}_{\theta \mathrm{JA}(\mathrm{~A})}\right]}{\left[\mathrm{R}_{\theta \mathrm{JA}(\mathrm{~K})}\right]+\left[\mathrm{R}_{\theta \mathrm{JA}(\mathrm{~A})}\right]}
\end{aligned}
$$

Where:
$\mathrm{R}_{\theta} \mathrm{JA}$ (comp)
$=$ Thermal resistance, junction to air, composite
The internal thermal resistances of IR Hockey-Puks, from junction to cathode and from junction to anode, are nearly the same, so that for most situations, where nearly equal thermal resistance is provided


Figure 12-3. Simplified Thermal Resistance Schematic
from each pole piece to the cooling medium, a composite internal thermal resistance value may be used in place of the individual values. This composite value is found on the published ratings sheets for IR Hockey-Puks, and its use simplifies the calculation of the thermal resistance of Hockey-Puk assemblies.

When the Hockey-Puk is considered as having a single, composite, thermal resistance, the thermal paths in an assembly become those shown in Figure 12-4, and the composite thermal resistance, junction to ambient, of the assembly, can be calculated from Formula 12-E

Quite frequently, identical heat exchangers will be used for cooling
a given Hockey-Puk. In this case, the thermal resistances in the anode and cathode paths external to the Hockey-Puk are identical, and the equation reduces to Formula 12 -Eb.

To use the equations shown below, the thermal resistances of the heat exchangers in the Hockey-Puk assembly must be known. Thermal resistance data for IR heat exchangers are included in the heat exchanger data sheet, PD-7.001. Similar thermal design considerations are necessary for semiconductor packages other than the Hockey-Puk.

## Thermal Resistance Measurements

If the heat exchangers are special ones, perhaps designed by the user.

$$
\begin{align*}
& \mathrm{R}_{\theta \mathrm{JA}(\text { comp })}=\mathrm{R}_{\theta \mathrm{JC}(\text { comp })}+ \\
& \frac{\left[\mathrm{R}_{\theta \mathrm{CS}(\mathrm{~K})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{~K})}\right]\left[\mathrm{R}_{\theta \mathrm{CS}(\mathrm{~A})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{~A})]}\right]}{\left[\mathrm{R}_{\theta \mathrm{CS}(\mathrm{~K})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{~K})}\right]+\left[\mathrm{R}_{\theta \mathrm{CS}(\mathrm{~A})}+\mathrm{R}_{\theta \mathrm{SA}(\mathrm{~A})}\right]} \tag{12-E}
\end{align*}
$$

This can be written more simply as in Formula 12-E(a).

$$
\begin{gather*}
\mathrm{R}_{\theta \mathrm{JA}(\text { comp })}=\mathrm{R}_{\theta \mathrm{JC}(\text { comp })}+ \\
\frac{\left[\mathrm{R}_{\theta \mathrm{CA}(\mathrm{~K})}\right]\left[\mathrm{R}_{\theta \mathrm{CA}(\mathrm{~A})}\right]}{\left[\mathrm{R}_{\theta \mathrm{CA}(\mathrm{~K})}\right]+\left[\mathrm{R}_{\theta \mathrm{CA}(\mathrm{~A})}\right]} \tag{12-Ea}
\end{gather*}
$$

Where:
$\mathrm{R}_{\theta \mathrm{CA}}(\mathrm{K}) / \mathrm{R}_{\theta \mathrm{CA}(\mathrm{A})}=$ Thermal resistance, case-to-air
$R_{\theta J A}($ comp $)=R_{\theta J C}+\frac{R_{\theta C A}}{2}$


Figure 12-4. Thermal Resistance Schematic
it becomes necessary to measure the thermal resistance values. In making thermal resistance measurements on a Hockey-Puk assembly, the test puk should be mounted between the desired heat exchangers (heat sinks) with recommended lubrication and mounting pressures. Thermal resistance measurements of stud devices are covered in the NEMA-EIA standard RS-282[1]

Free Convection Air Measurements
The test assembly with its heat exchangers should be supported with the heat exchanger surfaces in a vertical plane in a cubic enclosure whose dimensions are a minimum of four times the heat exchanger length, so as to allow natural convection, air circulation. The enclosure should be so designed that the inside walls are approximately the same temperature as the inside ambient temperature. The inside ambient temperature should be measured by means of a thermocouple mounted a minimum of 2 inches directly below the center of the bottom edge of the assembly.

The heat exchanger temperature should be measured by means of a peened thermocouple attached to the particular heat exchanger which makes contact to the anode of the device. The thermocouple should be attached no more than one quarter of an inch away from the anode pole of the test device and on its upper side. This measurement point should be located on the vertical center line of the assembly. The Hockey-Puk case temperature measurement should be made by means of a thermocouple attached to the anode pole piece on the same centerline as the heat exchanger thermocouple.

The thermal resistance is determined by dividing the observed temperature rise above ambient (with input power held constant and all measured temperatures at equilibrium) by the average input power. This calculation will provide the composite thermal resistance case to ambient, and will be conservative when the two thermal paths external to the Hockey-Puk are essentially identical.

## Forced Convection Air Measurements <br> The Hockey-Puk assembly should

 be firmly supported inside a rectangular air duct. It should be oriented in such a way that the heat exchanger fins are parallel to the air stream. The duct should have a height and width one inch greater than the test assembly. If the spacing between the Hockey-Puk assembly and the duct is less than one inch, proper air flow over all parts of the assembly may not occur during the test.The length of the duct from air input end to air exhaust end should be a minimum of six times the assembly length (measured parallel to the cooling fins of the heat exchanger). A duct length of six times the assembly length is recommended so that the effect of turbulence will be minimized. The Hock-ey-Puk assembly should then be located in the duct so that the leading edges of the heat exchangers are at least four exchanger lengths downstream from the air input end of the duct. The current carrying leads should be brought out horizontally at the exhaust end of the duct as shown in Figure 12-5.

Air velocities and ambient temperature should be measured one


Figure 12-5. Recommended Heat Exchanger Test Set-Up
exchanger length upstream from the leading edge of the assembly. The test air velocity should be considered the average of all point velocities over the air stream cross section. Individual velocities should not vary with respect to each other by more than $\pm 10 \%$.

The heat exchanger and case temperature test points should be the same as previously described for free convection thermal resistance measurements. The calculation of the composite thermal resistance, junction-to-case, is performed as described before.

## Precautions

The following precautions should be observed when making temperature measurements using thermocouples. The thermocouple junction should be formed by welding rather than soldering or twisting. Welding makes a more reliable junction with increased accuracy. The thermocouple should be attached to the surface of the heat exchanger by inserting it into a drilled hole and peening the hole closed.

Case temperature measurements are made by inserting a thermocouple into a drilled hole in the side of the anode pole piece. Care should be taken to be sure that the surface of the pole is not distorted, to prevent incorrect test results. Five or ten mil. diameter thermocouple wire is recommended (No. 30 AWG wire is often specified).

## Current Rating Calculations

The composite thermal resistance from Hockey-Puk case to ambient, when multiplied by the average power dissipated in the Hock-ey-Puk during operation, will give the temperature rise of the Hock-ey-Puk case above ambient temperature. This rise, when added to the maximum anticipated ambient temperature, should not exceed the maximum allowable Hockey-Puk case temperature, for the particular operating conditions to which the calculations pertain.

When calculating case temperature rise, all power dissipated in the Hockey-Puk must be considered. The power dissipated may be considered as falling into these categories:
A. On-state power losses, device fully turned-on, as given in the published curves for the Hock-ey-Puk.
B. Reverse blocking losses.
C. Switching losses, during turnon and turn-off periods. (These become significant at operating frequencies above 400 Hz )
If the case temperature rise shows the maximum allowable case temperature will be exceeded, one or more of the following steps can be taken to overcome this:
A. Increase the cooling provided the Hockey-Puk by increasing the cooling fluid velocity or using larger heat exchangers.
B. Switch to a different cooling method; use forced air cooling instead of free convection air, or water cooling instead of air.
C. Reduce the ambient temperature.
D. Switch to a larger Hockey-Puk or use two devices in parallel.
The above rating calculations are treated more fully in reference [3] and in other chapters of this book.

## Cooling for Specific Applications

The basic procedure of the overall analysis of cooling for a specific application is outlined as follows:
A. Determine the average watts loss developed in the component under steady-state operation. Using this value and the appropriate internal thermal resistance, determine the average temperature drop from junction-to-case for the device. For low duty cycles, the procedure described in steps E through H should be used to obtain the maximum junction temperature varia-
tion around this mean value.
B. Next, select a value of $\mathrm{R}_{\theta \mathrm{CS}}$, and using the same watts loss, calculate the temperature drop from the case to the surface of the cooling fin.
C. Again, using the same watts loss, having previously chosen the length of heat exchanger extrusion and the cooling air velocity, determine the thermal resistance for that operating condition and calculate the temperature drop from the heat exchanger surface where the device is mounted, to the ambient air.
D. Total the three temperature drops, and add these to the maximum expected ambient air temperature to find the average junction temperature of the device under a steadystate operating condition.
E. Calculations similar to A through D must now be made for all overload conditions which will be superimposed on the steady-state operation. Using the transient thermal impedance curves and the additional watts loss due to these overloads, the additional temperature rise caused by the overload condition should be calculated and added to the temperature rise previously calculated for the steadystate load.
F. Compare this last total junction temperature with the maximum allowable junction temperature of the device as listed on the detailed specifications to determine if operation is still within the limits specified for the particular device under study.
G. Note the time interval be tween the application of each overload. If there is sufficient time for the device to cool to its steady-state operating temperature, the calculation is complete. If other overloads are applied before cooling is complete, higher peak temperatures may be reached. Reference [2] indicates methods of calculation which can be used in cases such as this.
H. Adjustments may be necessary either to increase or decrease the cooling obtained from the heat exchanger, or to change the semiconductor device or the number in parallel to achieve a satisfactory operating system depending upon the results obtained in steps E, F, and G.
If the electrical overload surges of medium and large power devices are of duration less than $0.5 \mathrm{sec}-$ ond, the transient heat will not have time to flow from the device into the heat exchanger. In that case, the transient properties of the device and steady-state properties of the heat exchanger are of major importance. For overloads longer than 0.5 second, the thermal storage capacity of the heat exchanger becomes important.

Table XII-I shows the heat exchanger capabilities for some 12 metals. From these data, it is evident that if weight is of minor concern, nickel has the highest heat storage per cubic inch. However, where weight is important, aluminum has the highest heat storage per pound. It also has the highest thermal conductivity per pound
(given under conductivity density) which, coupled with a moderate material cost per pound, makes aluminum a very attractive choice for fabrication of heat exchangers.

Flat fin heat exchangers are sometimes used in low power applications for PACE/paks (hybrid assemblies) or discrete devices. Electrically isolated packages allow the system enclosure to be utilized as the heat sink. Figure $12-6$ is a nomogram for determining sink to ambient thermal resistance, $\mathrm{R}_{\theta} \mathrm{SA}$, for a flat heat exchanger using natural convection. To use, select the heat sink area at left and draw a horizontal line across the chart from this value. Read the value of $\mathrm{R}_{\theta} \mathrm{SA}$ depending on the thickness of the material, type of material and mounting position.

## Oil-Immersed Cooling

To apply semiconductor devices to oil-immersed power supply applications, use the curves shown on Figure 12-7, and the following recommended design procedure.

The basic steps in designing the cooling enclosure for the oil and rectifiers (and any other immersed equipment) are: (It is assumed that the rectifier devices are mounted on flat cooling fins.)
A. Establish the maximum ambient air temperature and the maximum device case temperature. (For industrial use, the maximum device case temperature may be indicated by the class of insulating materials used, Class A or B.)
B. Determine the losses in watts for all immersed components, i.e.,

1. Watts loss per rectifierdevice

Table XII-I. Heat Exchanger Properties of Various Metals

| MATERIAL | HEAT STORAGE CAPACITY |  | THERMAL CONDUCTIVITY (w/in. ${ }^{\circ} \mathrm{C}$ ) | DENSITY (POUND/ in. ${ }^{3}$ ) | THERMAL CONDUCTIVITY DENSITY (W-in. $2 /{ }^{\circ} \mathrm{C}-\mathrm{lb}$.) |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | (JOULE/in. ${ }^{3}$ ) | (JOULE/ POUND) |  |  |  |
| Aluminum (6061) | 40.5 | 413 | 4.35 | 0.098 | 44.4 |
| Brass | 50.5 | 165 | 2.94 | 0.306 | 9.6 |
| Copper | 57.5 | 178 | 9.93 | 0.323 | 32.4 |
| Gold | 41.3 | 59 | 7.48 | 0.698 | 10.7 |
| Lead | 24.2 | 59 | 0.88 | 0.41 | 2.15 |
| Molybdenum | 45.5 | 123 | 3.71 | 0.369 | 10.1 |
| Nickel | 67.0 | 208 | 1.54 | 0.322 | 4.8 |
| Silver | 40.5 | 107 | 10.55 | 0.380 | 27.8 |
| Steel, Carbon | 62.0 | 209 | 1.14 | 0.283 | 4.0 |
| Steel, Stainless | 65.0 | 224 | 0.413 | 0.29 | 1.4 |
| Tin | 28.6 | 110 | 1.54 | 0.261 | 5.9 |
| Zinc | 47.5 | 184 | 2.84 | 0.258 | 10.6 |


| $\mathrm{R}_{\text {OSA }}$-THERMAL RESISTANCE ( ${ }^{\circ} \mathrm{C} /$ WATT) |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MATERIA | IAL | COPPER |  |  |  | ALUMINUM |  |  |  |
| MOUNTI POSITIO | ING ON | HORI | TAL |  | AL | HOP | NTAL | VE | ICAL |
| THICKNESS (I | (INCHES) | 3/16 | $3 / 32$ | 3/16 | 3/32 | 3/16 | 3/32 | 3/16 | 3/32 |
| AREA OF ONE SIDE OF HEAT DISSIPATOR OR CHASSIS (SQUARE INCHES) |  |  |  |  |  |  |  |  |  |

Figure 12-6. Thermal Resistance of Flat Fin Heat Exchanger
2. Watts loss for complete assembly.
3. Watts loss for other immersed components (transformer, contactors, etc.)
C. From the above temperature and loss data, calculate:

1. Temperature drop from device case to fin center.
2. Temperature drop from mean fin temperature to oil (from Curve A on Fig. ure 12-7).
NOTE: Fin thicknessshould be $1 / 8$ inch minimum when using copper and $1 / 4$ inch thickness for aluminum. Compute area using both sides of the fin. To obtain the temperature drop from center (hottest spot) to oil, multiply the temperature drop from mean fin temperature by a factor of 1.9 approximately.
3. Select an enclosure size and from total area of vertical sides, and total watts loss, determine temperature drop from enclosure to air (using Curve S, if a plain enclosure is used, or Curve $R$ if cooling fins are used.
4. After enclosure dimensions have been fixed from 3. above, calculate the temperature drop from oil to enclosure, using Curve B internal area of enclosure, and total watts loss.
5. Total all of the temperature drop figures from 1. through 4. above and compare with temperature limits as established in A. above. (The sum of the individual temperature drops should always be 10 to 15
percent less than the total temperature difference to allow for hot spots and a small safety factor.)
D. The following notes concerning the curves may be of help: 1. The difference in location and slope between curves A and $B$ is empirically adjusted to approximately compensate for the difference in oil temperature under various conditions and ver ocity in oil movement at the two surfaces.
6. If a plain enclosure is used (no fins or tubes) and is painted black, and where radiation is unrestricted, Curve S may be used to determine temperature drop from enclosure to air (Curve $S$ is summation of Curves C and R).
7. If a finned tank or cooling tubes are used, it is necessary to use the total enclosure plus fin plus tube area, and Curve C to determine temperature drop by convection, but use only the envelope area and Curve $R$ to determine the temperature drop by unrestricted radiation.
NOTE: If the tank is located in direct sunlight, or near a furnace or boiler or other source of radiant energy, the radiant cooling of the enclosure will be partially offset by radiant heating from the external heat source. It is advisable to reduce the temperature drop from Curve R by $50 \%$, or sometimes not include it at all.

## References

1. "NEMA-EIA Standards for Silicon Rectifier Diodes and Stacks," NEMA Pub. No. SK-60-1963 EIA Std. RS-282 (Par. 7.09, 7.13).
2. F.W. Gutzwiller \& T.P. Sylvan, "Power Semiconductors under Transient and Intermittant Loads," AIEE Transactions, Part I, Communications and Electronics, 1960, pp. 699-706.
3. D.W. Borst, "Calculation of Rectangular Waveform Current Ratings," Rectifier News, Summer, 1967.
4. E.J. Diebold and W. Luft, "Thermal Impedance of Cooling

Fins," AIEE Transactions, Vol. 77, Part 1 (1958), pp. 739-745.
5. E.J. Diebold and W. Luft, "Transient Thermal Impedance of Semiconductor Devices," AIEE Transactions, Vol. 79, Part 1 (1961), pp. 719-726.
6. J.L. Saiers, "Optimum Cooling by Use of Finned Dissipators," Electronic Packaging and Production, Feb. 1963, pp. 10 to 14.
7. W.H. McAdams, "Heat Transmission," McGraw-Hill Book Co., Inc., New York, N.Y. (1942).

## Testing

In order to cover the area of testing SCRs, test circuit diagrams are presented with actual waveshapes expected at various points in the circuit during operation. The systems presented are not necessarily the same circu ts or systems used at IR during production and Quality Control inspection. The circuits presented here are designed for customer use to meet the same conditions and values established by IR's equipment.

International Rectifier has developed many specialized test systems. Some of these do use the circuits presented, while others use more extensive or multi-purpose circuits to meet the particular requirements of production and control procedures.

The test methods and circuits are generally those recommended by the EIA-NEMA standards for thyristors. ELA Standard RS-397 (NEMA Standard SK516-1972) as formulated by the JEDEC Solid-State Products Council in June, 1972.

Three tests which are usually performed on an SCR to ensure that it will meet the requirements of a specific application are:

1. Off-state (forward) and reverse blocking voltage.
2. On-state voltage during conduction (full-cycle average, instantaneous peak, or by a dc measurement).
3. DC triggering characteristics.

Other tests which may or may not be needed to verify that an SCR will adequately fill a particular application include:
4. Holding current
5. Latching current (as measured with a moderately long repetitive gate pulse).
6. Turn-on time into a resistive load (with or without distinction of delay and rise times).
7. Turn-on voltage in a resonant pulse circuit (often taken as an indirect measure of rate-of-rise of current capability).
8. Turn-off time under "standard" conditions (using properly gated dc supplies with a linear ramp of reapplied forward voltage).
9. Critical rate-of-rise of off-state voltage (dv/dt), with applied waveform approximating exponential as closely as possible.
10. Critical rate-of-rise of turned-on current (di/dt).
11. Thermal resistance from specified case point to "virtual junction," under steady-state dc equilibrium conditions.
Each of these parameters is discussed in relation to its test circuit on the following pages. In addition, a discussion on testing power triacs, trigger circuits, and additional comments are included at the end of this chapter.

## Parameter 1: Blocking Voltage

"Blocking voltage" is discussed in Chapter 1. It is usually determined dynamically at a specified case temperature. Peak voltage, either offstate or reverse, is determined at a given peak or full-cycle average forward or reverse leakage current. An oscilloscopic presentation is usual, so sharpness of breakdown is noted.

Figure $13-1$ shows a circuit suitable for this measurement. This circuit can test off-state and reverse blocking simultaneously, or it can show off-state or reverse characteristics alone. If the required reverse blocking capability should be appreciably different from forward, this feature is essential. Protective lamp bulbs, $\mathrm{L}_{1}$ to $\mathrm{L}_{4}$, distort waveform to a minimum, but still protect meters and transformer in the event of breakover, or disappearance of forward or reverse blocking capability.

The oscilloscope may be grounded at one side for both the vertical and horizontal inputs, with the heat dissipator to which the anode is attached floating above ground only by the few millivolts across the current shunt. The voltage divider used to produce oscilloscope
horizontal deflection can be of relatively low impedance in order to stabilize the sinusoidal waveform as a bleeder.

Peak-reading voltmeters, $\mathrm{M}_{1}$ and $\mathrm{M}_{2}$, should use high-sensitivity, taut-band microammeters; 1) to insure linear meter calibration, and 2) to allow use of small capacitors in the peak reading voltmeters, with resulting minimized clipping of peaks.

Steering diodes in series with leakage meters need not have high voltage ratings (because one meter circuit clamps the other at 3 volts or less), but, to avoid non-linearity of the leakage meters, two protective diodes, $R D_{4}$ and $R D_{6}$, should be used across the meters instead of one, with the resistors, $R_{3}$ and $R_{4}$, shown in series with the individual meters, adjusted for maximum protection of the movements with-


Figure 13-1. Blocking Voltage Test Circuit

| $\mathrm{L}_{1}-\mathrm{L}_{6}$ | Lamp Bank | $\mathrm{R}_{3}, \mathrm{R}_{4}$ | Potentiometer |
| :---: | :---: | :---: | :---: |
| $\mathrm{M}_{1}$ | Voltmeter, peak-reading, <br> "Forward Positive" | $R D_{1}, \mathrm{RD}_{2}$ | Rectifier, high voltage cartridges |
| $\mathrm{M}_{2}$ | Voltmeter, peak-reading, <br> "Reverse Negative" | $R D_{3}, R D_{5}$ | Rectifier |
| $\mathrm{M}_{3}$ | Milliammeter, highsensitivity, "Reverse Leakage" | $R D_{4}, R_{6}$ | Rectifier, 2 each, 1 amp (IR10D) |
|  |  | $\mathrm{S}_{1}$ | Switch, 2-pole, 3-throw |
| $\mathrm{M}_{4}$ | Milliammeter, highsensitivity, "Forward Leakage" | $\mathrm{T}_{1}$ | Transformer, variable, auto |
| $\mathrm{R}_{1}, \mathrm{R}_{2}, \mathrm{R}_{5}$ | Resistor | $\mathrm{T}_{2}$ | Transformer, step-up |

Figure 13-1. Blocking Voltage Test Circuit
out clipping of peaks at full-scale deflection.

Oscilloscope leads must be short, and excessive capacitance should be avoided from lead to lead, or from lead to chassis, to prevent a loop within the scope pattern. A small amount of hysteresis still is possible if the junction of the unit under test is pushed far enough into breakdown for it to increase in temperature. Every precaution should be taken to avoid ground loops.

## Parameter 2: On-state Voltage

"On-state voltage during conduction," is defined in Chapter 1. It is usually found by a half-wave test of brief duration, with the unit in a Kelvin (separate current and voltage contacts in a four-point configuration) jig of large thermal mass, to avoid excessive rise of case temperature during the test. Pulse techniques, with low pulse repetition rate and an oscilloscope readout of forward voltage versus forward current, require much less power and give forward voltages at a junction temperature quite close to the jig ambient.

Figure 13-2 shows a test circuit suitable for the usual half-wave test.

Full-cycle average on-state voltage can be read from meter $\mathrm{M}_{1}$ at a specified value of full-cycle average on-state current, read on meter $\mathrm{M}_{2}$ or peak on-state voltage can be read from a scope screen at a given peak on-state current.

The test unit must conduct for close to $180^{\circ}$ to retain the usual relationship between full-cycle average values and peak values. This requires 1) that gate signal be present from a point close to $0^{\circ}$ to a point almost at $180^{\circ}$, and 2) that peak supply voltage be much higher than the peak on-state voltage of the device under test.

Requirement 1) may be satisfied by a low impedance metered gate supply delivering ripple-free direct current, but this supply must be adjusted for each unit to insure nearly full half-cycle conduction without excessive gate dissipation. For gating without individual adjustment, this tester uses a $175^{\circ}$ wide square wave, properly phased with respect to the transformer which supplies the anode current; the output to the gate is ten volts open-circuit and short-circuit current is limited to a safe value. To obtain this gate pulse, an ac supply


Figure 13-2. On-State Voltage Test Circuit

| $\stackrel{\rightharpoonup}{\omega}$ | $\begin{aligned} & \mathrm{BD}_{1} \\ & \mathrm{~K}_{1} \\ & \mathrm{M}_{1} \end{aligned}$ | Voltage Regulator, 11 V <br> Contactor, or Wetted Mercury | $\begin{aligned} & R_{1}, R_{3} \\ & R_{4} \end{aligned}$ | Resistor <br> Resistor, Low Inductance, 50 mV Shunt | $\mathrm{RD}_{7}$ | Rectifier in a $70^{\circ} \mathrm{C}$ <br> Crystal Oven |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  | Voltmeter, Special |  |  | T1 | Transformer, Isolation |
|  |  | Voltage" | $R \mathrm{D}_{1}, \mathrm{RD}_{2}$ | Rectifier | $\mathrm{T}_{2}, \mathrm{~T}_{3}$ | Autotransformer, |
|  | $M_{2}$ | Ammeter, 50 mV DROP, "FCA | $\mathrm{RD}_{3}, \mathrm{RD}_{4}$ | Rectifier |  | Variable |
|  |  | On-State Current" | $\mathrm{RD}_{5}, \mathrm{RD}_{6}$ | Rectifier | T4 | Transformer, Stepdown, 230V, 24 V |

of high voltage feeds a power zener voltage regulator through a large dropping resistor, $R_{1}$. An isolating diode, $\mathrm{RD}_{1}$, is provided in series with the gate of the test unit.

Requirement 2) is satisfied by an ac on-state current supply of low impedance and of high enough output voltage to allow a voltage drop at peak of eight or more times the peak on-state voltage of the unit under test to appear across the series dropping resistors, $R_{2}$ and $R_{3}$. With conduction through a balancing rectifier string, $R D_{3}$ and $\mathrm{RD}_{4}$, during the $180^{\circ}$ to $360^{\circ}$ interval, the transformer secondary sees a nearly resistive load. The rating of the transformers should be several times that dictated for calculated dissipation, to avoid problems of possible saturation.

Diode isolation, by rectifier $R D_{7}$, of the on-state voltage meter, $\mathrm{M}_{1}$, is desirable, despite the working diode $\mathrm{RD}_{2}$ in the on-state circuit, to avoid the effect of possible reverse recovery spikes. The desired high front-to-back ratio of the isolating diode calls for a silicon unit. To reduce forward drop across the diode and to minimize the effect of varying ambient upon final calibration of this meter, the isolating diode, RD 7 , is housed in a $70^{\circ} \mathrm{C}$ crystal oven. The net result is a meter with a suppressed zero which reads from 0.5 volt full-cycle average to 2.0 volts and which must be hand-calibrated.

With this tester, physical layout of wiring is of prime importance. Poor layout leads to an excessive loop in the scope display and to more insidious errors. The shunt generally must be mounted directly upon the test jig. With the commonly used Hewlett Packard 120
oscilloscope, an internal ground exists at the horizontal input and the vertical input ground must not float by more than 100 millivolts. This means that the only true ground of the equipment must be at the horizontal input to the scope, although in the drawing, a ground is indicated at the scope jacks of the equipment itself. Ground shields may be used for scope connections, but the shield must not be a sensing lead (use a floating twisted pair through the shield).

## Parameter 3: DC Triggering Characteristics

"DC triggering characteristics" is discussed in Chapter 1. It can be determined by a tester such as shown in Figure 13-2, if a suitable dc gating supply is substituted for the half-wave network. The power supply which is a part of Figure $13-3$ is a suitable supply. The supply characteristics which are important are: 1) an extremely low internal impedance, 2) a low ripple voltage and 3) monitoring of gate current by a milliammeter of low constant impedance (to avoid excessive error occasioned by IR drop across the meter) and monitoring of gate voltage by a voltmeter of sufficiently high impedance so as not to draw appreciable current through the series milliammeter (if the voltmeter should be connected directly across the gate). The low impedance of the supply is necessary so the supply voltage does not drop when the unit triggers, and the low ripple of the supply output is necessary so the unit triggers at the de voltage indicated by the meter, and not a peak ripple point not shown by the average-reading voltmeter.


| $\begin{aligned} & \mathrm{BD}_{1}, \mathrm{BD}_{2} \\ & \mathrm{BD}_{4} \\ & \mathrm{BD}_{3} \end{aligned}$ | Voltage Regulator, 6.8 <br> $\mathrm{V}_{\mathrm{Z}}, 10 \mathrm{~W}$ (IR-1N2970B) | $\begin{aligned} & R_{3} \\ & R_{4} \end{aligned}$ | Resistor, 47ת, 2W, 5\% |
| :---: | :---: | :---: | :---: |
|  |  |  | Potentiometer, $1 \mathrm{~K}, 0.1 \%$ |
|  | Voltage Regulator, 12 <br> $\mathrm{V}_{\text {Z }}, 10 \mathrm{~W}$ (IR-1N2976B) |  | linear |
|  |  | $\mathrm{R}_{5}$ | Resistor, 470 , 2W, 5\% |
| $C_{1}$ | Capacitor, 4000 MF @ 15 VDC | $\mathrm{R}_{6}$ | Resistor, $25 \Omega, 10 \mathrm{~W}$ |
| $C_{2}, C_{3}$ | $\begin{aligned} & \text { Capacitor, } 2000 \text { MF @ } \\ & 15 \text { VDC } \end{aligned}$ | $\mathrm{R}_{7}$ | Resistor, $300 \Omega, 100 \mathrm{~W}$ |
|  |  | $\mathrm{R}_{8}$ | Resistor, 470, 2W, 5\% |
| DUT | Device under test | R 9 | Potentiometer, $40 \Omega, 4 \mathrm{~W}$ |
| $\mathrm{L}_{1}$ | Lamp, \#47 | RB1 | Rectifier Bridge, $400 \mathrm{~V}, 1.8$ |
| $\mathrm{M}_{1}$ | Voltmeter, $20,000 \mathrm{~V}$, sensitive multirange |  | amp (IR-18DB4) <br> Rectifier, $400 \mathrm{~V}, 1 \mathrm{~A}$ |
| $\mathrm{M}_{2}$ |  | RD1 | $\begin{aligned} & \text { Rectifier, } \\ & \text { (IR-10D4) } \end{aligned}$ |
|  | Milliammeter, multirange (max. FS "IR" drop of 50 MV or less) | $\mathrm{RD}_{2}$ | Rectifier, 300V, 6A (IR-6F80) |
| $\mathrm{Q}_{1}$ | Transistor, PNP,50V Silicon | $\mathrm{T}_{1}$ | Transformer, 115/19.5 VAC @ 3A RMS (Triad - F-600) |
| $\mathrm{O}_{2}$ | Transistor, PNP, 85W Germanium on heat sink | $\mathrm{T}_{2}$ | Transformer, 115/115 @ 50 <br> VA (Triad - N68X) |
| $\mathrm{R}_{1}, \mathrm{R}_{2}$ | Resistor, $2 \Omega, 10 \mathrm{~W}$ |  |  |

Figure 13-3. DC Triggering Characteristic Test Circuit

This technique can be ambiguous. As voltage is increased to the gate, the unit will first trigger at the peak of the half-wave dc waveform, and the voltage to the gate must be increased until the voltage across the unit just before triggering is at a specified point. To avoid this ambiguity, many customers and some military specifications call out the application of dc voltage to the anode, with a specified series anode current limiting resistor and meter. This technique is slow, because if voltage is varied rapidly, an excessive voltage requirement may be read, and if high accuracy is required, several trials may be necessary, with the anode connection broken each time to interrupt current and reset the test unit. In production screening, this technique can be quite quick if gate voltage of a specified value is applied, with a "pass" bulb included as part of the anode current limiting resistor.

An anode voltage of either 6 or 12 volts de is part of several industry standard specifications. The circuit shown in Figure 13-3 meets the requirements of a dc anode supply, but permits easy and exact adjustment, possibly with 60 Hz resetting, by use of a square anode pulse close to $180^{\circ}$ wide. The basic square wave is formed by a power zener voltage regulator, $\mathrm{BD}_{4}$, yield ing a waveform which extends approximately 6.8 volts above (positive) zero baseline and about 0.8 volts below (negative). The diode, $\mathrm{RD}_{1}$, which couples the zener voltage regulator output into a load resistor, $\mathrm{R}_{8}$, drops the 6.8 volts to approximately 6.0 volts. Potentiometer Rg is adjusted to 60 mA dc as read on a milliammeter short-
ing out the anode and cathode terminals. The lighting of lamp, $\mathrm{L}_{1}$, is a positive indication of anode triggering. The series resistor, R 9 , serves to adjust total anode load to a value (after triggering) which approximates that specified in MIL-S19500/108D.

## Parameter 4: Holding Current

"Holding current" is discussed in Chapter 1 and in Chapter 2. However, some stipulations on equipment are necessary. Certainly the supply voltage must have a value appreciably below the maximum which the device under test can normally block; for an apparatus to have general utility, this voltage must be low enough to handle all devices to be tested. In addition, the tester must provide a changing load rather than a changing supply voltage. To change the load smoothly, without generation of noise or interruption of current, even momentarily, is difficult with a commercial variable resistor, and an active element must be substituted.

Less obvious is the need for an initial anode current sufficient for full turn-on of the device. In MIL-S-19500/108B, a current of 500 milliamperes is specified. In IR production testing, a minimum current of 1 ampere is called out. Even at this level, however, high power units occasionally show evidence of incomplete turn-on.

This phenomenon generally is uncovered during a determination of dc thermal impedance. A prerequisite of this test is the determination of on-state voltage at a reference constant current (up to five amperes dc for the largest devices), with the case at a desired
maximum temperature (the assumption being that at relatively low dissipation, junction and stud temperatures are identical). Incomplete turn-on is evidenced by the fact that, as the initial turn-on current of the unit is increased, this reference on-state voltage will drop; an indication of lowered current density and thus of increased conducting cross section.

Figure 13-4 shows a circuit for a manual tester for holding current which, on the basis of complete turn-on at 0.5 ampere dc through the anode, can be used with any commercial controlled rectifier, and which meets the general requirements of MIL-S-19500/108D. The major portion of the tester is an extremely stable, hum or noise-free constant current supply, whose compliance voltage (with current regulation to a fraction of a percent) is fixed by a clamping zener voltage regulator, $\mathrm{BD}_{2}$, (outside the current-sensing loop) to six volts dc. The current through the unit under test is measured on the basis of voltage drop across a power resistor, R9, (working at a fraction of rating) connected in a Kelvin mode. While this technique of affording multiple range is deplorable in most applications, here it permits the meter range to be switched without interruption of load current. The rectifier under test is overgated to insure as complete turn-on as possible; the gate signal is the charging current of a Mylar capacitor $\mathrm{C}_{3}$, connected between the positive supply and the gate. When the PRESS TO READOUT switch, $S_{3}$, is closed, after the unit under test just drops out, a small silicon diode, $\mathrm{RD}_{1}$, is substituted for the controlled rectifier to read out the
constant current. The function of the clamping zener voltage regulator, $\mathrm{BD}_{1}$, is to assure reasonably constant thermal loading of the constant current transistor.

Figure 13-5 illustrates the shift of emphasis which must be made when a test is to be performed by production, rather than quality assurance, personnel. The tester in Figure 13-4 requires strict adherence to a specific procedure as outlined in Table XIII-I and yields quantitative data. The tester in Figure 13-5 can be used for rapid routine screening, since the criterion is simply whether a pilot lamp remains lighted after the gating button is pressed.

In the production tester, Figure $13-5$, two constant-current supplies are used, one of which is set permanently to one ampere dc, and the other is variable over any of four widespread ranges. Each supply is individually clamped by a zener voltage regulator. During gating, a minimum of one ampere anode current is supplied, which is abruptly, but smoothly, shifted down to the limit point when gate switch $S_{4}$ is open. Capacitor $\mathrm{C}_{5}$ between gate connection and negative common is necessary in perhaps five cases of a hundred; its use was permitted only after extensive evaluation and intercomparison with testers of the type shown in Figure 13-4. Whatever the capacitor's role, its presence actually improves reproducibility of permanent known standards when the tester is used quantitatively for holding current readout, with no shift from established values for these standards.

Indicator lamp, $\mathrm{L}_{2}$, intensity is consistent down to a current of a few milliamperes as a result of the


Figure 13-4. Holding Current Manual Test Circuit

|  | $\mathrm{BD}_{1}$ | Voltage Regulator, $12 \mathrm{~V}, 10 \mathrm{~W}$ | $R_{1}, R_{2}$ $R_{3}$ | Resistor, $1 \Omega$, 10 W <br> Resistor, 100 $\Omega$, 10W | $\mathrm{RD}_{1}$ | $\begin{aligned} & \text { Rectifier, } 1000 \mathrm{~V} \text {, } \\ & \text { 1A (IR - } 10 \mathrm{D} 10 \text { ) } \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | (IR - 1N2976B) | $\begin{aligned} & R_{3} \\ & R_{4} \end{aligned}$ | Resistor, $470 \Omega, 1 \mathrm{~W}, 5 \%$ | $\mathrm{RD}_{2}, \mathrm{RD}_{3}$ | Rectifier, 600V, |
|  | $\mathrm{BD}_{2}$ | $\begin{aligned} & \text { Voltage Regulato } \\ & 6.8 \mathrm{~V}, 10 \mathrm{~W} \\ & \text { (iR - } 1 \mathrm{~N} 2970 \mathrm{~B}) \end{aligned}$ |  | Resistor, $33 \Omega$, 1W, 10\% | $\mathrm{S}_{1}$ | Switch, DPST, 3A, 125 VAC "Power" |
|  | $\mathrm{C}_{1}$ | Capacitor, $1500 \mu \mathrm{~F}$, 50 VDC | $\mathrm{R}_{6}$ | Potentiometer, 100 2,10 Turn, "Current Adjust" | $\mathrm{S}_{2}$ | Switch, SPDT, Push, Button, Snap Action, |
|  | $\mathrm{C}_{2}, \mathrm{C}_{4}$ | Capacitor, $1000 \mu \mathrm{~F}$, | $\mathrm{R}_{7}$ | Resistor, 20ת, 50 W |  | "Press to Trigger" |
|  | $\mathrm{C}_{3}$ | 15 VDC <br> Capacitor, $5 \mu \mathrm{~F}$, 100V, Mylar | $\mathrm{R}_{8}$ | Potentiometer, $200 \Omega$, <br> "Calibration <br> Trimmer" | $\mathrm{S}_{3}$ | Switch, SPST, No Push Button, Snap Action, "Press to |
|  | $\mathrm{F}_{1}$ | Fuse, 2AFB | R 9 | Resistor, $2 \Omega, 10 \mathrm{~W}$, |  | Read Out" |
|  | $\mathrm{L}_{1}$ | Lamp, Neon Pilot, 115 VAC | $\mathrm{R}_{10}$ | Shunt <br> Potentiometer, $1000 \Omega$, | $\mathrm{S}_{4}$ | Switch, SPST, 1A, 125 VAC, "Meter Range: Open |
|  | M ${ }_{1}$ | Meter, $0-50 \mathrm{mV}$, 0-1 mADC Movement |  | "Calibration Trimmer" |  | 0-500 Closed $0-50$ |
|  | $\mathrm{o}_{1}, \mathrm{o}_{2}$ | Transistor (2N457A) <br> On Insulated Heat Exchanger | $\mathrm{RB}_{1}$ | Rectifier Bridge, 1.8 Amp, 600V (IR - 18DB6) | $\mathrm{T}_{1}$ | Transformer, 115 VAC/25.2 VAC @ 2A |



Figure 13-5. Holding Current Production Test Circuit

|  | $B D_{1}, B D_{3}$ | Voltage Regulator, $6.8 \mathrm{~V}_{\mathrm{z}}, 10 \mathrm{~W}$ (IR - 1N2970B) On Heat Exchanger | $\mathrm{Q}_{1}, \mathrm{Q}_{2}$ | Transistor, 2N458A, On Heat Exchanger | $\begin{aligned} & \mathrm{R}_{17} \\ & \mathrm{R}_{18} \\ & \mathrm{RB}_{1} \end{aligned}$ | Resistor, $55 \Omega$, 10 W <br> Resistor, $2 \Omega$, 10W <br> Rectifier Bridge, 7.5 Amp |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $B D_{2}$ | Voltage Regulator, $9.1 \mathrm{~V}_{\mathrm{z}}, 10 \mathrm{~W}$ (IR - 1N2974B) On Heat Exchanger | $\mathrm{O}_{3}$ | Transistor, 2N339, Insulated | $\mathrm{RD}_{1}$ | Full Wave (IR-75JB3) <br> Rectifier, 2 each, Lamp, 100V, (IR-10D10) |
|  |  |  | $\mathrm{R}_{3}$ | Resistor, $5 \Omega, 25 \mathrm{~W}$ | $\mathrm{RD}_{2}$ | Rectifier, 20 Amp |
| $\frac{1}{2}$ | $\begin{aligned} & \mathrm{C}_{1}, \mathrm{C}_{2} \\ & \mathrm{C}_{3}, \mathrm{C}_{4} \end{aligned}$ | Capacitor, 2000 MF, 50 VDC | $R_{4}$ $R_{5}$ | Rheostat, $15 \Omega, 25 \mathrm{~W}$ Rheostat, $50 \Omega, 25 \mathrm{~W}$ | $\mathrm{S}_{1}$ | Switch, DPST, 3A 125 VAC "Power" |
| ${ }_{c}^{\infty}$ | $\mathrm{C}_{5}$ | Capacitor, 33 MF , 35 VDC, <br> Tantalum | $R_{5}$ $R_{6}$ $R_{7}$ | Rhoestat, $150 \Omega, 25 \mathrm{~W}$ Rhoestat, $500 \Omega, 25 \mathrm{~W}$ | $\mathrm{S}_{2}$ | Switch, 2-Pole, 4-Position <br> Shorting, "Limit <br> Range" Pos $1=100$ <br> mADC, Pos $2=0.250$ <br> mADC, Pos $3=0-100$ <br> mADC, Pos. $4=$ <br> 0.25 mADC |
| $\stackrel{0}{2}$ | $\mathrm{F}_{1}$ | Fuse 2AFB | $\mathrm{R}_{8}$ | Trimmer, $2,000 \Omega \mathrm{Max}$. |  |  |
| $0$ | FAN | Muffin Fan, 115 VAC, 60 Hz , (Rotron) | $\mathrm{Rg}_{9}$ | Trimmer, $1,000 \Omega$ Max. |  |  |
| R |  |  | $\mathrm{R}_{10}$ | Trimmer, $500 \Omega$ Max. | $S_{3}$ | Switch, SPDT, 3A, 125 |
| 2 | $\mathrm{L}_{1}$ | Lamp, Neon, 115 VAC, "Line Pilot" | $R_{11}$ $R_{12}$ | Trimmer $50 \Omega$ Max. Resistor, $225 \Omega, 10 \mathrm{~W}$ | S | VAC, "Gate Range: <br> Closed, 400 mA |
| $\stackrel{7}{8}$ | $\mathrm{L}_{2}$ | Lamp, \#57, "Unit Triggered' | $\mathrm{R}_{13}$ | Potentiometer, $1000 \Omega$, 2W, "Adjust Lamp" |  | Max. Open, 100 mA Max. |
| $\approx$ | $\mathrm{M}_{1}$ | Meter, $50 \mathrm{MV}, 1 \mathrm{~mA}$ Movement, Scale, 0.25-100-250-1000 mADC, "Holding Current" | $\mathrm{R}_{14}$ | Potentiometer, 200 2,10 Turn, "Adjust Current" | $\mathrm{S}_{4}$ | Switch, DPST, Snap Action Push Button, "Operate Gate" |
| \% |  |  | $\mathrm{R}_{15}$ | Resistor, 20 , 10W | $\mathrm{T}_{1}$ | Transformer, $117 \mathrm{VAC} /$ |
|  |  |  | $\mathrm{R}_{16}$ | Rheostat, $15 \Omega, 50 \mathrm{~V}$ |  | 25.2 VAC @ 2A |

Table XIII-I. Holding Current Test Procedure

## Lab Procedure (Refer to Figure 13-4)

A. Press "PRESS TO READOUT" button and hold.
B. Adjust $\mathrm{Rg}_{9}$ and $\mathrm{R}_{10}$ to read 500 mA dc on Meter $\mathrm{M}_{1}$.
C. Release button.
D. Press "PRESS TO GATE" button and release.
E. Adjust "CURRENT ADJUST" potentiometer $\mathrm{R}_{6}$ until dropout.
F. Press "PRESS TO READOUT," and record reading.

## Production Procedure (Refer to Figure 13-5)

A. Adjust "ADJUST CURRENT" potentiometer for maximum.
B. Adjust Rheostats $\mathrm{R}_{4}$ thru $\mathrm{R}_{7}$ and trimmers $\mathrm{R}_{8}$ thru $\mathrm{R}_{11}$ for $10 \%$ overrange per range switch. Read on Meter $\mathrm{M}_{1}$.
C. Adjust Rheostat R 16 for 1A dc with standard meter across anodecathode, with "OPERATE GATE" switch closed and "ADJUST CURRENT" potentiometer at minimum.
D. Calibrate "HOLDING CURRENT" meter, $\mathrm{M}_{1}$, at $80 \%$ of full scale.
E. Turn "RANGE" switch $\mathrm{S}_{2}$, to appropriate range.
F. Insert device to be tested.
G. Press and release "OPERATE GATE" button.
H. Device passes if "UNIT TRIGGERED" lamp stays lit.
low dynamic impedance of the for-ward-biased rectifier, $\mathrm{RD}_{1}$ in series with the unit under test and the negative common.

Meter $\mathrm{M}_{1}$ at all times monitors the output current from the variable constant current supply. Whereas in the tester shown in Figure 13-4, and in the one ampere supply of this tester, the clamping zener voltage regulator is outside the current sensing loop, in this tester current passes from the variable supply either through the unit under test or through the clamping zener voltage regulator, $\mathrm{BD}_{3}$, of this supply; the net result is barely perceptible momentary meter needle flicker when the unit under test shuts off.

## Parameter 5: Latching Current

"Latching current" has been defined in Chapters 1 and 2 in this
book (refer to Index). There are major differences between holding current and latching current, as discussed in detail in other chapters.

In measuring holding current, the controlled rectifier is turned-on fully by over-gating to a relatively high anode current. The gate signal is called out specifically in measuring latching current. Not only may the unit not be turned-on fully, but conduction (for a minimal gate signal) may be confined strictly to the immediate vicinity of the gate, and di/dt stress (despite the low anode currents generally present), may be quite high. Dependent upon the specified gate signal, an order of magnitude spread between holding and latching current may be a signal of a faulty device design or a defective unit. (For dependable circuits, anode currents during gating should exceed latching current by a
wide margin.) In testing latching current, the gate signal should exist well beyond the usual turn-on time to insure spread of conduction.

Figure $13-6$ shows simple tester with which a standard laboratory pulse generator, constant current generator, and oscilloscope may be used to determine latching current. The wetted contact mercury relay, $\mathrm{K}_{1}$, serves three purposes economically. It acts first as an adjustable and stable free-running relaxation oscillator to establish the basic repetition rate of the test. Secondly, it provides a means of shorting the unit under test periodically by a reproducible resistance of a few milliohms for a period of time sufficient to turn off any commercial unit. Thirdly, it provides an independent trigger output of fixed amplitude and shape which can trigger the external pulse generator reliably. Since this pulse starts when the mercury string contacts 3 and 5 of the wetted mercury relay collapses, and ceases when contact 3 first meets contact 5 (although the string between contacts 2 and 3 still shorts out the unit under test for 100 microseconds or more). The external pulse generator must be capable of variable delay of the output. While numerous other commercial equipments may be used, those specified in Figure 13-6 perform quite adequately.

The sequence of shorting out, re-arming, and gating evident from the anode waveforms of Figure $13-6$, should be followed. With this arrangement, time $t_{A}$ is typically $9-10$ milliseconds. Time $t_{B}$ is set by the delay of the pulse generator and is not critical past a certain minimum point. Time $\mathrm{t}_{\mathrm{C}}$ (when the unit does not latch) is quite close to the
duration of the gate pulse. Within the limits of 1.7 pulses-per-second to 10 Hz obtained with this arrangement, time $t_{D}$ (the reciprocal of the pulse repetition rate) is not critical. The current through 1) the short imposed by the mercury-wetted reed, 2) the clamping zener voltage regulator, $\mathrm{BD}_{2}$ (which sets untriggered anode voltage at a nominal 6.8 volts de), or 3 ) the triggered unit under test (during gating or later while latched) is constant and can be measured simply by a series milliammeter of desired accuracy.

The arrangement in Figure 13-6 is effective and is useful over a wide range of triggering and latching current requirements. The equipment required is costly and its operation requires a skillful technician. Figure 13-7 shows a tester which is suitable for both production screening and for quality assurance use and which yields test results consistent with those obtained with the laboratory equipment.

A point-to-point check shows the same basic elements. A stable constant current generator is provided which extends from two milliamperes to 100 milliamperes. The meter is rescaled for ranges $0-25$ mA dc and $0-100 \mathrm{~mA} \mathrm{dc}$ in black, and $0-50 \mathrm{~mA}$ dc and $0-10 \mathrm{~V}$ dc in red. Red is "Gate Pulse." Black is "Latching Current." Calibrate $\mathrm{M}_{1}$ at $75 \%$ F.S. Use $\mathrm{R}_{5}$ to adjust 0-25 mA scale; $\mathrm{R}_{6}, 0-100 \mathrm{~mA} \mathrm{dc} ; \mathrm{R}_{21}$, $0-10 \mathrm{~V} \mathrm{dc} ; \mathrm{R}_{25}, 0-50 \mathrm{~mA} \mathrm{dc}$. The basic mercury-wetted reed circuit, $\mathrm{K}_{1}$, is incorporated. When installing $\mathrm{K}_{1}$; use \#14 copper wire from 2 and 3 to DC, a hybrid circuit, using a second mercury-wetted reed and a controlled rectifier, completes an internal pulse generator triggering


## ANODE WAVEFORMS



CONTROLLED RECTIFIER NOT LATCHED
CONTROLLED RECTIFIER LATCHED
PULSE GENERATOR: HEWLETT-PACKARD 214 A SET TRIGGER MODE TO "EXT
SLOPE TO (-) GATE INPUT TO "NORM," TRIGGER OUTPUT TO ( + ), SW. TO "PULSE DELAY, DELAY PULSE AS REQ'D FOR SEQUENCE SHOWN
CONSTANT CURRENT GENERATOR: ELECTRONIC MEASUREMENTS CORP C 631 OR EQUIVALENT

| $\mathrm{BD}_{1}$ | Voltage Regulator, $30 \mathrm{~V}_{\text {Z }}$, | $\mathrm{R}_{2}$ | Resistor, 10K, 25W |
| :---: | :---: | :---: | :---: |
|  | heat exchanger | $\mathrm{R}_{3}$ | Resistor, 2.2K, 2W, 5\% |
| $\mathrm{BD}_{2}$ | Voltage Regulator, $6.8 \mathrm{~V}_{\mathrm{Z}}$. <br> 1W (IR-1N3016B) | $\mathrm{R}_{4}$ | Resistor, 1000ת, 2W, 5\% |
|  |  | $\mathrm{R}_{5}$ | Potentiometer, linear, 0.5 K , 4W, 10 PPS to 1.7 PPS |
| $\mathrm{BD}_{3}$ | Voltage Regulator, $6.8 \mathrm{~V}_{\mathrm{Z}}$, 10W (IR-1N2970B), on heat exchanger | $\mathrm{R}_{6}$ | Resistor, $4.7 \Omega, 1 \mathrm{~W}, 10 \%$ |
| $C_{1}$ |  | $\mathrm{R}_{7}$ | Resistor, 10 $\Omega$, 1W, 1\% non-inductive |
| $\mathrm{C}_{2}, \mathrm{C}_{3}$ | Capacitor, $100 \mathrm{mF}, 50$ VDC | RB1 | Rectifier bridge, 1.8 amp , 800 V, Full Wave (IR - 18DB8) |
| $\mathrm{K}_{1}$ | Relay, wetted mercury (Clare - HGP-1002) | $\mathrm{T}_{1}$ | Transformer, isolation, 50 VA |
| $M_{1}$ | Milliammeter, DC |  |  |
| $\mathrm{R}_{1}$ | Resistor, $10 \Omega, 10 \mathrm{~W}$ |  |  |

Figure 13-6. Latching Current Laboratory Test Circuit


|  | $\begin{aligned} & \mathrm{BD}_{1} \\ & \mathrm{BD}_{2} \end{aligned}$ | Voltage Regulator, 10W, 10V, 5\% (IR - 1N2974RB) | $\begin{aligned} & F_{1} \\ & K_{1}, K_{2} \end{aligned}$ | Fuse, 2 Amp, Fast Blow Relay, Reed, Mercury- | $\mathrm{R}_{6}$ | Potentiometer, $500 \Omega$, Wirewound (See Text) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Voltage Regulator, <br> 10W, 2V, 5\% <br> (IR - 1N2984RB) | $L_{1}$ | (See Text) <br> Lamp, Neon, 115 VAC, "Power On" | $R_{7}, R_{25}$ | Potentiometer, $5000 \Omega$, Wirewound (See Text) |
|  | $B D_{3}$ | Voltage Regulator, 10W, 13V, 5\%, 2 Each, One Standard, One | $\mathrm{L}_{2}$ | Lamp, 28V, 40 mA , (No. 1918) "Out when SCR Triggered" | $\mathrm{R}_{8}$ | Resistor, 10ת, 10W, 5\% Wirewound |
|  |  | 1N2977B \& 1N2977RB) | $\mathrm{M}_{1}$ | Meter, Basic 0.200 | $\mathrm{R}_{9}$ | Resistor, $5 \Omega, 50 \mathrm{~W}$ |
|  | $\mathrm{BD}_{4}$ | Voltage Regulator, <br> 10W, 10V, 5\% <br> (IR - 1N2974B) |  | $\mu$ ADC Movement (Simpson \#29) (See Text) | $R_{10}$ $R_{11}$ | Resistor, $200 \Omega, 10 \mathrm{~W}$ Resistor, $2.2 \mathrm{~K}, 2 \mathrm{~W}, 5 \%$ |
| $\begin{aligned} & \text { A } \\ & \text { on } \end{aligned}$ | $\mathrm{BD}_{5}$ | Voltage Regulator, <br> 10W, 5.6V, 5\% <br> (IR - 10ZS5,6T5) | $\mathrm{Q}_{1}$ | Transistor, High Power, Ger. | $\mathrm{R}_{12}$ | Resistor, 1K, 10W |
|  |  |  |  |  | $\mathrm{R}_{13}$ | Resistor, $50 \Omega, 100 \mathrm{~W}$ |
|  | $B D_{6}$ | Voltage Regulator, <br> $10 \mathrm{~W}, 30 \mathrm{~V}$, <br> (IR - 1N2989) | $\mathrm{O}_{2}$ | Transistor, Unjunction (1 N2160, or equivalent) | $R_{14}$ $R_{15}$ | Resistor, $47 \Omega, 1 \mathrm{~W}, 5 \%$ Resistor, $270 \Omega, 1 \mathrm{~W}, 5 \%$ |
|  |  |  |  |  | $\mathrm{R}_{16}$ | Resistor, 150ת, 1W, 5\% |
|  | $C_{1}$ | Capacitor, 2000 mF , 25V | $\mathrm{Q}_{3}$ | Transistor, Power (RCA - 2N2339) | $\mathrm{R}_{17}$ | $\begin{aligned} & \text { Potentiometer, 10K, } \\ & 2 W, 10 \text { Turn } \\ & \text { Helical, "Adjust } \\ & \text { Gate Width" } \end{aligned}$ |
|  | $\mathrm{C}_{2}$ | Capacitor, $1000 \mathrm{mF}, 15 \mathrm{~V}$ | $\mathrm{R}_{1}$ | Resistor, $75 \Omega, 50 \mathrm{~W}$ |  |  |
|  | $\mathrm{C}_{3}$ | Capacitor, $8000 \mathrm{mF}, 75 \mathrm{~V}$ | $\mathrm{R}_{2}$ | Resistor, 250』, 10W |  |  |
|  | $\mathrm{C}_{4}$ | Capacitor, 2000 mF , 50 V | $\mathrm{R}_{3}$ | Resistor, $60 \Omega, 10 \mathrm{~W}$ | $\mathrm{R}_{18}$ | Resistor, $50 \Omega, 10 \mathrm{~W}$ |
|  | $\mathrm{C}_{5}$ | Capacitor, 0.7 MG, 200V, Mylar | $\mathrm{R}_{4}$ | Potentiometer, $1000 \Omega$, 2W, 10 Turn, Helical | $\mathrm{R}_{19}, \mathrm{R}_{23}$ | Potentiometer, $500 \Omega$, 2 W , Composition, |
|  | $C_{6}$ | Capacitor, 0.22 mF 200V, Mylar |  | "Adjust Latching Current" |  | R19-"Adjust Gate |
|  | $C_{7}$ | Capacitor, 100 mF , 150 V | $\mathrm{R}_{5}$ | Resistor, 220ת, 5W, 5\% |  |  |


with proper sequence. The output pulse has a rise time (10-90 percent) of seven microseconds and a fall time of even less, with less than five percent ringing or undershoot. Droop is less than one percent. Pulse duration can be extended from 38 microseconds to 1.34 milliseconds ( $50 \%$ level). Time $t_{B}$ is consistently $10-11$ milliseconds.

Switch $\mathrm{S}_{2}$ makes it possible to set open-circuit gate voltage (when called out) and short-circuit gate current (through the gate) on a dc basis, with meter instead of expensive oscilloscope viewing. In actual gate voltage, it may be monitored by an external 20,000 Ohms-per-Volt multimeter.

While an oscilloscope is needed initially to set gate pulse width, in performance of the test, it is not required. In place of viewing the anode waveform, a simple transistor amplifier gates a pilot lamp on when current passes through the clamp made up of zener voltage regulator $\mathrm{BD}_{5}$ and forward-biased rectifier $\mathrm{RD}_{5}$. If the controlled rectifier under test latches, current through the lamp has a low duty cycle and the lamp lights but faintly; if it does not latch, the duty cycle exceeds perhaps $90 \%$ and the lamp lights brightly.

A relatively unskilled operator may thus set gate current and voltage by simple meter readings and read out latching current readily after rotating $R_{4}$ slowly to increase current until the lamp turns off.

## Parameter 6: Turn-On Time

Turn-on time was defined in Chapters 1 and 2 in this book. The delay time portion of turn-on time is particularly important in the parallel operation of controlled recti-
fiers. If two devices operating in parallel exhibit large differences in delay time and the rate-of-rise of on-state current in the circuit is high, the device with the shorter delay time will carry a larger portion of the total current. The test circuit for measuring turn-on time is shown in Figure 13-8.

Capacitor $\mathrm{C}_{1}$ is half-wave charged through $\mathrm{RD}_{1}$ and $\mathrm{R}_{1}$. The peak voltage on $\mathrm{C}_{1}$ should be equal to the voltage rating of the test device. $\mathrm{R}_{3}$ is a non-inductive resistor whose value depends on the test current for the particular controlled rectifier.

Resistor $\mathrm{R}_{2}$ is a low impedance, non-inductive shunt. The controlled rectifier under test should be triggered during the non-charging portion of the 60 Hertz ac input, so that there will be no current flow from the input through the controlled rectifier. Circuit configuration and wiring components can change the rise time of the controlled rectifier. The circuit wiring using heavy lines must be made short and low impedance to minimize its inductance and resistance. Parts values are not given in Figure $13-8$, since these depend on ratings of thyristor under test.

## Parameter 7: Turn-On Voltage

Turn-on voltage of controlled rectifiers is commonly used as an indirect measure of rate-of-rise of on-state current capability. The principle behind measuring the voltage across the SCR during turn-on under a resonant pulse condition is that the lower the $\mathrm{V}_{\mathrm{TO}}$ (turn-on voltage), the lower the power dissipation under these conditions, and, therefore, the greater the di/dt capability the device may have. The


Figure 13-8. Turn-On Time Test Circuit


Figure 13-9. Turn-On Voltage Test Circuit
test circuit shown in Figure 13-9 is used for measuring the turn-on voltage of a controlled rectifier.

During operation, $\mathrm{SCR}_{1}$ is triggered and charges Capacitor $\mathrm{C}_{1}$ through inductor $\mathrm{L}_{2}$. The inductance $L_{2}$ causes $S_{1} R_{1}$ to resonantly commutate, therefore isolating the dc power supply from the test portion of the circuit. One millisecond after $\mathrm{SCR}_{1}$ is triggered on, the device under test is triggered, discharging $\mathrm{C}_{1}$ through $\mathrm{L}_{1}$. ( $\mathrm{R}_{1}$ is a non-inductive shunt used to determine amplitude and waveshape of the on-state current pulse). Figure $13-10$ shows a typical waveshape as seen on an oscilloscope and indicates at what instants to measure $\mathrm{V}_{\mathrm{TO}} 1$ and $\mathrm{V}_{\mathrm{TO}}$. Table XIII-II lists typical parameters during the test. Because of the high rates-of-rise of current, good instrumentation prac-
tices must be adhered to. As always, ground loops must be avoided.

## Parameter 8: Turn-Off Time

Turn-off time is defined in other chapters in this book. Figure 13-11 shows the waveshapes associated with this test. Figure $13-12$ is a diagram showing the basic modules required to construct a turn-off time tester. The high current onstate and reverse module is used to supply principal current for the test device. The linear $\mathrm{dv} / \mathrm{dt}$ module supplies a linear ramp of voltage to the test device at a variable time after the test device has been triggered. The sequential triggering module controls the duty cycle and time relationship between the high current on-state and reverse module and linear dv/dt module.

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on-state voltage (Volts)

Figure 13-10. Typical Turn-On Voltage Waveform

Table XIII-II. Typical Turn-On Voltage Test Parameters (For 35A to 50A Thyristors


The on-state and reverse current supply is shown in Figure 13-13. Capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ are charged up to approximately 200 volts. Thyristors $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$ control the pulse width of the on-state current. This is accomplished by changing the triggering of $\mathrm{SCR}_{2}$. In other words, triggering $\mathrm{SCR}_{2}$ reverse biases the controlled rectifier under test causing $\mathrm{SCR}_{1}$ to commutate off. Using this scheme, pulse widths from 10 microseconds to about 150 microseconds are available. The pulse width can be further increased if capacitors $\mathrm{C}_{1}$ and $\mathrm{C}_{2}$ are increased.

Turn-off time is affected by reverse recovery currents. By definition, the controlled rectifier under test should be reverse-biased until


Figure 13-12. Turn-Off Tester - Block Diagram
the reapplication of forward blocking voltage occurs. To accomplish this, the reverse recovery time of the diode in series with the test device must be variable so that the diode reverse recovery characteristic can be matched to the turn-off time of the controlled rectifier under test. Figures 13-14 and 13-15 show a method to vary the reverse recovery characteristic of the circuit. Diodes having a wide range of recovery times are mounted in a coaxial configuration utilizing two devices in series per recovery diode. The recovery time of the circuit can be varied by switching in the discrete recovery diodes (A, B, C, D, E , or F ) singly or in various parallel combinations, so that a configuration is obtained which more nearly matches the turn-off time of the test device.

The parallel combinations of recovery diodes provided by the two selector switches in Figure 13-14 are shown in Table XIII-III.

The circuit for the reapplied linear dv/dt is shown in Figures 13-16 and 13-17. The linear dv/dt section can be broken down into three parts. Figure 13-16 shows the con-
stant current and high voltage supply. Figure 13-17 shows the switching section, which is the most critical and must be designed in a noninductive configuration. The linear $d v / d t$ is generated by charging the dv/dt capacitors with a constant current. In this case, the dv/dt capacitors are charged up to the voltage rating of the device by the high voltage power supply (Figure 13-16) through half the full wave bridge and 80 millihenry choke of the constant current supply. The charging rate of the $\mathrm{dv} / \mathrm{dt}$ capacitors is determined by the current flow through the choke of the constant current supply. The level of the constant current supply can be varied by $R_{1}$ and $R_{2}$, which changes the $\mathrm{dv} / \mathrm{dt}$ stress level during turn-off. The fast-recovery diodes are necessary to assure that the current for the $\mathrm{dv} / \mathrm{dt}$ capacitors flows through the 80 millihenry choke. If fast recovery diodes are not used in this portion of the circuit, when $\mathrm{SCR}_{4}$ and $\mathrm{SCR}_{5}$ are switched on, current will flow through the diodes until the devices recover. At this time, there will appear across the test device a step

$\mathrm{C}_{1}, \mathrm{C}_{2}$ Capacitor, $1300 \mathrm{mF}, 350 \mathrm{~V}$
$\mathrm{R}_{1}, \mathrm{R}_{3}$ Resistor, 1000 $\Omega$, 200W
$\mathrm{R}_{2}$ Resistor, $0.5 \Omega, 1220 \mathrm{~W}$ ( GE - C5B50)
$\mathrm{R}_{4}$, R5 Resistor, variable, 0.25 to $12 \Omega, 2.250 \mathrm{~V}$ (Allen-Bradley-Carbon Pile Form SM), R4 "ADJ. Itm," R5 "ADJ. Irev.' Resistor, 16 each, $100 \Omega$, 2W, 5\% (Magic 16)
minimum inductance configuration
$\mathrm{R}_{7}$ Resistor, shunt, $0.01 \Omega$, 50W, 1\% (T\&M Modified -F-500-2)
R8 Resistor, Shunt, $0.01 \Omega$, non-linear
$\mathrm{SCR}_{1}, \quad \mathrm{SCR}, 70 \mathrm{amp}, 800 \mathrm{~V}$
$\mathrm{SCR}_{2}$ (IR - 72RA80)
$\mathrm{SCR}_{3} \mathrm{SCR}, 150 \mathrm{amp}, 800 \mathrm{~V}$ (IR - 150RA80)

Figure 13-13. Turn-Off Tester - On-State and Reverse Current Module
of voltage that is three or four times the dv/dt desired. This step of $\mathrm{dv} / \mathrm{dt}$ will depend on the recovery time of those diodes. The longer the recovery time, the higher its amplitude, and a greater rate of rise of the dv/dt initially. Therefore, it is best to use the fastest recovery device that can handle the required current of 7 to 8 amperes.

The third module is the sequential triggering module that determines the time relationships between the high current and linear dv/dt module (see Figure 13-18). The duty cycle of the sequencing network is controlled by a linesynchronized unijunction triggering
circuit which triggers $\mathrm{SCR}_{6}$. (The triggering of $\mathrm{SCR}_{6}$ must be accomplished when capacitor $\mathrm{C}_{3}$ is not being charged.) Capacitor $\mathrm{C}_{3}$ now acts as a power source for three unijunction circuits and $\mathrm{C}_{4}$. The charging of $\mathrm{C}_{4}$, occurring when $\mathrm{SCR}_{6}$ is triggered on, causes a trigger pulse to appear at the gate of the test device. This is considered time zero. At time $t_{1}$, $Q_{2}$ triggers. The pulse of $\mathrm{Q}_{2}$ triggers $\mathrm{SCR}_{2}$ which determines the on-state current pulse duration. The on-state current pulse duration is controlled by a $1 \mathrm{~K}, 2$-watt potentiometer, $\mathrm{R}_{13}$. At some time later $\mathrm{t}_{2}, \mathrm{Q} 3$ triggers. The trigger pulse from Q3


Figure 13-14(a). Turn-off Tester-On-State Module-Construction Techniques


| $\mathrm{K}_{1}$ | Relay Network, 110 VAC <br> coils. UHF conductor (Dow- <br> Key - DKC71-SP6T Rating) | $\mathrm{S}_{1}$ | Rotary Switch, 10-position, 2 <br> disc, "units" (Centralab- <br> 2513, 2P10T N.S. SW) |
| :--- | :--- | :--- | :--- |
| RD $_{1}$Rectifiers, reverse recovery, <br> bank of 6 series pairs | $\mathrm{S}_{2}$ | Rotary Switch, 10-position, <br> (tens" (Centralab - 2505, |  |
|  |  | 2P4T N.S. SW) |  |

Figure 13-14(b). Turn-Off Tester-On-State Module-Construction Techniques


Figure 13-15. Turn-Off Tester-On-State Module-Construction Techniques




| $\mathrm{C}_{1}$ | Capacitor, $0.25 \mathrm{mF}, 2 \mathrm{KV}$ |
| :---: | :---: |
| $\mathrm{C}_{2}$ | Capacitor, $0.10 \mathrm{mF}, 2 \mathrm{KV}$ |
| $\mathrm{C}_{3}$ | Capacitor, $0.05 \mathrm{mF}, 2 \mathrm{KV}$ |
| $\mathrm{C}_{4}$ | Capacitor, $0.02 \mathrm{mF}, 2 \mathrm{KV}$ |
| $\mathrm{R}_{1}$ | Resistor, 9 each, $100 \mathrm{~K}, 2 \mathrm{~W}$, $5 \%$ in minimum inductance configuration |
| $\mathrm{S}_{1}$ | Switch, 5-position rotary (Centralab - JV9001) "dv/dt caps," Pos. 1 "0.02 mF ," etc. |
| $\mathrm{SCR}_{4}$, <br> $\mathrm{SCR}_{5}$ | SCR, $70 \mathrm{amp}, 1200$ volts (IR-81RL120) low inductance fixture |

Figure 13-17. Turn-Off Tester - dv/dt Module - Switching Section

Table XIII-III. Switch Positions for Turn-Off Tester

|  | RECOVERY DIODE SWITCHED FOR: |  |
| :---: | :---: | :---: |
| SWITCH | "UNITS" | "TENS" |
| POSITION | SWITCH | SWITCH |
| 0 | Open | Open |
| 1 | A | E |
| 2 | B | F |
| 3 | C | E \& F |
| 4 | C \& B |  |
| 5 | D |  |
| 6 | D \& A |  |
| 7 | D \& B |  |
| 8 | D \& C |  |
| 9 |  |  |

triggers $\mathrm{SCR}_{4}$ and $\mathrm{SCR}_{5}$ (Figure 13-17), which are the reapplied $\mathrm{dv} / \mathrm{dt}$ controlled rectifiers. The time relationship between $\mathrm{Q}_{2}$ and $\mathrm{Q}_{3}$ is determined by a $2.5 \mathrm{~K}, 2$-watt, single potentiometer, $R_{17}$, and a 500 -Ohm, 10 -turn current helipot, $\mathrm{R}_{16}$. The 10 -turn helipot is used so that very fine adjustments can be made between $t_{1}$ and $t_{2}$. Q4 triggers $\mathrm{SCR}_{7}$ and completes the cycle. $\mathrm{SCR}_{7}$ completely discharges $\mathrm{C}_{3}$ so
that there is no longer a voltage supply for the other trigger circuits. The discharge pulse of $C_{3}$ triggers $\mathrm{SCR}_{3}$ (Figure 13-13) which crowbars the high current on-state module and sets the conditions for the beginning of the next cycle.

The turn-off time tester is a complex piece of test equipment, and only by rigorously following schematics, can a tester be built that repeats turn-off time readings


Figure 13-18(a). Turn-Off Tester-Sequential Triggering Module


Figure 13-18(b). Turn-Off Tester-Sequential Triggering Module

and correlates with users and manufacturers throughout the industry.

## Parameter 9: Critical dv/dt

The term "critical rate-of-rise of forward voltage," or "critical dv/dt," has been interpreted several ways by the industry. These are discussed in detail in Chapter 1 of this book. The actual dv/dt and at what fraction of peak applied offstate voltage it is measured is important to the designer and user of controlled rectifier circuits. The manufacturer can test dv/dt by one of two techniques: he can generate the applied dv/dt by a circuit which produces a linearly rising sawtooth, or a circuit which produces an exponentially rising sawtooth. At low rates of dv/dt, this latter is easy to produce; primarily for this reason, the industry standardized upon this waveform when only low dv/dt-re-
sistant controlled rectifiers could be made. Its use has remained to plague both manufacturer and user because of its inclusion in military specifications. In Figure 13-19(a), an idealized test circuit is shown which appears in several military specifications. Figure 13-19(b) shows the voltage curve which results when a capacitor is charged through a resistor from a constant voltage source. In graph (c), the instantaneous dv/dt present at any point of this voltage curve has been plotted as a fraction of the maximum dv/dt (which occurs at time zero).

Note that the particular relationship of $\mathrm{dv} / \mathrm{dt}$ to applied forward voltage at any point can only be reproduced when the curve is truly exponential and follows the equations shown in these two graphs. Correlation problems occur when

(a) Ideal Test Circuit

Figure 13-19. dv/dt Test Circuit and Waveforms

(b) VOLTAGE

(c) DV/DT

Figure 13-19. dv/dt Test Circuit and Waveforms
either the manufacturer or the user disregards a particular convention promulgated by both manufacturer and military, By this convention, $\mathrm{dv} / \mathrm{dt}$ is defined for a true exponential waveform as given in Formula 13-A.

$$
\begin{array}{r}
\text { "Critical dv/dt" }= \\
\frac{0.632 \mathrm{~V}_{\text {supply }}}{\mathrm{R}_{\text {test }} \mathrm{X} \mathrm{C}_{\text {test }}} \tag{13-A}
\end{array}
$$

This presumably was arrived at by assuming the exponential waveform to be linear from zero time to one time constant. Since the instantaneous dv/dt (that value which will determine capacitive charging current) varies from $157 \%$ of this "critical dv/dt" at zero time to $58 \%$ at one time constant, the designer can only use this figure as a relative order of merit when comparing two controlled rectifiers, and his incoming inspector must use equipment which satisfies all the requirements of the exponential waveform.

## Requirements

In the test circuit of Figure 13-19, to obtain an exponential curve which does not show error when viewed upon a suitable laboratory oscilloscope,
A. Capacitor $\mathrm{C}_{1}$ must be a minimum of 99 times as great in capacitance as $\mathrm{C}_{2}$.
B. The time constant $\mathrm{R}_{2} \mathrm{C}_{2}$ must be at least 4.6 times the maximum test period (to achieve full $\mathrm{V}_{\mathrm{S}}$ across $\mathrm{C}_{2}$ ).
C. Capacitor $\mathrm{C}_{2}$ must have a value of at least 0.02 microfarad for the curve not to be influenced by the middle junction capacitance of the unit under test (appreciably higher values for $\mathrm{C}_{2}$ make switch increments ex-
tremely difficult and for high $\mathrm{dv} / \mathrm{dt}$ values require absurdly low values of $\mathrm{R}_{2}$ ).
D. Inductance within the capacitor charging loop (for extremely high values of $\mathrm{dv} / \mathrm{dt}$ ) must be kept to a very small fraction of a microhenry, to avoid distortion of the initial portion of the exponential curve.
E. The series switch must operate instantaneously and with no appreciable voltage drop.
This last requirement rules out the use of controlled rectifiers for exponential $\mathrm{dv} / \mathrm{dt}$ testers used at dv/dts of above about 400 volts per microsecond. Such testers do check $\mathrm{dv} / \mathrm{dt}$ but do not reproduce the exponential waveform, and results obtained must be corrected extensively. An error can also be introduced at low dv/dts when an oscilloscope is used to adjust peak offstate voltage, which may not be equal to supply voltage because of dropout of the SCR switch when charging current reaches the holding current level. Supply voltage, and not peak off-state, is called out.

The detailed sketches and schematic of Figure $13-20$ show how to make a true exponential dv/dt tester which has been used up to 1000 volts and a "critical dv/dt" of above 6000 volts per microsecond. It introduces some interesting techniques of field cancellation employed at International Rectifier. The pressure upon graphite discs within the cylindrical coaxiallycoupled carbon resistor, $\mathrm{R}_{4}$, is increased until the series milliammeter, $\mathrm{M}_{1}$, shows consistent fullscale excursion; the pressure is then decreased gradually until meter fluctuations just cease and the time constant (the time from zero volts




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Figure 13-20. True Exponential dv/dt Test Circuit
to a voltage $63.2 \%$ of the supply voltage) is read out by use of a very fast oscilloscope.

Peak currents through the mer-cury-wetted contact relay are several times greater than those recommended by the manufacturer. The applied voltages are also much higher than recommended. The connection of contacts is unorthodox. This relay is a make-before-break (Form D) unit, and in this circuit switching occurs only during bridg-
ing (when the coil is either energized or deenergized). This mode of operation has yielded rise times (with properly non-inductive external circuits) of a very few nanoseconds, with a closed switch duration of about 400 microseconds, and relays have lasted an average of six months.

Parameter 10: Critical di/dt
Critical di/dt is discussed in Chapter 1 (refer to Index). The
basic test circuit schematic and onstate current waveshapes are shown in Figure 13-21. The following conditions are specified:
A. The time $t_{1}$ shall be $\geqslant 1$ microsecond.
B. ITM shall be $\geqslant$ twice the rated value of on-state current at $\mathrm{T}_{3}$. (The rated value of on-state current at $T_{3}$ will be an average [ $T_{3}$ is case temperature where derating of average on-state current starts] value for ac rated devices and a dc value for dc rated devices.)
C. The pulse repetition rate shall be 60 pps.
D. The off-state voltage $\mathrm{V}_{\mathrm{DM}}$ shall be equal to the rated value at $\mathrm{T}_{5}$ ( $\mathrm{T}_{5}$ is maximum operating temperature).
E. The temperature shall be $25^{\circ} \mathrm{C}$.

F . The gate trigger pulse shall be specified as to:

1) Pulse width, $t_{w}$.
2) Rise time, $t_{r}$
3) Gate source voltage and resistance.
G . The test duration shall be:
4) 1000 hours to establish the repetitive rating.
5) 300 on-state current pulses to establish the gate-triggered non-repetitive rating.
di/dt ratings given at power frequencies $(50-60 \mathrm{~Hz})$ do not necessarily reflect the inrush capabilities of the same device at high frequency (above 400 Hz ), because of the greater cumulative effect of the turn-on losses at higher repetition rates. Thus, this is only a test of device capability to handle fast rising current pulses of short duration at power frequencies. It is a figure of merit and can be used to compare one device with another.

Current capabilities at specific repetitive values of di/dt and other concurrent test conditions are often


Figure 13-21. Critical di/dt Test Circuit and Waveform
included on data sheets for those SCRs intended for inverter applications.

Parameter 11: Thermal Resistance
Thermal resistance is discussed in detail in Chapter 1. A block diagram of the test circuit used for the measurement of thermal resistance is shown in Figure 13-22. The junction of the device under test is heated by a direct on-state current having an RMS ripple content of $5 \%$ or less, which is passed continuously through the device under test except for a 400 microsecond period every 0.167 seconds or more. During this 400 microsecond period, the junction temperature is measured by reducing the on-state current to a small fixed value and measuring the on-state voltage. Current and on-state voltage waveshapes are shown in Figure 13-23.

A calibration point along the curve of on-state voltage vs. junc-
tion temperature is used to convert the on-state voltage reading to a junction temperature. In addition, the case temperature of the device under test is measured by a thermocouple. DC thermal resistance is calculated using the relationship in Formula 13-B.
$R_{\theta J C}=\frac{T_{J(M A X)}-T_{C}}{V_{T M ~ X ~ I H E A T ~}}$
Where:
$\mathrm{V}_{\mathrm{TM}}=$ On-state voltage
IHEAT $=$ Heating current
Control of the heating current through the device under test is accomplished by $\mathrm{SCR}_{1}$ and $\mathrm{SCR}_{2}$, which function as a dc flip-flop. Switching is at a 60 hertz repetition rate to facilitate oscillographic observations. Current is carried by $\mathrm{SCR}_{1}$ only during the 400 microsecond periods that heating current is not flowing through the device


Figure 13-22. Thermal Resistance Test Circuit


Figure 13-23. Thermal Resistance Test Waveforms
under test, and so $\mathrm{SCR}_{1}$ may be considerably smaller than $\mathrm{SCR}_{2}$.

The value of heating current selected should be large enough to create significant heating in the device under test. Inductances in the heating current power supply and circuit wiring make it possible to abruptly turn this current off without creating transient voltages which interfere with the measurement being made.

Instead, a diverter circuit consisting of rectifier diodes $\mathrm{RD}_{1}$ through $\mathrm{RD}_{4}$ is provided so that the heating current is not interrupted by $\mathrm{SCR}_{2}$, but simply switched to a different path. The inductor, $\mathrm{L}_{1}$, is included to make it certain that the heating current is not varied while it is being switched from
one path to another. This inductor also serves to reduce to a negligible value undesired flow of current from $\mathrm{C}_{1}$ through the device under test and the heating current power supply.

The measuring current which remains flowing through the device under test must be held at a fixed value during the 400 microsecond interval when the heating current is diverted by $\mathrm{SCR}_{1}$. During this measuring interval, the impedance of the controlled rectifier under test is not constant. To assure a constant measuring current, a low level constant-current supply is used. Fast recovery diode $\mathrm{RD}_{6}$ prevents any voltage from capacitor $\mathrm{C}_{1}$ from damaging the low level supply. In addition, the value of meas-
uring current used must be several times the holding current for the device under test, but at the same time, must be low enough not to cause significant junction heating.

The junction temperature ideally must be measured at the exact instant that the heating current is switched to the diverting diodes. This is not possible, as it is first necessa\%y for the carriers in excess of those needed to support the measuring current (carriers injected in the semiconductor by the heating current) to be dissipated. Until this takes place, the on-state voltage of the device under test is not a true measure of its junction temperature. In addition, if the case of the device is fabricated from magnetic parts, the collapsing magnetic flux in the case may induce a voltage which will distort the on-state voltage reading. Furthermore, the action of the capacitor $\mathrm{C}_{1}$ on turning off $\mathrm{SCR}_{2}$ may influence the onstate voltage of the device under test. These spurious effects on the on-state voltage will disappear after a brief interval, in the order of 200 microseconds, $t_{2}$ in Figure 13-23. It is therefore possible to measure junction temperature at $\mathrm{t}_{2}$ to $\mathrm{t}_{3}$ and the value obtained at $\mathrm{t}_{2}$ will be essentially the same as the junction temperature immediately after the flow of heating current ceases ( $\mathrm{t}_{1}$ in Figure 13-23)

In order to accurately read the on-state voltage at the items specified, a cathode ray oscilloscope is used as a null balance, and the forward voltage drop at any desired instant is balanced against the voltage fed from a potentiometer connected across a low voltage source. The voltage used to create this balance is then read by a voltmeter.

The calibration of the on-state voltage due to the low-level measuring current against junction temperature is obtained by placing the device under test in an oven and measuring on-state voltage at a temperature (usually $125^{\circ} \mathrm{C}$ ), which is equal to, or higher than, the maximum allowable operating temperature for the device under test, but which is less than a temperature at which the device may be damaged. If the maximum safe temperature is not known, the maximum allowable storage temperature for the device may be used as the calibration temperature. When initiating the flow of low-level measuring current through a device being calibrated, increase the forward current to a value equal to approximately $67 \%$ of the nominal average current rating of the device under test, to be sure it is fully turned-on. Then reduce the current to the value of low-level measuring current being used.

A special jig, which accommodates a thermocouple is mounted to, or a small hole for the thermocouple is drilled in, the hex base of the device under test, or a hole is drilled in the side of one of the pole pieces if a Hockey-Puk type device is to be measured. This thermocouple is used to measure case temperature.

The magnitude of the heating current used should be sufficient to cause a substantial difference betweęn the junction and case temperatures of the DUT. This will increase the accuracy of the test results, since a small error in reading either the case or junction temperature will have very little effect on the value obtained for the temperature rise of the junction above
the case. If the case of the DUT is cooled well (water cooling is recommended), it is possible to use a large value of heating current and hence obtain a large difference between junction temperature and case temperature without running the danger of overheating the junction of the DUT.

When measuring the temperature of the junction during the brief intervals, the DUT is conducting the low-level measuring current, it is not possible to make the measurement exactly when it is desirable to do so which is at the exact instant when the high-level forward current ceases. At that instant, the forward voltage of the DUT is abnormally low (which would indicate a junction temperature much higher than is actually the case), because recombination of minority carriers is taking place. In addition, some semiconductor devices exhibit inductance, and therefore produce, for a brief instant, a voltage which tries to prevent the current from decreasing. This voltage tends to cancel out the forward voltage of the DUT, again resulting in too low a forward voltage at the instant the high-level current ceases. After approximately $100 \mu \mathrm{sec}$, these transient voltage effects disappear in most semiconductor devices, and the actual junction temperature is then able to be measured.

A small amount of cooling of the junction will take place during the interval when junction temperature cannot be read, and therefore, a refinement of the test method is to extrapolate the curve of forward voltage vs. time during the measuring interval back to the instant the high-level current ends. A straight line extrapolation is a close approx-
imate. The approximate junction temperature at exactly the end of conduction of high level current can then be obtained from the forward voltage determined by extrapolating back.

Further details on how to conduct this test for thermal resistance are found in JEDEC Publication No. 88, "Thermal Resistance and (Transient) Thermal Impedance Test Methods for Stud- and BaseMounted Rectifier Diodes and Thyristors," which is available from the Electronic Industries Association, 2001 Eye St., N.W., Washington, D.C. 20006.

In building the test circuit shown in Figure 13-22, inductance must be minimized in those portions of the circuit drawn with heavy lines. Figures 13-24, 13-25, $13-26$, and $13-27$ are detailed schematics showing the power supply module and all the associated circuitry and systems.

## Testing Power Triacs

The testing of a power triac as compared to that for a power controlled rectifier becomes somewhat more involved. Parameters of triacs are discussed in Chapter 1 (refer to Index). Since the triac must be tested bi-directionally under certain conditions, it is often more difficult to arrange the circuitry, especially in the case of large power triacs, to yield irrefutable data.

One of the basic tests, of course, is for current rating. Although a computer program can be (and is being) used to determine current ratings of power triacs, certain basic inputs are necessary for meaningful results. One must be able to measure thermal impedance accurately in order to properly calculate the









| $B_{1}, \mathrm{BD}_{2}$, | Voltage Regulator, | $\mathrm{Q}_{1}$ | Transistor (2N1256) | $\mathrm{R}_{14}, \mathrm{R}_{15}$ | Resistor, 47 , 2W, 5\% |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | $(I R-1 N 3031 B)$ | $\mathrm{O}_{2}, \mathrm{O}_{3}$ | Unjunction <br> Transistor (2N2160) | $\mathrm{R}_{16}, \mathrm{R}_{22}$ | Resistor, 47 ${ }^{\text {, 1W, 5\% }}$ |
| $B D_{4}, B_{5}$ | Voltage Regulator, $47 \mathrm{~V}_{\mathrm{Z}}$, 10W (IR - 1N2994B) | $\mathrm{R}_{1}$ | Resistor, $20 \Omega, 25 \mathrm{~W}$ | $\mathrm{R}_{17}$ | Resistor, 1.0K, 2W, 5\% <br> Resistor, 300 $\Omega$, 2W, 5\% |
|  |  | $\mathrm{R}_{2}, \mathrm{R}_{3}$ | Resistor, $500 \Omega$, 20W | RB1 | Rectifier Bridge, |
| $B D_{7}, B_{9}$ | Voltage Regulator, $10 \mathrm{~V}_{\mathrm{Z}}, 1 \mathrm{~W}$, (IR - 1 N 3020 B ) | $\mathrm{R}_{4}$ | Resistor, 2000 ${ }^{\text {, 10W }}$ |  | 4 Each, 1 Amp 1000 V (IR - 10D10) |
|  |  | $R_{5}, R_{18}$ | Resistor, 1.5K, 2W, 5\% | $\mathrm{S}_{1}$ | Switch SPST, 3A, 125V |
| BD10 | Voltage Regulator | $\mathrm{R}_{6}$ | Resistor, 2.0K, 2W, 5\% |  | Labeled "Power" |
| BD11 | Voltage Regulator | $\mathrm{R}_{7}, \mathrm{R}_{8}$ | Resistor, $500 \Omega, 50 \mathrm{~W}$ | $\mathrm{S}_{2}$ | Switch DPDT, 3A, 125V |
| $\mathrm{C}_{1}, \mathrm{C}_{2}$ | Capacitor, 140 mF , 200 VDC (Sprague 32D1121T) | $\mathrm{R}_{9}$ | Resistor, 4.7K, 1W, 5\% | S3 |  |
|  |  | $\mathrm{R}_{10}, \mathrm{R}_{20}$ | Potentiometer, 30K, 10 Turn Labeled R10 $=$ | $\mathrm{S}_{3}$ | (Centralab - 2515) |
| $\mathrm{C}_{3}, \mathrm{C}_{4}$ | Capacitor, 50 mF , 50 VDC, (Sprague -TE-1307) |  | Turn Labeled $\mathrm{R}_{10}=$ "Fine, $\mathrm{R}_{20}=$ " Pulse Width" |  | Labeled "Type Pulse" $1=\text { "Off", } 2=" \mathrm{On}^{\prime \prime}$ |
| $\mathrm{C}_{5}$ |  | $\mathrm{R}_{11}$ | Resistor, 2.7K, 1W, 5\% | $\begin{aligned} & \mathrm{SCR}_{1}, \\ & \mathrm{SCR}_{2} \end{aligned}$ | SCR, 7.4A, 500V <br> (IR - 2N1778- |
|  | Capacitor, 0.3 mF , 400 V , Mylar | $\mathrm{R}_{12}$ | Potentiometer, 9 Each, 27K, |  | Specially Selected) |
| $\mathrm{C}_{6}$ | Capacitor, 0.2 mF , 400V, Mylar |  | 1W, 10\% Resistors Mounted On Switch (Centra-lab-25021P11TSH) | $\mathrm{T}_{1}, \mathrm{~T}_{2}$ | Transformer <br> (Sprague - 31Z286) |
| $\mathrm{F}_{1}$ | Fuse (3AFB) | $\mathrm{R}_{13}, \mathrm{R}_{19}$ | Resistor, $270 \Omega, 1 \mathrm{~W}, 5 \%$ | $\mathrm{T}_{3}$ | Transformer <br> (Sprague - 3Z209) |

device rating. The ratings so calculated can then be verified by tests in order to establish the accuracy of the program. Since only a portion of the triac is dissipating heat during each conduction half cycle, and since the total silicon chip is a homogeneous thermal mass, accurate theoretical thermal impedance determinations are impossible. A test circuit was derived in order to measure this thermal impedance accurately using junction temperature and device base temperature measurements as absolute quantities. This circuit is shown in Figure 13-28.

By supplying three power sources to the test device, a single circuit can be used to obtain three ratings:
A. Bi-directional thermal impedance.
B. Dynamic current rating.
C. Bi-directional surge current rating.
By substituting a source of low ampere level test current for the surge current source shown in Figure 13-28, the bi-directional apparent thermal impedance can be obtained. If the device is brought to a steady-state operating current with the power "current source" and the forward voltage of the device has been previously measured by interrupting the main current and gating on $\mathrm{SCR}_{1}$ or $\mathrm{SCR}_{2}$. (Interruption of the main current can be achieved by gating on $\mathrm{SCR}_{6}$, thus removing the gate signal from $\mathrm{SCR}_{4}$.) The current source of known magnitude then yields a forward voltage for the device under test during this test half cycle (which can be read on a differential input to an oscilloscope to give an accurate reading). Knowing, from previous calibration
what the device forward voltage vs. temperature is at this current level, will yield an accurate reading of junction temperature. By monitoring device base temperature, both effective thermal resistance and dynamic current rating can be calculated.

The same general test circuit can be used to determine surge current rating. By using the circuit shown in Figure 13-28, the device can be brought to maximum operating conditions by means of the power current source, a surge current can be superimposed at the desired time for a predetermined duration by means of the surge current source and at the end of this surge, the ability fo the device to block voltage can be determined by turning on $\mathrm{SCR}_{5}$ and $\mathrm{SCR}_{6}$.

## Triggering Circuits

Triggering thyristors is discussed in many places in this book (refer to Index for locations). Often it is desirable to trigger a controlled rectifier at a point within a very few degrees of the start of a 60 Hz sine wave. On a 60 Hz basis, this can be done readily by a sine wave from a high ac supply voltage, clipped by a zener voltage regulator fed from the supply through a large dropping resistor, with diode isolation of the gate. This technique is used in the circuit of Figure 13-29.

In many tests, however, this gating must be done on a single shot basis, with a gate pulse present for a portion of one positive half-cycle, within a very few degrees of the start of the cycle. In other tests, instead of a single shot basis, repeated manually at a low and random repetition rate, low repetition rate triggering must be automatic


CIRCUIT USED FOR:
A) BI-DIRECTIONAL THERMAL IMPEDANCE
B) DYNAMIC CURRENT RATING
C) BI-DIRECTIONAL SURGE CURRENT RATING


| BD | Voltage Regulator, $51 \mathrm{~V}, 1 \mathrm{~W}$ (IR-3037B) | $\begin{aligned} & \mathrm{R}_{3} \\ & \mathrm{RD}_{1} \end{aligned}$ | Resistor, 47 $\Omega$, 1W, 5\% Rectifier |
| :---: | :---: | :---: | :---: |
| $\mathrm{C}_{1}$ | Capacitor, $1 \mu \mathrm{~F}, 1000 \mathrm{VDC}$ |  | Rectifier, 1000V, 1A |
| $\mathrm{C}_{2}$ | Capacitor, $0.1 \mu \mathrm{~F}, 200 \mathrm{VDC}$ |  | (IR - 10D10) |
| $\mathrm{R}_{1}$ | Resistor, 1000 ${ }^{\text {, }} 100 \mathrm{~W}$ | $\mathrm{S}_{1}$ | Switch SPDT, pushbutton, snap action, "press to trigger" |
| $\mathrm{R}_{2}$ | Resistor, 47ת, 2W, 10\% | $\mathrm{T}_{1}$ | Transformer, pulse. |

Figure 13-29. Single Shot Triggering Circuit
and highly reproducible. This latter circumstance is essential where energy is stored in a capacitor bank, charged on alternative negative half-cycles, and discharged rapidly over a small portion of a single positive half-cycle, since it governs the dissipation rating of components.

A circuit which has been used often, with or without amplification, to trigger a thyratron or a controlled rectifier close to zero cross-over on a single-shot basis is shown in Figure 13-30. Its performance depends critically upon the characteristics of the pulse transformer and upon the gate triggering characteristics of the unit to be triggered.

Table XIII-IV shows some typical pulse transformers used in test equipment at International Rectifier. For minimum delay of peak pulse after zero cross-over, an otherwise suitable unit of low OCL (open-circuit primary inductance)
and minimum rise time would be specified. Volt-microsecond product is a measure of energy which can be passed by the transformer before core saturation. For small pulse transformers with an OCL of two millihenries or less, the typical volt-microsecond product is too low to trigger a run-of-mill high current controlled rectifier properly, and triggering under such conditions (wherein only a small portion of the active area of the unit is turned on) could lead to di/dt failure. With a pulse transformer with an OCL of 5 millihenries or so, and a volt-microsecond product of 300 or more, most units of 25 amps RMS rating or less can be turned on properly, if the anode voltage is high enough and load impedance is low enough for latching current limits to be met.

Another difficulty with the circuit in Figure 13-29 is the way by which successive gate triggering

Table XIII-IV. Pulse Transformers

| MANUFACTURER AND TYPE | TURNS RATIO | $\begin{gathered} \text { APPROX. } \\ \text { OCL IN } \\ \text { MILLIHENRIES } \end{gathered}$ | APPROX. MAXIMUM VOLTMICROSECOND | $\begin{gathered} \text { APPROX. } \\ \text { RISE TIME } \\ \text { 10/90 IN } \\ \text { MICROSECONDS } \end{gathered}$ | APPROX. 50\% PULSE WIDTH, STEP INPUT IN MICROSECONDS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Sprague 31 Z201 <br> Sprague 35ZM300 <br> Pulse Engineering PE-2228 | 1.1 | 1-2 | 100-250 | 0.04-0.08 | 4.8 |
| Sprague 31 Z281 <br> Sprague 35ZM315 <br> Pulse Engineering PE-2229 | 1:1:1 | 1-2 | 100-250 | 0.04-0.08 | 4-8 |
| Sprague $31 Z 204$ <br> Sprague 35ZM904 <br> Pulse Engineering PE-2230 | 1:1 | 4-7 | 200-400 | 0.07-0.11 | 17-22 |
| Sprague $31 \mathrm{Z286}$ <br> Sprague 35ZM930 <br> Pulse Engineering PE-2231 | 1:1:1 | 4-7 | 200-400 | 0.07-0.11 | 17-22 |
| Sprague $31 \mathrm{Z307}$ <br> Sprague $43 Z 307$ <br> Pulse Engineering PE-2242 | 1:1 | 40-50 | 1000-1500 | 0.5-1.5 | 140-200 |
| Sprague 31 Z387 Pulse Engineering PE-2479 | 1:1:1 | 40-50 | 1000-1500 | 0.5-1.5 | 140-200 |



| $B D_{1}$ | Voltage Regulator, $51 \mathrm{~V}_{\mathrm{Z}}$, 1W (IR - 1N3037B) | $R_{3}$ $R_{4}$ | Resistor, 1000 , 1W, 5\% <br> Resistor, $47 \Omega$, 2W, 5\% |
| :---: | :---: | :---: | :---: |
| $\mathrm{BD}_{2}$ | Voltage Regulator, $50 \mathrm{~V}_{\mathrm{Z}}$. 10W (IR - 1N2990) | $\mathrm{RD}_{1}, \mathrm{RD}_{2}$ | Rectifier, 1000V, 1A $(I R-10 D 10)$ |
| $\mathrm{BD}_{3}$ | Voltage Regulator, $10 \mathrm{~V}_{\mathrm{Z}}$. 1W (IR - 1N3020B) | $\mathrm{S}_{1}$ | Switch, pushbutton (Unimax - ABB) |
| $\begin{aligned} & C_{1}, C_{2} \\ & R_{1} \end{aligned}$ | Capacitor, $1 \mathrm{mF}, 1000 \mathrm{~V}$, Oil Resistor, $17 \Omega$, 2W, 10\% | $\mathrm{SCR}_{1}$ | $\begin{aligned} & \text { SCR, 7.4A, 400V } \\ & (I R-5 R C 40 \mathrm{~A}) \end{aligned}$ |
| $\mathrm{R}_{2}$ | Resistor, 1000 2 , 100W (tapped at 950 ${ }^{\text {) }}$ | $\mathrm{T}_{1}$ | Transformer, $115 \mathrm{~V} /$ 230 VAC, centertap, 50 VA |
|  |  | $\mathrm{T}_{2}, \mathrm{~T}_{3}$ | Transformer, pulse |

Figure 13-30. Zero Voltage, Single Shot Triggering Circuit
pulses after the first are blocked. The 0.1 Mfd capacitor charges up almost to peak positive output voltage from the transformer secondary on the first pulse, but enough difference between its charged voltage and unloaded source voltage exists to enable several more, much smaller pulses to be passed. Were sufficient output voltage available, alternate output configurations could be used to eliminate this effect, but with proximity to zero cross-over a must, output pulses are generally neither high enough or long enough.

The circuit shown in Figure 13-30 not only permits the use of a low OCL transformer, near-ideal for
differentiation, but also yields a nearly simultaneous pulse, which 1) can supply enough energy, either directly or through an overdriven pulse transformer, to trigger any size controlled rectifier, and 2) does not result in successive after pulses. With the pushbutton pressed down and held firmly, one and only one husky line-synchronized pulse is produced within three degrees of the zero cross-over point.

In both Figures 13-29 and 13-30, a fifty-volt zener voltage regulator is placed across the primary of the pulse transformer. A regular diode, such as IR's 10D6, could suffice, but the zener regulator also prevents overvolting of the primary
should line surges occur. The zener voltage regulator in the primary of the second pulse transformer also helps shape output pulse waveform and a non-zener should not be substituted.

The output pulse waveform of the circuit in Figure 13-30 is shown in Figure 13-31. For these oscilloscope photographs, $\mathrm{T}_{2}$ was a PE2231. The lack of droop and uniform output voltage is the reason for the zener voltage regulator in the circuit. A ten-volt zener voltage regulator could have been substituted for the 50 volt regulator, and a 47 -ohm terminating resistor used, but the output pulse then would have been rounded and with a peak of but 7 to 8 volts, because of IxR drop through the transformer secondary. Without the zener regulator or a terminating resistor, high-frequency transients and excessive ringing are present.

Figure 13-32 shows a line-synchronized countdown triggering circuit developed at International Rectifier. It has been used at repetition rates of as high as 10 pulses per second and as low as 1 pulse per 10 minutes, with extremely high reliability and reproducibility. Output waveforms are shown in Figure 13-33. Again, the pulse transformer
used was a PE-2231, although the circuit has been used successfully with a PE-2479 to produce a pulse with a rise time ( $10-90 \%$ ) of a microsecond, a pulse width (50\%) of 170 microseconds, and a fall time $(90-100 \%)$ of 170 microseconds. The top of the pulse shows little droop over a full 66-microsecond period.

In operation, the phasing of the pulse within a given positive halfcycle can be shifted but a small amount before the triggering rate increases or decreases by a cycle per second.

When supply line $B$ is positive, the $100 \mu \mathrm{~F}$ capacitor, $\mathrm{C}_{3}$, charges to the zener regulator voltage of $\mathrm{BD}_{2}(30 \mathrm{~V})$ less the on-state voltage of the rectifier, $\mathrm{RD}_{3}$. During this half cycle, the base voltage of $Q_{1}$ is zero, and no current passes through $R_{1}$ and $Q_{1}$ to charge $C_{1}$. When supply line A is negative, a sharply rising square wave exists across $\mathrm{BD}_{1}$ $(10 \mathrm{~V})$ and a square wave pulse of about 8 volts occurs across the 1000 -ohm load resistor, $\mathrm{R}_{5}$ through the two diodes $\mathrm{RD}_{1}$ and $\mathrm{RD}_{2}$. This biases $\mathrm{Q}_{1}$ to charge capacitor $\mathrm{C}_{1}$ from supply capacitor, $C_{3}$. At the same time, it produces through capacitor $\mathrm{C}_{2}$ by differentiation, a negative pulse at base 2 of the unijunc


Figure 13-31. Output Waveforms for Zero Cross-over Trigger Circuit


```
BD1 Voltage Regulator, 10 V Z, 10W
    (IR - 1N2974RB)
BD2 Voltage Regulator, 30 V Z, 10W
    (IR - 1N2989RB)
BD3 Voltage Regulator, 10 V _, 1W
    (IR - 1N3020B)
C
C2 Capacitor, 0.33 \muF,400 VDC,
    Mylar
C3 Capacitor, 100 \muF,50 VDC
```

| $\mathrm{Q}_{1}$ | Transistor (see text) |
| :--- | :--- |
| $\mathrm{Q}_{2}$ | Transistor, unijunction <br> (2N2160) selected |
| $R_{1}$ | Resistor (see text) |
| $R_{2}$ | Resistor, $330 \Omega, 1 \mathrm{~W}, 5 \%$ |
| $R_{3}, R_{4}$ | Resistor, $500 \Omega, 50 \mathrm{~W}$ |
| $R_{5}$ | Resistor, $1 \mathrm{~K}, 1 \mathrm{~W}, 5 \%$ |
| $R_{1}$, | Rectifier, 1000V, 1A |
| $R_{2}$, | (IR -10D10) |
| $R_{3}$ |  |
| $T_{1}$ | Transformer, pulse (see text) |

Figure 13-32. Countdown Triggering Circuit


Figure 13-33. Output Waveforms for Countdown Trigger Circuit
tion transistor, Q2. At the start of this negative pulse, if the voltage across $C_{1}$ is high enough, the unijunction will trigger.

For proper operation of the circuit, a value of $\mathrm{C}_{1}$ of one $\mu \mathrm{fd}$ or more should be used, even at fairly high repetition rates. This capacitor should be paper, oil, Mylar, or a tantalum electrolytic, for stability and proper discharge characteristics. If smaller values of $\mathrm{C}_{1}$ are used, under some conditions multiple pulses may be produced.

The circuit has worked with a variety of silicon and germanium

PNP transistors, but best performance is possible with a silicon PNP high-frequency transistor such as mentioned, with a typical $\mathrm{BV}_{\text {CEO }}$ of 60 V or above, and a small-signal beta of 100 or more at 5 mA dc .

In the circuit as shown, with $\mathrm{C}_{1}$ a $10-\mathrm{mfd}$, 100 Vdc Mylar, a value for $R_{1}$ of 10 kilohms yielded a pulse repetition rate of 4.1 pulses per second, while a value of 20 kilohms yielded 1.9 pulses per second. Down to a certain minimum value for $\mathrm{R}_{1}$, different for each $Q_{1}$, pulse repetition rate appears linearly inversely proportional to value of $\mathrm{R}_{1}$.

## References

1. H.F. Haight, "Testing Procedures and Test Equipment for Controlled Rectifiers," Rectifier News, Summer 1966 and Spring 1966, International Rectifier.
2. F. Durnya, "Inrush Current Testing," Rectifier News, Fall 1968 International Rectifier.

## INTERNATIONAL RECTIFIER ISR



Large diameter wafers of high-purity silicon are arranged in a glass "boat" and loaded into a diffusion furnace. The boat also contains a small amount of an additive element which will precisely change the electrical characteristics of the silicon. The two are heated together until the additive element gasifies into the lattice structure of the silicon.

## Triggering Circuits

## Gate Triggering Circuits

The simplest means for triggering a controlled rectifier is to apply a positive dc potential between the gate and cathode. This is the operating condition used to determine compliance with published specifications for maximum gate current and voltage required to trigger all units of a given type. The designer quickly learns that there are a number of considerations which require the application of greater current and voltage to the gate in order to achieve successful device operation in a practical piece of equipment. Fortunately, in modern devices the maximum gate current and voltage which may be applied greatly exceed the values required to trigger under dc conditions. This is illustrated in Figure 14-1, which shows the gate characteristics for a 70 ampere (average) device. It can be seen that the designer has a large region within which to operate where the gate can be driven harder than the amount barely required to turn the device on and yet not be driven beyond its maximum peak power rating. Care must be taken to avoid exceeding the maximum average power rating of the gate when applying a high peak signal.

## Gate Triggering to Accommodate High Load Circuit di/dt <br> For applications using conventionally gated devices where the initial rate-of-rise of anode current is more than a few amperes per microsecond it becomes important to provide a considerably greater current pulse than that which will

barely turn the device on. A larger than minimum gate current pulse will cause a larger portion of the total cross section of the device to turn on initially, thus reducing the turn-on current density and minimizing the chance of a device failure due to the di/dt effect. In Figure 14-1, a region is shown where best results will be obtained when the device must accommodate a high di/dt. In addition, the gate pulse should have a fast rise time, in the order of 0.1 microseconds. The objective is to inject a significant charge into the gate region during the delay period.

ACE gated and Di-Vergence ${ }^{\text {© }}$ gated devices in general require the above mentioned precautions except that di/dt and switching losses are less severe for fast rising anode currents.

## Short Gate Triggering Pulses

For reasons of economy, both to reduce the size of components used to build the gate excitation circuit and the power consumed by this circuit, a relatively short pulse is often applied to the gate rather than a song pulse or a continuous dc signal. As pulse width is reduced it is found that the peak current and voltage required to trigger a given device becomes greater. This effect is most noticeable for pulse widths shorter than 10 microseconds, as shown in Figure 14-2. For such short pulses it can be seen that essentially a fixed electrical charge is required to trigger the controlled rectifier.

There is another problem which
is encountered with a lagging power factor load. In many inverter circuits, the power SCR may not be forward-biased until well into the half-cycle. At the same time, reactive current is flowing through the free-wheeling diodes. In this case a short pulse triggering scheme cannot be used. A relatively long cur-
rent pulse must be supplied to the gate to ensure that the device triggers when it becomes forward biased. This is often accomplished by providing, immediately after the initial gate pulse, a longer but lower amplitude pulse which is commonly called the "back porch" of the gate drive signal. See Figure 14-3.


Figure 14-1. Gate characteristics for 70 A controlled rectifier


Figure 14-2. Gate current required to trigger controlled rectifier vs. gate trigger pulse width


Figure 14-3. Generalized waveform of gate trigger pulse with back porch

Several circuits that can be used for pulse drive are shown in Figure 14-4.

The circuit shown in Figure $14-4(a)$ is a unijunction relaxation
oscillator circuit, timed by $\mathrm{R}_{1}$ and $\mathrm{C}_{1}$ with a pulse transformer coupling the energy to the gate. This rather simple circuit puts out a pulse with no back porch. The circuit shown in Figure 14-4(b) has a little more wave shaping by using a speed-up capacitor $\mathrm{C}_{1}$ across $\mathrm{R}_{1}$ to decrease the pulse rise time. $\mathrm{R}_{2}$ in both circuits reduces the gatecathode impedance, thus lowering the SCR's susceptibility to noise and $\mathrm{dv} / \mathrm{dt}$ triggering. This resistor is usually in the order of 100 ohms and is mounted as close physically to the SCR as is practical. The diode $R D_{1}$ functions to block the reverse voltage kick produced when the pulse transformer resets, protecting the gate-cathode junction in the reverse direction.


Figure 14-4. Pulse gate drive circuits


Figure 14-5. Picket fence drive

## Picket Fence Drive

The Picket Fence Drive Circuit, shown in Figure 14-5, is a variation of pulse drive (using a small pulse transformer) but has the effect of putting pulses on the gate all through the conduction period. While $Q_{3}$ is turned on, unijunction $Q_{1}$ is allowed to cycle many times as set by $\mathrm{R}_{1}$ and $\mathrm{C}_{1}$. The output would be typically as shown in Figure 14-5.

A modification of the picket fence drive is shown in Figure 14-6. In this circuit the pulse transformer is driven in both directions and the output is rectified to give a dc gate signal. This circuit has the added feature of requiring only one oscillator, which can be directed to any SCR by use of logic gates. This is useful for multi-device circuits.


Figure 14-6. Rectified picket fence drive


Figure 14-7(a). Local energy storage type gate trigger pulse cricuit (for triggering two thyristors is shown)

Local Energy Storage Gate Triggering
Local energy storage gate trigger circuit design will be discussed briefly in order to give the circuit designer some tips on ways of achieving the rise times recommended above in a relatively inexpensive manner. The circuit shown in Figure 14-7(a) serves as a pulse sharpening circuit to give good voltage isolation without requiring the isolation transformer to have good high frequency characteristics. In this circuit, the combination of $\mathrm{v}_{\mathrm{g}}$ and $\mathrm{i}_{\mathrm{g} 1}$ for $\mathrm{SCR}_{1}$ and also $\mathrm{R}_{\mathrm{G}}$ should be chosen to give a triggering characteristic which is uniform for all combinations of $\mathrm{v}_{\mathrm{g}}, \mathrm{R}_{\mathrm{G}}$, and
$\mathrm{SCR}_{1}$ which are to be used in each of the SCR trigger circuits. Capacitors $C_{1}$ and resistors $R_{1}$ act not only as delay circuits to square up the collector (point B) vs. time characteristic shown in Figure 14-7(b), but also as noise suppressors to the gates of the SCRs which are connected in parallel. $R_{2}$ simply acts as a pulse stretcher to stretch out the discharge of the local energy storage capacitor $\mathrm{C}_{1}$ and should be chosen so that there is no discontinuity in the SCR gate triggering current between the discharge of the capacitor and the follow-up of the slower current from the pulse transformer.


Figure 14-7(b). Waveforms pertaining to circuit in Figure 14-7(a)


Figure 14-8(a). Local energy storage type gate trigger pulse circuit which provides $D C$ gate trigger pulse

Figure 14-8(a) shows an alternate method of achieving voltage isolation and yet using pulse gating techniques with local energy storage where it may be important, because of a reactive load in the main power circuit, that the gate current will essentially be continuous. This can be achieved by supplying a series of gate pulses from two circhits operating alternately and connetted through diodes to the same gate. These pulses (refer to Figure 14-8(b)) need not be overlapping or continuous as far as the gate is concorned. A ratio of time-on to time-between-pulses might be about $70 \%$ on, $30 \%$ off for large SCRs, as long as the $30 \%$ off time is well below the turn-off time of the SCR. In the case of devices of 300 ampere rat-
ing or more, the off-time should probably be kept below about 30 or 40 microseconds. It would not then be normal for the devices to achieve a great deal of recombination during the off-time.

If diodes $R D_{1}$ are used in the gate circuit for isolation, their turnon characteristics should be studied by the circuit designer to be sure that they do not affect the gate current rise characteristic. Normally a diode doped for fast recovery characteristics will serve well in this type of application.

The gate circuit of Figure 14-9 combines the qualities of a fast rise time gate current to minimize delay time effects and a wide pulse for inductive loads.


Figure 14-8(b). Gate current waveform pertaining to circuit in Figure 14-8(a)


Figure 14-9. Combined fast rise time and wide pulse trigger circuit

Opto-Coupled SCR Gate Drive
The interwinding capacitance of conventional pulse transformers may be prohibitively high for proper operation of SCRs when high rates of rise of anode voltage are encountered. High dv/dt can induce currents to flow in the interwinding capacitance, which may falsely trigger an SCR. This problem can be avoided by the use of optical couplers to provide extremely high voltage isolation between the trigger circuits of different SCRs. The gate circuit of Figure 14-10 uses a light emitting diode (LED) and photo-sensitive $\operatorname{SCR}\left(\mathrm{SCR}_{1}\right)$ to provide optical isolation for each main SCR $\left(\mathrm{SCR}_{2}\right)$.

The circuit in Figure 14-10 has the advantage of being positive and simple. However, it suffers from the problem that $\mathrm{SCR}_{1}$ must have the same blocking characteristics as the main $\mathrm{SCR}, \mathrm{SCR}_{2}$. This could be a serious handicap if $\mathrm{SCR}_{2}$ is an inverter SCR or very high voltage SCR.


Noise
There are general rules that can be followed to reduce false triggering from noise (some were mentioned above), whether generated in the circuit, or externally.
A. Introduce a gate-to-cathode resistor (mentioned above) near the deivce.
B. Add snubbing devices anode to cathode to reduce voltage spikes generated during device recovery.
C. Twist the auxiliary gate and cathode leads, especially when running any distance. This reduces inductive pick up.
D. Introduce a diode or zener diode in series with the gate to raise the effective threshold voltage of the device gate. If this method is used, a gate-cathode resistor must be used on the device, otherwise the impedance in the gate to cathode region will be very high and this will make the device more susceptible to noise.
E. Reverse gate-cathode bias has been used in the past, not only to act as a sink for circuit noise, but also to enhance the $d v / d t$ characteristics of an SCR by bleeding off capacitive leakage from the anode circuit. However this is no longer needed with the emitter shorting used in modern devices. There is still some noise immunity achieved by this method but the amount is questionable when considered against the cost.
F. Capacitors have been placed from gate to cathode to reduce the effect of high frequency noise in the circuit. However, in most cases this is not recommended any longer because it also reduces the rise time
of the desired gate signal. There are a few cases where this may not be detrimental (i.e., low di/dt anode currents) and a capacitor can be safely used.
G. A great deal of noise immunity can be achieved by using a gate transformer with extremely low interwinding capacitance, in the order of 5 pf or less. This not only reduces the noise from the control circuit side of the transformer that gets to the devices, but reduces the noise from the power circuit that gets into and falsely triggers the control circuit.
H. Operate parallel and potentially interacting thyristor circuits from a stiff (low reactance) supply line. Notches in the voltages of power lines, particularly those tied to control circuits, can cause a false change of state in logic elements; one shot multivibrators are especially susceptible to this type of noise.
J. If the supply line is soft (high reactance), consider using separate transformers to feed the parallel branch circuits; each transformer should be rated no more than required by the rating of the branch circuit load.
K. Avoid purely resistive loads operating from stiff lines - they give highest rates of current rise on switching.
L. Keep both leads of each power circuit run together; avoid loops that encircle sensitive control circuitry.
M. Arrange magnetic components so as to avoid interacting stray fields.

## References

1. General Electric SCR Manual, 4th Edition.
2. L.R. Carver, "How the Experts Use SCR Ratings," Machine Design, July 12, 1973.

## High Speed Thyristors

## Comparing Gate Structures

A glance at Figure $15-1$ clearly shows a major problem associated with the design of high frequency, high current thyristors; the equalization time (the time necessary to turn the thyristor fully on) increases with the current rating.

The solution is to use an interdigitated gate structure; i.e., a multiplicity of gate arms such that no point on the cathode is more than a few millimeters away from the gate. Combining this concept with the ACE gate construction yields a device which:
A. Requires a relatively low external gate drive.
B. Propagates rapidly and effi-
ciently over the main cathode.
C. Turns on the entire main cathode in less than 20 microseconds.

To illustrate the effect of the several gate structures, consider three thyristors* with a cathode diameter of 25 mm , differing only in gate structure. Figure 15-2 shows not only the advantage of the ACE and interdigitated gates, but also the trade-off in top (cathode) surface area.
A. The point gate thyristor uses $100 \%$ of the surface as cath-
*Calculations based on realistic designs and a constant $0.1 \mathrm{~mm} / \mu \mathrm{s}$ turn-on propagation velocity.


Figure 15-1. Typical time for SCRs of various average current ratings to turn on fully (conventional point gate devices, hard firing gate pulse)
ode, but takes $250 \mu$ s to turn on completely.
B. The ACE gate thyristor uses less than $91 \%$ of the surface as cathode, but always has significantly more area "on" until it is completely on in $215 \mu$ s.
C. The interdigitated (DiVergence) gate thyristor uses approximately $82 \%$ of the surface, but is completely on in $13.2 \mu \mathrm{~s}$.

With a larger Di-Vergence gate thyristor, the length of each gate arm increases in proportion to the
area of the surface and the equalization time is relatively constant. The gate arm width remains about constant and so the percentage of surface area aevoted to the gate is relatively constant.

The effect of incomplete turn-on is increased watts loss and therefore heating of the thyristor during the turn-on interval. This is true even at intermediate frequencies where the ACE gate device is completely turned on at the end of the current pulse.


Figure 15-2. Typical turn-on characteristics of three gate structures


Figure 15-3. Maximum Allowable Peak On-State Current versus Frequency


Figure 15-4. Maximum Allowable Peak On-State Current Rating as a Percent of Low Frequency Rating

Figure $15-3$ shows the Maximum Allowable Peak On-State Current for sinusoidal waveforms and $50 \%$ duty cycle at a case temperature of $65^{\circ}$ with $\mathrm{V}_{\mathrm{R}} \leqslant 50$ volts for the 420PBL ACE gate thyristor and the 550 PBQ interdigitated gate thyristor. * Figure $15-4$ shows the same information except that it is plotted as a percentage (\%) of the low frequency rating.

As expected at 5 kHz , the 550 PBQ is significantly better than the 420PBL. At frequencies below 3 kHz the 420 PBL is completely
turned on at the end of each current pulse, yet the 550 PBQ can handle more current (or conversely requires less cooling) than the 420 PBL . For example, at 1.5 kHz the 550 PBQ can carry up to $88 \%$ of its rated low frequency current but the 420 PBL can carry only $70 \%$ of its rated low frequency current.

[^3]di/dt Ratings and Gate Structure
A conventional point gate device driven with a high level (hard) external gate source can have a medium di/dt rating.

An ACE gate device has a consistently high di/dt rating with hard or soft external gate drive.

With an ACE gate device, the auxiliary cathode is initially turned on at the most sensitive point or several points on the main cathode gate line. Until the remainder of the main cathode gate line is turned on, these one or two points must carry any high inrush current, hence the di/dt limitation. After one or two microseconds, the entire gate line (about 1 cm ) is turned on and the current density propagates laterally across the main cathode.

Di-Vergence (interdigitated) gate device has the same di/dt rating as an ACE gate device. With an interdigitated device, the gate line is considerably longer. For example, in the 500 PBQ device, the length is approximately 20 cm . However, initially the auxiliary cathode turns on at the most sensitive point or several points on the main cathode gate line and once again these one or two points must carry any high inrush currents for the first one or two microseconds. After one or two microseconds, the entire gate line is turned on, and the current density propagates laterally across the main cathode. After approximately $15 \mu$ s the entire cathode is turned on.

With the introduction of interdigitated gate structures, thyristors can now be applied efficiently in high frequency power conversion systems and they are now being used in such applications as induction heating generators operating at
frequencies up to 10 kHz .

## Recovery Current and Recovered Charge

As the frequency capability of high current thyristors increases, the recovery characteristic becomes of greater importance to the users and hence the manufacturer for several reasons:
A. Magnitude of recovery losses. It can be shown that the reverse recovery losses in a thyristor are:

$$
\begin{equation*}
P_{R(R E C)}=f_{R(R E C)} V_{R M} \tag{15-A}
\end{equation*}
$$

Where:
$\mathrm{P}_{\text {R(REC) }}$ = Reverse recovery power loss in watts
$\mathrm{f} \quad=$ Operating frequency
$\mathrm{Q}_{\mathrm{R}(\text { REC })}=$ Recovered charge
$\mathrm{V}_{\mathrm{RM}}=$ Applied reverse voltage
At higher operating frequencies, these losses represent an increasingly important percentage of the total losses.
B. Shape of the Recovery Current. The positive slope of the recovery current as the current decreases towards zero creates a self-induced voltage across the thyristor, which, when added to the supply voltage, may exceed the voltage rating of the device. If another thyristor is connected in anti-parallel, the dv/dt of this voltage may cause triggering of the other thyristor.

Each of these matters will be considered separately.

## Magnitude of Recovery Losses

The recovered charge of a thyristor in any application is a combination of parameters controlled by the manufacturer and controlled by the circuit.

Keeping the circuit parameters constant, the recovered charge of a given thyristor type is:

$$
\begin{equation*}
\mathrm{Q}_{\mathrm{R}(\mathrm{REC})}=\mathrm{f}\left(\mathrm{I}, \mathrm{~V}, \& 1 / \tau_{\mathrm{eff}}\right) \tag{15-B}
\end{equation*}
$$

Where:
I = Current rating for which the type was designed
V = Highest voltage rating for which the type was designed
$1 / \tau_{\text {eff }}=$ Reciprocal of the effective lifetime of minority carrier silicon used in the particular device type

For a given current and voltage rating, the only design freedom left to the device designer is lifetime control. Since high frequency thyristors must have short turn-off
times, the $\tau_{\text {eff }}$ of these types is already controlled and low. The effective lifetimes of these types can be lowered further by several additional means in order to lower the recovered charge. It must be remembered that lifetime control is a trade-off. As lifetime is lowered, the on-state voltage increases and the on-state current rating is decreased.

With a given device type:

$$
\begin{equation*}
\mathrm{Q}_{\mathrm{R}(\mathrm{REC})}=\mathrm{f}\left(\mathrm{~T}_{\mathrm{JX}}, \mathrm{I}_{\mathrm{TM}}, \&-\mathrm{di} / \mathrm{dt}\right) \tag{15-C}
\end{equation*}
$$

Where:
$\mathrm{T}_{\mathrm{JX}}=$ Instantaneous junction temperature at the end of on-state current flow
$\mathrm{I}_{\mathrm{TM}}=$ Peak on-state current (see Figure 15-5)
-di/dt = Rate of change of on-state current (see Figure 15-6)


Figure 15-5. Peak On-State Current Ratio


Figure 15-6. Rate of Change of Current Ratio

This relationship shows that the circuit parameters are in opposition to the desires of the circuit designer. The designer wants high currents at high frequencies (hence high di/dt's) but low recovered charge. The only freedom allowed is peak junction temperature.

As has been shown previously for a given base width, peak current and case temperature, a Di-Vergence gate thyristor operates at a lower peak junction temperature than non-interdigitated devices and therefore, for this reason alone, will have a lower recovered charge.

## Shape of the Recovery Current

Both the voltage overshoot and negative $\mathrm{dv} / \mathrm{dt}$ can be limited by a snubber circuit. (Refer to Figure

15-7.) The specification sheet may have suggested snubber circuit values, however, the optimum snubber values for a particular application depend on the component values of the circuit.

Snubber circuits are designed with an eye to several considerations: $\mathrm{V}_{\mathrm{RM}} / \mathrm{V}_{\mathrm{S}}, \mathrm{dv} / \mathrm{dt}$, snubber losses in $\mathbf{R}$, and snubber losses in the thyristor.

If the damping ratio $\zeta=$ $\mathrm{R} / 2 \sqrt{\mathrm{C} / \mathrm{L}}$ is selected to be 0.5 :

$$
\frac{\mathrm{V}_{\mathrm{RM}}}{\mathrm{~V}_{\mathrm{S}}} \approx 1.3
$$

and

$$
\mathrm{dv} / \mathrm{dt}=\zeta\left(\frac{4 \mathrm{~V}_{\mathrm{S}}}{\mathrm{RC}}\right)=\frac{\mathrm{V}_{\mathrm{S}}}{\mathrm{RC}}(15-\mathrm{D})
$$

## Where:

$\mathrm{V}_{\mathrm{RM}}=$ Peak Reverse Voltage (V)
$\mathrm{V}_{\mathrm{S}}=$ Reverse Supply Voltage (V)
C $=$ Snubber Capacitance ( $\mu \mathrm{F}$ )
R = Snubber resistance (ohms)
$\mathrm{L} \quad=$ Effective circuit inductance ( $\mu \mathrm{H}$ )

See Figure 15-7 for the snubber circuit and Figure 15-8 for waveshapes.

If: $\mathrm{V}_{\mathrm{S}}=600 \mathrm{~V}, \mathrm{~V}_{\mathrm{SCR}}=1000 \mathrm{~V}$, $\mathrm{dv} / \mathrm{dt}_{\mathrm{SCR}}=200 \mathrm{~V} / \mu \mathrm{s}$ and $\mathrm{L}=$ $35 \mu \mathrm{H}$ :
$\zeta=0.5=\frac{\mathrm{R}}{2} \sqrt{\frac{\mathrm{C}}{\mathrm{L}}}$ and $\frac{200}{600}=\frac{1}{\mathrm{RC}}$

## Hence:

$\mathrm{R}^{2} \mathrm{C}=35$
and
$\mathrm{RC}=3$
$\mathrm{R}=11.7 \Omega \quad$ and $\quad \mathrm{C}=0.257 \mu \mathrm{~F}$
Select 10 ohms and $0.25 \mu \mathrm{~F}$.
Losses in Resistor during Recovery This loss has been shown to be:

$$
\begin{array}{r}
\mathrm{J}_{\mathrm{R}}=\frac{\mathrm{CV}^{2}}{2}\left(1+\frac{\mathrm{LI}^{2}}{\mathrm{CV}_{\mathrm{S}}^{2}}\right)=\frac{\mathrm{CV}^{2}}{2}\left(1+\chi^{2}\right) \\
\chi^{2}=\frac{\mathrm{LI}^{2}}{\mathrm{CV}_{\mathrm{S}^{2}}}=\frac{4 \zeta^{2} \mathrm{I}^{2}}{\mathrm{~d}\binom{\mathrm{dv}}{\mathrm{dt}}^{2}}(15-\mathrm{E})
\end{array}
$$

Where:
$\mathrm{J}_{\mathrm{R}}=$ Energy dissipated in resistor during recovery

That is, these extra losses are proportional to the damping factor and inversely proportional to the $\mathrm{dv} / \mathrm{dt}$.

## Losses during Turn-On

These have been shown as a first order approximation to be:

$$
\begin{align*}
& \mathrm{J}_{\mathrm{THY}} \approx \frac{\mathrm{CV}}{2}\left(\frac{\mathrm{t}_{\mathrm{r}}}{\mathrm{t}_{\mathrm{r}}+\mathrm{t}_{\mathrm{s}}}\right)  \tag{15-G}\\
& \mathrm{J}_{\mathrm{RES}} \approx \frac{\mathrm{CV}}{}{ }^{2}\left(\frac{\mathrm{t}_{\mathrm{s}}}{2}\left(\frac{\mathrm{t}_{\mathrm{r}}+\mathrm{t}_{\mathrm{s}}}{}\right)\right. \tag{15-H}
\end{align*}
$$

Where:
$\mathrm{J}_{\mathrm{THY}}=$ Energy dissipated in thyristor during turn-on
$\mathrm{J}_{\text {RES }}=$ Energy dissipated in resistor during turn-on
$\mathrm{t}_{\mathrm{S}}=$ Snubber circuit time constant
$=\mathrm{RC}$
$=$ Thyristor rise time
$=\mathrm{t}_{\mathrm{on}}-\mathrm{t}_{\text {delay }}$


Figure 15-7. Typical snubber circuit


Figure 15-8. Recovery waveform

More simply, the loss is divided between the thyristor and resistor in proportion to their respective time constants.

If the thyristor loss at turn-on is found to be excessive, a polarized snubber may be considered to reduce the current supplied by the snubber during turn on.

If $\mathrm{dv} / \mathrm{dt}$ is not a consideration, a reverse polarized snubber, as in Figure $15-9$, may be used.


Figure 15-9. Reverse polarized snubber

Here the damping resistor $\mathrm{R}_{1}$ is effective during reverse recovery and $R_{2}$ serves to bleed the snubber capacitor during the period of offstate voltage before the thyristor is triggered again.

If the snubber is also across a diode connected in anti-parallel to the thyristor, and $\mathrm{dv} / \mathrm{dt}$ is a major consideration, then an off-state polarized snubber, as shown in Figure $15-10$, may be used.

Here the effective damping resistor is the parallel combination of $R_{1}$ and $R_{2}$, but the discharge resistor at turn-on is $R_{2}$.


Figure 15-10. Off-state polarized snubber

There are two things to note: polarized snubbers do not reduce the turn-on losses, they only serve to reduce the loss in the resistor. It is not practical to design a polarized snubber across two thyristors connected in anti-parallel. A non-linear reactor may be used advantageously in this case to minimize the extra power loss resulting from the snubber during turn-on or reverse recovery. The arrangement is shown in Figure 15-11.


Figure 15-11. Unpolarized snubber with non-linear reactor

## Symbols and Terms

The symbols and terms listed here are from EIA-NEMA Standard "Recommended Standards for Thyristors," June 1972 (EIA Standard RS-397 and NEMA Standard SK516-1972). Additional figures illustrating the symbols and some specific definitions are presented from International Rectifier's Application Note AN-313.

## Classes of Thyristors

## Thyristor

A bistable semiconductor device comprising three or more junctions, which can be switched from the off-state to the on-state or vice versa, such switching occurring within at least one quadrant of the principal voltage-current characteristic.

Reverse Blocking Diode Thyristor
A two-terminal thyristor which switches only for positive anode-to-cathode voltages and exhibits a reverse blocking state for negative anode-to-cathode voltages.

Reverse Blocking Triode Thyristor
A three-terminal thyristor which switches only for positive anode-tocathode voltages and exhibits a reverse blocking state for negative anode-to-cathode voltages.

## Reverse Conducting

## Diode Thyristor

A two-terminal thyristor which switches only for positive anode-tocathode voltages and conducts large currents at negative anode-to-cathode voltages comparable to magnitude to the on-state voltages.

## Reverse Conducting <br> Triode Thyristor <br> A three-terminal thyristor which

switches only for positive anode-tocathode voltages and conducts large currents at negative anode-to-cathode voltages comparable in magnitude to the on-state voltages.

## Bidirectional Diode Thyristor

A two-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

## Bidirectional Triode Thyristor

A three-terminal thyristor having substantially the same switching behavior in the first and third quadrants of the principal voltage-current characteristic.

Turn-Off Thyristor
A thyristor which can be switched from the on-state to the off-state and vice versa by applying control signals of appropriate polarities to the gate terminal, with the ratio of triggering power to triggered power appreciably less than one.

## P-Gate Thyristor

A thyristor in which the gate terminal is connected to the Pregion adjacent to the region to which the cathode terminal is connected and which is normally switched to the on-state by applying a positive signal between
the gate and cathode terminals. Standard production SCRs are Pgate thyristors.

## N-Gate Thyristor

A thyristor in which the gate terminal is connected to the N region adjacent to the region to which the anode terminal is connected and which is normally switched to the on-state by applying a negative signal between gate and anode terminals.

Semiconductor Controlled Rectifier (SCR)

An alternative name used for the reverse blocking triode thyristor.

## Physical Structure

Nomenclature
Electrode (of a semiconductor device)

An electric and mechanical contact to a region of a semiconductor device.

Anode
The electrode by which current enters the thyristor, when the thyristor is in the on-state with the gate open-circuited.

Note: This term does not apply to bidirectional thyristors.

## Cathode

The electrode by which current leaves the thyristor, when the thyristor is in the on-state with the gate open-circuited.

Note: This term does not apply to bidirectional thyristors.

## Gate

An electrode connected to one
of the semiconductor regions for introducing control current.

Junction (of a semiconductor device)

A region of transition between semiconductor regions of different electrical properties (e.g., $n-\mathrm{n}^{+}, \mathrm{p}-\mathrm{n}$, p-p+ semiconductors), or between a metal and a semiconductor.

## Collector Junction

The junction across which the polarity of the voltage reverses when switching occurs.

Terminal (of a semiconductor device)

The externally available point of connection to one or more electrodes.

## Main Terminals

The terminals through which the principal current flows.

Main Terminal 1 (of a bidirectional thyristor)

The main terminal which is named " 1 " by the device manufacturer.

Main Terminal 2 (of a bidirectional thyristor)

The main terminal which is named " 2 " by the device manufacturer.

## Anode Terminal

The terminal which is connected to the anode.

Note: This term does not apply to bidirectional thyristors.

## Cathode Terminal

The terminal which is connected to the cathode.

Note: This term does not apply to bidirectional thyristors.

## Gate Terminal

A terminal which is connected to a gate

## Electrical Characteristic Terms

Principal Voltage-Current Characteristic (Principal Characteristic)

The function, usually represented graphically, relating the principal voltage to the principal current with gate current, where applicable, as a parameter.

## Anode-to-Cathode Voltage-Current

 Characteristic (Anode Characteristic)A function, usually represented graphically, relating the anode-tocathode voltage to the principal current with gate current, where applicable, as a parameter.

Note: This term does not apply to bidirectional thyristors.

## On-State

The condition of the thyristor corresponding to the low-resistance, low-voltage portion of the principal voltage-current characteristic in the switching quadrant(s).

Note: In the case of reverse conducting thyristors, this definition is applicable only for a positive an-ode-to-cathode voltage.

## Off-State

The condition of the thyristor corresponding to the high-resistance, low-current portion of the principal voltage-current characteristic between the origin and the breakover point(s) in the switching quadrant(s).

## Breakover Point

Any point on the principal volt-age-current characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.

## Negative Differential Resistance Re-

 gionAny portion of the principal voltage-current characteristic in the switching quadrant(s) within which the differential resistance in negative.

## Reverse Blocking State (of a re-

 verse blocking thyristor)The condition of a reverse blocking thyristor corresponding to the portion of the anode-to-cathode voltage-current characteristic for reverse currents of lower magnitude than the reverse breakdown current.

## On-Impedance

The differential impedance between the terminals through which the principal current flows, when the thyristor is in the on-state at a stated operating point.

## Principal Voltage

The voltage between the main terminals.

Notes:

1. In the case of the reverse blocking and reverse conducting thyristors, the principal voltage is called positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.
2. For bidirectional thyristors, the polarity designation is arbitrary, and must be specified.

## Anode-to-Cathode Voltage (Anode Voltage)

The voltage between the anode terminal and the cathode terminal.

Notes:

1. It is called a positive when the anode potential is higher than the cathode potential, and called negative when the anode potential is lower than the cathode potential.
2. This term does not apply to bidirectional thyristors.

Forward Voltage (of a reverse blocking or reverse conducting thyristor)

A positive anode-to-cathode voltage.

## Off-State Voltage

The principal voltage when the thyristor is in the off-state.

## Working Peak Off-State Voltage

The maximum instantaneous value of the off-state voltage which occurs across a thyristor, excluding all repetitive and nonrepetitive transient voltages.

Repetitive Peak Off-State Voltages
The maximum instantaneous value of the off-state voltage which occurs across a thyristor, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

## Nonrepetitive Peak Off-State Voltage

The maximum instantaneous value of any nonrepetitive transient off-state voltage which occurs across the thyristor.

## Critical Rate-of-Rise of Off-State Voltage <br> The minimum value of the rate-

of-rise of principal voltage which will cause switching from the offstate to the on-state.

## Breakover Voltage

The principal voltage at the breakover point.

## On-State Voltage

The principal voltage when the thyristor is in the on-state.

## Minimum On-State Voltage

The minimum positive principal voltage for which the differential resistance is zero with the gate open-circuited.

## Principal Current

A generic term for the current through the collector junction.

Note: It is the current through the main terminals.

## On-State Current

The principal current when the thyristor is in the on-state.

## Forward Current (of a reverse blocking or reverse conducting

 thyristor)The principal current for a positive anode-to-cathode voltage.

Peak Repetitive On-State Current
The peak value of the on-state current including all repetitive transient currents.

## Overload On-State Current

An on-state current of substantially the same waveshape as the normal on-state current and having a greater value than the normal on-state current.

## Surge (Nonrepetitive) On-State Current

An on-state current of shorttime duration and specified waveshape.

Critical Rate-of-Rise of On-State Current

The maximum value of the rate-of-rise of on-state current which a thyristor can withstand without deleterious effect.

## Off-State Current

The principal current when the thyristor is in the off-state.

Breakover Current
The principal current at the breakover point.

## Holding Current

The minimum principal current required to maintain the thyristor in the on-state.

Reverse Voltage (of a reverse blocking or reverse conducting thyristor)

A negative anode-to-cathode voltage.

Working Peak Reverse Voltage (of a reverse blocking thyristor)

The maximum instantaneous value of the reverse voltage which occurs across the thyristor, excluding all repetitive and nonrepetitive transient voltages.

Repetitive Peak Reverse Voltage (of a reverse blocking thyristor)

The maximum instantaneous value of the reverse voltage which occurs across the thyristor, including all repetitive transient voltages, but excluding all nonrepetitive transient voltages.

Nonrepetitive Peak Reverse Voltage (of a reverse blocking thyristor)

The maximum instantaneous value of any nonrepetitive transient reverse voltage which occurs across a thyristor.

Reverse Breakdown Voltage (of a reverse blocking thyristor)

The value of negative anode-tocathode voltage at which the differential resistance between the anode and cathode terminals changes from a high value to a substantially lower value.

Reverse Current (of a reverse blocking or reverse conducting thyristor)

The principal current for negative anode-to-cathode voltage.

Reverse Blocking Current (of a reverse blocking thyristor)

The reverse current when the thyristor is in the reverse blocking state.

## Reverse Breakdown Current (of a

 reverse blocking thyristor)The principal current at the reverse breakdown voltage.

## Gate Voltage

The voltage between a gate terminal and a specified main terminal.

## Gate Trigger Voltage

The gate voltage required to produce the gate trigger current.

## Gate Nontrigger Voltage

The maximum gate voltage which will not cause the thyristor to switch from the off-state to the on-state.

## Forward Gate Voltage

The voltage between the gate terminal and the terminal of an
adjacent region resulting from forward gate current.

Note: This term does not apply to bidirectional thyristors.

## Reverse Gate Voltage

The voltage between the gate terminal and the terminal of an adjacent region resulting from reverse gate current.

Note: This term does not apply to bidirectional thyristors.

Gate Turn-Off Voltage (of a turnoff thyristor)

The gate voltage required to produce the gate turn-off current.

## ..

## Gäte Trigger Current

The minimum gate current required to switch a thyristor from the off-state to the on-state.

## Gate Nontrigger Current

The maximum gate current which will not cause the thyristor to switch from the off-state to the on-state.

## Forward Gate Current

The gate current when the junction between the gate region and the adjacent anode or cathode region is forward-biased.

Note: This term does not apply to bidirectional thyristors.

## Reverse Gate Current

The gate current when the junction between the gate region and the adjacent anode or cathode region is reverse-biased.

Note: This term does not apply to bidirectional thyristors.

Gate Turn-Off Current (of a turnoff thyristor)

The minimum gate current re-
quired to switch a thyristor from the on-state to the off-state.

Thermal Resistance (of a semiconductor device)

The temperature difference between two specified points or regions divided by the power dissipation under conditions of thermal equilibrium.

Transient Thermal Impedance (of a semiconductor device)

The change of temperature difference between two specified points or regions at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval causing the change of temperature difference.

## Gate Controlled Turn-On Time

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified low (high) value during switching of a thyristor from the off-state to the on-state by a gate pulse.

## Gate Controlled Delay Time

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal voltage (current) has dropped (risen) to a specified value near its initial value during switching of a thyristor from the off-state to the on-state by a gate pulse.

## Gate Controlled Rise Time

The time interval between the instants at which the principal voltage (current) has dropped (risen) from a specified value near its initial value to a specified low (high)

## Thyristor Letter Symbols

| General Letter Symbols: |  |
| :---: | :---: |
| Ambient Temperature. . . $\mathrm{T}_{\mathrm{A}}$ |  |
| Case Temperature . . . . TC |  |
| Virtual Junction |  |
| Temperature | TJ |
| Storage Temperature | $\mathrm{T}_{\text {stg }}$ |
| Thermal Resista |  |
| Junction-to-Ambient. . R $\mathrm{\theta}_{\theta} \mathrm{JA}$ |  |
| Junction-to-Case . . . R $\mathrm{R}_{\theta \mathrm{JC}}$ |  |
| Case-to-Ambient | $\mathrm{R}_{\theta} \mathrm{CA}$ |
| Transient Thermal |  |
| Impedance . . . . . . . $\mathrm{Z}_{\theta(\mathrm{t})}$ |  |
| Junction-to-Ambient. . $\mathrm{Z}_{\theta \mathrm{JA}}(\mathrm{t})$ |  |
| Junction-to-Case . . | . $\mathrm{Z}_{\theta \mathrm{JC}}(\mathrm{t})$ |
| Delay Time . . . . . . . $\mathrm{t}_{\mathrm{d}}$ |  |
| Rise Time |  |
| Fall Time. |  |
| Reverse Recovery Time. . $\mathrm{t}_{\text {rr }}$ |  |
| Gate-Controlled |  |
| Turn-On Time |  |
| Gate-Controlled |  |
| Turn-Off Time |  |
| Circuit-Commutated |  |
| Turn-Off Time |  |

Letter Symbol Subscripts
The following letters are used as qualifying subscripts for Thyristor Letter Symbols:
A-a . . . . . Anode
K-k . . . . . Cathode
G-g . . . . . Gate
R-r . . . . . Reverse or, as a Second Subscript, Repetitive
D-d . . . . . Off-State, Non-Trigger
T-t . . . . . On-State, Trigger
M-m. . . . . Maximum Value
MIN-min. . Minimum Value
AV-av . . . Average Value
RMS . . . . Total RMS Value
W . . . . . . Working
O-o . . . . . Open Circuit
S-s . . . . . Short Circuit, or as a
Second Subscript, Non-Repetitive
X-x . . . . . Specified Circuit
H-h . . . . . Holding
(BR) . . . . Breakdown
(BO) . . . . Breakover
Q-q . . . . . Turn-Off, Recovery
(TO) . . . . Threshold
(OV) . . . . Overload
value during switching of a thyristor from the off-state to the onstate by a gate pulse.

Note: This time interval will be equal to the rise time of the on-state current only for pure resistive loads.

Gate Controlled Turn-Off Time (of a turn-off thyristor)

The time interval between a specified point at the beginning of the gate pulse and the instant when the principal current has decreased to a specified value during switching from the on-state to the off-state by a gate pulse.

Circuit-Commutated Turn-Off Time
The time interval between the instant when the principal current has decreased to zero after external switching of the principal voltage circuit, and the instant when the thyristor is capable of supporting a specified principal voltage without turning on.

Reverse Recovery Time (of a reverse blocking thyristor)

The time required for the principal current or voltage to recover to a specified value after instantaneous switching from an on-state to a reverse voltage or current.

Letter Symbol Table

| QUANTITY | TOTAL RMS VALUE | $\qquad$ | $\qquad$ | INSTANTANEOUS TOTAL VALUE | MAXIMUM (PEAK) TOTAL VALUE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| On-State Current | IT(RMS) | IT | IT(AV) | iT | ITM |
| Repetitive Peak On-State Current | - | - | - | - | ITRM |
| Surge (Non-Repetitive) On-State Current | - | - | - | - | ITSM |
| Overload On-State Current | - | - | - | - | IT(OV) |
| Breakover Current | - | '(BO) | - | i(BO) | - |
| Off-State Current | ID(RMS) | ID | $\mathrm{I}(\mathrm{AV})$ | id | IDM |
| Repetitive Peak OffState Current | - | - | - | - | IDRM |
| Reverse Current | IR(RMS) | IR | I (AV) | iR | IRM |
| Repetitive Peak Reverse Current | - | - | - | - | IRRM |
| Reverse Breakdown Current | - | ${ }^{\prime}(\mathrm{BR}) \mathrm{R}$ | - | i(BR)R | - |
| On-State Voltage | $\mathrm{V}_{\mathrm{T} \text { (RMS) }}$ | $\mathrm{V}_{\mathrm{T}}$ | $\mathrm{V}_{\mathrm{T}(\mathrm{AV})}$ | vT | $V_{\text {TM }}$ |
| Breakover Voltage | - | $V_{(B O)}$ | - | v (BO) | - |
| Off-State Voltage | $\mathrm{V}_{\mathrm{D}}(\mathrm{RMS})$ | $V_{D}$ | $\mathrm{V}_{\mathrm{D}}(\mathrm{AV})$ | vD | $\mathrm{V}_{\text {DM }}$ |

Letter Symbol Table (Continued)


Letter Symbol Table (Continued)

| QUANTITY | TOTAL RMS VALUE | $\begin{gathered} \text { DC VALUE, } \\ \text { NO } \\ \text { ALTERNATING } \\ \text { COMPONENT } \end{gathered}$ |  | INSTANTANEOUS TOTAL value | MAXIMUM (PEAK) TOTAL VALUE |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Gate Trigger Current | - | IGT | - | igT | IGTM |
| Gate Non-Trigger Current | - | IGD | - | igo | IGDM |
| Gate Turn-Off Current | - | IGO | - | igo | IGQM |
| Gate Voltage | - | $\mathrm{V}_{\mathrm{G}}$ | $\mathrm{V}_{\mathrm{G}}(\mathrm{AV})$ | vG | $\mathrm{V}_{\mathrm{GM}}$ |
| Gate Trigger Voltage | - | $\mathrm{V}_{\mathrm{GT}}$ | - | vGT | $V_{\text {GTM }}$ |
| Gate Non-Trigger Voltage | - | $V_{G D}$ | - | vGD | $V_{\text {GDM }}$ |
| Gate Turn-Off Voltage | - | $\mathrm{V}_{\mathrm{GQ}}$ | - | vGQ | VGQM |
| Gate Power Dissipation | - | $\mathrm{PG}_{\mathrm{G}}$ | PG(AV) | PG | PGM |
| Turn-On Dissipation | - | - | PTT(AV) | PTT | PTTM |
| Turn-Off Dissipation | - | - | Pro(AV) | PRQ | PROM |

## Specific Definitions Used in International Rectifier Data Sheets

ITSM
Peak One-Cycle Non-Recurrent Surge Current. The maximum on-state current having a single half cycle ( 8.3 milliseconds) duration for a 60 Hz , single phase resistive load. The surge may be preceded and followed by maximum rated voltage, current, and junction temperature conditions and maximum allowable gate power may be concurrently dissipated. However, limitations with respect to on-state current during switching should not be exceeded.
$\mathrm{I}^{2} \mathrm{t} \quad I$ Squared $t$. A measure of maximum on-state non-recurrent over-current capability for pulse durations between 1.5 and 8.3 milliseconds. I is in RMS amperes and $t$ is pulse duration in seconds. (The same conditions as listed above for ITSM apply.)

IRQM Peak Reverse Recovery Current. The peak reverse current obtained when instantaneously switching from an on-state current to a reverse voltage in a given circuit.

VAM Peak Anode Voltage. The maximuminstantaneous va lue of principal voltage which may be applied to the anode. If breakover occurs at this voltage or at some lower value, no damage to the SCR will result. If a higher voltage is applied and breakover occurs, the SCR may be damaged.
$\mathrm{V}_{\mathrm{TO}}$ Turn-On Voltage. The principal voltage at some specified principal current and at some specified time during the transition between the off-state and the on-state.

Figure 1. Reverse Voltage Symbols

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Figure 2. Instantaneous Forward and Reverse Characteristics (Reverse Blocking Thyristor)


Figure 3. Anode Voltage and Current Waveforms During Turn-On Time Test


Figure 4. Anode Voltage Waveform During Critical dv/dt Test


Figure 5. Anode Voltage and Cur-
Waveforms During Turn-Off Time Test

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Silicon Controlled Rectifiers

## Power Triacs



International Rectifier offers a broad and growing range of SCR types and ratings to serve SCR users, with new series of SCRs being added to this edition for low, medium, high power and inverter applications.
INVERTER SERVICE SCRs are listed in a separate summary table on page 6, in addition to being defined by notes within the main tables.

| $1_{\text {T/Rms) ( }}(\mathrm{A})$ | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 4.0 | 4.7 | 4.7 | 7.4 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\operatorname{Max}}(\mathrm{AV})(\mathrm{A}) \times(\mathrm{O})$ $\text { Max. } \mathrm{T}_{\mathrm{C}}=\left({ }^{\circ} \mathrm{C}\right)$ | $\begin{aligned} & 1.00 \\ & 800^{\circ} \\ & \hline \end{aligned}$ | $\begin{gathered} 1.00 \\ 800 \end{gathered}$ | $\begin{aligned} & 1.09 \\ & 850 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.00 \\ & 850 \end{aligned}$ | $\begin{aligned} & 1.0 e \\ & 850 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.0 \because \\ & 850 \\ & \hline \end{aligned}$ | $\begin{gathered} 2.55 e \\ 300 \end{gathered}$ | $\begin{gathered} 3.09 \\ 800 \\ \hline \end{gathered}$ | $\begin{aligned} & \hline 3.09 \\ & 1050 \\ & \hline \end{aligned}$ | $\begin{aligned} & 4.7 e \\ & 60^{\circ} \\ & \hline \end{aligned}$ |
| Max. $16 T$ © $25^{\circ} \mathrm{C}$ (mA) | 10 | 2 | 0.2 | 0.2 | 1 | 0.1 | 0.2 | 10 | 15 | 15 |
| dv/dt (V/ms), typical | 20 | 20 | 20 | 20 | 20 | 20 | 8 | 20 | 20 | 20 |
| ITSM (A) | 15 | 15 | 15 | 15 | 10 | 15 | 25 | 25 | 40 | 60 |
| Notes | (1) | (1) | (1) | (1) | (1) | (1) | (1) (2) | - | - | - |
| Cone Stylo | T0.5 | T0.5 | T0.5 | T0.5 | T0.5 | T0.5 | A-2 | 10.54 | T0.64 | T0.64 |
|  |  | 2N1595A 2N1596A | IRSU <br> IRSF <br> IR5A | $\begin{aligned} & 2 N 2322 \\ & \begin{array}{l} 2 N 2323 \\ 2 N 2324 \end{array} \end{aligned}$ | $\begin{aligned} & \text { IREU } \\ & \text { IR6F } \\ & \text { IREA } \end{aligned}$ | $\begin{aligned} & 2 \mathrm{~N} 4212 \\ & 2 N 4213 \\ & 2 \mathrm{~N} 4214 \end{aligned}$ | IR106a1 <br> 1R106Y1 IR106F1 <br> iR106A | 2N1600 <br> 2N1601 | 3RC10A | 2 2M1770 201771 221772 |
| 150 Volts 250 Voits 300 Volts 400 Volts | $\begin{aligned} & 2 \mathrm{~N} 1597 \\ & \text { 2N } \mathrm{N} 598 \\ & 2 \mathrm{~N} 1599 \end{aligned}$ | 2N1597A <br> 2N1598A 2N1599A |  | 2N2325 222326 $2 N 2327$ 2N2328 $2 N 2329$ |  | 2N4215 2N4216 2N4217 2N4218 2N4219 | \|R106B1 <br> IR106C1 IR106D1 | $\begin{aligned} & 2 \mathrm{~N} 1602 \\ & 2 \mathrm{~N}, 603 \\ & 2 \mathrm{~N} 1604 \end{aligned}$ | 3RC20A <br> 3RC30A <br> 3RC40A | 2217773 $2 N 1774$ $2 N 1775$ $2 N 176$ $2 N 1777$ $2 N 17$ |
| 500 Volts 500 Volts | - | - | - | - | - | - | - | - | $\begin{aligned} & \text { 3RC50A } \\ & 3 \mathrm{RC60A} \end{aligned}$ | $\frac{2 N 1778}{2 N 2619}$ |
| $I_{\text {T }}$ (RMSS ( ${ }^{\text {( }}$ ) | 1.4 | 1.4 | 8.0 | 16 | 16 | 25 | 25 | 25 | 25 | 25 |
| ${ }^{\prime}$ TIAV) (A) Max. $\left.\mathrm{T}_{\mathrm{C}}={ }^{\circ}{ }^{\circ} \mathrm{C}\right)$ | $\begin{aligned} & 4.7 \\ & 800 \end{aligned}$ | $\begin{aligned} & 4.7 @ \\ & 1050 \\ & \hline \end{aligned}$ | $\begin{gathered} 5.1 e \\ 85^{\circ} \\ \hline \end{gathered}$ | $\begin{aligned} & 10 @ \\ & 350 \\ & \hline \end{aligned}$ | $\begin{gathered} 100 \\ 800^{\circ} \\ \hline \end{gathered}$ | $\begin{aligned} & 169 \\ & 450 \\ & \hline \end{aligned}$ | $\begin{aligned} & 16 \ominus \\ & 65^{\circ} \\ & \hline \end{aligned}$ | $\begin{gathered} 16 e \\ 95^{\circ} \\ \hline \end{gathered}$ | $\begin{array}{r} 16 e \\ 950 \\ \hline \end{array}$ | $\begin{array}{r} 169 \\ 950 \\ \hline \end{array}$ |
| Max. $16 T \mathrm{C}^{\text {P } 25^{\circ} \mathrm{C}(\mathrm{mA})}$ | 15 | 15 | 25 | 90 | 75 | 90 | 40 | 25 | 25 | 25 |
| dv/dt (V/usec), typital | 20 | 20 | 50 (min.) | 20 | 20 | 10 (min.) | 20 | 20 | 20 | 20 |
| ITSM (A) | 75 | 60 | 80 | 125 | 125 | 200 | 150 | 250 | 250 | 250 |
| Notes | - | (1) | - | - | - | - | $\dagger$ | - | - | - |
| Case Style | 10-64 | T0.64 | T0-200AB | T0-48 | T0.48 | T0-48 | T0 48 | A.8A | A.8B | T0.203AA |
|  |  | ${ }_{2}^{2 N 1770 A}$ 2N1772A 2N1773A 2 N 1774 A | IR122F IR122A <br> IR122B | $\begin{aligned} & \text { 2N 1842 } \\ & \text { 2N1843 } \\ & \text { 2N1844 } \\ & \text { 2N1845 } \\ & \text { 2N1846 } \end{aligned}$ | 2N1842A 2N1844A 2N1845A 2N $1846 A$ |  |  | $\begin{aligned} & \text { IR30U } \\ & \text { R1R30F } \\ & \text { R } 30 \mathrm{~A} \\ & \text { IR308 } \end{aligned}$ | 1R30U2 iR30A2 IR30B2 | IR32U IR3F IR32A IR32B In |
| 250 Volts 400 Volts 500 Volts 600 Volts 600 Voits | 5RC30A 5RC40A 5RC50A 5RC60A | $\begin{aligned} & \text { 2N1775A } \\ & \text { 2N1776A } \\ & \text { 2N1717A } \\ & \text { 5RC50B } \\ & 5 R C 60 B \end{aligned}$ | 1R122C IR1220 | $2 N 1847$ 221848 $2 N 1849$ $2 N 1850$ | 2N1847A 2N1848A 2N1849A 2N 1850 A | 10RC30A 10RC40A 10RC60A $\qquad$ | 2N686 2N687 $2 N 68$ 2N639 2N690 | $\begin{aligned} & \text { IR30C } \\ & \text { iR300 } \\ & \text { IR30E } \end{aligned}$ | $\begin{aligned} & \text { IR } 30 C 2 \\ & \text { IR3002 } \\ & \text { IR30E2 } \\ & - \end{aligned}$ | $\begin{aligned} & \text { IR32C } \\ & \text { iR320 } \\ & \text { IR32E } \end{aligned}$ |
| 700 Volts 1000 Volts 1100 Volts | $=$ $=$ $=$ |  | - | Z |  | $\begin{aligned} & \text { 10RC70A } \\ & 10 R C 80 \mathrm{~A} \\ & 10 R \mathrm{Cl100} \\ & 10 \mathrm{RCl110A} \\ & 10 \mathrm{RCl20A} \end{aligned}$ | $\begin{aligned} & \text { 2N691 } \\ & 2 N 692 \end{aligned}$ | = | Z | $\overline{=}$ |

## Silicon Controlled Rectifiers <br> Power Triacs



| $I_{\text {T (RMS) }}(\mathrm{A})$ | 25 | 35 | 35 | 35 | 35 | 35 | 35 | 35 | 35 | 35 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IT(AV) (A) © Max. $\mathrm{T}_{\mathrm{C}}={ }^{\circ} \mathrm{C}$ ) | $\begin{aligned} & 16 e \\ & 950 \\ & \hline \end{aligned}$ | $\begin{gathered} 22 @ \\ 35^{\circ} \end{gathered}$ | ${ }_{650}^{229}$ | $\begin{gathered} 22 e \\ 650 \end{gathered}$ | $\begin{aligned} & 229 \\ & 700 \\ & 70 \end{aligned}$ | $\begin{gathered} 22 @ \\ 85^{20} \end{gathered}$ | $\begin{array}{r} 22 \text { @ } \\ 85^{\circ} \\ \hline \end{array}$ | $\begin{array}{r} 25 \mathrm{dc} @ \\ 400 \\ \hline \end{array}$ | $\begin{gathered} 25 \mathrm{dc} @ \\ 400 \\ \hline \end{gathered}$ | $\begin{gathered} 25 \mathrm{dc} @ \\ 40^{\circ} \\ \hline \end{gathered}$ |
| Max. $\mathrm{IGT}^{\text {¢ }}{ }^{\text {® }} 25^{\circ} \mathrm{C}$ (mA) | 25 | 40 | 40 | 40 | 40 | 40 | 40 | 180 | 180 | 180 |
| $\mathrm{dv} / \mathrm{dt}(\mathrm{V} / \mu \mathrm{s})$, min. | 20 (typ.) | 10 | 10 | 10 | 20 | 20 | 20 | 200 | 200 | 200 |
| 1 ISM (A) | 250 | 300 | 350 | 350 | 250 | 350 | 350 | 180 | 180 | 180 |
| Notes | - | - | - | - | ( | - | - | (3) | (1) | (3) |
| Case Styla | A. 17 | T0.48 | T0.203AA | A.8A | A. 1 | A. 17 | A.8B | A.8B | A.8B | A.8B |
| 25 Volts 100 Volts 300 Volts |  | 16RC5A 16RC10A 16RC20A 16RC30A $\qquad$ | 2N3870 2N3871 |  |  | 20RA5 20RA10 20RA20 | 22RA5 <br> 22RA10 22RA20 <br> 22RA30 | IR140U IR140F IR140A $\underset{\text { IR140C }}{1 \text { IR }}$ | 2N 2649 2N 2650 2N 3651 $2 N 3652$ <br> 2N3652 | IR141UIR141F IR141AIR1418 <br> IR141C |
| 400 Voits 500 Volts 700 Volts $\qquad$ | $\begin{aligned} & \text { 1R3202 } \\ & \text { 1R32E2 } \end{aligned}$ = | 16RC40A $16 R C 50 A$ 16RC60A <br> 16RC80A | 2N3872 <br> 2N3873 <br> - | $\begin{aligned} & \text { 2N3898 } \\ & \text { 2N3899 } \end{aligned}$ | $\begin{aligned} & \text { 22RC40 } \\ & \text { 22RC50 } \\ & \text { 22RC60 } \end{aligned}$ | $\begin{aligned} & \text { 20RA40 } \\ & \text { 20RA50 } \\ & \text { 20RA60 } \\ & \text { 20RA70 } \\ & \text { 20RA80 } \end{aligned}$ | $\begin{aligned} & \text { 22RA40 } \\ & \text { 22RA50 } \\ & \text { 22RA60 } \\ & \text { 22RA70 } \\ & \text { 22RAB0 } \\ & \hline \end{aligned}$ | IR1400 | 2N3653 | IR1410 |
| 1000 Volts 1200 Volts |  | 16RC100A 16RC120A | - | = | - | - | - | - | = | - |
| $I_{\text {T (RMSS) (a) }}$ | 35 | 63 | 80 | 80 | 80 | 80 | 110 | 110 | 110 | 110 |
| $\begin{aligned} & { }^{T}(A V)(A) @ \\ & \text { Max. } T_{C}=\left({ }^{\circ} \mathrm{C}\right) \end{aligned}$ | $\begin{gathered} 25 \mathrm{dc} @ \\ 400^{\circ} \\ \hline \end{gathered}$ | $\begin{aligned} & 409 \\ & 870 \\ & 8 \end{aligned}$ | $\begin{aligned} & \hline 50 @ \\ & 750 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 50 @ \\ & 750 \\ & \hline \end{aligned}$ | $\begin{aligned} & 50 @ \\ & 870 \\ & \hline \end{aligned}$ | $\begin{aligned} & 50 @ \\ & 1050 \\ & \hline \end{aligned}$ | $\begin{aligned} & 70 @ \\ & 62^{\circ} \\ & \hline \end{aligned}$ | $\begin{aligned} & 70 @ \\ & 620 \\ & \hline \end{aligned}$ | $\begin{aligned} & 70 @ \\ & 62^{\circ} \\ & \hline \end{aligned}$ | $\begin{array}{r} 70 @ \\ 650 \\ \hline \end{array}$ |
| Max. $1 \mathrm{GT} \mathrm{C}^{\text {2 }} 5^{\circ} \mathrm{C}$ (mA) | 180 | 110 | 70 | 200 | 110 | 200 | 70 | 70 | 110 | 150 |
| dv/dt ( $\mathrm{V} / \mathrm{/ss}$ ), min. | 200 | 20 | 20 | 200 | 25 | 4 | 20 | 20 (typ.) | 20 | 200 |
| ITSM (A) | 180 | 1,000 | 1,000 | 1,200 | 1,200 | 1,000 | 1,200 | 1,000 | 1,000 | 1,200 |
| Companion Series | - | - | 37RC-A | 37RA. | - | 37REH | 72 RC - A | - | - | 72R8 |
| Notes | (3) | - | (4) | (3) | - | (5) | (4) | 1 | $\dagger$ | (3) |
| Casa Style | A 88 | T0.65 | A-13 | A-11 | T0-65 | A. 11 | A. 13 | A. 13 | A. 11 | A. 11 |
|  | $\begin{aligned} & \text { 2N }-\quad \\ & \text { 2N3654 } \\ & \text { 2N } 3655 \\ & \hline \end{aligned}$ |  |  |  | 50RCS5 <br> 50RCS10 <br> 50RCS20 |  |  |  | - |  |
| 250 Volts 400 Volts 500 Volts 600 Volts 600 Voirs | $\begin{array}{r} \text { 2N3657 } \\ 2 N 3658 \end{array}$ |  |  | 36RA50 36RA60 | 50RCS30 50RCS40 50RCS50 50 RCS60 50 c 6 |  | 71RC30A 71RCC0A 71RC50A 71RC60A | 2N1914 2N1915 2N1916 2N1805 2N1806 |  |  |
|  | - |  | 36AC80A <br> $=$ <br> $=$ | 36RABO <br> 36RA 100 <br> 36RA110 |  | 36REH80 <br> 36REH 100 36REH 110 | 71RC8oa | 2N1807 | 2N3092 2N3093 2N3094 2N3095 2N3096 | 71R880 <br> 71RB100 <br> 71RB110 |
| 1200 Volts 1300 Volts 1500 Volts 1600 Volts | - $=$ | 40RCS120 $=$ $=$ $=$ | - | $\begin{aligned} & \text { 36RA120 } \\ & \text { 36RA130 } \\ & \text { 36RA110 } \\ & \text { 36RA150 } \\ & \text { 36RA160 } \end{aligned}$ | 50RCS120 <br> - <br> - <br> - | 36REH 120 36REH 130 | - | - | 2N3907 2N3908 |  |

Silicon Controlled Rectifiers
Powar Triacs
T0-94 (A-11)

| $\mathrm{IT}_{\text {(Rms) ( }}(\mathbf{A})$ | 110 | 110 | 110 | 110 | 110 | 125 | 125 | 125 | 150 | 160 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & 1 T(A V)(A) Q \\ & M a x C=(O C) \end{aligned}$ $\operatorname{Max} . T_{C}=(O C)$ | $\begin{aligned} & 709 \\ & 650 \end{aligned}$ | $\begin{gathered} 7009 \\ 800 \end{gathered}$ | $\begin{gathered} 709 \\ 850 \end{gathered}$ | $\begin{gathered} 700 \\ 850 \end{gathered}$ | $\begin{aligned} & 70 \ominus \\ & 1050 \\ & \end{aligned}$ | $\begin{aligned} & 800 \\ & 700 \end{aligned}$ | $\begin{aligned} & 80 \otimes \\ & 700 \end{aligned}$ | $\begin{gathered} 806 \\ 850 \\ 85 \end{gathered}$ | $\begin{aligned} & 958 \\ & 650 \\ & \hline 8 \end{aligned}$ | $\begin{aligned} & 1000 \\ & 800 \end{aligned}$ |
| $1 \mathrm{GT} \mathrm{P}^{25^{\circ} \mathrm{C}}$ (mA) | 70 | 150 | 70 | 70 | 150 | 150 | 150 | 150 | 150 | 250 |
| dv/dt ( $V / / \mu s)$, min. | 20 (typ.) | 200 | 20 | 20 (typ.) | 50 | 200 | 200 | 200 | 200 | 200 |
| $\mathrm{I}_{\text {TSM }}(\mathrm{A})$ | 1,000 | 1,600 | 1,000 | 1,000 | 1,400 | 1,600 | 1,600 | 1,800 | 1,800 | 2,500 |
| Companion Series | - | 72RA | 72RC-B | - | 72REH | 82RLB | 82RM/1182RL | 82RLA | 92RM/9192RL | - |
| Notas | $\dagger$ | (5) | (1) 1 | (1) $\dagger$ | (3) (1) | (3) (3) (1) | (1) (3) (1) (1) | (1) (1) | (3) (3) (1) | - |
| Case Style | A.14 | A. 11 | A. 13 | A. 13 | A. 11 | A. 11 | A. 11 | A. 11 | A. 11 | T0.93 |
| 25 Volts 50 V Vols 100 Volts 150 V Volts 200 Volts | $\begin{aligned} & 2 N 1792 \\ & 221793 \\ & 21794 \\ & 2 N 1794 \end{aligned}$ |  | 71RC2B <br> 71RC58 <br> 71RC108 <br> 71RC158 <br> 71RC20B | 2N2023 2N2024 2N2025 2N2026 2N2027 | $\bar{Z}$ |  | 81RM10 <br> 81RM20 |  | 91RM10 91RM20 |  |
| 250 Volts 400 Volts 500 Volts 600 Volts 600 Voits | 2N1796 2N1797 21798 $2 N 1799$ $2 N 1800$ |  | $\square$ | $\begin{aligned} & \text { 2N2028 } \\ & \text { 2N2029 } \\ & \text { 2N2030 } \end{aligned}$ | 7IREM6O | 81RLB50 81RLB60 | $\begin{aligned} & \text { 81RM30 } \\ & \text { BiRM40 } \\ & \text { BiRM50 } \\ & \text { B1RMG60 } \end{aligned}$ | 81RLA50 <br> 81RLA60 | 91 RM30 91RM50 91RM60 | 101RA50 <br> 101RA60 |
| 700 Volts 800 Volts 900 Volts 1000 Volts 1100 Volts |  | 71RA80 <br> 71RA100 <br> 71RA110 |  |  | 71REH80 <br> 71REH100 <br> 71REH11 | sirlbbo <br> 81RLB100 81RLB110 | 81RM80 81RM100 | 81RLABO <br> 81RLA100 <br> 81RLA110 | Z | 101RA80 <br> 1018A100 101RA110 |
| 1200 Volts 1400 Volts 1500 Volts |  |  | - |  | $\begin{array}{\|c} \text { 71REH120 } \\ \text { T1REH130 } \\ = \\ - \end{array}$ | 81RLB120 | - | $\begin{gathered} \text { 81RLA120 } \\ = \\ = \end{gathered}$ |  | 101RA120 101RA130 $1018 A 140$ $101 R A 150$ $101 R A 160$ 101R1 |

Silicon Controlled Rectifiers Power Triacs

| $1_{\text {TIRMS }}(\mathrm{A})$ | 160 | 180 | 210 | 210 | 235 | 235 | 235 | 235 | 235 | 245 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ITAV) (A) © Max. $\mathrm{T}_{\mathrm{C}}=\left({ }^{\circ} \mathrm{C}\right)$ | $\begin{gathered} 100 e \\ 800 \end{gathered}$ | $\begin{gathered} 115 \\ 850 \end{gathered}$ | $\begin{array}{r} 135 e \\ 650 \\ \hline \end{array}$ | $\begin{gathered} 1359 \\ 650 \end{gathered}$ | $\begin{gathered} 150 @ \\ 700 \end{gathered}$ | $\begin{gathered} 1500 \\ 800 \\ \hline \end{gathered}$ | $\begin{gathered} 150 \circledast \\ 850 \\ \hline \end{gathered}$ | $\begin{gathered} 1500 \\ 75^{\circ} \end{gathered}$ | $\begin{gathered} 150 e \\ 900 \\ 90 \end{gathered}$ | $\begin{aligned} & 155 @ \\ & 180^{\circ} \\ & \hline \end{aligned}$ |
| $1 \mathrm{GT} \mathrm{P}^{25} 5^{\circ} \mathrm{C}(\mathrm{mA})$ | 150 | 150 | 150 | 150 | 150 | 150 | 150 | 200 | 200 | 150 |
| $\mathrm{dv} / \mathrm{dt}(\mathrm{V} / \mathrm{sus})$, min. | 20 | 200 | 200 | 200 | 20 | 20 | 200 | 200 | 200 | 200 |
| ITSM (A) | 2,000 | 1,600 | 1.600 | 1,600 | 3,000 | 3,500 | 4.250 | 3,300 | 4.250 | 4,000 |
| Companion Series | - | - | - | 125PAL | - | - | - | - | - | 151AL |
| Notes | - | - | (3) (1) | (1)(1)(1) | - | - | - | - | (3) | (3) (1) |
| Cose Style | 10.93 | T0.200AB | T0.200AB | to-200AB | T0.93 | 10.93 | 10.93 | 10.93 | T0.93 | 10.93 |
| 50 Volts 150 Volts 200 Volts 250 Volts | 1014c10 <br> 1018C20 | $\begin{aligned} & 115 \overline{\text { PA A } 10} \\ & 115 \text { PA A } 20 \end{aligned}$ | $\bar{Z}$ | 125PAM10 <br> 125PAM20 | 151RC10 <br> 151RC20 | 151RC10A <br> 151RC20A |  | - <br> - | 151RF5 151RF10 151RF15 151RF20 151RF25 $\qquad$ |  |
| 300 Volts 500 Volts 800 Volts | 101RC30 101RC40 $101 R C 50$ $101 R C 60$ $101 R C 80$ | $115 P A 30$ $115 P A 40$ $115 P A 50$ $115 P A 60$ $115 P A 80$ | $\begin{aligned} & \overline{-} \\ & \text { 125PALB50 } \\ & \text { 125PALB60 } \\ & \text { 125PALB80 } \end{aligned}$ |  | 151RC30 $151 R C 40$ $151 R C 50$ $15 R C 60$ $151 R C 80$ | 151RC30A 151RC50A 151RC60A 151RC80A | 151RA50 <br> 151RA60 <br> 151RA80 | 151R850 151RB60 151R880 | 151RF30 151RF50 151RF60 | 151RM50 151RM60 151RM80 |
| 1000 Volts 1200 Vols 1400 Volt |  | $115 P A 100$ $115 P^{2} A 120$ $115 P A 130$ $15 P A 140$ | 125PALB100 125 PALB110 125PALB120 | 125PAM100 |  | Z | 151RA100 151RA120 151RA140 | 151R8100 151R8120 151RB140 | I - | 151RM100 151 RM110 151RM120 = |
| $\begin{aligned} & 1500 \text { Volts } \\ & 1600 \text { Volts } \end{aligned}$ | Z | $\begin{array}{\|l\|} \hline 115 P A 150 \\ 115 P A 160 \\ \hline \end{array}$ | - | - | - | Z | 151RA150 151RA160 | 151RB150 151RB160 | $\vdots$ | - |


| $I_{\text {T }}^{\text {(RMS }}$ ) (A) | 250 | 275 | 275 | 285 | 400 | 400 | 400 | 400 | 450 | 455 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & { }^{1}(A V)(A) P \\ & M a x . T_{C}=\left({ }^{\circ} \mathrm{C}\right) \end{aligned}$ | $\begin{gathered} 100 e \\ 650 \end{gathered}$ | $\begin{gathered} 175 \odot \\ 85^{\circ} \end{gathered}$ | $\begin{gathered} 175 @ \\ 90^{\circ} \end{gathered}$ | $\begin{gathered} 180 @ \\ 750 \end{gathered}$ | $\begin{gathered} 250 e \\ 650 \end{gathered}$ | $\begin{gathered} 2500 \\ 750 \end{gathered}$ | $\begin{gathered} 2500 \\ 700 \end{gathered}$ | $\begin{gathered} 255 \text { e } \\ 650 \end{gathered}$ | $\begin{gathered} 285 e \\ 700 \end{gathered}$ | $\begin{aligned} & 295 e \\ & .650 \end{aligned}$ |
| ${ }_{\mathrm{G}} \mathrm{T}$ ¢ $25^{\circ} \mathrm{C}(\mathrm{mA})$ | 150 | 200 | 150 | 150 | 150 | 150 | 150 | 150 | 150 | 150 |
| dV/dt (V/us), min. | 200 | 200 | 200 | 200 | 20 | 100 | 200 | 200 | 200 | 200 |
| ITSM (A) | 1,800 | 3,300 | 5,000 | 4.500 | 4.000 | 6,500 | 4.250 | 4,000 | 8,000 | 4,500 |
| Companion Series | 140 PAL | - | - | 161 RL | - | - | - | 240 PAL | 250RL | 250 PaL |
| Notes | (3) (1) | - | - | (3) (1) | - | - | - | (3) (1) | (3) (b) | (3) 5 |
| Cose Styie | 10.200AB | 10.200AB | 70.93 | T0.93 | T0-200AB | 10.418 | T0-200AB | T0-200AB | T0.118 | T0-200AB |
| 100 Volts 300 Volts 400 Volts 500 Volts 500 Valts | 140PAM10 140P AM 20 140PA30 140P AMM 140P AM 50 |  |  | $\begin{aligned} & \hline \text { 161RM10 } \\ & \text { 1612M20 } \\ & \text { 161RM30 } \\ & \text { 161RM40 } \\ & \text { 161RM50 } \end{aligned}$ |  | $\begin{aligned} & \text { 250RA10 } \\ & \text { 250RAD } \\ & \text { 250RA30 } \\ & \text { 250RAO } \\ & \text { 250RA50 } \\ & \hline \end{aligned}$ |  | 240PAM10 240PAM20 240PAM 30 240PAM40 240PAM50 | $\begin{aligned} & \bar{Z} \end{aligned}$ | 250PAM10 25PAM20 25PAM 20 25PPAM40 250PAM50 |
|  | 140PAM60 |  |  | 161RM60 |  |  |  | 240PAM60 240PAM80 240P AM 100 |  | 250PAM60 $\vdots$ $=$ - |
|  |  | 175PA130 175PA 150 175PA160 |  |  |  | $\begin{aligned} & \text { 250RA } 130 \\ & \text { 250RA40 } \\ & \text { 250RA } 150 \\ & \text { 250RA150 } \\ & \text { 20RR A170 } \end{aligned}$ | $\begin{aligned} & \text { 250PA130 } \\ & \text { 250PA140 } \\ & \text { 250PA150 } \\ & \text { 250PA150 } \end{aligned}$ | Z | = | $=$ $=$ |

\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \(I_{\text {T/(Rms) ( }}(\mathrm{A})\) \& 470 \& 470 \& 470 \& 470 \& 550 \& 660 \& 710 \& 740 \& 785 \& 785 \\
\hline \[
\begin{aligned}
\& { }^{1 T}(A V)(A) @ \\
\& M a x . T_{C}=\left({ }^{\circ} \mathrm{C}\right)
\end{aligned}
\] \& \[
\stackrel{300}{ } n^{\circ}
\] \& \[
\begin{gathered}
300 \times \\
700 \\
\hline 0
\end{gathered}
\] \& \[
\begin{gathered}
3000 \\
750
\end{gathered}
\] \& \[
\begin{gathered}
3000 \\
750 \\
\hline
\end{gathered}
\] \& \[
\begin{gathered}
350 \circledast \\
750 \\
\hline
\end{gathered}
\] \& \[
\begin{aligned}
\& 4200 \\
\& 680 \\
\& \hline
\end{aligned}
\] \& \[
\begin{gathered}
450 @ \\
650 \\
\hline
\end{gathered}
\] \& \[
\begin{gathered}
4700 \\
670 \\
\hline
\end{gathered}
\] \& \[
\begin{gathered}
5000 \\
650 \\
\hline 650
\end{gathered}
\] \& \[
\begin{gathered}
5000 \\
650 \\
65
\end{gathered}
\] \\
\hline \({ }_{6} \mathrm{~T}^{\text {¢ }} 2^{\circ}{ }^{\circ} \mathrm{C}(\mathrm{mA})\) \& 150 \& 150 \& 150 \& 150 \& 150 \& 150 \& 150 \& 150 \& 150 \& 150 \\
\hline dv/dt (V/us), min. \& 200 \& 20 \& 100 \& 100 \& 100 \& 100 \& 200 \& 100 \& 500 \& 500 \\
\hline ITSM (A) \& 5,500 \& 5,000 \& 8,000 \& 7,000 \& 8,000 \& 6,500 \& 8,000 \& 7,00 \& 7,500 \& 7,500 \\
\hline Companion Series \& - \& - \& - \& - \& - \& - \& 420 PBL \& - \& - \& - \\
\hline Notes \& - \& - \& - \& - \& - \& - \& (1) (b) \& - \& (3) (11) \& (1). (II) \\
\hline Case Style \& T0.200AB \& T0-200AB \& T0.118 \& 10.118 \& T0.118 \& T0.200AC \& T0-200AC \& T0.200AC \& T0-200AC \& T0-200AC \\
\hline 100 Valts 300 Volts 400 Volts
500 Volts \& 300PA50 \& \(300 \mathrm{PAC10}\) 300PAC30 300PACA
300PA \& 300RA10 300RA30 300RA40
300RA50 \& \[
\begin{array}{|l|}
\hline 300 R B 10 \\
300 R R 20 \\
30 R B 230 \\
300 R R 40 \\
300 R B 50
\end{array}
\] \& 350RA10
350RA20
35RA 30
35RA40
350RA50 \&  \& \[
\begin{gathered}
\bar{Z} \\
\text { 420РBM50 }
\end{gathered}
\] \&  \& 500РBQ50 \& 501p8050 \\
\hline \begin{tabular}{l}
600 Volts
800 Volts \\
1000 Volts \\
1200 Volts
\end{tabular} \& \(300 \mathrm{PA60}\)
300 PA 80 300 PA 100
300 PA 110 300 PA 12 \& 300PAC60 \&  \& 300RB60
300RB80
300RB100
30008100
300R8120 \& \({ }^{350 R A 60}\) 350RA100 350RA120 \&  \& 420P8M60
420PM
420P
420PM100
420PM110
420PBM120 \&  \&  \&  \\
\hline 1300 Volts
1400 Volts 1500 Velts 1700 Volt \& ב
-
- \& - \& \[
\begin{aligned}
\& \text { 300RA130 } \\
\& \text { 30RA140 } \\
\& \text { 30RA } \\
\& \text { 30RA A 150 } \\
\& \text { 300RA150 } \\
\& \text { 300RA A177 }
\end{aligned}
\] \& 300R8130
30RBB140
300RB150
300RB650
300RB170 \& \[
\begin{aligned}
\& \text { 350RA130 } \\
\& \text { 350RA140 } \\
\& \text { 350RA150 } \\
\& \text { 350RA150 } \\
\& \text { 350RA170 }
\end{aligned}
\] \&  \& I- \&  \& \(=\)

$=$ \& ב
ב

- <br>
\hline
\end{tabular}


## Silicon Controlled Rectifiers <br> Power Triacs




## Silicon Controlled Rectifiere

## Power Triacs

SCRs FOR INVERTER SERVICE
There is an ever-increasing number of inverter circuits which demand more sophisticated devices operating under more stringent dynamic circuit conditions. Many IR devices are designed, custom built, and tested to meet these demanding applications. In addition, units may be selected for specific parameters from standard product runs.

The table below includes IR series specifically designed for in verter service. In specific cases, the second letter of the part number code is changed to indicate a change in $t_{q}$ rating.

For the best solution to your problems in standard, selected, or ustom devices, contact your local IR Distributor, or local IR Field Office, or IR's EI Segundo offices.

SILICON CONTROLLED RECTIFIERS FOR INVERTER SERVICE

| MAX. CURRENT RMS (A) | VOLTAGE RANGE | MAX. TURN-OFF TIME $\mathrm{t}_{\mathrm{q}}=\mu \mathrm{s}$ | dv/dt ( $\mathrm{V} / \mathrm{\mu s}$ ) | CASE | in SERIES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} 35 \\ 35 \\ 35 \\ 35 \\ 125 \\ \hline \end{array}$ | $\begin{gathered} 50-600 \\ 50.400 \\ 50-600 \\ 50.400 \\ 100-1000 \\ \hline \end{gathered}$ | $\begin{aligned} & 10 \\ & 10 \\ & 15 \\ & 15 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \\ & \hline \end{aligned}$ | $\begin{aligned} & A-8 B \\ & A-8 B \\ & A-8 B \\ & A-8 B \\ & T O-94(A-11) \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { IR141 } \\ & \text { 2N3654-58 } \\ & \text { 1R140-5 } \\ & \text { 2N3649-53 } \\ & \text { 81/82RM } \\ & \hline \end{aligned}$ |
| $\begin{aligned} & 125 \\ & 125 \\ & 150 \\ & 150 \\ & 160 \\ & \hline \end{aligned}$ |  | 30 40 10 20 20 | 200 200 200 200 200 | $\begin{aligned} & \text { TO-94 (A-11) } \\ & \text { TO-94 }(\mathrm{A}-11) \\ & \text { TO-94 }(\mathrm{A}-11) \\ & \text { TO-94(A-11) } \\ & \text { TO-200AB } \end{aligned}$ | $81 / 82 R \mathrm{LL}$ <br> 81/82RLB <br> $91 / 922 \mathrm{~B}$ <br> 91/92RL <br> 100PAM <br>  |
| $\begin{aligned} & 160 \\ & 210 \\ & 210 \\ & 210 \\ & 235 \\ & \hline \end{aligned}$ | $100-1200$ $100-1200$ $100-1200$ $50-600$ | $\begin{aligned} & 30 \\ & 20 \\ & 30 \\ & 40 \\ & 20 \\ & \hline \end{aligned}$ | 200 200 200 200 200 | $\begin{aligned} & \text { TO-200AB } \\ & \text { TO-200AB } \\ & \text { TO-200AB } \\ & \text { TO-200AB } \\ & \text { TO-93 } \end{aligned}$ | 100PAL 125PAM 125PAL 125PALB 151RF |
| $\begin{aligned} & 245 \\ & 245 \\ & 250 \\ & 250 \\ & 285 \end{aligned}$ | $\begin{aligned} & 100-1200 \\ & 100-1200 \\ & 100-600 \\ & 100-600 \\ & 100-600 \end{aligned}$ | $\begin{aligned} & 20 \\ & 30 \\ & 10 \\ & 20 \\ & 10 \end{aligned}$ | $\begin{aligned} & 200 \\ & 200 \\ & 200 \\ & 200 \\ & 200 \end{aligned}$ | $\begin{aligned} & \text { TO-93 } \\ & \text { TO-93 } \\ & \text { TO-200AB } \\ & \text { TO-200AB } \\ & \text { T-. } 93 \end{aligned}$ | 151RM 151 RL 140PAM 140PAL 161 RM |
| 285 400 400 450 450 |  | $\begin{aligned} & 20 \\ & 25 \\ & 30 \\ & 40 \\ & 60 \\ & \hline \end{aligned}$ | 200 200 200 200 200 | $\begin{aligned} & \text { TO.93 } \\ & \text { TO-200AB } \\ & \text { TO. } 200 \mathrm{AB} \\ & \text { TO-118 } \\ & \text { T0.118 } \end{aligned}$ | 161RL 240PAM <br> 240PAL ${ }^{250 R M}$ |
| 455 455 660 660 785 |  | 10 20 40 60 15 | 200 200 200 200 500 | TO-200AB TO-200AB TO-200AC TO-200AC TO-200AC | $\begin{aligned} & \text { 250PAM } \\ & \text { 250PAL } \\ & \text { 420PBM } \\ & \text { 420PBL } \\ & \text { 550PBO } \end{aligned}$ |
| $\begin{aligned} & 785 \\ & 785 \end{aligned}$ | $\begin{aligned} & 500-1200 \\ & 500-1200 \end{aligned}$ | $\begin{aligned} & 30 \\ & 40 \end{aligned}$ | $\begin{aligned} & 500 \\ & 500 \end{aligned}$ | $\begin{aligned} & \text { TO-200AC } \\ & \text { TO-200AC } \end{aligned}$ | 501 PBO |

CROSS REFERENCE OF OBSOLETE PART NUMBERS TO NEW PART NUMBERS
The following part numbers have been discontinued since the previous edition of this Product Locator

| OLD PART NUMBER | $\underset{B Y}{\text { REPLACED }}$ | MAJOR DIFFERENCES OF REPLACEMENT PART TO ORIGINAL | OLD PART NUMBER | $\underset{\text { BY }}{\text { REPLACED }}$ | MAJOR DIFFERENCES OF REPLACEMENT PART TO ORIGINAL |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 35 RCS -A* | 37RC-A | 1/2-20 threaded stud, flag cathode | 420 PA | ${ }^{420 P B}$ | None: Change of nomenclature |
|  |  | ${ }_{1}^{\text {terminal }} 1 / 20$ threaded stud | $\begin{aligned} & 450 \mathrm{PF} \\ & 451 \mathrm{PF} \end{aligned}$ | 550PBQ-S52 550PBQ-S52 | Di-Vergence Gate (higher di/dt) |
| 51RCG | 61RM-S54 | ACE gate (higher dildt) |  |  | ceramic case (higher di/dt) |
| 52 RCG | 62RM-S54 | ACE gate (higher di/dt) | 470PA | 550PB | None: Change of nomenclature |
| 71 RCG | 91RL-S53 | ACE gate (higher di/dt) | 500PA | 470PB | 1 TSM $=7000 \mathrm{~A}$ |
| 72RCG | 92RL-S53 | ACE gate (higher di/dt) | 501 PA | 470PB | 1 TSM $=7000 \mathrm{~A}, 1$ inch thick |
| 70RCS-A* | 72RC-A | 1/2-20 threaded stud, flag terminal |  |  | ceramic case |
| 71 7CSSA* | 71RC-A 250RM-S53 | 1/2-20 threaded stud | 550PA <br> 551PA | 550PB | $\begin{aligned} 1 T S M & =8000 \mathrm{~A} \\ \text { ITSM } & =8000 \mathrm{~A}, 1 \text { inch this }\end{aligned}$ |
| 275RF | 250RM-S53 | ACE gate, $\mathrm{t}_{\mathrm{a}}=15 \mu \mathrm{sec}$ max. (higher di/dt) |  | 550PB | ${ }^{1}$ TSM $=8000 \mathrm{~A}, 1$ inch thic ceramic case |
| 325 RA | 30088 | ITSM $=7000 \mathrm{~A}$ | $700 \mathrm{~Pa}{ }^{\text {- }}$ |  | ACE gate (higher di/dt) |
| 375RA | 350RA | $1 \text { TSM }=8000 \mathrm{~A}$ | 850PA | $\begin{aligned} & \text { 850PK } \\ & \text { 1000PK } \end{aligned}$ | ACE gate (higher di/dt) |
| 420PM | 420 PBM | None: Change of nomenclature | 1000PA |  | ACE gate (higher di/dt) |

## Power Transistors and Darlingtons

International Rectifier's Power Transistors and Power Darlingtons offer state-of-the-art processes and techniques in popular device ratings. IR's unique glass passivation ensures high reliability and exceptional stability. The triple-diffused process used offers high voltage, fast switching times, and low saturation voltages. 34 types of high voltage Silicon Power Transistors offer high power, high voltage, and high current ratings. Applications include inverters, choppers, deflection circuits, etc. In addition, there are 15 types of fast switching power transistors.
25 types of high voltage Monolithic Darlingtons offer high power, high voltage, high current and high gain. 9 types of fast-switching Darlingtons. Hich
HIGH VOLTAGE NPN POWER TRANSISTORS


| ${ }^{\text {I }}$ C Cont. (A) | 1.0 | 2.0 | 3.0 | 3.0 | 3.0 | 3.0 | 3.0 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC Peak (A) | 4.0 | 5.0 | 5.0 | 5.0 | 5.0 | 7.0 | 7.0 |  |  |
| $\mathrm{V}_{\text {cboiv) }}$ | 800 | 1,000 | 275 | 300 | 375 | 900 | 900 |  |  |
| SERIES | 18701 | 18801 | 2 L 5838 | 2N5839 | 2N5840 | 18708 | IR709 |  |  |
|  -1c (A) | $\begin{aligned} & 600 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 700 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 250 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 275 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 350 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 600 \\ & 0.50 \end{aligned}$ | $\begin{aligned} & 600 \\ & 0.50 \end{aligned}$ |  |  |
| $\begin{aligned} & I_{C E O} \text { max. (mA) } \\ & \text { ©NE } \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 800 \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 800 \\ & \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 200 \end{aligned}$ | $\begin{aligned} & 250 \\ & 250 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 250 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 900 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 900 \end{aligned}$ |  |  |
|  | $=$ | - | $\begin{array}{r} 5.0 \\ 265 \\ -1.5 \\ \hline \end{array}$ | $\begin{gathered} 2.0 \\ 290 \\ -1.5 \end{gathered}$ | $\begin{gathered} 2.0 \\ 360 \\ -1.5 \end{gathered}$ | $\begin{gathered} 0.25 \\ 9.90 \\ \begin{array}{c} 1.5 \end{array} \end{gathered}$ | $\begin{gathered} 0.25 \\ 900 \\ 900 \\ \hline 1.5 \end{gathered}$ |  | -:075 |
| hFE (min) ${ }^{1 / \mathrm{C}}(\mathrm{A})$ - $V_{C E}$ (V) | $\begin{gathered} 20 \\ 0.150 \\ 5.0 \end{gathered}$ | $\begin{gathered} 20 \\ 0.200 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 8 \\ & \begin{array}{l} 8.0 \\ 2.0 \end{array} \end{aligned}$ | $\begin{aligned} & 10 \\ & 2.0 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 10 \\ & 2.0 \\ & 3.0 \end{aligned}$ |  |  |  | \% |
|  | $\begin{aligned} & \text { I } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { I } \end{aligned}$ | $\begin{gathered} 1.0 \\ 3.0 \\ 0.375 \end{gathered}$ | $\begin{gathered} 1.5 \\ 2.0 \\ 0.20 \end{gathered}$ | $\begin{aligned} & 1.5 \\ & 2.0 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 1.0 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 2.0 \\ & 0.80 \\ & \hline \end{aligned}$ | T0-3 |  |
| $\mathrm{P}_{\mathrm{d}}(\mathrm{W})$ | 50 | 100 | 100 | 100 | 100 | 50 | 50 |  |  |
| IC Cont. (A) | 3.0 | 3.0 | 3.5 | 3.5 | 3.5 | 3.5 | 3.5 | 5.0 | 5.0 |
| IC Peak (A) | 7.0 | - | 10 | 10 | 10 | - | - | 7.0 | 7.0 |
| $\mathrm{v}_{\text {cBo }}$ (V) | 900 | - | 200 | 400 | 700 | 700 | 700 | 400 | 400 |
| SERIES | IR710 | IR721 | IR660 (1) | IR663 (1) | IR665 (1) | 2N3902 | 2 N 5157 | IR401 | IRA13 |
|  | $\begin{aligned} & 5000 \\ & 0.50 \\ & \end{aligned}$ | $\begin{aligned} & 800 \\ & 0.50 \\ & 0.50 \end{aligned}$ | $\begin{aligned} & 200 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 400 \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 4000 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 300 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ |
| $\begin{aligned} & { }^{1} \mathrm{CEEO} \max .(\mathrm{mA}) \\ & \text { eV } \mathrm{V}_{\mathrm{CE}}(\mathrm{~V}) \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 900 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 1,000 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 200 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \end{aligned}$ | $\begin{gathered} 0.25 \\ 500 \end{gathered}$ | $\begin{aligned} & 0.25 \\ & 400 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 500 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \end{aligned}$ |
|  | - | $\begin{aligned} & 0.25 \\ & 1.000 \\ & -1.5 \end{aligned}$ | $\begin{aligned} & 0.50 \\ & 200 \\ & 1.5 \\ & 120 \end{aligned}$ | $\begin{aligned} & 0.50(2) \\ & 400 \\ & -1.5 \end{aligned}$ | $\begin{aligned} & 0.50{ }^{0.1} \\ & 700 \\ & -1.5 \end{aligned}$ | $\begin{gathered} 2.5 \\ 700 \\ -1.5 \end{gathered}$ | $\begin{aligned} & 0.50 \\ & 700 \\ & .00 \\ & \hline 1.5 \end{aligned}$ | $\begin{aligned} & \hline 0.50(2) \\ & 400 \\ & -1.5 \end{aligned}$ | $\begin{aligned} & \hline 0.5(2) \\ & 400 \\ & -1.5 \end{aligned}$ |
| $h_{\text {FE }}($ min $/$ max $)$ ©IC (A) (e VCE (V) | $10 / 50$  <br>  7 <br> 0.15 1.0 <br> 5.0 5.0 | $\begin{gathered} 20 / 60 \\ 0.150 \\ 5.0 \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} \hline 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 20 / 100 \\ 0.5 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 20 / 80 \\ 0.5 \\ 5.0 \\ \hline \end{gathered}$ |
|  | - | - | $\begin{gathered} 0.8 \\ 1.0 \\ 0.10 \end{gathered}$ | $\begin{gathered} 0.8 \\ 1.0 \\ 0.10 \\ 0.10 \end{gathered}$ | $\begin{gathered} 0.8 \\ 1.0 \\ 0.10 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 1.0 \\ & 0.10 \end{aligned}$ | $\begin{gathered} 0.8 \\ 1.0 \\ 0.10 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 0.5 \\ & 0.05 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 0.5 \\ & 0.05 \end{aligned}$ |
| $P_{d}(\mathbb{W})$ | 50 | 50 | 60 | 60 | 60 | 100 | 100 | 100 | 100 |
| Ic Corit. (A) | 5.0 | 5.0 | 5.0 | 5.0 | 7.0 | 7.0 | 7.0 | 7.0 | 7.0 |
| IC Prak (A) | 15 | 15 | - | 10 | 10 | 10 | 10 | 10 | 10 |
| $V_{\text {ceo }}(\mathrm{V})$ | 300 | 375 | 400 | 400 | 300 | 400 | 400 | 400 | 400 |
| SERIES | 2N5804 | 2N5805 | 2 N 5241 | 18410 | 18411 | 18430 | IR431 | IR409 | IR423 |
|  | $\begin{aligned} & 2255 \\ & 0.20 \end{aligned}$ | $\begin{array}{r} 300 \\ 0.20 \\ \hline \end{array}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 200 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 300 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 300 \\ & 0.10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ |
|  | $\begin{aligned} & 15.0 \\ & 150 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 150 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 400 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 300 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 300 \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.5 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \\ & \hline \end{aligned}$ |
|  | $\begin{aligned} & 5.0 \\ & 270 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{array}{r} 5.0 \\ 340 \\ -1.5 \\ \hline \end{array}$ | $\begin{aligned} & 0.5 \\ & 400 \\ & 1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.50(2) \\ & 200 \\ & -1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 300 \\ & -1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.00^{(2)} \\ & 400{ }^{2} \\ & 0 \end{aligned}$ | $\begin{aligned} & 5.00^{(2)} \\ & 400 \\ & 0 \end{aligned}$ | $\begin{aligned} & \hline 0.5(2) \\ & 400 \\ & -1.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.5(2) \\ & 400{ }^{2} \\ & -1.5 \end{aligned}$ |
| $h_{\text {hfE (min/max) }}$ © 1 C (A) <br> - $V_{C E}(V)$ | $\begin{gathered} 10 / 100 \\ 5.0 \\ 4.0 \end{gathered}$ | $\begin{gathered} 10 / 100 \\ 5.0 \\ 4.0 \end{gathered}$ | $\begin{gathered} 15 / 35 \\ 2.5 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \end{gathered}$ | $\begin{gathered} 15 / 45 \\ 2.5 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{gathered} 15 / 35 \\ 2.5 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{aligned} & 15(1) \\ & 1.0 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \\ \hline \end{gathered}$ |
|  | $\begin{aligned} & 2.0 \\ & 5.0 \\ & 0.5 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 5.0 \\ & 0.50 \end{aligned}$ | $\begin{aligned} & 0.7 \\ & 2.5 \\ & 0.50 \end{aligned}$ | $\begin{gathered} 0.8 \\ 1.0 \\ 0.10 \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 1.0 \\ & 0.10 \end{aligned}$ | $\begin{gathered} 0.9 \\ 2.5 \\ 0.50 \end{gathered}$ | $\begin{aligned} & 0.7 \\ & 2.5 \\ & 0.5 \end{aligned}$ | $\begin{gathered} 1.2 \\ 1.0 \\ 0.167 \\ \hline \end{gathered}$ | $\begin{aligned} & 0.8 \\ & 1.0 \\ & 0.10 \end{aligned}$ |
| $\mathrm{Pd}_{\text {d }}(\mathrm{W})$ | 110 | 110 | 125 | 100 | 100 | 125 | 125 | 125 | 125 |

## Power Transistors and Darlingtons

T0.66


HIGH VOLTAGE NPN POWER THANSISTORS (Continued)
$\mathrm{T}_{\mathrm{C}}=25^{\circ} \mathrm{C}$ unless otherwise specified

| It Cont. (A) | 7 | 7 | 7 | 7 | 10 |  | 10 |  | 10 |  | 10 |  | 10 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {c P Peak (A) }}$ | 10 | 10 | 10 | 10 | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  |
| $\mathrm{V}_{\text {CBO }}(\mathrm{V})$ | 400 | 700 | 700 | 700 | 300 |  | 400 |  | 500 |  | 600 |  | 700 |  |
| SERIES | IR403 | IR402 | IR424 | IR425 | IR515 |  | 18516 |  | 18517 |  | 18518 |  | IR519 |  |
| $V_{\text {CEO (sus) min. (V) }}$ elc (A) | $\begin{aligned} & 325 \\ & 0.10 \\ & \hline \end{aligned}$ | $\begin{aligned} & 325 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 350 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 400 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 250 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 250 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 250 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 2755 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 275 \\ & 0.10 \end{aligned}$ |  |
| $\begin{aligned} & \text { ICEO max. (mA) } \\ & \mathrm{QV}_{\mathrm{CE}}(\mathrm{~V}) \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 400 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 400 \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 500 \\ & \hline \end{aligned}$ | $\begin{array}{r} 0.25 \\ 500 \\ \hline \end{array}$ | $\begin{aligned} & 0.5 \\ & 300 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 400 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 700 \\ & \hline \end{aligned}$ |  |
| $\begin{aligned} & \text { ICEV max. }(\mathrm{mA}) \\ & e V C E(V) \\ & e V_{B E}(V) \end{aligned}$ | $\begin{aligned} & \hline 0.5(2) \\ & 400 \\ & -1.5 \end{aligned}$ | $\begin{aligned} & 0.5(2) \\ & 700 \\ & 1.5 \end{aligned}$ | $\begin{aligned} & 0.5 \text { (2) } \\ & 700 \\ & -1.5 \end{aligned}$ | $\begin{aligned} & 0.5(2) \\ & 700 \\ & -1.5 \\ & \hline \end{aligned}$ | $\bar{I}$ |  | $\bar{I}$ |  | - |  | - |  | - |  |
| $h_{\text {hFE }}$ (min/max) -IC (A) - $\mathrm{V}_{\text {CE }}$ (V) |  |  | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \end{gathered}$ | $\begin{gathered} 30 / 90 \\ 1.0 \\ 5.0 \end{gathered}$ | $\begin{gathered} 15 / 80 \\ 3.0 \\ 5.0 \end{gathered}$ | $\left[\begin{array}{r} \text { (1) } 3.5 \\ 10 \\ 5.0 \end{array}\right.$ | $\begin{gathered} 20 / 80 \\ 3.0 \\ 5.0 \end{gathered}$ | $\begin{array}{r} (3) 4 \\ 10 \\ 5.0 \end{array}$ | $\begin{gathered} 20 / 80 \\ 300 \\ 5.0 \end{gathered}$ | $\begin{gathered} (3) 5 \\ 10 \\ 5.0 \end{gathered}$ | $\begin{gathered} 25 / 75 \\ 3.0 \\ 5.0 \end{gathered}$ | $\begin{array}{r} (1) 5 \\ 10 \\ 5.0 \end{array}$ | $\begin{gathered} 25 / 75 \\ 3.0 \\ 5.0 \end{gathered}$ | 13 10 10 5.0 |
| $\mathrm{V}_{\text {CE (sat) max. (V) }}$ <br> eic (A) <br> $11_{8}$ (A) | $\begin{aligned} & 1.1 \\ & 3.5 \\ & 0.8 \end{aligned}$ | $\begin{aligned} & 2.0 \\ & 3.0 \\ & 0.6 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.0 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 0.8 \\ & 1.0 \\ & 0.10 \end{aligned}$ | $\begin{aligned} & 1.8 \\ & 3.0 \\ & 0.30 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 7.0 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 3.0 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 1.9 \\ & 7.0 \\ & 1.4 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 3.0 \\ & 0.3 \end{aligned}$ | 1.6 7.0 1.4 | $\begin{aligned} & 1.0 \\ & 3.0 \\ & 0.3 \end{aligned}$ | 1.4 7.0 1.4 | $\begin{array}{r} 1.0 \\ 3.0 \\ 0.3 \\ \hline \end{array}$ | 1.4 <br> 7.0 <br> 1.4 |
| $\mathrm{Pd}_{\text {d }}($ (w) | 125 | 125 | 125 | 125 |  | 125 |  | 25 |  | 25 |  |  |  | 25 |

FAST-SWITCHING, HIGH VOLTAGE NPN POWER TRANSISTORS

| Ic Cont. (A) | 5.0 |  | 5.0 |  | 8.0 |  | 8.0 |  | 8.0 |  | 8.0 |  | 8.0 |  | 10 |  | 10 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {IC P Peak ( }}$ ( $)$ | - |  | - |  | 16 |  | 16 |  | - |  | 16 |  | - |  | 15 |  | 15 |  |
| $\mathrm{V}_{\text {CBO }}(\mathrm{V})$ | 650 |  | 850 |  | 500 |  | 600 |  | 650 |  | 700 |  | 850 |  | 500 |  | 600 |  |
| SERIES | 2N6542 |  | 2N6543 |  | 2N6306 |  | 2 C 6307 |  | 2 W 6544 |  | 2 N 6308 |  | 2N6545 |  | 2N6573 |  | 2N6574 |  |
| VCEO(sus) min. (V) elc (A) | $\begin{aligned} & 300 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 4000 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 250 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 300 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 300 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 0.10 \end{aligned}$ |  | $0.10$ |  | $\begin{aligned} & 250 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 275 \\ & 0.10 \end{aligned}$ |  |
| $\begin{aligned} & \text { TCEO max. }(\mathrm{mA}) \\ & \propto V_{C E}(\mathrm{~V}) \end{aligned}$ | - |  | - |  | $\begin{aligned} & 0.5 \\ & 250 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 300 \end{aligned}$ |  | - |  | $\begin{aligned} & 0.5 \\ & 350 \end{aligned}$ |  | - |  |  |  |  |  |
| $\begin{aligned} & \text { CEV max }(\mathrm{mA}) \\ & \varrho \mathrm{VCE}^{(V)} \\ & \qquad V_{B E}(\mathrm{~V}) \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 650 \\ & 1.5 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 850 \\ & 1.5 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 500 \\ & 1.5 \end{aligned}$ |  | $\begin{aligned} & 0.5 \\ & 600 \\ & 1.5 \end{aligned}$ |  | $\begin{gathered} 0.5 \\ 650 \\ -1.5 \end{gathered}$ |  | $\begin{aligned} & 0.5 \\ & 700 \\ & -1.5 \end{aligned}$ |  | $\begin{gathered} 0.5 \\ \hline 850 \\ \hline 1.5 \end{gathered}$ |  | $\begin{gathered} 0.5 \\ 500 \\ .1 .5 \end{gathered}$ |  | $\begin{aligned} & 0.5 \\ & 600 \\ & 1.5 \end{aligned}$ |  |
| hFE (min/max) <br> OIC (A) <br> e VCE (V) | $\begin{gathered} 12 / 60 \\ 1.5 \\ 2.0 \end{gathered}$ | $\begin{aligned} & 7 / 35 \\ & 3.0 \\ & 2.0 \end{aligned}$ | $\begin{array}{\|c\|} \hline 12 / 60 \\ 1.5 \\ 2.0 \\ \hline \end{array}$ | $\begin{aligned} & 7 / 35 \\ & 3.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 5 / 75 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{array}{\|c\|} \hline 8.0 \\ \hline 8.0 \\ 5.0 \end{array}$ | $\begin{gathered} 15 / 75 \\ 3.0 \\ 5.0 \end{gathered}$ | $\begin{array}{r\|} \hline 1]^{4} .0 \\ 5.0 \end{array}$ | $\begin{gathered} \hline 12 / 60 \\ 2.5 \\ 3.0 \end{gathered}$ | $\begin{gathered} 7 / 35 \\ 5.0 \\ 3.0 \end{gathered}$ | $\begin{gathered} 12 / 60 \\ 3.0 \\ 5.0 \end{gathered}$ | $\begin{array}{r} (3) 3 \\ 8.0 \\ 5.0 \end{array}$ | $\begin{gathered} 12 / 60 \\ 2.5 \\ 3.0 \end{gathered}$ | $\begin{array}{\|c\|} \hline 7 / 35 \\ 50 \\ 3.0 \\ \hline \end{array}$ | $\begin{gathered} 15 / 60 \\ 3.0 \\ 3.0 \end{gathered}$ | $\begin{array}{r} 05 \\ 10 \\ 5.0 \end{array}$ | $\begin{gathered} 20 / 60 \\ 3.0 \\ 3.0 \end{gathered}$ | (3) 5 10 5.0 |
|  | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 5.0 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 8.0 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 8.0 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 8.0 \\ & 2.0 \end{aligned}$ |  | $\begin{gathered} 5.0 \\ 8.0 \\ 2.67 \end{gathered}$ |  | $\begin{aligned} & 5.0 \\ & 8.0 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 1.2 \\ & 3.0 \\ & 0.3 \end{aligned}$ | 5.0 10 2.0 | $\begin{aligned} & 1.0 \\ & 3.0 \\ & 0.3 \end{aligned}$ | 50 10 2.0 |
| $\mathrm{P}_{\mathrm{d}}(\mathrm{W})$ | 100 |  | 100 |  | 125 |  | 125 |  | 125 |  | 125 |  | 125 |  | 125 |  | 125 |  |
|  | $\begin{gathered} 0.7 / 4.0 / 0.8 \\ 3.0 \end{gathered}$ |  | $\begin{array}{r} 0.714 .0 / 0.8 \\ 3.0 \end{array}$ |  | $\begin{gathered} 0.6 / 1.6 / 0.4 \\ 3.0 \end{gathered}$ |  | $\begin{gathered} 0.6 / 1.6 / 0.4 \\ 3.0 \end{gathered}$ |  | $\begin{gathered} 1.0 / 4.0 / 1.0 \\ 5.0 \end{gathered}$ |  | $\begin{gathered} 0.6 / 1.6 / 0.4 \\ 3.0 \end{gathered}$ |  | $\begin{aligned} & 1.0 / 4.0 / 1.0 \\ & 5.0 \end{aligned}$ |  | $\begin{gathered} 0.9 / 2.5 / 0.7 \\ 7.0 \end{gathered}$ |  | $\begin{aligned} & 0.9 / 2.5 / 0.7 \\ & 7.0 \end{aligned}$ |  |


| IC Cont (A) | 10 |  | 10 | 10 | 10 | 15 |  | 15 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC Peak (A) | 15 |  | 30 | 30 | 30 | 30 |  | 3 |  |
| $\mathrm{V}_{\text {CBO }}(\mathrm{V})$ | 700 |  | 300 | 375 | 450 | 650 |  | 85 |  |
| SERIES | 2 W6575 |  | 2N6249 | 2 W 6250 | 2 W 6251 | 2N65 |  | 2 N 6 |  |
| $\mathrm{V}_{\text {CEO (sus) min. (V) }}$ -IC (A) | $\begin{aligned} & 300 \\ & 0.10 \\ & 0.10 \end{aligned}$ |  | $\begin{aligned} & 200 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 275 \\ & 0.20 \\ & 0.20 \end{aligned}$ | $\begin{aligned} & 350 \\ & 0.20 \\ & \hline \end{aligned}$ | 300 0.1 |  | 40 |  |
| $\begin{aligned} & \text { ICEO max, }(\mathrm{mA}) \\ & \varrho V_{C E}(\mathrm{~m}) \end{aligned}$ | - |  | $\begin{aligned} & 5.0 \\ & 150 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 225 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 300 \end{aligned}$ | - |  |  |  |
| $\begin{aligned} & \text { ICEV max }(\mathrm{mA}) \\ & e V_{\mathrm{CE}}(V) \\ & e V_{B E}(V) \end{aligned}$ | $\begin{aligned} & 0.5 \\ & 700 \\ & 1.5 \end{aligned}$ |  | $\begin{array}{r} 5.0 \\ 225 \\ -1.5 \end{array}$ | $\begin{aligned} & 5.0 \\ & 300 \\ & -1.5 \end{aligned}$ | $\begin{array}{r} 5.0 \\ 375 \\ -1.5 \end{array}$ | $\begin{array}{r}1.0 \\ \hline 650 \\ \hline 1.5\end{array}$ |  | 1. |  |
| hFE ( $\min /$ max) eIc (A) <br> VCE (V) | $\begin{array}{\|c\|} \hline 20 / 60 \\ 3.0 \\ 3.0 \\ \hline \end{array}$ | $\begin{aligned} & 5(1) \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 10 / 50 \\ 10 \\ 3.0 \end{gathered}$ | $\begin{aligned} & 8 / 50 \\ & 10 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 6 / 50 \\ & 10 \\ & 3.0 \end{aligned}$ | $\begin{gathered} 12 / 60 \\ 5.0 \\ 2.0 \end{gathered}$ | $\begin{aligned} & 6 / 30 \\ & 10 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 12 / 60 \\ & 5.0 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 6 / 30 \\ & 10 \\ & 2.0 \end{aligned}$ |
| $\begin{aligned} & V_{C E(\text { sat })}^{\text {max. (V) }} \\ & \text { Q } 1 C_{B}(A) \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 3.0 \\ & 0.3 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & \hline 10 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 10 \\ & 1.0 \end{aligned}$ | $\begin{gathered} 1.5 \\ 10 \\ 1.25 \end{gathered}$ | $\begin{array}{r} 1.5 \\ 10 \\ 1.67 \end{array}$ | $\begin{aligned} & 1.5 \\ & 10 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 15 \\ & 3.0 \end{aligned}$ | $\begin{aligned} & 1.5 \\ & 10 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 5.0 \\ & 15 \\ & 3.0 \end{aligned}$ |
| $P_{\text {d }}(W)$ | 125 |  | 1.0 175 | 175 | 175 | 175 |  |  |  |
|  | $\begin{aligned} & \text { 0.9/2.5/0.7 } \\ & \hline 7.0 \end{aligned}$ |  | $\begin{gathered} 2.0 / 3.5 / 1.0 \\ 10 \end{gathered}$ | $\begin{gathered} \hline 2.0 / 3.5 / 1.0 \\ 10 \\ \hline \end{gathered}$ | $\begin{array}{r} 2.0 / 3.5 / 1.0 \\ 10 \\ \hline \end{array}$ | $0.7 / 4.0$ 10 | $\overline{70.8}$ | 0.714 | $0 / 0.8$ |



Power Transistors and Darlingtons


| Ic Cont. (A) | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC Peak (A) | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  |
| $\mathrm{v}_{\text {CBO }}(\mathrm{V})$ | 400 |  | 400 |  | 400 |  | 450 |  | 500 |  | 500 |  | 600 |  | 600 |  | 500 |  |
| SERIES | IR5000 |  | IR4040 |  | IR4045 |  | IR5001 |  | IR4050 |  | IR4055 |  | IR4059 |  | IR4061 |  | IR500 |  |
| $\begin{aligned} & \mathbf{V}_{\text {CEO }(\text { sus }) \text { min. (V) }} \\ & e_{C}(A)(A) \end{aligned}$ | $\begin{aligned} & 300 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 325 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & 325 \\ & 1.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 1.0 \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 1.0 \\ & \hline \end{aligned}$ |  | 3501.0 |  | $\begin{aligned} & 350 \\ & 1.0 \\ & \hline \end{aligned}$ |  | 400200 |  |
| $\begin{aligned} & \mathrm{ICEO}_{\mathrm{max} .}(\mathrm{mA}) \\ & \mathrm{VV}_{\mathrm{CE}}(\mathrm{~V}) \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 400 \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & 400 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & \text { ann } \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 450 \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & 500 \\ & \hline \end{aligned}$ |  | $\begin{array}{r} 0.25 \\ 500 \end{array}$ |  | $\begin{aligned} & 0.25 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & 600 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 500 \end{aligned}$ |  |
| $h_{\text {FE (min.) }}$ elc (A) ev $\mathrm{V}_{\text {CE }}(\mathrm{V})$ | $\begin{aligned} & 15 \\ & 15 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 140 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 250 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 15 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 500 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 15 \\ & \hline \end{aligned}$ | $\begin{aligned} & 140 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 250 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 15 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 500 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 5.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 200 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 5 \\ 15 \\ 15 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{aligned} & 250 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 15 \\ 5.0 \\ \hline \end{gathered}$ | $\begin{aligned} & 140 \\ & 50.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 5.0 \end{aligned}$ |
|  | $\begin{aligned} & 1.8 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{gathered} 1.2 \\ 5.0 \\ 0.25 \end{gathered}$ |  | $\begin{aligned} & 1.8 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & 2.0 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & 1.8 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & 5.0 \\ & 15 \\ & 3.0 \end{aligned}$ |  | $\begin{aligned} & 2.2 \\ & 15 \\ & 3.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.8 \\ & 15 \\ & 3.0 \end{aligned}$ |  |
| $\mathrm{P}_{\mathrm{d}}(\mathrm{W})$ | 125 |  | 125 |  | 125 |  | 125 |  | 125 |  | 125 |  | 100 |  | 100 |  | 125 |  |


| IC Cont. (A) | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 15 |  | 20 |  | 20 |  | 20 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IC Peak (A) | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 20 |  | 25 |  | 25 |  | 25 |  |
| $\mathrm{v}_{\text {CBO }}(\mathrm{V})$ | 600 |  | 600 |  | 600 |  | 700 |  | 850 |  | 1,000 |  | 350 |  | 400 |  | 450 |  |
| SERIES | IR4060 |  | IR4065 |  | 1R5063 |  | IR5064 |  | IR5065 |  | IR5066 |  | IR5060 |  | IR5061 |  | 1R5662 |  |
| $\begin{aligned} & \mathbf{V}_{\text {CEO (us) }} \text { min. (V) } \\ & e_{\mathrm{C}}(A) \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline 400 \\ & 1.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 400 \\ & 1.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 500 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 600 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 750 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 900 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 300 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 400 \\ & 2.0 \end{aligned}$ |  |
| $\begin{aligned} & \text { ICEO max. }^{\text {mat }} \\ & \text { ©VEE }(\mathrm{mA}) \end{aligned}$ | $\begin{aligned} & 0.25 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 0.25 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 500 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 750 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 900 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 350 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 400 \end{aligned}$ |  | $\begin{array}{r} 1.0 \\ 450 \\ \hline \end{array}$ |  |
| hFE (min.) IC(A) <br> @ $\mathrm{V}_{C E}$ (V) | $\begin{aligned} & 250 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 15 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 500 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 12 \\ & 15 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 20 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 14 \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{gathered} 8 \\ 15 \\ 5.0 \end{gathered}$ | $\begin{aligned} & 10 \\ & 10 \\ & 5.0 \end{aligned}$ | 4 15 15 5.0 | $\begin{gathered} 8 \\ 10 \\ 5.0 \end{gathered}$ | $\begin{gathered} 5 \\ 312 \\ 5.0 \end{gathered}$ | $\begin{gathered} 100 \\ 10 \\ 5 \end{gathered}$ | 40 15 5 | $\begin{gathered} 100 \\ 10 \\ 5 \end{gathered}$ | 40 15 5 | 100 10 5 | 40 15 5 |
| $\begin{aligned} & V_{C E}(s a t) \text { max. (V) } \\ & \text { @1C } \\ & \text { @ } \\|_{B}(A) \\ & \hline(A) \end{aligned}$ |  |  | $\begin{aligned} & 1.8 \\ & 15 \\ & 3.0 \end{aligned}$ |  | 1. |  | 1.2 |  |  |  | 2 1 1 |  |  |  |  |  |  |  |
| $\mathrm{P}_{\mathrm{d}}(\mathrm{W})$ |  |  | 12 |  | 12 |  | 12 |  |  |  |  |  |  |  |  |  |  |  |

FAST-SWITCHING, HIGH VOLTAGE NPN POWER DARLINGTONS *

| $I_{C}$ Cont. (A) | 10 |  | 10 |  | 10 |  | 15 |  | 15 |  | 15 |  | 20 |  | 20 |  | 20 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {c }}$ P Peak (A) | 15 |  | 15 |  | 15 |  | 20 |  | 20 |  | 20 |  | 25 |  | 25 |  | 25 |  |
| $\mathrm{V}_{\text {CBO }}(\mathrm{V})$ | 00 |  | 450 |  | 500 |  | 400 |  | 450 |  | 500 |  | 350 |  | 400 |  | 450 |  |
| SERIES | 1R6251 |  | 1R6252 |  | IR5253 |  | IR6000 |  | IR6001 |  | IR6002 |  | IR6050 |  | IR6061 |  | IR6062 |  |
| $\begin{aligned} & v_{C E O(\text { (us) }) \text { min. }(\mathbf{v})} \\ & \left.\qquad I_{C}(A)\right) \end{aligned}$ | $\begin{aligned} & 350 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 400 \\ & 2.0 \end{aligned}$ |  | $\begin{aligned} & 450 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 300 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 4000 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 300 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 350 \\ & 2.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 400 \\ & 2.0 \\ & \hline \end{aligned}$ |  |
| $\begin{aligned} & I_{C E D} \text { max. (mA) } \\ & \mathrm{V}_{\mathrm{CE}}(\mathrm{~V}) \end{aligned}$ | $\begin{aligned} & 1.0 \\ & 400 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 455 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 400 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 450 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 500 \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 350 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 400 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 1.0 \\ & 450 \end{aligned}$ |  |
| hFE (min) ${ }^{\text {el }} \mathrm{C}$ ( $A$ ) © VCE (V) | $\begin{aligned} & 140 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 100 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 140 \\ & \text { 3.0 } \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 100 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 140 \\ & 3.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 100 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 150 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 60 \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 150 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 60 \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 150 \\ & 5.0 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & \hline 60 \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{array}{l\|} \hline 100 \\ 10 \\ 5.0 \end{array}$ | $\begin{aligned} & 40 \\ & 15 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 100 \\ & 10 \\ & 5.0 \end{aligned}$ | $\begin{aligned} & 40 \\ & 15 \\ & 15 . \end{aligned}$ | $\begin{aligned} & 100 \\ & 10 \\ & 5.0 \end{aligned}$ | 40 15 5.0 |
| $\begin{aligned} & V_{C E}(\text { sat ) max. (V) } \\ & \text { © } 1 \mathrm{C}(A) \\ & \odot 1_{\mathrm{B}}(A) \\ & \hline \end{aligned}$ | 2. 1 2 |  | 2 2 2 |  | 2.0 |  |  |  | 3.0 |  | 3. |  | 2.0 2.0 |  | 2 2 2 |  | 2 |  |
| $P_{\text {d }}(\mathrm{W})$ | 10 |  |  |  | 10 |  |  |  | 12 |  | 12 |  | 12 |  |  |  |  |  |
|  | $\begin{gathered} 0.25 / 2 \\ 5.1 \end{gathered}$ | $5 / 1.0$ | $\begin{array}{r} 0.25 / 2 . \\ 5.0 \end{array}$ | 5/1.0 | $\begin{array}{r} 0.25 / 2 \\ 5 . \\ \hline \end{array}$ | $5 / 1.0$ | 0.4/2 | 51.0 | $0.4 / 2$ 10 |  | 0.4/2 | 51.0 | 0.4/2 |  | 0.4/2 | $5 / 1.0$ | 0.4/2 |  |

## Silicon Rectifiers

| C－10 | C－12 <br> 0.040 DIA． <br> $\frac{\text { MAX }}{\frac{0.145}{0.130} \text { DIA．}}$ | C－15 |  |  |
| :---: | :---: | :---: | :---: | :---: |

IR has been a major producer of low－current，low－voltage silicon increased the need for high－speed，Iow－loss rectifiers．To satisfy rectifier diodes for many years．Through continuous improve－ ments in engineering and manufacturing techniques，IR is now producing standard rectifiers with current handling capacities from 400 mA to 3000 amps in a wide array of lead－mounted， stud－mounted，and Hockey－Puk packages．
increased the need for high－speed，low－loss rectifiers．To satisty
this need，IR now lists 15 series of fast recovery rectifiers in a separate tabl
Power Schottky Rectifiers．IR now offers six series of Schottky barrier rectifiers from 20 to 50 amps ．Included are two JEDEC Fast Recovery Rectifiers．The growing demand for high fre－

Bold Face Listings．Those series listed in heavier，bold face type

| $\begin{aligned} & \mathrm{IF}(\mathrm{AV})(\mathrm{A}) \\ & Q \operatorname{Max} . \mathrm{TC}^{\circ}\left({ }^{\circ} \mathrm{C}\right) \end{aligned}$ | $\begin{aligned} & 750 \mathrm{~mA} \\ & @ 25^{\circ} \end{aligned}$ | $\begin{aligned} & 750 \mathrm{~mA} \\ & @ 25^{\circ} \end{aligned}$ | $\begin{aligned} & 750 \mathrm{~mA} \\ & @ 25^{\circ} \end{aligned}$ | $\begin{aligned} & 750 \mathrm{~mA} \\ & @ 75^{\circ} \end{aligned}$ | ${ }^{1} 5_{5}^{\circ}$ | $\text { @ }{ }^{1} 5^{\circ}$ | $\text { @ }{ }_{75}$ | $\begin{gathered} 1.5 \\ @ 40^{\circ} \end{gathered}$ | $\stackrel{2}{20}^{2}$ | $@_{50^{\circ}}$ | ${\stackrel{3}{3} 0^{\circ}}^{\circ}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IFSM（A） | 10 | 22 | 22 | 40 | 30 | 40 | 50 | 50 | 50 | 25 | 40 |
| Notes | （1） | （1） | （1） | （1） | （1） | （1） | （1） |  | （2）（1） | （1）（1） | （3） |
| Case Style | C－10 | D0－39 | 00.39 | C－10 | D0．41 | C－10 | D0．39 | 00－39 | D0－39 | 00.4 | 004 |
| PRV | PART NUMBERS |  |  |  |  |  |  |  |  |  |  |
| 50 Volts100 V Vols150 Volts200 Voiss300 Volts | $1{ }^{12103}$ |  | ${ }^{1} 2069 \mathrm{~A}$ | 1N3193 | 1 N4001 1 N4002 1N4063 | 10 C 1 <br> 10C2 <br> 10 C 3 | $\begin{aligned} & 10005 \\ & 1001 \\ & 10 \overline{202} \\ & 1003 \\ & \hline \end{aligned}$ | 1N4816 1N4817 1N4818 N4819 | 200052001-120022003 | $\begin{aligned} & \text { iN2348 } \\ & \text { iN249 } \\ & \text { iN2350 } \\ & \text { iN1124 } \\ & \text { iN1125 } \end{aligned}$ | $\begin{aligned} & 3 F-10 \\ & 3 F 20 \\ & 3 F 30 \end{aligned}$ |
|  | 1N2104 |  |  |  |  |  |  |  |  |  |  |
|  | 12105 iN2106 | 1N2069 |  |  |  |  |  |  |  |  |  |
| 500 Volts | iN2108 | TW2010 | in2070A | 1N3194 | 194004 |  | ${ }_{1}^{1004}$ |  | ${ }_{2004}^{2005}$ | 1N1126 | $3 F 40$ $3 F 50$ |
| 600 V Vits | W210 | 1N2071 | 1N2071A | 1N3195 | 124005 | 10c6 | 1006 | 1N4822 | 2006 | 1N1128 | 3F60 |
| 700 Vois 800 Vols |  |  |  |  |  |  |  | 1N5052 |  |  |  |
| 1000 Vots | － | － | － | $\frac{1 \text { N3196 }}{1 \text { N3563 }}$ | $1 \times 4006$ <br> 1 | $\begin{aligned} & \begin{array}{l} 10 c 8 \\ 10 c 10 \\ \hline \end{array} ⿳ ⺈ ⿴ 囗 十 一 ~ \end{aligned}$ | $\begin{aligned} & 1008 \\ & 10010 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 1N5053 } \\ & \text { NN5054 } \end{aligned}$ | ${ }_{20010}^{2008}$ |  | $\begin{aligned} & 3 F 80 \\ & 3 F 100 \\ & \hline \end{aligned}$ |
| $\begin{aligned} & \mathrm{IF}(\mathrm{AV})(\mathrm{A}) \\ & \text { © Max. } \left.\mathrm{TC}_{\mathrm{C}}{ }^{\circ} \mathrm{C}\right) \end{aligned}$ | $\stackrel{3}{3}_{\substack{125}}$ | $\begin{gathered} 3.3 \\ 0.30^{\circ} \end{gathered}$ | $\begin{aligned} & 3.5 \\ & 085^{\circ} \end{aligned}$ | $\text { @ } 95^{\circ}$ | ${ }^{6}{ }_{95^{\circ}}$ | ${ }_{100^{6}}^{6}$ | $\stackrel{6}{6}$ | $\stackrel{6}{6} 100^{0}$ | $\begin{gathered} { }^{6} 0^{\circ} \end{gathered}$ | ${ }^{6}{ }^{6} 50^{\circ}$ | $\stackrel{6}{6}{ }^{\circ}$ |
| IFSM（A） | 150 | 25 | 35 | 150 | 400 | 75 | 75 | 75 | 75 | 150 | 150 |
| Notes | （3） | － | － | （3） | 2 | （b） 1 | （3）（b） | B）${ }^{\text {c }}$ | （3）（6） | （3） | （3） |
| Case Style | C－12 | 00－4 | D04 | 004 | C－15 | D04 | D0－4 | D0．4 | 00.4 | D0．4 | 004 |
| PRV |  |  |  |  |  | ART NUN |  |  |  |  |  |
| 50 Volts |  |  |  | 1N1341 | 60s05 | 1 12879 |  |  |  | 1 I 1341 A |  |
| 100 Voits 150 Volis | ${ }^{3051}$ | － | 1N3569 | 1N1342 | 60s1 | 1N3880 | 6FLL 10 | 6FT10 | 6FV10 | 1N1342A | 1N13428 |
| 200 Volts | 3052 | 1N1124A |  | － $1 \times 1344$ | 6052 |  |  |  |  | （1N1343A | （1N13438 |
| 300 Vols | 3053 | 1N1125A | 1N3571 | 1N1345 | 6053 | 1N3882 | 6FL30 | 6FT30 | 6FV30 | 1N1345A | 1 113458 |
| 400 Volts | 3054 | 1 N 126 A | 1 1 3572 | ${ }^{1} 11346$ | ${ }^{6054}$ | 1 13883 | 6 FL40 | 6FT40 | 6FV40 | 1 N 1346 A | 1N13468 |
| 500 Volts | 3055 | ${ }^{1 N 1127 A}$ | 1N3573 | 1N1347 | ${ }^{6055}$ |  | ${ }_{6}^{6 F L 50}$ | 6FT50 | 6FV50 | 1 N 1347 A | 1N13478 $1 \times 13488$ |
| 600 Volts | ${ }^{3056}$ | $\frac{1 \mathrm{~N} 1128 \mathrm{~A}}{1 \mathrm{~N} 3649}$ | 1N3574 | 1N1348 | ${ }^{6056}$ |  | ${ }^{6 F L 60}$ | 6FT60 | 6FV60 | $\frac{1 \mathrm{~N} 1348 \mathrm{~A}}{1 \text { 13987 }}$ | 1N13488 |
| ${ }^{700}$ Volts | 3058 | － | － | － | 6058 | － | － |  |  | （1N3988 | － |
| 900 Vots |  | － | － | － |  | － | － | ${ }^{\text {6FT90 }}$ ST100 | 6FF90 | 1 1 3989 | － |
| 1000 Voits | 30510 | － | － | － | 60s10 | － | － | 6 FT100 | 6FV100 | 1 1 3990 | － |

Silicon Rectifiers

| D0-4 $\qquad$ <br> $=-8$ $=0$ $=0$ <br> 0.434 0.429 <br> ACROSS FLATS 10.32 UNF-2A <br> 10-32 UNF-2A |  | $00.30$ | DO-9 (B-6) | D-09 (B-13) |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |


|  | $\begin{gathered} 6^{6} \\ \text { @ } 150^{\circ} \end{gathered}$ | $\begin{gathered} 6 \\ \text { @ } 150^{\circ} \end{gathered}$ | $\begin{gathered} 12 \\ 100^{\circ} \end{gathered}$ | $\begin{gathered} 12 \\ 100^{\circ} \end{gathered}$ | $\begin{gathered} 12 \\ 100^{\circ} \end{gathered}$ | $\begin{gathered} 12 \\ 100^{\circ} \end{gathered}$ | $\text { @ } 150^{12}$ | $\underbrace{}_{150^{12}}$ | $\text { @ } 120^{12}$ | $\text { @ } 120^{12}$ | $\begin{gathered} 12 \\ 1500 \\ \hline \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $I_{\text {FSM }}(\mathrm{A})$ | 150 | 160 | 150 | 150 | 150 | 150 | 200 | 240 | 250 | 240 | 250 |
| Notes | (3) | (s) | B) | 3) 6 | s) | () 6 | ( ${ }^{\text {d }}$ | (3) 1 | s) 1 | (1) | (3) |
| Case Style | 004 | 004 | D04 | D04 | D04 | 00.4 | D0.4 | 00.4 | D04 | D0.4 | D04 |
| PRV | PART NUMBERS |  |  |  |  |  |  |  |  |  |  |
|  | 6 65A | 6F58 | 1N3889 | $12 \mathrm{FL5}$ | 12FT5 | 12FV5 | $\begin{aligned} & \text { iN1 } 199 \\ & \text { IN1200 } \\ & \text { NN1200 } \\ & \text { IN1202 } \\ & \text { N1202 } \end{aligned}$ |  | 1N119981N120081N1218iN12028iN12038 |  |  |
|  | 6F10A | ${ }^{6 F 108}$ | 1N3890 | $12 \mathrm{FL10}$ | 12 FT 10 | ${ }_{12}^{2 F V 10}$ <br> 12 FV20 <br> 12 FV 3 O |  |  |  |  |  |
|  | ${ }_{6} 6$ F 15A | ${ }_{6}^{6 F 158}$ |  | - | - |  |  |  |  |  |  |
|  | 6F20A | 6 F 208 | 1N3891 | $12 \mathrm{FL20}$ | 12 FT 20 |  |  |  |  |  |  |
|  | 6F30A | 67308 | 1N3892 | 12 FL 30 | 12FT30 |  |  |  |  |  |  |
| 400 Voits | ${ }^{6} 64040$ A | ${ }^{6 F 408}$ | 1N3893 | 12 FL 40 | 12 FT 40 | $\begin{array}{\|l\|l\|} \hline 12 F V 40 \\ 12 F V 50 \\ 12 F V 60 \\ 12 F V 770 \\ 12 F V 80 \\ \hline 12 \end{array}$ | $\begin{aligned} & \text { 1N1204 } \\ & \text { 1N1205 } \\ & \text { IN1206 } \\ & \text { IN3670 } \\ & \text { N3670 } \end{aligned}$ | IN1204A <br> iN1205A <br> IN206A <br> INB670A <br> IN3671A | IN1204BiN1205BiN1206B | $\begin{aligned} & 12 F 40 \mathrm{~A} \\ & 12750 \mathrm{~A} \\ & 12 F 60 \mathrm{~A} \\ & 12780 \mathrm{~A} \end{aligned}$ | 12 F 40 B 12550 B 12 F 60 B <br> 12F80B |
| 500 Volts | $6 \mathrm{6F50A}$ | 6 F 50 B |  | 12 F L50 | 12 FT 50 |  |  |  |  |  |  |
| 600 V vis | ${ }_{6}^{6 F 509}$ | ${ }^{6 F 5608}$ | - | $12 \mathrm{FL60}$ | 12 F 560 |  |  |  |  |  |  |
| 700 Vols 800 Volts |  |  |  |  | $12 \mathrm{FF70}$ $12 \mathrm{FT80}$ |  |  |  |  |  |  |
| 900 Volts | 6F90A |  |  |  |  |  |  |  |  | 12F100A | 12F 1008 |
|  | 6F100A | 6F 100B |  | - | 12 FT 100 | 12FV100 | 1N3673 | 1 N 3673 A |  |  |  |
| $\begin{aligned} & \mathrm{IF}(\mathrm{AV})(\mathrm{A}) \\ & \mathrm{G}\left({ }^{\circ} \mathrm{Cax} .\right. \end{aligned}$ | 15 | 16 | 16 | 20 | ${ }^{35}$ | ${ }^{40}$ | 40 | ${ }^{60}$ |  | $\begin{array}{\|c\|} \hline 70 \\ @_{125} \\ \hline \end{array}$ | $\varrho_{100}^{100}$ |
|  |  |  |  |  |  |  |  |  |  |  |  |
| IFSM (A) | 250 | 300 | 300 | 400 | 500 | 500 | 800 | 700 | 900 | 1,200 | 1,600 |
| Notes | (3) | (5) | (3) | (5) | (3) | (3) | (3) | (3) | (3) | 3 | $\begin{gathered} \frac{(3)}{00-8} \\ \hline \end{gathered}$ |
| Case Style | D0-5 | D0-4 | D0-4 | D0-4 | D0.5 | D0-5 | D0.5 | 00.5 | 00.5 | D0.5 |  |
| PRV | PART NUMBERS |  |  |  |  |  |  |  |  |  |  |
|  | ${ }^{1} 1 \times 3208$ | 1655 | 1N3615 |  | 1 11183 | 40HF5 | 1N1183A | 1N2128 | 1 N2128A | 70Н10A 70H15A 70H25Aпичз | 1N3288 <br> 1N3289 |
|  | 1 133209 | 16510 | ${ }^{1+3616}$ | 20 F 10 | ${ }^{1 \times 1184}$ | 40HF10 | IN184A | 1N2129 | 1N2129A |  |  |
|  |  | $16 F 15$ | 1 1 3617 |  | 1 W1185 | 40HF15 | IN1185A | ${ }^{1} 12130$ | 1N2130A |  |  |
|  | IN3210 | 16F20 | 1N3618 | 20 F 20 | 1W1186 | 40HF20 | 1N1186A | ${ }^{1} \mathbf{N} 2131$ | 1 N 2131 A |  |  |
|  |  |  |  |  |  |  |  | 1N2132 | 1N2132A |  |  |
| 300 Volts 400 Volts 450 Volts 500 Vol | 1N3211 | 16 F 30 | 1N3619 | 20F30 | 1 121187 | 40HF30 | 1N1187A | 1N2133 | ${ }^{1} 12133 \mathrm{~A}$ | $\begin{aligned} & 70 \mathrm{H} 30 \mathrm{~A} \\ & 70 \mathrm{H} 40 \mathrm{~A} \\ & 7 \mathrm{OH} 50 \mathrm{~A} \end{aligned}$ | 1 1 3290 1N3291 1N3292 |
|  |  |  |  |  |  |  |  | ${ }^{1} \mathbf{N} 2134$ | 1N2134A |  |  |
|  | 1N3212 | 16 F 40 | 1N3620 | 20 F 40 | 1N1188 | 40HF40 | 1N1188A | ${ }^{1} \mathbf{N} 2135$ | 1N2135A |  |  |
|  | 1N3213 | 16F50 | 1N3621 |  | 1 11189 | 40HF50 | IN1189A | 1N2136 | 1N2136A |  |  |
| 600 Volts700 Volts800 Volts900 Volts1000 Volts1200 Volts | $\begin{gathered} \text { IN3214 } \\ = \\ = \\ = \end{gathered}$ | $\begin{aligned} & 16 F 60 \\ & 16 F 80 \\ & 16 F 100 \end{aligned}$ | $\begin{aligned} & \text { IN3622 } \\ & \text { iN3623 } \\ & \text { iN3624 } \end{aligned}$ | z | 1 11190 | $\begin{aligned} & 40 \mathrm{HFEO} \\ & 40 \mathrm{FF} 70 \\ & 40 \mathrm{FFO} \\ & 40 \mathrm{FF} 0 \\ & 40 \mathrm{FP90} \\ & 40 \mathrm{HF} 100 \end{aligned}$ | iN1190A$=$$=$$=$ | $\begin{gathered} \text { 1N2138 } \\ = \\ = \\ = \end{gathered}$ | $\begin{gathered} 1 \mathrm{~N} 2138 \mathrm{~A} \\ = \\ = \\ = \end{gathered}$ | $\begin{aligned} & \text { 70H60A } \\ & 70 \mathrm{H} 70 \mathrm{~A} \\ & 70 \mathrm{HBOA} \\ & 70 \mathrm{H90A} \\ & 70 \mathrm{H} 100 \mathrm{~A} \\ & 70 \mathrm{H} 120 \end{aligned} .$ | $\begin{aligned} & \text { iN3293 } \\ & \text { iN3294 } \\ & \text { in3295 } \\ & \text { 1N3296 } \end{aligned}$ |
|  |  |  |  |  | 103765 |  |  |  |  |  |  |
|  |  |  |  |  | ${ }^{113} 37356$ |  |  |  |  |  |  |
|  |  |  |  |  | (1N3767 |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |

(1) Ambient temperature.
(2) Lead temperature, measured $3 / 8$-inch from body.
(1) Cathode to-Stud only.
(5) Cathode-to-Stud. For anode-to-stud, add " R " to base number
(3FR10, 1 N 3569 R ).
(1) Fast recovery rectifiers, see table on page 10.
(1) Note that thermal resistance is lower and operating temperatures
higher on "Reverye Pol arity" devics.
$\dagger$ JAN types ovailable.
(1) $I_{0}$-Current Rating. $1 \mathrm{~N} 3196=500 \mathrm{~mA} ; 1 \mathrm{~N} 3563=400 \mathrm{~mA}$.
(1) $\mathrm{t}_{\mathrm{r}}=5 \mu \mathrm{~m}$ max.
(iD) IN 2348 series he
(10) IN2348 series has 15 A surge rating.

Silicon Rectifiers


Silicon Rectifiers

| $\begin{aligned} & \mathrm{IF}(\mathrm{AV})(\mathrm{A}) \\ & \mathrm{QMax} . \mathrm{TC}^{\left({ }^{\circ} \mathrm{C}\right)} \end{aligned}$ | $\begin{gathered} 400 \\ @ 97^{\circ} \end{gathered}$ | $\varrho^{470}{ }^{4050}$ | $\begin{gathered} 500 \\ \varrho \\ \varrho 105^{\circ} \end{gathered}$ | $500$ | $\begin{gathered} 500 \\ \text { @ } 125^{\circ} \\ \hline \end{gathered}$ | $\begin{array}{r} 650 \\ @ 80^{\circ} \\ \hline \end{array}$ | ⑩0 | $\begin{gathered} 800 \\ @ 125^{\circ} \\ \hline \end{gathered}$ | $\begin{aligned} & 1600 \\ & \text { @1070 } \\ & \hline \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IFSM (A) | 3,500 | 6,250 | 8,000 | 10,000 | 10,000 | 8,000 | 8,000 | 10,000 | 25,000 |
| Notes | (6) | - | (3) 1) | (5) (1) | (5) | ( | - | - | - |
| Case Style | D0-200AA | DO-200AA | B-8 | B-8 | B-22 | D0-200AB | D0-200AB | D0-200AB | B-19 |
| PRV | PART NUMBERS |  |  |  |  |  |  |  |  |
| 50 Volts 200 Volts 400 Volts |  |  | Z | $\bar{Z}$ | 500V5A 500 V 20 A 500 V 30 A 500 V 40 A | $\begin{aligned} & \text { I } \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { Z } \end{aligned}$ |  |  |
| 500 Volts 600 Volts <br> 800 Voils 1000 Volts <br> 1200 Volts | 401POAGOL 401PDA80L 401PDA100L 401PDA120L | $\begin{gathered} \bar{Z} \\ \bar{Z} \\ \text { 471PDA120 } \end{gathered}$ | 501 V 120 | 501 V 60 B 501 V 80 B 501V100B 501V120 | 500 V 50 A 500 V 60 A $\square$ |  | 801PDB120 | 801PDB60B 801PDB80B 801 PDB1008 801PDB120B | $\begin{gathered} \overline{\mathrm{E}} \\ \text { 1601PDK } 120 \end{gathered}$ |
| 1300 Volts 1400 Volss 1600 Volts 2000 Volts | 401PDA130L 401PDA140L 401PDA1G0L - | 471PDA140 471PDA160 471PDA180 471PDA200 <br> 471PDAZO | 501 V 140 501 V 160 501 V 200 | 501V140B $=$ | I | 651PDB130L 651PD8140L 651PDB160L <br> - | 801PDB140 ${ }^{801 P D B 160}$ 801PDB200 | 801PDB140B | 1601PDK140 1601PDK160 1601PDK180 1601POK200 |
|  | $=$ | = $=$ $=$ | ${ }_{501 \mathrm{~V} 210}^{5010}$ 501 V 230 501 V240 | $\begin{aligned} & \text { I } \\ & \text { I } \\ & \hline \end{aligned}$ | - | Z I | $801 P D 8210$ 801 PD 8220 801 DD8230 801PDB240 | = | 1601PDK220 1601PDKK240 1601POK250 |


| $\begin{aligned} & \mathrm{IF}(A V)(A) \\ & \text { © } \max . \mathrm{T}_{\mathrm{C}}\left({ }^{(0} \mathrm{C}\right) \\ & \hline \end{aligned}$ | $\begin{aligned} & 2000 \\ & { }^{2050} 0 \end{aligned}$ | $\begin{aligned} & 24000 \\ & \text { e } 1070 \end{aligned}$ | $\begin{aligned} & 3000 \\ & \varrho \end{aligned}$ |
| :---: | :---: | :---: | :---: |
| IFSM (A) | 30,000 | 39,000 | 45,000 |
| Notes | - | - | - |
| Case Style | B.19 | B-20 | B. 20 |
| PRV | PART NUMBERS |  |  |
| 600 Volts 800 Volts 1000 Volts 1400 Volts | 2001 PDK60 2001PDK80 2001PDK100 2001POK120 2001POK 140 | 2601PDN 120 <br> 2601PDN 140 | 3001PDN60 3001 PON8O 3001PON 100 3001PON 120 3001PDN 140 |
| 1600 Volts | 2001POK160 | 2601PON160 | 3001PON160 |
| 1800 Volis |  | 2601P0N180 | - |
| 2000 Volts 2200 Volss | - | 2601PON200 2601PON220 | - |
| 2400 Volis | - | 2601 PON 240 | - |
| 2500 Volts | - | 2601PON250 | - |


| $\begin{aligned} & \text { IF(AV) (A) } \\ & Q T_{C}\left({ }^{\circ} \mathrm{C}\right) \end{aligned}$ |  |  | $\begin{gathered} 20 \\ 85^{\circ} \end{gathered}$ | $\begin{gathered} 25 \\ 70^{\circ} \end{gathered}$ | $\begin{gathered} 25 \\ 85^{\circ} \end{gathered}$ | $\begin{aligned} & 40 \\ & 80^{\circ} \end{aligned}$ | $\begin{gathered} 50 \\ 80^{\circ} \end{gathered}$ | $\begin{aligned} & 50 \\ & 80^{\circ} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| IFSM (A) |  |  | 800 | 400 | 800 | 800 | 800 | 800 |
| $\mathrm{V}_{\mathrm{FM}}(\mathrm{V})$ |  |  | 0.8 | 0.86 | 0.7 | 0.97 | 0.86 | 0.87 |
| $@_{\text {¢ }}^{\text {FM }}$ ( $(\mathrm{A}) @ \mathrm{~T}_{\mathrm{J}}=25^{\circ} \mathrm{C}$ |  |  | 80 | 80 | 80 | 160 | 160 | 160 |
| Case Style |  |  | D0-4 | D0.4 | D0-4 | D0-5 | D0-5 | D0.5 |
| $\mathrm{V}_{\text {RRM }}(\mathrm{V})$ | $\mathrm{V}_{\text {RSM }}(\mathrm{V})$ | $V_{\text {f }}(\mathrm{v})$ |  |  |  |  |  |  |
| 10 | 12 | 10 |  |  | ${ }^{25 F} 0010$ |  |  | ${ }^{50 \mathrm{HOOTO}} 5$ |
| 15 20 | 18 24 | 15 20 | - | - |  | - | - | ( $\begin{aligned} & \text { 50H0015 } \\ & 50 \mathrm{HOO20}\end{aligned}$ |
| 25 | 24 30 | 25 | 20F0025 | - | ${ }^{25 F}$ | 40H2025 | - |  |
| 30 | 36 | 30 | $20 F 0030$ | IN6095 | 25F0030 | 40НС030 | 1w6097 | 50H0030 |
| $\begin{aligned} & 35 \\ & 40 \end{aligned}$ | $\begin{aligned} & 42 \\ & 48 \end{aligned}$ | $\begin{aligned} & 35 \\ & 40 \end{aligned}$ | $20 F 0035$ | 1世6096 | - | 40 H 0040 | 1N6098 | - |

FAST RECOVERY RECTIFIERS

International Rectifier fast recovery diodes are similar to conventional diffused diodes of comparable current and voltage rating, but they have been specially processed so that the peak recovery current is lower and recovery time is shorter.
The three major uses for fast recovery rectifier diodes are: 1. Rectifiers for high frequency $A C$. The largest IR fast recovery rectifiers are capable of efficient rectification up to 10 kHz , smaller devices at even higher frequencies.
2. By-pass (free-wheeling) diodes on the output of a phase-By-pass (free-wheeling) diodes on the output of a phase-
controlled rectifier unit. They substantially reduce the momentary high load and junction heating on SCRs during reverse recovery of the by-pass diode.
3. By-pass diodes in a DC chopper or inverter. In addition to the benefits described above, in \#2, IR fast recovery in potentor this application also make a significant reduction recovery.

| max. Continuous CURRENT (A) | $\begin{aligned} & \text { VOLTAGE RANGE } \\ & \text { (V) } \end{aligned}$ | trr $^{\text {-RECOVERY TIME }}$ ( $\mu \mathrm{sec}$ ) | $\begin{aligned} & \text { IRM(REC) - RECOVERY } \\ & \text { CURRENT (A) } \end{aligned}$ | CASE STYLE | IR SERIES |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} \hline 6 \\ 6 \\ 6 \\ 6 \\ 6 \\ \hline \end{array}$ | 50.400 $500 \cdot 600$ $50 \cdot 1000$ 50.1000 50.400 |  | 2 MAX 2 MAX 3 MAX 4 MAX 2 MAX. | 004 004 $00-4$ 00.4 00.4 $00-4$ | $\begin{aligned} & \text { 1N } 3879 \\ & \text { 6FL } \\ & \text { 6FT } \\ & \text { 6FV } \\ & \text { 1N } 3889 \\ & \hline \end{aligned}$ |
| $\begin{array}{r} 12 \\ 12 \\ 12 \\ 100 \\ 100 \\ \hline \end{array}$ | $500 \cdot 600$ 50 -1000 400 - 1200 | 0.20 MAX . 0.50 MAX 1.5 MAX 2.0 MAX | $\begin{aligned} & 2 \mathrm{MAX} \\ & 2 \mathrm{MAX} \\ & 4 \mathrm{MAXX} \\ & \text { 25 MAX } \\ & 33 \mathrm{MAX} . \end{aligned}$ | $\begin{aligned} & 004 \\ & 004 \\ & 004 \\ & 004 \\ & 00.8 \\ & 00-8 \\ & \hline 008 \\ & \hline \end{aligned}$ | 12 FL <br> 101 KL S. 15 <br> 101KL.S20 |
| $\begin{aligned} & 100 \\ & 250 \\ & 250 \\ & 250 \\ & 250 \\ & \hline 400 \\ & \hline \end{aligned}$ |  |  | $\begin{aligned} & 50 \text { MAX } \\ & 25 \text { MAX } \\ & 33 \text { MAX } \\ & 50 \text { MAX } \\ & 30 \text { MAX. } \end{aligned}$ | D0-8 <br> D0-9 <br> D0-9 D0-9 <br> DO-200AA | 101KLS30 251UL-S15 251ULS20 401PD 401PDA-L15 |
| $\begin{aligned} & 400 \\ & 400 \\ & 650 \\ & 650 \\ & 650 \\ & 650 \\ & \hline \end{aligned}$ |  |  | 35 MAX. 60 MAX. 33 MAX 41 MAX. 49 MAX. |  | 401PDA- 20 401PDA-L30 651PDB-L20 651PDB-L30 |

## ZenerVoltage Regulators

 t.C. Voltage References

## Zener Voltage Regulators T.C. Voltage References



| Pown Rating | 250 mW |  | 400 mW |  | 400mW |  | 400mW |  | 400 mW |  | 500mW |  | 1W |  | 1w |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { Max Op. } \\ & \text { Temp } \left.{ }^{\circ} \mathrm{C}\right) \end{aligned}$ | 2000 |  | 1750 |  | 1750 |  | $150{ }^{\circ}$ |  | 2000 |  | 2000 |  | 1650 |  | 1650 |  |
| Tolerance (\%) | 5,10\% |  | 5, 10\% |  | 5, 10, 20\% |  | 5, 10\% |  | 15\% |  | 5. 10, 20\% |  | 5, 10\% |  | 5.10,20\% |  |
| Notes | (9) |  | (1) $\dagger$ |  | (12) |  | (3) |  | $=$ |  | (13) |  | (1) |  | ( D) |  |
| Case Style | D0.7 |  | D0.7 |  | D0.7 |  | D0.7 |  | D0.7 |  | D0.7 |  | D0-13 |  | D0.13 |  |
|  | Part No. | $\begin{aligned} & \mathbf{l}_{12 t} \\ & (\mathrm{mAA}) \end{aligned}$ | Part No. |  | $\begin{aligned} & \text { Pant } \\ & \text { No. } \end{aligned}$ | $\begin{gathered} \left.\mathrm{l}_{\mathrm{l}}^{\mathrm{mA}}\right) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \mathbf{l}_{27} \\ & \left(\mathrm{~mA}^{\prime}\right. \end{aligned}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{gathered} \mathbf{c}_{12 t} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{gathered} \mathbf{c}_{\mathrm{zt}} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{gathered} 1 \mathrm{zt} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | (mat |
| 2.4 | - | - | 1 N 4370 | 20 | - | - | - | - | - | - | 1 N5221 | 20 |  |  |  |  |
| (2.5) | - | - |  |  | - | - | - | - | - | - | 1 1N5222 | 20 | - | $=$ | - | - |
| (2.8) | - | - | 1N4371 | 20 | - | - | - | = | - | - | (1N5223 | 20 20 | - | $=$ | - | - |
| 3.0 | - | - | 1 1N372 | 20 | - | - | - | - |  | - | in5225 | 20 | - | - | - | - |
| 3.3 | - | - | ${ }^{1} 1 \times 746$ | 20 | - | - | - | - | - | - | 1 105226 | ${ }^{20}$ | - | - | - | - |
| 3.6 3.9 | - | - | 1N747 NT748 | ${ }_{20}^{20}$ | - | - | - | - | - | - | 1N5227 | ${ }_{20}^{20}$ | 1 N 1518 | 50 | 123.9 | 50 |
| 4.3 | - | - | WN749 | ${ }_{20}^{20}$ | - | - | - | - | - | - | iN5229 | 20 | 1N1518 | 5 | 184.3 | 50 |
| 4.7 | - | - | 1N750 | 20 | - | - | - | - | 1N3510 | 20 | IN5230 | 20 | 1N1519 | 40 | 124.7 | 40 |
| 5.1 |  |  | 1N751 | 20 | - | = |  | 5 | 1N3511 | 20 | 1N5231 | ${ }_{20}^{20}$ | 1N1520 |  | 125.1 125.6 | 40 35 |
| 5.6 $(6.0)$ | 1N708 | 25 | 1N752 | 20 | - | - | 1N1956 | ${ }_{5}^{5}$ | 1N3512 | 20 | TN5233 | 20 | 1N1520 |  | 125.6 | 35 |
| 6.2 | 1N709 | 25 | 1N753 | 20 |  | $\overline{-}$ | - | - | ${ }^{1} \times 3513$ | 20 | ${ }_{1} \mathbf{N 5 5 2 3}$ | 20 | 15 | $\overline{3}$ | 176.2 | 35 |
| 6.8 | 1N710 | 25 | 1N754 | 20 | IN957 | 18.5 | 1N1957 | 5 | 1N3514 | 20 | 1N5235 | 20 | 1N1521 | 30 | 128.8 | 30 |
| 7.5 | 1 N711 | 25 | 1 1755 | 20 | 1N958 | 16.5 |  | 5 | ${ }^{\text {1N3515 }}$ | 10 | 1 1N5236 | ${ }^{20}$ |  |  | 177.5 |  |
| ${ }^{8.2} 8$ | 1N712 | 25 | 1N756 | ${ }^{20}$ | 1N959 | ${ }^{15.0}$ | 1N1958 | 5 | 1N3516 | $\stackrel{10}{-}$ | 105237 | ${ }_{20}^{20}$ | 1N1522 | $\stackrel{25}{-}$ | 128.2 | 25 |
| 9.1 | 1N713 | 12 | 1N757 | 20 | 1 12960 | 14.0 |  | - | 1N3517 | 10 | 1N5239 | 20 | - |  | 129.1 | 25 |
| 10 | 1N714 | 12 | 1 1758 | 20 | 1N961 | 12.5 | 1N1959 | 5 | 1N3518 | 10 | 1 N5240 | 20 | 1N1523 | 20 | 1210 | 20 |
| 11 | 1 1N715 | 12 | 759 |  | ${ }^{1 \times 1} 962$ | 11.5 | 900 | - | ${ }^{11} 3519$ | 10 | IN5241 | ${ }^{20}$ |  |  | 1211 |  |
| 12 | 1 1N716 | 12 | 1 N759 | 20 | 1 11963 | 10.5 | 1N1960 | 1 | 1 $1 \times 3520$ | 10 | ${ }^{1} \mathbf{N 5 2 4 2}$ | 20 | 1N1524 | 15 | 1212 | 15 |
| ${ }^{13}$ | 1 12717 | 12 | - | - | 1N964 | 9.5 | - | - | 1N3521 | 5 | 1N5243 | 9.5 | = | - | 1213 | 15 |
| (14) | 1 N718 | - | - | - | 1N965 | 95 | 1N1961 | 1 | 1N3522 |  | ${ }^{1} \mathbf{N} 5244$ | 8.0 | - 152 | 13 |  |  |
|  |  | 12 | - |  | 1N965 | 8.5 |  |  | 1N3522 | 5 | 1 W5245 | 8.5 |  | 13 | 1215 | 13 |
| ${ }^{16}$ | 1N719 | 12 | - | - | 1N966 | 7.8 | - | - | 1 1N3523 | 5 | 1 1N5246 | 78 | - | - | 1216 | 13 |
| (17) | 1N720 | 12 | - | - | 1N967 | 7.0 | 1N1962 | 1 | 1N3524 | 5 | 1N5247 | 7.4 | 1N1526 | $\overline{10}$ | $12 \overline{18}$ | $\overline{10}$ |
| (19) |  |  | - | - |  |  |  | - |  |  | iN5249 | 6.6 | w1526 |  |  |  |
| 20 | 1N721 | 4 | - | - | 1 1968 | 6.2 | - | - | 1N3525 | 5 | iN5250 | 6.2 | - | - | 1220 | 10 |
| 22 | ${ }_{1}^{1 N 722}$ | 4 | - | = | 1 1N969 |  | 1N1963 | 1 |  |  | ${ }^{\text {N N5251 }}$ |  | 1N1527 | 9 | 1722 | 9 |
| (25) | 1 12723 | 4 | - | - | 1 19970 | 5.2 | = | - | 1N3527 | 5 | 1N5252 | 55.2 | - | - | 1224 | 9 |
| 27 | 1N724 | 4 | - | - | 1ल971 | 4.6 | 1N1964 | 1 | 1N3528 | 4 | iN5254 | 5.6 4.6 | 1N1528 | - | 1227 | 7 |
| (28) |  | - | - | - |  | . 6 |  | - |  | - | 1N5255 | 4.5 |  | - |  |  |
|  | 1N725 |  |  |  |  |  |  |  |  |  | 1 1N5256 |  |  |  | 1230 |  |
| ${ }_{36} 33$ | - | - | - | - | 1 19973 | 3.8 | IN1965 | 0.2 | 1N3530 | 3 | 1 N525] | 3.8 | - | - | - |  |
| 36 39 | - | - | - | - | -1N974 | 3.2 <br> 3.2 | - | = |  | - | 1N5258 | 3.4 <br> 3.2 | - | - | - | - |
| 43 | - | - | - | - | 1N976. | 3.0 | - | - | - | - | 1N5260 | 3.0 | - | - | - | - |
|  |  |  |  |  | 1 19977 |  |  |  | - |  | 1 1N5261 |  |  |  |  |  |
| $\begin{aligned} & 51 \\ & 56 \end{aligned}$ | - | - | = | - | $\begin{aligned} & \text { iN978 } \\ & \text { iN979 } \end{aligned}$ | 2.5 <br> 2.2 | - | - | - | = | 1N5262 | 2.5 2.2 | - | = | - | $=$ |
| (180) |  |  |  | - |  |  |  |  |  | - | 1N5264 | 2.1 |  | - |  | = |
| 62 |  | - | - | - | 1 N980 | 2.0 | - | - | - | - | 1 N5265 | 2.0 | - | - | - |  |
|  |  |  |  |  |  |  |  |  |  |  | ${ }^{1} 512266$ |  | - |  | - | - |
| 75 82 | - | = | - | - | 1N982 in983 | 1.7 | - | - | - | - | - 1 N5267 | 1.5 | - | - | - | - |
| (87) | - | - | - | - | - | - | - | - | - | - | ${ }^{1152529}$ | 1.4 | - | - | - | - |
| 91 100 | - | - | - | = | (1N984 | 1.4 1.3 | - | - | - | - | (1N5270 $\begin{aligned} & 1 \times 27 \\ & \text { N5271 }\end{aligned}$ | 1.4 <br> 1.3 | - | - | - | - |

ZenerVoltage Regulators t.C. Voltage References


| Power Rating | 1w |  | 1w |  | 1w |  | 1w |  | 1w |  | 3.5W |  | 3.5W |  | 5W |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \hline \begin{array}{l} \text { Max. Op. } \\ \text { Temp. }\left(O^{\circ}\right) \end{array} \end{aligned}$ | 1750 |  | 1750 |  | 1750 |  | 2000 |  | $200{ }^{\circ}$ |  | 1650 |  | $165^{\circ}$ |  | 2000 |  |
| $\begin{array}{\|l\|} \hline \begin{array}{l} \text { Tolerance } \\ (\%) \end{array} \\ \hline \end{array}$ | 5, 10,20\% |  | 5,10\% |  | 5, 10, 20\% |  | 5.10\% |  | 5, 10\% |  | 5, 10\% |  | 5, 10, 20\% |  | 5, 10, 20\% |  |
| Notes | 9. 1 |  | (3) |  | (12) |  | (3) |  | (1) |  | (1). (1) |  | (13), (16) |  | (12) |  |
| CaseStyle. | D0-13 |  | D0.13 |  | D0-13 |  | D0.41 |  | D041 |  | D0-4 |  | 004 |  | C-12 |  |
| $\mathrm{V}_{2}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline \begin{array}{l} I_{2 t} \\ (\mathrm{~mA}) \end{array} \\ \hline \end{array}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \mathrm{I}_{\mathrm{tz}}(\mathrm{~mA}) \end{aligned}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \mathbf{c}_{(12} \\ & (\mathrm{mAA}) \end{aligned}$ | $\begin{aligned} & \text { Part } \\ & \text { No } \end{aligned}$ | $\begin{gathered} 12 \mathrm{I} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \text { No. } \end{aligned}$ | $\begin{gathered} \mathrm{I}_{2 \pi} \\ (\mathrm{~mA}) \end{gathered}$ | $\begin{aligned} & \text { Part } \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \begin{array}{l} \ln \\ (\mathrm{mA}) \end{array} \end{aligned}$ | Part No. | $\begin{gathered} \mathrm{c}_{\mathrm{It}}\left(\mathrm{~mA}^{\prime}\right. \end{gathered}$ | Part No. | $\begin{aligned} & 1 \mathrm{l} 2 \mathrm{t} \\ & (\mathrm{~mA}) \end{aligned}$ |
| $\begin{aligned} & 3.3 \\ & 3.6 \\ & 3.9 \\ & 4.3 \\ & 4.7 \\ & \hline \end{aligned}$ | 1N3821 1N3822 1N3823 1N3824 iN3825 | 76 <br> 69 <br> 64 <br> 58 <br> 53 | Z |  | $\bar{Z}$ | $\bar{Z}$ | $\begin{aligned} & \text { 1N4728 } \\ & \text { 1N4729 } \\ & \text { 1N4730 } \\ & \text { 1N4731 } \\ & \text { 1N4732 } \\ & \hline \end{aligned}$ | 76 <br> 69 <br> 64 <br> 58 <br> 53 | $\begin{aligned} & 1283.3 \\ & 1283.6 \\ & 1283.9 \\ & 1124.9 \\ & 1284.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & 76 \\ & 69 \\ & 64 \\ & 58 \\ & 53 \\ & \hline \end{aligned}$ | $\begin{gathered} \overline{-} \\ \text { 1N1588 } \\ \text { 1N } 1589 \\ \hline \end{gathered}$ | $\begin{gathered} \overline{7} \\ \frac{150}{125} \\ \hline 125 \end{gathered}$ | $\begin{aligned} & \overline{-} \\ & 3 z 3.9 \\ & 374.3 \\ & 374.7 \\ & \hline \end{aligned}$ | $\begin{aligned} & - \\ & 150 \\ & 150 \\ & 125 \\ & \hline \end{aligned}$ | 1N5333 1N5334 1N5335 1N5336 iN5337 | $\begin{aligned} & 380 \\ & 3500 \\ & 3200 \\ & 2990 \\ & 260 \\ & \hline \end{aligned}$ |
| 5.1 <br> 5.6 <br> $(6.0)$ <br> 6.2 <br> 6.8 <br> 7.5 | $\begin{aligned} & \text { 1N3826 } \\ & \text { iN3827 } \\ & \text { 1N } 3828 \\ & \text { iN3829 } \\ & \hline \end{aligned}$ | $\begin{array}{\|l\|} \hline 49 \\ 45 \\ \hline 41 \\ 37 \\ \hline \end{array}$ | $\begin{array}{\|l\|} \hline \text { 1N1765 } \\ \text { 1N1766 } \\ \text { 1N1767 } \\ \hline \text { 1N1768 } \end{array}$ | $\begin{aligned} & 100 \\ & 100 \\ & 100 \\ & 100 \end{aligned}$ |  | $\begin{array}{\|l} \hline- \\ \overline{37} \\ \hline 34 \end{array}$ | 1N4733 <br> 1N4734 <br> - <br> 1N4735 <br> iN4736 <br> 1N 4737 | $\begin{aligned} & 49 \\ & 45 \\ & \hline 41 \\ & 37 \\ & 34 \end{aligned}$ | $\begin{aligned} & 12 \mathrm{ZS5.1} \\ & 1 \mathrm{ZS5.6} \\ & 18-. \\ & 1 \mathrm{SS6.2} \\ & \hline 17 S 7.5 \end{aligned}$ | $\begin{aligned} & 49 \\ & 45 \\ & \hline 41 \\ & 37 \\ & \hline 34 \end{aligned}$ |  | $\begin{gathered} \overline{110} \\ \overline{100} \end{gathered}$ | $\begin{aligned} & 325.1 \\ & 325.6 \\ & 326.2 \\ & 32.8 \\ & \hline 377.5 \\ & \hline \end{aligned}$ | $\begin{aligned} & 125 \\ & 110 \\ & 110 \\ & 100 \\ & \hline 100 \end{aligned}$ | 1N5338 <br> 1N5339 <br> 1N5340 <br> 1N5341 <br> iN5342 | 240 <br> 220 <br> 200 <br> 200 <br> 175 <br> 175 |
| $\begin{aligned} & 7.5 \\ & 8.2 \\ & 18.71 \\ & 9.1 \\ & 10 \end{aligned}$ |  | $\bar{z}$ | $1 N 1768$ iN1769 <br> 1 N1770 <br> 1N177 | $\begin{array}{r} 100 \\ 100 \\ 50 \\ 50 \\ 50 \end{array}$ | N N 3017 iN3018 <br> 1N3019 iN3020 <br> in3020 | $\begin{aligned} & 34 \\ & 31 \\ & 28 \\ & 28 \\ & 25 \end{aligned}$ | $\begin{aligned} & \text { iN4737 } \\ & \text { iN4738 } \\ & \text { iN } \mathrm{N} 739 \\ & \text { iN474 } \end{aligned}$ | $\begin{aligned} & 34 \\ & 31 \\ & 28 \\ & 25 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1257.5 \\ & 1258.2 \\ & 1259.1 \\ & 12510 \end{aligned}$ | $\begin{aligned} & 34 \\ & 31 \\ & 28 \\ & 25 \end{aligned}$ | $\begin{gathered} \text { 1N } 1592 \\ = \\ \text { 1N } 1593 \end{gathered}$ | $\begin{aligned} & \overline{80} \\ & \overline{7} \\ & \overline{70} \end{aligned}$ | $\begin{aligned} & 377.5 \\ & 328.2 \\ & 329.1 \\ & 3210 \\ & \hline \end{aligned}$ | $\begin{array}{r} 100 \\ 80 \\ \hline 80 \\ 70 \\ \hline \end{array}$ |  | 175 <br> 150 <br> 150 <br> 150 <br> 125 |
| $\begin{array}{r} 11 \\ 12 \\ 13 \\ (14) \\ 15 \\ \hline 18 \\ \hline \end{array}$ | I | $\bar{Z}$ |  | $\begin{aligned} & 50 \\ & 50 \\ & 50 \\ & 50 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { iN3021 } \\ & \text { N302 } \\ & \text { iN3023 } \\ & \text { in } 3024 \\ & \hline \end{aligned}$ | $\begin{array}{\|l} 23 \\ 21 \\ 19 \\ 19 \\ \hline 17 \end{array}$ | $\begin{aligned} & \text { 1N4741 } \\ & \text { N } 14742 \\ & \text { N } 44743 \\ & \text { iN } 47444 \end{aligned}$ | $\begin{aligned} & 23 \\ & 21 \\ & 19 \\ & \hline 17 \\ & \hline 1 \end{aligned}$ | $\begin{aligned} & 12511 \\ & 12812 \\ & 12513 \\ & 1 z 515 \\ & \hline \end{aligned}$ | $\begin{aligned} & 23 \\ & 21 \\ & 19 \\ & 19 \\ & \hline 17 \\ & \hline \end{aligned}$ | 1N1594 | 50 <br>  | $\begin{aligned} & 3211 \\ & 3212 \\ & 3213 \\ & 3215 \\ & \hline 2716 \\ & \hline \end{aligned}$ | $\begin{aligned} & 70 \\ & 50 \\ & 50 \\ & 50 \\ & \hline 40 \\ & \hline \end{aligned}$ |  | 125 <br> 100 <br> 100 <br> 100 <br> 75 |
| $\begin{aligned} & 16 \\ & 167 \\ & 18 \\ & 18 \\ & (19) \\ & 20 \\ & \hline \end{aligned}$ |  |  | $\begin{gathered} \hline \text { 1N1776 } \\ \text { 1N1777 } \\ \text { in̄78 } \end{gathered}$ | $\begin{aligned} & \frac{50}{50} \\ & \frac{50}{15} \end{aligned}$ | $\begin{gathered} \text { iN3025 } \\ \text { iN } 3026 \\ \text { in } 3027 \end{gathered}$ | $\begin{gathered} 15.5 \\ \overline{14.0} \\ 12.5 \\ \hline 1.5 \end{gathered}$ | $\begin{aligned} & \text { 1N4745 } \\ & \text { iN4746 } \\ & \text { iN4747 } \end{aligned}$ | 15.5 <br> 14.0 <br> 12.5 | $\begin{aligned} & 12 S 16 \\ & 12518 \\ & 12520 \end{aligned}$ | $\begin{aligned} & \frac{15.5}{} \overline{14.0} \\ & \overline{12.5} \\ & \hline \end{aligned}$ | 1N1596 |  | $\begin{aligned} & 3216 \\ & 3218 \\ & 3220 \\ & \hline \end{aligned}$ | $\begin{aligned} & 40 \\ & \frac{30}{35} \\ & \overline{35} \\ & \hline \end{aligned}$ |  | 75 70 75 65 65 65 |
| $\begin{aligned} & 22 \\ & 24 \\ & 24 \\ & (25) \\ & 27 \\ & (28) \\ & \hline \end{aligned}$ | Z |  | $\begin{array}{\|l\|l} \hline 1 \text { N1779 } \\ \text { iN1780 } \\ \text { iN1781 } \end{array}$ | $\begin{aligned} & 15 \\ & 15 \\ & \hline 15 \end{aligned}$ | $\begin{aligned} & \text { 1N3028 } \\ & \text { 1N3029 } \\ & \text { 1N } 3030 \end{aligned}$ | $\begin{gathered} 11.5 \\ 10.5 \\ \hline 9.5 \end{gathered}$ | $\begin{aligned} & \text { 1N4748 } \\ & \text { N } \mathrm{N} 4749 \\ & \text { 1N4750 } \end{aligned}$ | $\begin{gathered} 11.5 \\ 10.5 \\ \hline 9.5 \end{gathered}$ | $\begin{aligned} & 1 z 522 \\ & 1 z 524 \\ & 1 z 527 \end{aligned}$ | $\begin{gathered} 11.5 \\ 10.5 \\ 9.5 \end{gathered}$ | $\begin{gathered} \hline \text { 1N1597 } \\ = \\ \text { iN1598 } \end{gathered}$ | $\begin{aligned} & 30 \\ & \frac{30}{25} \end{aligned}$ | $\begin{aligned} & 3222 \\ & 3224 \\ & 3227 \end{aligned}$ | $\begin{aligned} & 30 \\ & 30 \\ & 25 \end{aligned}$ |  | 50 50 50 50 50 50 |
| $\begin{aligned} & 30 \\ & 33 \\ & 36 \\ & 39 \\ & 43 \\ & \hline \end{aligned}$ |  |  | $\begin{array}{\|l\|l\|l\|l\|} \hline \text { N1782 } \\ \text { 117783 } \\ \text { 1N7784 } \\ \text { 1N1775 } \\ \text { } 11778 \\ \hline \end{array}$ | 15 15 15 15 15 15 | $\begin{aligned} & \text { iN3031 } \\ & \text { NN3032 } \\ & \text { N3033 } \\ & \text { N } 30303 \\ & \text { N3035 } \\ & \hline \end{aligned}$ | $\begin{aligned} & 8.5 \\ & 7.5 \\ & 7.0 \\ & 6.5 \\ & 6.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 8.5 \\ & 7.5 \\ & 7.0 \\ & 6.5 \\ & 6.0 \\ & \hline 58 \end{aligned}$ | $\begin{aligned} & 12530 \\ & 12533 \\ & 17536 \\ & 12539 \\ & 12543 \\ & \hline 17 c 47 \end{aligned}$ | 8.5 7.5 7.0 7.5 6.0 | - |  | $\begin{gathered} 3230 \\ = \\ - \end{gathered}$ | 25 - - | 1N5363 N5364 N5365 N N5366 N5536 N | 40 <br> 40 <br> 30 <br> 30 <br> 30 |
| $\begin{gathered} 47 \\ 51 \\ 56 \\ 601 \\ 62 \\ \hline \end{gathered}$ | $\bar{z}$ |  | $\begin{aligned} & \text { 1N1787 } \\ & \text { 1N1788 } \\ & \text { 1N1789 } \\ & \text { in1790 } \end{aligned}$ | $\begin{aligned} & 15 \\ & 15 \\ & 15 \\ & \hline 5 \\ & \hline 5 \end{aligned}$ | $\begin{aligned} & \text { 1N3036 } \\ & \text { iN3037 } \\ & \text { N } 3038 \\ & \text { iN3039 } \end{aligned}$ | $\begin{aligned} & 5.5 \\ & 5.0 \\ & 4.5 \\ & \hline 4.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 1N4756 } \\ & \text { N47757 } \\ & \text { NA } 4758 \\ & \text { iN } 7759 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5.5 \\ & 5.0 \\ & 4.5 \\ & \hline 4.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 17547 \\ & 1751 \\ & 1 Z 556 \\ & 12562 \\ & 1266 \end{aligned}$ | $\begin{aligned} & 5.5 \\ & 5.0 \\ & 4.5 \\ & \hline 4.0 \\ & \hline \end{aligned}$ | Z |  | Z | - | 1N5368 N55369 N5390 N5537 N5537 in532 | 25 <br> 25 <br> 20 <br> 20 <br> 20 |
| $\begin{aligned} & \hline 68 \\ & 75 \\ & 82 \\ & 1871 \\ & 91 \\ & \hline \end{aligned}$ | $\bar{Z}$ | $\bar{Z}$ | $\begin{array}{\|l\|l\|} \hline 1 \mathrm{~N} 1791 \\ \text { 1N1792 } \\ \text { 1N1793 } \\ \text { iN1794 } \\ \hline \end{array}$ | $\begin{aligned} & 5 \\ & 5 \\ & 5 \\ & \hline 5 \\ & \hline \end{aligned}$ | iN3040 <br> iN3041 <br> iN3042 <br> in 3043 | $\begin{aligned} & 3.7 \\ & 3.3 \\ & 3.0 \\ & \hline 2.8 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 3.7 \\ & 3.3 \\ & 3.0 \\ & \hline 2.8 \end{aligned}$ | $\begin{aligned} & 17558 \\ & 1255 \\ & 12582 \\ & 12859 \\ & 12891 \end{aligned}$ | $\begin{aligned} & \begin{array}{l} 3.7 \\ 3.3 \\ 3.0 \\ \hline 2.8 \\ \hline \end{array} \begin{array}{l}  \\ \hline \end{array} \\ & \hline \end{aligned}$ | = | $\bar{z}$ | $\bar{Z}$ | Z | $\begin{aligned} & 1 \text { N5373 } \\ & \text { N5374 } \\ & \text { 1N5374 } \\ & \text { N } 53376 \\ & \text { NN5377 } \end{aligned}$ | 20 20 15 15 15 15 |
| $\begin{aligned} & 100 \\ & 110 \\ & 120 \\ & 130 \\ & 130 \\ & \hline \end{aligned}$ | = | $\begin{aligned} & \bar{Z} \\ & \overline{2} \end{aligned}$ | $\begin{array}{\|l\|l\|l\|l\|l\|l\|} \hline \text { N1795 } \\ \text { 1N1796 } \\ \text { 1N1797 } \\ \text { 1N17989 } \\ \text { 1N179 } \end{array}$ | $\begin{aligned} & 5 \\ & 5 \\ & 5 \\ & \hline \end{aligned}$ | 1N3044iN3045 iN30461N3047 <br> 1N3048 | 2.5 2.3 2.0 1.9 1.7 | ${ }^{1 N 47764}$ 12 1212012 Z 130 <br> $1 \mathrm{ZV1} 150$ <br> 2 | 2.5 2.3 2.0 1.9 1.7 | 125100 125120 125130 $12 S 150$ | 2.5 <br> 2.3 <br> 2.0 <br> 1.9 <br> 1.7 <br> 1.8 | = | z- | = | z |  | 12 - - |
| $\begin{aligned} & 160 \\ & 180 \\ & 200 \\ & \hline \end{aligned}$ | I | Z | 1N1800 IN1801 iN1802 | $\begin{aligned} & 5 \\ & 5 \\ & 5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { 1N3049 } \\ & \text { 1N3050 } \\ & \text { N3051 } \end{aligned}$ | $\begin{aligned} & 1.6 \\ & 1.4 \\ & 1.2 \\ & \hline \end{aligned}$ | $\begin{aligned} & 127160 \\ & 127180 \\ & 127200 \end{aligned}$ | $\begin{aligned} & 1.6 \\ & 1.4 \\ & 1.2 \end{aligned}$ | $\begin{aligned} & 1725160 \\ & 1 z S 180 \\ & 1 Z S 200 \end{aligned}$ | 1.6 <br> 1.4 <br> 1.2 | = | - | - | - | - | - |

## ZenerVoltage Regulators

 t.C. Voltage References| (eater | \% |  | ow |  | 10w |  | ow |  | 10w |  | 10w |  | 50W |  | 50w |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ceme | 2000 |  | 150 |  | 1650 |  | 150 |  |  |  |  |  |  |  |  |  |
| ${ }_{\text {Tome }}^{\text {Totarane }}$ | 5.10,20x |  | . $10 \%$ |  | 5.10,20x |  | 108 |  | 5.10,20\% |  | 5.108 |  | 5.10, 200 |  |  |  |
|  | ${ }_{\text {c }}^{6} .12$ |  | 004 |  | 004 |  | 004 |  | 004 |  | 00.4 |  | 5.10 |  | ${ }_{\text {c. }}^{6}$ |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| $\mathrm{v}_{2}$ | ${ }_{\substack{\text { Pmor } \\ \text { No. }}}$ | ${ }_{(m \times 1}^{\text {ma }}$ | Pors | lma |  | ${ }_{\text {cma }}^{\text {lma }}$ | Por | (man | Pion | (mat | No. | (mat | Po. | (ma) | ${ }_{\text {Pann }}^{\text {Pang. }}$ | ${ }_{\text {l }}^{\text {lna }}$ |
|  |  |  | ${ }^{1 \times 159}$ inisoo | $500$ |  | $\begin{gathered} 500 \\ 4000 \\ 400 \end{gathered}$ | $\underset{\substack{1 \\ \text { N393 } \\ \text { N3394 } \\ \text { N395 }}}{2}$ | $\underset{\substack{80 \\ 50 \\ 50}}{50}$ |  | $\bar{Z}$ |  | $\bar{Z}$ |  | $\begin{aligned} & 3200 \\ & \begin{array}{l} 32000 \\ 26050 \end{array} \end{aligned}$ | $\begin{aligned} & \text { 1N4557 } \\ & \text { 1N4558 } \\ & \text { iNAFEO } \end{aligned}$ |  |
|  |  | $\begin{gathered} 2000 \\ \text { and } \\ 2000 \\ 20175 \end{gathered}$ |  | $\begin{aligned} & 250 \\ & \hline \\ & \hline 300 \\ & \hline 000 \end{aligned}$ | $\begin{aligned} & 1025.1 \\ & \hline 1025.6 \\ & 10282628 \\ & 10268 \end{aligned}$ | $\begin{aligned} & 400 \\ & \begin{array}{l} 350 \\ 350 \\ 300 \\ 300 \end{array} \end{aligned}$ |  |  | iN1805 | $\begin{aligned} & \overline{1} \\ & 1000 \end{aligned}$ | 1w2970 | $3 \overline{3}$ |  |  |  | (2450 |
|  |  | $\begin{aligned} & 175 \\ & \hline 1750 \\ & 1850 \end{aligned}$ | $\bar{i}$ | 250 | $\left\lvert\, \begin{aligned} & 1027.57 \\ & 10282 \end{aligned}\right.$ | $\begin{aligned} & 300 \\ & \frac{300}{250} \end{aligned}$ | $1 \mathrm{1m0}$ | ${ }^{3} 35$ | $\begin{aligned} & \begin{array}{l} \text { Wi806 } \\ \text { iviso } \end{array} \end{aligned}$ | $\begin{aligned} & 1000 \\ & 1000 \\ & 100 \end{aligned}$ | $\begin{array}{\|c} \begin{array}{l} \text { w} \\ \hline \end{array}{ }_{29} \end{array}$ | $\begin{aligned} & 335 \\ & 305 \end{aligned}$ |  |  |  | (1850 |
| $\begin{aligned} & 9.1 \\ & 101 \\ & 112 \\ & \hline 13 \end{aligned}$ |  |  | $\begin{array}{\|l\|l\|} \hline \begin{array}{l} \text { miver } \\ \text { invers } \end{array} \end{array}$ | $\begin{aligned} & 200 \\ & 100 \\ & 100 \end{aligned}$ |  | $\begin{aligned} & \text { 250 } \\ & \text { and } \\ & \text { 2200 } \\ & 100 \\ & 10 \end{aligned}$ |  | $\begin{array}{\|c} \substack{500 \\ \text { sion } \\ \text { sion } \\ 500} \end{array}$ |  |  |  |  |  |  |  |  |
|  |  |  | iwive <br> iniso | $\frac{100}{\frac{100}{100}}$ | ${ }_{10216}^{10216}$ | $\begin{aligned} & 190 \\ & \hline 1000 \\ & 100 \\ & 10 \\ & \hline \end{aligned}$ | $\begin{aligned} & \left.1 \begin{array}{l} 11817 \\ 1 \times 1818 \\ \text { wisi819 } \end{array}\right) \end{aligned}$ | $\begin{aligned} & \begin{array}{l} 500 \\ 500 \\ 500 \\ 500 \end{array} \end{aligned}$ |  | $\begin{aligned} & 500 \\ & 5000 \\ & 5 \\ & 150 \end{aligned}$ |  |  |  |  |  | cisi |
|  |  |  | 1 T 168 | $\stackrel{\square}{9}$ | $\underset{\substack{10220 \\ 10224 \\ 1022}}{\substack{102}}$ | $\begin{aligned} & \overline{n i n}_{\substack{90 \\ 90}} 0 \end{aligned}$ |  | $\begin{gathered} 250 \\ 250 \\ 250 \\ \hline 250 \end{gathered}$ |  | $\begin{aligned} & \text { is0 } \\ & \text { is } \\ & \hline 150 \end{aligned}$ |  |  |  |  |  |  |
|  |  | $\begin{aligned} & 50 \\ & 50 \\ & 40 \\ & 40 \\ & 30 \\ & 30 \end{aligned}$ | 131609 | $\stackrel{70}{\square}$ | $\begin{aligned} & 10277 \\ & 10230 \end{aligned}$ | $\frac{70}{20}$ |  | $\begin{aligned} & 250 \\ & \begin{array}{l} 250 \\ \text { 250 } \\ \text { 150 } \\ \hline 150 \end{array} \end{aligned}$ |  | 150 <br> $\substack{150 \\ 150 \\ 150 \\ 1}$ |  |  |  | $\begin{aligned} & 460 \\ & 460 \\ & 360 \\ & 350 \\ & 350 \end{aligned}$ |  | 460 <br> 480 <br> 430 <br> 350 |
|  |  | $\begin{aligned} & 30 \\ & \begin{array}{l} 30 \\ \frac{30}{25} \end{array} \end{aligned}$ |  |  |  |  |  | $\begin{aligned} & 150 \\ & \left.\begin{array}{l} 150 \\ 150 \\ 150 \end{array}\right) \end{aligned}$ |  | $\begin{aligned} & 150 \\ & \left.\begin{array}{l} 150 \\ 150 \\ \hline 150 \end{array} \right\rvert\, \end{aligned}$ |  | $\begin{aligned} & \text { 65 } \\ & 50 \\ & 505 \\ & 505 \\ & \hline 50 \end{aligned}$ |  | $\begin{aligned} & 320 \\ & 320 \\ & 230 \\ & 230 \\ & 250 \end{aligned}$ |  |  |
| $\begin{array}{\|l\|} \hline \\ \hline \end{array}$ |  | $\begin{aligned} & 25 \\ & \hline 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ |  |  |  | $\bar{\vdots}$ |  | $\begin{aligned} & \text { 150 } \\ & \begin{array}{l} 150 \\ 150 \end{array} \end{aligned}$ |  | $\begin{array}{\|c} \frac{150}{150} \\ \hline 50 \end{array}$ |  | $\begin{aligned} & 50 \\ & \hline \\ & \hline \\ & \hline \end{aligned}$ | $\underset{\substack{13332 \\ \text { NT333 } \\ \text { N333 }}}{\substack{3 \\ \hline}}$ <br> in3355 | $\begin{aligned} & 250 \\ & 2200 \\ & 220 \end{aligned}$ |  | 205 220 2 2 |
|  |  | $\begin{aligned} & \text { 20 } \\ & 20 \\ & 20 \\ & 10 \\ & \hline 15 \\ & \hline 15 \end{aligned}$ | $\bar{~}$ |  |  | $\bar{z}$ |  | $\begin{aligned} & 50 \\ & 50 \\ & 50 \\ & 50 \end{aligned}$ |  | $\begin{aligned} & 30 \\ & 500 \\ & 50 \\ & \hline 0 \end{aligned}$ |  | $\begin{aligned} & 33 \\ & 30 \\ & 28 \\ & 28 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 180 \\ & 180 \\ & 150 \\ & 150 \\ & \hline 100 \end{aligned}$ |  | (180 |
| $\begin{array}{\|l\|l} 1006 \\ 1005 \\ 1050 \\ 130 \\ 130 \end{array}$ | ${ }^{525100}$ | $\begin{aligned} & 12 \\ & \vdots \\ & \vdots \end{aligned}$ |  |  |  |  |  | $\begin{aligned} & 50 \\ & 50 \\ & 50 \\ & 50 \\ & 50 \end{aligned}$ |  | $\begin{aligned} & 50 \\ & -50 \\ & -50 \\ & 50 \\ & 50 \end{aligned}$ |  | $\begin{aligned} & 25 \\ & 25 \\ & 20 \\ & 208 \\ & 290 \end{aligned}$ | 1 10330 | 120 | 1w238 | ${ }^{120}$ |
|  |  |  |  | $\bar{Z}$ |  |  | 1N2012 | 50 |  | ${ }_{50}^{501}$ |  |  |  |  |  |  |

## Power Circuits: PACE/paks

PACE/paks are IR's family of electrically isolated, solid-state They are now available in both 25 Amp and 42.5 Amp current power assemblies, which provide complete control functions. They offer a wide variety of advantages over conventional methods of fabricating power supplies, control circuits, battery chargers, and choppers, including reduced costs, more efficient
heat-sinking, greater reliability, and a sharp reduction in total
package size.
ratings in seven circuit configurations. All are available in both 120 V and 230 V RMS ratings. witch configurat can be made using PACE/paks in an AC switch configuration, as replacements for conventionally assemAmp (rms) series.

AC SWITCHES


Case D-20


|  |  | PACE/pak Circuits |  | PACE/pak AC Switches |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | P100 | P200 | P240 | P640 | P340 |
| CASE |  | 0. 19 | 0.20 | 0.20 | 0.20 | 0.20 |
| Id | $\begin{aligned} & \text { max. dc output } \\ & \text { current © } 15^{\circ}{ }_{\mathrm{I}}^{\mathrm{C}}(\mathrm{~A}) \end{aligned}$ | 25 | 42.5 | - | - | - |
| ${ }^{\text {It }}$ (RMS) | max. output current e $75^{\circ} \mathrm{C}$ base plate | - | - | 50 | 60 | 100 |
| $\mathrm{V}_{\text {RMS }}$ | AC input voltage (V) | 120, 240 | 120, 240 | $\begin{gathered} 120.240, \\ 480 \end{gathered}$ | $\begin{gathered} 120.240 \\ 480 \end{gathered}$ | $\begin{gathered} 120,240, \\ 480 \end{gathered}$ |
| ${ }^{\text {TSSM }}$ | max. non-repetitive surge current ( A ) | 250 | 600 | 600 | 1000 | 1200 |
| $1^{2}$ | $\begin{aligned} & \text { max. } 12, \text { for fusing. } \\ & t=5108.3 \mathrm{msec}\left(\mathrm{~A}^{2} \mathrm{sec}\right) \end{aligned}$ | 260 | 1500 | 1500 | 4000 | 6000 |
| dildt | max. rate of rise of turned-on current (A/ $\mu \mathrm{sec}$ ) | 100 | 100 | 100 | 100 | 100 |
| dv/dt | min . critical rate of rise of turned-on current ( $\mathrm{A} / \mu \mathrm{sec}$ ) $\qquad$ | 20 | 20 | 20 | 20 | 20 |
| ${ }^{\text {IGT }}$ | $\begin{aligned} & \text { max. required gate, } \\ & \text { current to trigger. } \\ & 25^{\circ} \mathrm{C}(\mathrm{~mA}) \end{aligned}$ | 40 | 110 | 110 | 110 | 110 |
| $\mathrm{V}_{\text {GT }}$ | max. required gate voltage to trigger, $25^{\circ} \mathrm{C}$ (V) | 2.5 | 3.0 | 3.0 | 3.0 | 3.0 |
| $\mathrm{R}_{\text {ecs }}$ | thermal resistance. case to sink ( ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ) | 0.10 | 0.10 | 0.10 | 0.10 | 0.10 |

(1) Higher dv/dt available.

## Power Circuits: PACE/paks

P100 SERIES - VOLTAGE RATINGS AND CIRCUITS

|  | Cirevit BC |  | Cireuir BA |  | Cireuir BD |  | Circuir Bs |  | Circuit A |  | Circuit DA |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Terminal Positions |  |  |  |  |  |  |  |  | $5$ |  | $5_{\underline{2}}^{7}$ |  |
| Schematic Disgram |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Single Phase Hybrid Bridge, Common Cathode |  | Single Phase Hybrid Bridge, Common Anode |  | $\begin{gathered} \text { Single Phase, } \\ \text { Hyybrid Bridge } \\ \text { Doubber Connection } \end{gathered}$ |  | $\begin{gathered} \text { Single Phase, } \\ \text { All SSR } \\ \text { Bridge } \\ \hline \end{gathered}$ |  | $\begin{gathered} \text { Hybrid } \\ \text { AC Switch } \end{gathered}$ |  | $\begin{aligned} & \text { Hybrid } \\ & \text { Doubler } \end{aligned}$ |  |
| Basic series | P101 | P102 | P111 | P112 | P121 | P122 | P131 | P132 | P141 | P142 | P161 | P162 |
| $\begin{array}{\|l\|} \hline \text { With Klip-Sel } \\ \text { voltage } \\ \text { suppression } \end{array}$ | P101k | P102K | P111K | ${ }^{\text {P112K }}$ | $\mathrm{P}^{\text {P121K }}$ | P122K | P131K | P132K | P141K | P142K |  |  |
| $\begin{aligned} & \text { With free- } \\ & \text { wheeling } \\ & \text { diode } \end{aligned}$ | P101w | P102w | P111w | P112W | - | - | - | - |  | - |  |  |
| With both <br> KKip-Sel and <br> Kree-wheeling <br> diode <br> diode | P101KW | P102KW | P111 Kw | P112kw | - | - | - | - | - | - | - | - |
| $\begin{array}{\|l\|} \hline \text { V RMS-Max. }^{\text {Voltage }} \\ \hline \end{array}$ | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 |

P200 SERIES - VOLTAGE RATINGS AND CIRCUITS

|  | Cirevit BC |  | Circuir BA |  | Circuit BD |  | Circuit BS |  | Circuit A |  | Circuin DA |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Terminal Positions |  |  |  |  |  |  | $5^{8)^{A C 2}}{ }^{\text {al }}$ |  | $\underbrace{\left(®^{A C 1}\right.}$ |  |  |  |
| Schematic <br> Diagram |  |  |  |  |  |  |  |  |  |  |  |  |
|  | Single Phase Hybrid Bridge, Common Cathode |  | Single Phase Hybrid Bridge, Common Anode |  | Single Phase, Hybrid Bridge Doubler Connection |  | Single Phase, All SCR Bridge |  | Hybrid AC Switch |  | Hybrid Doubler |  |
| Basic series | P201 | P202 | P211 | P212 | P221 | P222 | P231 | P232 | P241 | P242 | P261 | P262 |
| With Klip-Sel voltage suppression | P201K | P202K | P211K | P212K | P221K | P222K | P231K | P232K | P241K | P242K |  |  |
| With freewheeling diode | P201w | P202W | P211w | P212W | - | - | - | - | - | - | - | - |
| With both Klip-Sel and free-wheeling diode | P201KW | P202kW | P211kW | P212KW | - | - | - | - | - | - | - | - |
| $\begin{aligned} & \text { VRMS-Max. } \\ & \text { Voltage } \end{aligned}$ | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 | 120 | 240 |

## Power Circuites: <br> Molded Circuit Assemblies



SINGLE PHASE DIODE BRIDGES

| SERIES | 18DB | 2208 | 75, ${ }^{\text {B }}$ | 1003B | 150J8 | 250 JB | 300JB | 400JB | 500JB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & I_{\text {dc }} \text { (A) } \\ & \text { Output Current } \end{aligned}$ | 1.8 | 2.2 | 7.5 | 10 | 15 | 25 | 30 | 40 | 50 |
| $@_{\text {© }} \mathrm{C}^{\left({ }^{\circ} \mathrm{C}\right)}$ | 50 (1) | 50 (1) | 75 | 75 | 75 | 75 | 75 | 75 | 75 |
| IFSM (surge) (A) | 50 | 50 | 75 | 100 | 150 | 300 | 350 | 500 | 600 |
| Circuit | B | B | B | B | B | 8 | 8 | 8 | 8 |
| Case Style | D. 2 | 0.2 | 0.17A | 0.17A | D.17A | 0.17A | D.17A | D.17A | D.17A |
| $V_{\text {RRM }}$ | PART NUMBERS |  |  |  |  |  |  |  |  |
| $\begin{array}{r} 50 \\ 500 \\ 200 \\ 300 \\ 400 \\ \hline \end{array}$ | 180805A 18082A 18083 A 18084 A |  | $75 \mathrm{JBO5L}$ 75JB2L 75JB4L | $1000805 L$ 100811 1000822 1000832 $100 J 841$ 10 | 1500805 L 1501811 150JB2L $150 \mathrm{JB4L}$ | $\begin{aligned} & 2501805 L \\ & 250 \mathrm{~L} \\ & 2501 \mathrm{~L} \\ & 25082 \mathrm{~L} \\ & 250 \mathrm{OB3LL} \\ & 250 \mathrm{BALL} \\ & \hline \end{aligned}$ | ${ }^{30001805 L}$ $300 \mathrm{JB2L}$ $300 \mathrm{BB4L}$ | ${ }^{4000 \mathrm{JB05L}}$ 400 B 2 L $400 \mathrm{BB3L}$ 400 B AL | $500 \mathrm{JB05L}$ $500 \mathrm{JB2L}$ 5000884 L |
| $\begin{gathered} 500 \\ 500 \\ 700 \\ 800 \\ 1000 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 22085 A \\ & 22086 \mathrm{~A} \\ & 22087 \mathrm{~A} \\ & 22008 \mathrm{~A} \\ & 220810 \mathrm{~A} \\ & \hline \end{aligned}$ | $75 \mathrm{JB5L}$ 75JB6L $\qquad$ | 100JB5L 100J86L $\qquad$ | 150 J B L <br> 150 L <br>  <br> $=$ <br> - | $250 J B 5 L$ $250 J B 6 L$ $=$ $=$ | $\begin{gathered} 300 \mathrm{JB5L} \\ 300 \mathrm{JB6L} \\ = \\ = \end{gathered}$ | $400 \mathrm{JB5L}$ $400 \mathrm{JB6L}$ , | 500JB5L $500 \mathrm{JB6L}$ $\qquad$ |

## Power Circuits:

Molded Circuit Assemblies


## Power Circuits: Molded Circuit Assemblies

| If(AV) - Current rating (A) © $50^{\circ} \mathrm{C}$ NATURAL CONVECTION |  |  | IFM(Surge) RGE RATING (A) |  | RM(rep) age range (v) | circuit |  | CASE STYLE | IR SERIES | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 75 mA to $250 \mathrm{~mA} @ 25^{\circ} \mathrm{C}$ 25 mA to 100 mA e $100^{\circ} \mathrm{C}$ |  |  | 50 |  | 6-10kV | H |  | 0.98 | 1N2373-84 | Miniature Cartridgess. |
| 75 mA to 250 mA e $25^{\circ} \mathrm{C}$ 25 mA to 010 mA e $100^{\circ} \mathrm{C}$ |  |  | 50 |  | 6-30kV | H |  | 0.98 | 67D006H 53PNN to 670300 H | Miniature Cartridges. |
| $45 \mathrm{~mA} \mathrm{to} 100 \mathrm{~mA} @ 75^{\circ} \mathrm{C}$ |  |  | 50 |  | 5-16KV | H |  | D.9A | 1N1133-49 | Ferrule mounted. |
| $250 \mathrm{~mA} \mathrm{~S}^{50}{ }^{\circ} \mathrm{C}$ |  |  | 50 |  | 5.50kV | H |  | D.9A | 670015H-55FNN to 67 D500HFNN | Ferrule mounted. |
| 250 mA to $440 \mathrm{~mA} @ 75^{\circ} \mathrm{C}$ Oil 220 mA to $360 \mathrm{~mA} @ 75^{\circ} \mathrm{C}$, 200 LFM |  |  | 50 |  | 5. 16KV | H |  | D-9A | 1N1745-62 | High current type |
| $\begin{aligned} & 375 \mathrm{~mA} \text { to } 500 \mathrm{~mA} \text { e } 50^{\circ} \mathrm{C} \text { Oil } \\ & \text { or } 200 \mathrm{LFM} \end{aligned}$ |  |  | 50 |  | 5.50kV | H |  | D.9A | 670015H-55FNN to 670500 HFNN | Higli current type |
| HIGH VOLTAGE MOLDED ASSEMBLIES |  |  |  |  |  |  |  |  |  |  |
| 250 mA |  |  | 50 |  | -40kV | H (1) |  | 0. 7 | 670050H0-4TNN to 670400 H | Avalanche selected devices |
| 350 mA |  |  | 50 |  | . 75 KV | H |  | $\begin{aligned} & 0.8 \mathrm{~A} \\ & 0.8 \mathrm{~B} \\ & \text { (2) } \end{aligned}$ | 670050H-20TTS to 670750 H | RC compensated for system reliability. |
| 1.25 |  |  | 90 |  | 5. 75 KV | H (1) |  | 0.8A | 1N4865-77 <br> \& 1N4887 | RC compensated |
| 1.25 |  |  | 90 |  | 5. 75 KV | H (1) |  | $\begin{gathered} \text { D-8A D-8B } \\ \hline(2) \end{gathered}$ | $\begin{aligned} & \text { 67S015H-20LSS } \\ & \text { to } 675750 \mathrm{H} \end{aligned}$ | RC compensated |
| (1) Standard circuit is halfwave. To order as doubler, change " H " to " O ". (Ex.: 67D015H20TTS becomes 670015020TTS) <br> (2) $0-8 \mathrm{~A}$ is halfwave. $D-8 \mathrm{~B}$ is doubler. |  |  |  |  |  |  |  |  |  |  |
| SOLID-STATE TUBE REPLACEMENTS <br> International Rectifier's solid-state tube replacement line provides retrofit capabilities for mercury-vapor and vacuum rectifier tubes. These offer the following advantages; no filament require- |  |  |  |  |  | ment, no warm-up, long life, and high mechanical shock resistance. <br> For detailed information on pre-engineered assemblies or spe cial designs, please contact your local IR Office. |  |  |  |  |
| IR PART NUMBER | VERL(rep)(V) |  | IFM(AV) - MAX. OC OUTPUT CURRENT $070^{\circ} \mathrm{C}(\mathrm{mA})$ |  | VFM - VOC PER LEG (VOC)$0.5 A D C 巴 25^{\circ} \mathrm{C}$ |  | MAX$\left.\begin{array}{c}\text { DIMENSIONS } \\ (\text { Case } 0-18 A) \\ (I) .)\end{array}\right)$ |  | REPLACES TUBES |  |
|  |  |  | $L$ | 0 |  |  |  |  |
| $\begin{aligned} & \text { 1N570 (ST-1A) } \\ & \text { 1N1150A } \\ & \text { 1N1237 } \\ & \text { 1N1238 } \end{aligned}$ | $\begin{aligned} & 1,500 \\ & 1,600 \\ & 1,600 \\ & 1,600 \end{aligned}$ |  |  |  | $\begin{aligned} & 75 \\ & 750 \\ & 750 \text { (1) } \\ & 750 \text { (1) } \end{aligned}$ |  | $\begin{aligned} & 1.8 \\ & 3.0 \\ & 3.0 \\ & 3.0 \end{aligned}$ |  | Case D-188 <br> 2.65 1.25 <br> 2.65 1.25 <br> 2.65 1.25 |  | MIL-6X4, MIL-12X4, 523, 80, 82, 83 . 83 V . <br> $024,5 \times 4,5 \times 4,6 \mathrm{AX5}, 6 \times 5$ 5AV4, 5AW4, 5AZ4, 5T4, 5U4, 5V4, 5W4, 5 Y3, $5 Z 4$. |  |
| ${ }_{1}^{1} 121239$ (ST-7) | $\begin{aligned} & 2,880 \\ & 4.500 \end{aligned}$ |  | $\begin{aligned} & 500 \text { (1) } \\ & 250 \text { (1) } \end{aligned}$ |  | 4.5 |  | 3.75 2.65 | 5 1.38 <br> 1.25  | 5R4 <br> 6AU4, 6AX4, 6BL4, 6W4, 12AX4, <br> 17AX4, 25W4 <br> $5 \mathrm{AY} 4,5 \mathrm{AW4}, 5 \mathrm{AX} 4,5 \mathrm{~T} 4,5 \mathrm{U} 4,5 \mathrm{~V} 4$, <br> 5W4, 5Y3, 5Z4, 6004 |  |
| 1 12389 | 1,600 |  | 600 |  | 5.3 (2) |  | 1.50 | 1.44 |  |  |
| $\begin{aligned} & \text { 1N2490 } \\ & 1 \mathrm{~N} 2630 \text { (ST-1) } \\ & 1 \mathrm{~N} 2631 \text { (ST-2) } \end{aligned}$ | $\begin{aligned} & 1,600 \\ & 1,500 \\ & 1,600 \end{aligned}$ |  | $\begin{aligned} & 500 \text { (1) } \\ & 850 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 3.0 \\ & 1.8 \\ & 1.8 \end{aligned}$ |  | $\begin{aligned} & 1.50 \\ & 1.81 \\ & 2.65 \end{aligned}$ | 0 0.87 <br> 1 0.88 <br>  1.25 | 6AX <br> $6 \times 4,12 \times 4$ <br> $5 A W 4,5 A X 4,5 A Z 4,5 \mathrm{~T} 4,5 \mathrm{U} 4,5 \mathrm{Y} 3$, 6004 |  |
| 1N2632 | 2,800 |  |  |  | 2.7 |  | 2.65 | 51.25 |  |  |
| 1 12633 (ST-3) | $\begin{aligned} & 1,600 \\ & 1,600 \\ & 1,500 \\ & 1,500 \\ & \hline \end{aligned}$ |  | 600 |  | 1.8 |  | 2.65 | 1.25 |  |  |
| $\begin{aligned} & \text { iN2634 (ST.4) } \\ & \text { iN2635 ST.5) } \\ & \text { iN2636 (ST-6. } \end{aligned}$ |  |  | $\begin{array}{r} 600 \\ 85 \\ 85 \\ \hline \end{array}$ |  | $\begin{aligned} & 3.6 \\ & 3.6 \\ & 3.6 \end{aligned}$ |  | $\begin{aligned} & 2.65 \\ & 1.81 \\ & 2.45 \end{aligned}$ |  |  |  |
|  | 10,4001,25010,00010,0007,500 |  | $\begin{array}{r} 250 \\ 80 \\ 1,250 \\ 1,250 \\ 125 \\ \hline \end{array}$ |  | $\begin{gathered} 11.0 \\ 6.2 \\ 14.0 \\ 14.0 \\ 8.0 \\ \hline 8.1 \\ \hline \end{gathered}$ |  | $\begin{aligned} & 5.05 \\ & 1.10 \\ & 8.05 \\ & 8.05 \\ & 4.20 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 3828,2498,866,866 \mathrm{~A} \\ & 004,6 \times 5 \\ & 8008 \\ & 812 \mathrm{~A} \\ & 816 \end{aligned}$ |  |
| $\begin{aligned} & \text { ST.12(2) } \\ & \text { ST.13 } \\ & \text { ST.14 } \end{aligned}$ | $\begin{array}{r} 40,000 \\ \begin{array}{c} 40,275 \\ 1,600 \end{array} \\ \hline \end{array}$ |  | $\begin{aligned} & 100 \\ & 130 \\ & 600 \end{aligned}$ |  | $\begin{aligned} & 54.0 \\ & 1.8 \\ & 5.3 \text { (2) } \end{aligned}$ |  | $\begin{aligned} & 7.90 \\ & 2.00 \\ & 1.50 \end{aligned}$ | 0 2.40 <br> 0 0.82 <br> 1.44  | 8020 <br> 6BW4, 128W4 <br> 5AV4, 5AW4, 5AX4, 5T4, 5U4,5Y4, 5W4, 5Y3, 5Z4, 6004 |  |
| $\begin{aligned} & \text { ST.15(3) } \\ & \text { ST } 16 \text { (3) } \end{aligned}$ | $\begin{aligned} & 15,000 \\ & 15,000 \end{aligned}$ |  | $\begin{array}{r} 1,750 \\ 1,750 \\ \hline \end{array}$ |  | $\begin{aligned} & 15.0 \\ & 15.0 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 9.65 \\ & 9.65 \end{aligned}$ | 55 3.88 <br> 3.88 | $\begin{aligned} & 673 \\ & 575 \mathrm{~A} \end{aligned}$ |  |

(1) ${ }^{\text {Notes }} 100^{\circ} \mathrm{C}$. (3) Including internal current limiting resistor. (3) Incorporates compensating R-C networks. (1) Surge rating: ST-1 thru ST-14 $=50 \mathrm{~A} ; \mathrm{ST}-15$ \& $\mathrm{ST} \cdot 16=200 \mathrm{~A}$.

Selenium Rectifiers


Listed are the basic specifications for selected IR selenium rectifiers. IR offers an extensive selection of standard and special order selenium devices including: power stacks, cartridges, miniature stacks, diodes, loose cell kits, voltage suppressors (Klip-Sels) and contact protectors.
Your local IR Distributor, or IR Field Office, will gladly supply you with com-
plete specifications, ordering assistance, price, and delivery quotations plete specifications, ordering assistance, price, and delivery quotations.

| OUTPUT |  | VOLTS |  <br> CONNEETING <br> DIAG. <br> FIG. | IR PART | FIG. | DIMENSIONS(Inches) |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DC VOLTS | $\begin{gathered} \text { DG } \\ \text { AMP } \end{gathered}$ |  |  |  |  | A | B | MD | $x$ | Y | STUD |
| 0 | 0.5 | ${ }^{36}$ | 1 | J14C04 | 3 | 1.0 | 1.0 | 1.12 | 38 | 44 | ${ }^{8.32}$ |
|  | 1.5 | 36 | 1 | J14C1 | 3 | 1.5 | 1.5 | 1.12 | . 38 | . 44 | 8-32 |
| to | 5.0 | 36 | 1 | J14C5 | 3 | 3.0 | 3.0 | 1.12 | . 75 | . 63 | 3/8.16 |
|  | 10.0 | 36 | 1 | J14C8 | 3 | 4.0 | 4.0 | 1.88 | . 75 | 1.12 | 3/8.16 |
| 14 | 20.0 | 36 | 1 | J14C17 | 3 | 6.0 | 5.0 | 2.12 | . 75 | 1.25 | 3/8.16 |
| 0 | 0.5 | 36 | 2 | J29804 | 4 | 1.0 | 1.0 | 1.5 | . 38 | . 44 | 8-32 |
|  | 1.5 | 36 | 2 | J2981 | 4 | 1.5 | 1.5 | 1.5 | 38 | . 44 | $8 \cdot 32$ |
| to | 5.0 | 36 | 2 | J2985 | 4 | 3.0 | 3.0 | 2.63 | . 75 | . 63 | 3/8.16 |
|  | 10.0 | 36 | 2 | J2988 | 4 | 4.0 | 4.0 | 2.63 | 75 | 1.12 | 3/8.16 |
| 29 | 20.0 | 36 | 2 | $J 29817$ | 4 | 6.0 | 5.0 | 3.25 | . 75 | 1.25 | 3/8.16 |
| 0 | 0.5 | 72 | 2 | J58804 | 4 | 1.0 | 1.0 | 2.25 | . 38 | . 44 | 8.32 |
|  | 1.5 | 72 | 2 | J5881 | 4 | 1.5 | 1.5 | 2.25 | . 38 | . 44 | $8 \cdot 32$ |
| to | 5.0 | 72 | 2 | J5885 | 4 | 3.0 | 3.0 | 4.19 | . 75 | . 63 | 3/8.16 |
|  | 10.0 | 72 | 2 | J5888 | 4 | 4.0 | 4.0 | 4.19 | . 75 | 1.12 | 3/8.16 |
| 58 | 20.0 | 72 | 2 | 158817 | 4 | 6.0 | 5.0 | 5.63 | . 75 | 1.25 | 3/8.16 |
| 0 | 0.5 | 144 | 2 | J116804 | 4 | 1.0 | 1.0 | 3.81 | . 38 | . 44 | 8.32 |
|  | 1.5 | 144 | 2 | J11681 | 4 | 1.5 | 1.5 | 3.81 | . 38 | . 44 | $8 \cdot 32$ |
| to | 5.0 | 144 | 2 | J11685 | 4 | 3.0 | 3.0 | 7.19 | . 75 | . 63 | 3/8.16 |
|  | 10.0 | 144 | 2 | J11688 | 4 | 4.0 | 4.0 | 7.19 | . 75 | 1.12 | 3/8-16 |
| 116 | 20.0 | 144 | 2 | J116817 | 4 | 6.0 | 5.0 | 10.25 | . 75 | 1.25 | 3/8.16 |
| 0 | 0.5 | 180 | 2 | J135804 | 4 | 1.0 | 1.0 | 4.56 | . 38 | . 44 | 8.32 |
|  | 1.5 | 180 | 2 | J13581 | 4 | 1.5 | 1.5 | 4.56 | . 38 | . 44 | 8.32 |
| to | 5.0 | 180 | 2 | J13585 | 4 | 3.0 | 3.0 | 8.69 | . 75 | . 63 | 3/8-16 |
|  | 10.0 | 180 | 2 | J13588 | 4 | 4.0 | 4.0 | 8.69 | . 75 | 1.12 | 3/8.16 |
| 135 | 20.0 | 180 | 2 | J135817 | 4 | 6.0 | 5.0 | 12.56 | . 75 | 1.25 | 3/8.16 |

## UNIVERSAL QUICK CHARGER STACKS

Maximum AC voltage input is 33 volts line-to-line (see figures 5 \& 6). DC output
is 6 to 12 volts. All ratings are based on forced convection is 6 to 12 volts. All ratings are based on forced convection cooling.


## Selenium Rectifiers

Replacement stacks - Often a standard IR stack with custom brackets, will meet the needs of a custom stack replacement. IR can also design and produce custom stacks to meet your requirements.

MINIATURE STACKS

| MAX. AC INPUT (VOLTS RMS) | MAX. DCOUTPUT (mA) | PEAKREVERSEVOLTAGE VOLTAGE (V) | $\begin{array}{\|c\|} \text { MIN. } \\ \text { SERERIISS } \\ \text { RESTANCE } \\ (\Omega) \end{array}$ | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \end{aligned}$ | fig. | DIMENSIONS(Inches) |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | A SO. | 8 |
| ENTERTAINMENT POWER SUPPLY REPLACEMENT RECTIFIERS Half Wave Rectifiers for $A C$ to $D C$ Conversion |  |  |  |  |  |  |  |
| $\begin{aligned} & 130 \\ & 130 \\ & 130 \\ & 130 \\ & 130 \\ & \hline \end{aligned}$ | $\begin{aligned} & 75 \\ & 750 \\ & 150 \\ & 500 \\ & 550 \\ & 650 \end{aligned}$ | $\begin{aligned} & \begin{array}{l} 380 \\ 380 \\ 380 \\ 380 \\ 380 \\ 380 \end{array} \end{aligned}$ |  | E075L E150L $E 300 L$ $E 500 L$ $E 650 L$ | 8 8 8 8 8 8 | $\begin{aligned} & 0.66 \\ & 1.0 \\ & 1.2 \\ & 1.5 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.75 \\ & 1.05 \\ & 1.25 \\ & 1.25 \\ & 1.25 \end{aligned}$ |
| HALF WAVE RECTIFIERS |  |  |  |  |  |  |  |
| $\begin{aligned} & \hline 36 \\ & 36 \\ & 36 \\ & 36 \\ & 36 \\ & \hline \end{aligned}$ | $\begin{aligned} & 65 \\ & 100 \\ & 150 \\ & 150 \\ & 250 \\ & 500 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 47 \\ & 22 \\ & 15 \\ & 5 \\ & 5 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { O1H } \\ & \text { A1H } \\ & \text { BH } \\ & \text { CH } \\ & \text { CIH } \\ & \hline \end{aligned}$ | 8 8 8 8 8 8 | $\begin{aligned} & 0.67 \\ & 1.0 \\ & 1.2 \\ & 1.5 \\ & 2.0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.44 \\ & 0.44 \\ & 0.44 \\ & 0.44 \\ & 0.44 \end{aligned}$ |
| FULL WAVE RECTIFIER BRIDGES |  |  |  |  |  |  |  |
| $\begin{gathered} 36 \\ \hline 130 \\ 260 \\ 260 \\ 36 \\ 130 \\ 36 \\ 36 \\ 36 \\ \hline \end{gathered}$ | $\begin{aligned} & 100 \\ & 100 \\ & 100 \\ & 180 \\ & 1800 \\ & 1300 \\ & 600 \\ & \hline 600 \end{aligned}$ |  |  | Q18 048 088 A18 A4B A1B C18 M18 | $9 A$ $9 A$ $9 A$ $9 A$ $9 A$ $9 A$ $9 A$ $9 A$ 9 | $\begin{aligned} & 0.67 \\ & 0.67 \\ & 0.67 \\ & 1.0 \\ & 1.0 \\ & 1.2 \\ & 1.5 \\ & 2.0 \end{aligned}$ | $\begin{aligned} & 0.81 \\ & 1.25 \\ & 1.75 \\ & 0.81 \\ & 1.25 \\ & 0.81 \\ & 0.81 \\ & 0.81 \\ & \hline \end{aligned}$ |
| MAGNETIC-AMPLIFIER BRIDGE, SINGLE PHASE |  |  |  |  |  |  |  |
| $\begin{aligned} & 130 \\ & 260 \end{aligned}$ | $\begin{aligned} & 100 \\ & 100 \end{aligned}$ | I- | I | 04M 08 M | ${ }_{98}^{98}$ | $\begin{aligned} & 0.67 \\ & 0.67 \end{aligned}$ | $\begin{aligned} & 1.25 \\ & 1.75 \end{aligned}$ |
| VOLTAGE DOUBLER SINGLE PHASE (1) |  |  |  |  |  |  |  |
| 260 | 100 | - | - | 080 | ${ }^{3}$ | 0.67 | 1.25 |

CARTRIDGE RECTIFIERS - A complete line of selenium cartridge rectifiers is available from IR with peak reverse voltages ranging from 63.5 to 30,000 volts. Four cell sizes ( $1 / 8$ to $1 / 2$ inch nominal diameter) and lengths from 1 inch to 7-7/8 inches.

| APPLICATION | OUTPUT <br> VOLTAGE (V) | DC OUTPUT CURRENT (mA) | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \\ & \hline \end{aligned}$ | L - LENGTH (SEE FIGURE 10) |
| :---: | :---: | :---: | :---: | :---: |
| TV Boost TV Focus | $\begin{aligned} & 8500 \\ & 6500 \end{aligned}$ | $\begin{aligned} & 2 \\ & 2 \end{aligned}$ | US17HFP US144HFP | $\begin{aligned} & 0.690 \text { in. max. } \\ & 2.5 \text { in. max. } \end{aligned}$ |


| All Dimensions in Inches. <br> Fig. 8 - Half Wave Stacks |
| :---: |
| Fig. 9A - Full Wave Stacks |
| Fig. 9B - Magnetic Amplifier Stacks |
| $\underset{\text { Fig. }}{9 \mathrm{CO}}-\mathrm{Doubler}$ |
| Fig. 10 - Cartridge Rectifiers |


| SOLID STATE DEVICE |  | UPPRESSOR |  | FOR INDIVIDUAL RECTIFIER RATED THRU 3 AMP |  | FOR INDIVIDUAL RECTIFIER RATED THRU 16 AMP |  | FOR INDIVIDUAL RECTIFIER RATED THRU 60 AMP |  | FOR INOIVIOUAL RECTIFIER RATED THRU 250 AMP |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MAXOPERATING voltage ( $V_{\text {RMS }}$ | MAX.CLAMPING VOLTAGE @ PEAK CURRENT$\left(V_{\mathrm{pk}}\right)$ | $\begin{gathered} \text { PEAK CURRENT } \\ 0.25 \mathrm{~A} \\ \hline \end{gathered}$ |  | $\begin{aligned} & \text { PEAK CURRENT } \\ & \hline 1.0 \mathrm{~A} \end{aligned}$ |  | $\begin{aligned} & \text { PEAK CURRENT } \\ & 3.0 \mathrm{~A} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \text { PEAK CURRENT } \\ & 15 \mathrm{~A} \\ & \hline \end{aligned}$ |  |
| VOLTAGE RATING(VRMM) | TRANSIENT VOLTAGE RATING (VRSM) |  |  | $\begin{gathered} \text { Fig. } 11 \\ \left(A=.57^{\prime \prime} \text { max. dia. }\right) \end{gathered}$ |  | $\left(A=\begin{array}{c} \text { Fig. } \\ (11 \\ \hline 0^{\circ} \\ \text { max, die. }) \end{array}\right.$ |  | $\begin{gathered} \text { Fig. } 12 \\ \left(A=1^{\prime \prime} \mathrm{Sq} .\right) \end{gathered}$ |  | $\begin{gathered} \text { Fig. } 12 \\ \left(\mathrm{~A}=2^{\prime \prime} \mathrm{Sq} . \text { Cells }\right) \end{gathered}$ |  |
|  |  |  |  | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \end{aligned}$ | $\begin{aligned} & \mathrm{I} \operatorname{Dim} . \\ & (\text { max. }) \end{aligned}$ | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \end{aligned}$ | LDim. | $\begin{aligned} & \text { IR PART } \end{aligned}$ | LDim. | IR PART NO. | $\underset{(\max ) \pm .06^{\prime}}{\mathrm{L} \text { Dim. }}$ |
| 100 | 150 | 52 | 140 | KY20PF | 0.63" | KZ20PF | 0.63"' | KSA2DAF | 1.50" | KSL2DAF |  |
| 150 | 250 | 78 | 210 | KY2DPF | ${ }^{0.63 " \prime}$ | KZ3DPF | $0.63^{\prime \prime}$ | KSA30AF | ${ }^{1.62^{\prime \prime}}$ | KSL3DAF |  |
| 200 | 300 | 104 | 280 | KY4DPF | 0.63"' | K24DPF | 0.63"' | KSAADAF | 1.75"' | KSL4DAF |  |
| 250 | 350 | 130 | 350 | KY5DPF | ${ }^{0.63 "}$ | K25DPF | $0.63^{\prime \prime}$ | KSASDAF | 1.87" | KSL5DAF | 2.25". |
| 300 | 425 | 156 | 420 | KY6DPF | 0.88" | KZ6DPF | 0.88" | KSA6DBF | $2.00^{\circ}$ | KSL60日F |  |
| ${ }^{400}$ | 525 | 182 | 490 | KY70PF | 0.88" | K270PF | ${ }^{0.888^{\prime \prime}}$ | KSA708F | $212{ }^{2 \prime \prime}$ | KSLIDEBF | ${ }^{2.533^{\prime \prime}}$ |
| 500 | 650 | 234 | ${ }^{630}$ | KY9DPF | 0.88"' | Kz90PF | ${ }^{0.888^{\prime \prime}}$ | KSASOBF | $234{ }^{2 \prime \prime}$ | KSL9DBF | 2.81" |
| 600 | 800 | 260 | 700 | KY10DPF | 0.88" | KZ100PF | 0.88" | KSAIODAF | 2.46" | KSL 1008 F | 2.96" |
| 700 | 925 | 312 | 840 | KY12DPF | 0.88" | K2120PF | 0.88" | KSA120BF | 2.71" | KSL1208F | 3.28" |
| 800 | 1050 | 364 | 980 | KY140PF | $1.63^{*}$ | KZ140PF | ${ }^{1.63 *}$ | KSA140PF | $2.93{ }^{\prime \prime}$ | KSL1408F | $3.56^{\prime \prime}$ |
| 900 | 1175 | 416 | 1120 | KY16DPF | 1.63" | KZ160PF | 1.63" | KSAI60BF | $3.18{ }^{\text {" }}$ | KSL1608F | ${ }^{3.87{ }^{\prime \prime}}$ |
| 1000 | 1300 | ${ }^{468}$ | 1260 | KY18DPF | 1.63"' | KZ18DPF | 1.63"' | KSA180BF | $3.43{ }^{\prime \prime}$ | KSL1808F | 4.15"', |
| 1200 | 1600 | 520 | 1400 | KY200PF | 1.63 | KZ200PF | $1.63^{\prime \prime}$ | KSAZODBF | 3.65" | KSL2008F | $4.46{ }^{\prime \prime}$ |

Not standardized. Check device specifications.

## Selenium Rectifiers

| Fig. 11 |  | Fig. 12 |  |
| :---: | :---: | :---: | :---: |

KLIP-SELS (DC Types)

| SOLID STATE DEVIICE |  | ESSOR |  | FOR INDIVIDUAL RECTIFIER RATED RECTIFIER RATE THRU 3 AMP <br> peak current 0.25A |  |  |  | FOR INDIVIDUALRETTIIIE RATEDTHR GO AMPPEAK CURENT3.0A |  | FOR INDIVIDUAL <br> THRU 250 AMP <br> PEAK CURAENT <br> 15A |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |  |
|  | TRANSIEN |  |  | $\left(A=57^{\text {Fig. . } \mathrm{Hax}} \mathbf{\text { maia. }}\right)$ |  | $\left(A=70^{\text {Fig max. }} 11\right.$ |  |  |  |  |  |
| $\begin{aligned} & \text { ODLTAGE } \\ & \text { ARTAGE } \\ & \text { INRMM } \end{aligned}$ |  |  |  | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \end{aligned}$ | $\begin{aligned} & \operatorname{Lomim}_{(\text {max }} \\ & (\text { max } \end{aligned}$ | $\begin{aligned} & \text { IR PART } \\ & \hline \text { NO. } \end{aligned}$ | $\begin{array}{\|l\|l\|} \hline \operatorname{Dimim}_{(\text {max },)} \\ \hline \end{array}$ | $\begin{aligned} & \text { IR PART } \\ & \text { NO. } \end{aligned}$ | $\begin{aligned} & \text { (0imi } \\ & (\text { maxx }) \end{aligned}$ | $\begin{gathered} \text { IRPART } \\ \text { NO. } \end{gathered}$ |  |
| $\begin{aligned} & 100 \\ & \hline 100 \\ & \hline 500 \\ & 2000 \\ & \hline 500 \end{aligned}$ | $\begin{aligned} & 150 \\ & \begin{array}{l} 150 \\ 500 \\ 350 \\ 350 \end{array} \\ & \hline 200 \end{aligned}$ | $\begin{aligned} & 44 \\ & 86 \\ & 86 \\ & 80 \\ & 132 \\ & \hline 132 \end{aligned}$ | $\begin{aligned} & 198 \\ & \begin{array}{l} 198 \\ \text { 230 } \\ 3306 \\ 3966 \end{array} \end{aligned}$ |  | $\begin{aligned} & 0.0^{0.3 \%} \\ & 0.3^{\circ} \\ & 0.3^{\circ} \\ & 0.63^{\prime \prime} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0.63^{2} \\ & 0.63 \\ & 0.63^{\prime \prime} \\ & 0.63 \end{aligned}$ |  |  |  |  |
| $\begin{aligned} & 400 \\ & 500 \\ & 500 \\ & 500 \\ & 600 \\ & \hline 000 \\ & \hline 00 \end{aligned}$ |  | $\begin{aligned} & \begin{array}{l} 154 \\ 198 \\ \text { P20 } \\ 284 \\ 2866 \end{array} \end{aligned}$ |  |  | $\begin{aligned} & 0.63^{\prime \prime} \\ & 0.03^{\prime \prime} \\ & 0.03^{\circ} \\ & 0.88^{\prime \prime} \\ & 0.89^{\prime \prime} \end{aligned}$ |  | $\begin{aligned} & 0.63^{\prime \prime \prime} \\ & 0.63^{\prime \prime} \\ & 0.3^{0.88^{\prime}} \\ & 0.88^{\prime \prime} \end{aligned}$ |  | $\begin{aligned} & 1.59^{\prime \prime \prime} \\ & 1.88^{\prime \prime} \\ & 1.1877^{\prime \prime} \\ & 1.93^{\prime \prime} \end{aligned}$ |  | $\begin{aligned} & 1.87^{\prime \prime \prime} \\ & 2.00^{209} \\ & 2.25{ }^{2.25} \\ & 2.31^{\prime \prime} \end{aligned}$ |
| $\begin{gathered} 800 \\ \hline 900 \\ 1000 \\ 1200 \end{gathered}$ | $\begin{aligned} & 1050 \\ & \hline 1050 \\ & 11300 \\ & 15600 \end{aligned}$ | $\begin{aligned} & 330 \\ & 334 \\ & 3184 \\ & 484 \\ & 484 \end{aligned}$ | $\begin{aligned} & 990 \\ & \begin{array}{c} 9122 \\ 1254 \\ 1455 \end{array} \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 0.0 .8^{\circ "} \\ & 0.88^{\circ "} \\ & 0.88^{\prime \prime \prime} \\ & 0.8)^{\prime} \end{aligned}$ |  | $\begin{aligned} & 0.88^{0 \prime \prime} \\ & 0.888^{\prime \prime \prime} \\ & 0.88 \end{aligned}$ | KSAP1508F KAPPIDBF KSAPITOBE <br> KSAP220BF | $\begin{aligned} & 2.1 .0^{\prime \prime \prime} \\ & 2.8^{2.8^{\prime}} \\ & 2.46^{\prime \prime} \end{aligned}$ |  <br> KSLP220BF | $\begin{aligned} & 2.46^{\prime \prime \prime \prime \prime \prime} \\ & 2.2_{1}^{\prime \prime} \\ & 3.00^{\prime \prime} \end{aligned}$ |



|  | max <br> coIl <br> cur <br> Une <br> ReNT <br> (AMP) <br> (AM | $\begin{aligned} & \text { In PaRT } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \text { dimension } \\ & \text { FIG. } 15 \end{aligned}$ |  | WORAINGVOLTSIVOC) |  |  | $\begin{aligned} & \text { ir Paft } \\ & \text { No. } \end{aligned}$ | $\begin{aligned} & \text { DIMENSION } \\ & \text { FIG. } 15 \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | AIM | 8 max) | MIN. | max. |  |  | A(MAX) |  |
| $\begin{aligned} & 26 \\ & 78 \\ & 78 \\ & 104 \\ & 130 \\ & 156 \\ & 156 \end{aligned}$ | $\begin{aligned} & 20 \\ & .20 \\ & 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ |  | $\begin{aligned} & 380 \\ & \begin{array}{l} 380 \\ 380 \\ 380 \\ 380 \\ 380 \\ 3880 \end{array} \end{aligned}$ | $\begin{aligned} & 6200 \\ & .820 \\ & .820 \\ & .620 \\ & .600 \\ & 990 \end{aligned}$ | 15 23 25 67 89 811 133 | 22 <br> 44 <br> 66 <br> 88 <br> 110 <br> 132 <br> 154 | $\begin{aligned} & 25 \\ & 25 \\ & 25 \\ & 25 \\ & 25 \\ & 25 \\ & 25 \\ & \hline 25 \\ & \hline \end{aligned}$ |  | 338 <br> 330 <br> 330 <br> 330 <br> 330 <br> 330 <br> 380 | 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 |
| $\begin{aligned} & 26 \\ & 728 \\ & 78 \\ & 104 \\ & 130 \\ & 156 \end{aligned}$ | $\begin{aligned} & .40 \\ & .40 \\ & .40 \\ & .40 \\ & .40 \\ & 40 \end{aligned}$ |  | $\begin{aligned} & 500 \\ & 500 \\ & 500 \\ & 500 \\ & 500 \\ & 500 \\ & 500 \end{aligned}$ |  | 15 23 25 45 89 89 133 13 | 22 <br> 446 <br> 866 <br> 888 <br> 110 <br> 132 <br> 154 | .60 <br> 60 <br> 60 <br> 60 <br> 60 <br> 60 <br> 60 <br> 60 <br> 60 <br> .60 <br>  |  | 500 500 500 500 500 500 500 | .620 <br> 620 <br> .620 <br> .620 <br> 620 <br> 620 <br> 620 |
| $\begin{aligned} & 26 \\ & 78 \\ & 78 \\ & 104 \\ & 130 \\ & 156 \end{aligned}$ | $\begin{aligned} & .60 \\ & .60 \\ & .60 \\ & .60 \\ & .80 \\ & .80 \\ & .60 \end{aligned}$ |  |  |  | $\begin{aligned} & 15 \\ & 15 \\ & 23 \\ & 45 \\ & 69 \\ & 89 \\ & 131 \\ & \hline 133 \\ & \hline \end{aligned}$ | 22 <br> 44 <br> 46 <br> 88 <br> 818 <br> 132 <br> 154 | 90 90 90 90 90 90 90 |  | 640 <br> .640 <br> .640 <br> .640 <br> .640 <br> .640 <br> .640 | 754 <br> 7.74 <br> 7.54 <br> 7.754 <br> 7.754 <br> 754 <br> 754 |
| $\begin{gathered} 26 \\ 78 \\ 78 \\ 104 \\ 130 \\ 156 \end{gathered}$ | 90 90 90 90 90 90 90 |  | $\begin{array}{\|l\|l} 1.060 \\ 1.060 \\ 1.060 \\ 1.060 \\ 1.060 \\ 1.060 \\ 1.060 \end{array}$ | $\begin{aligned} & .620 \\ & .620 \\ & .620 \\ & .620 \\ & .620 \\ & .990 \end{aligned}$ | 15 25 25 45 89 89 133 13 | 22 <br> 44 <br> 66 <br> 98 <br> 9810 <br> 132 <br> 154 | $\begin{aligned} & 1.4 \\ & 1.4 \\ & 1.4 \\ & 1.4 \\ & 1.4 \\ & 1.4 \\ & \hline \end{aligned}$ |  | 1.060 1.060 1.060 1.060 1.060 1.060 1.0650 1.050 1 | 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> .620 |
| $\begin{aligned} & 26 \\ & 78 \\ & 78 \\ & 104 \\ & 110 \\ & 156 \end{aligned}$ | $\begin{aligned} & 1.2 \\ & 1.2 \\ & 1.2 \\ & 1.2 \\ & 1.2 \\ & 1.2 \end{aligned}$ |  | 1.380 <br> 1.380 <br> 1.380 <br> 1380 <br> 1.380 <br> 1.380 | .620 6.820 620 620 690 690 | 15 23 45 67 89 111 133 | 22 <br> 46 <br> 68 <br> 88 <br> 110 <br> 1152 <br> 154 | 2.0 20 20 20 20 20 20 20 | SIWP STWP S3W2P SsW2P SSW2P SSWWP STW2P | $\begin{array}{\|l\|} \hline 1.000 \\ \hline 1.380 \\ 1.380 \\ 1.380 \\ 1.380 \\ 1.380 \\ 1.380 \\ 1.380 \\ \hline \end{array}$ | 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 <br> 620 |



## Heat Exchangers and Hardware

International Rectifier offers a wide variety of heat These were designed by power semiconductor spe cialists to maximize semiconductor operation and facilitate assembly. Specific units offer unique channels for the mounting of accessories and terminals. $R$ also offers an extensive selection of liquidcooled Heat Exchangers for both stud-mounted and Hockey-Puk semiconductors. Contact your El Segundo Offices for further information. IR also offers two types of yokes for mounting Hockey-Puk type devices. These are used in conunction with Heat Exchangers HE72 and HE75, t should be noted that there is a definite cost savings, without sacrificing thermal dissipation pro perties, in using an irridite finish.


| $\begin{aligned} & \mathrm{K}-0.200 \\ & \mathrm{~L}=0.270 \\ & \mathrm{H}=0.497 \\ & \mathrm{M}-0.765 \end{aligned}$ | $\begin{gathered} \mathrm{d}^{\prime} \\ 0.50 \\ 0.750 \\ 1 . \overline{812} \end{gathered}$ | d $\mathrm{N}-0.330$ $\mathrm{P}=0.390$ $\mathrm{Q}-0.520$ $\mathrm{R}-1.030$ $\mathrm{~W}-0.765$ | d 1.00 1.000 1.125 1.125 1.812 2.250 |
| :---: | :---: | :---: | :---: |
| $\mathrm{Y}-2$ holes for C3 yoke mounting. <br> I - HE75, 4-hole pattern. <br> $\mathrm{Z}-2$ holes for C 4 yoke mounting. |  |  |  |
|  |  | $\begin{aligned} & U-1 / 2 \cdot 20 \\ & V-5 / 6.24 \\ & X-3 / 4.16 \end{aligned}$ |  |
| hole requirements |  |  |  |
| D0.4 JEDEC ${ }^{\text {K }}$ |  |  |  |
|  |  |  |  |
| 00.5 | T0.64 | 40 | s |
| ${ }^{00.9} \mathrm{M}$ | ${ }_{\text {T0, }}$ | a M |  |
| (00.30 |  | a ${ }^{4}$ |  |
| T0.48 L | $\begin{aligned} & \text { To. } 118 \\ & \hline 0.203 \mathrm{AA} \end{aligned}$ | 告 ${ }^{\text {H }}$ | 0 |



HEAT EXCHANGER SPECIFICATIONS

| FIGURE | IR | THERMAL RESISTANCE R gSA ${ }^{\circ} \mathrm{C} / \mathrm{W}$ ) |  | LENGTH(INCHES) |
| :---: | :---: | :---: | :---: | :---: |
|  |  | NATURAL CONVECTION | FONVECTION (100011m) |  |
| 0 | HE32-1.5A3 | 3.3 | 1.1 | 1.5 |
| 0 | HE32-3A3 | 2.0 | 0.65 | 3.0 |
| E | HE40-75A3 | 3.4 | 1.2 | 0.75 |
| E | HE40-1.5A3 | 2.7 | 0.7 | 1.5 |
| E | HE40-3A3 | 1.85 | 0.6 | 3.0 |
| F | HE50-1.5A3 | 1.85 | 0.65 | 1.5 |
| F | HE50-3A3 | 1.5 | 0.4 | 3.0 |
| 6 | HE52.3A3 | 0.9 | 0.3 | 3.0 |
| H | HE53-3A3 | 0.7 | 0.19 | 3.0 |
| H | HE53-5.5A3 | 0.58 | 0.16 | 5.5 |
| J | HE63.6A3 | 0.27 | 0.11 | 6.0 |
| J | HE63-9A3 | 0.25 | 0.105 | 9.0 |
| K | HE72.5A3 | $0.23{ }^{*}$ | $0.10^{*}$ | 5.0 |
| K | HE72.8A3 | $0.18{ }^{*}$ | $0.08{ }^{*}$ | 8.0 |
| L | HE75-4A3 | $0.45{ }^{\circ}$ | $0.09^{*}$ | 4.0 |
| L | HE75-6A3 | $0.35^{*}$ | $0.08{ }^{+}$ | 6.0 |
| M | HE80-4A3 | 0.66 | 0.23 | 4.0 |
| M | HE80-5A3 | 0.6 | 0.21 | 5.0 |
| M | HE80-6A3 | 0.55 | 0.19 | 6.0 |
| N | HE81-5A3 | 0.8 | 0.14 | 5.0 |
| P | HE85-2A3 | 2.0 | 0.48 | 2.0 |
| P | HE85-4A3 | 1.5 | 0.35 | 4.0 |

Heat Exchangers and Hardware


MOUNTING HARDWARE FOR SEMICONDUCTOR DEVICES

| Device Series | Stud | Description | Part No. | Device Series | $\begin{aligned} & \text { Stud } \\ & \text { Size } \\ & \hline \end{aligned}$ | Description | Part No. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ZENERS: <br> 3.5 to 10 watt <br> RECTIFIERS: <br> 3 to 16 amp <br> SCRs: <br> 3 to 4.7 amp <br> CASE STYLES: <br> DO-4, TO-64 | 10-32 | MOUNTING HARDWARE$\left.\begin{array}{\|ll} \begin{array}{l} \text { (1) } \end{array} & \text { Nut } \\ \text { (1) } & \text { Flatwasher } \\ \text { (1) } & \text { Lockwasher } \end{array}\right\} \text { bagged }$ | 40.8020 | (Continued) | 1/4-28 | (100) Mica Washers - bagged <br> (50) Glass Mel. Bush. - bagged <br> (50) Terminals - bagged | 40-1309 |
|  |  |  |  |  |  | MOUNTING PLUS INSULATING HARDWARE COMBINED: |  |
|  |  | $\begin{aligned} & \text { (50) Nut - bagged } \\ & \text { (50) Flatwashers - bagged } \\ & \text { (50) Lockwashers - bagged } \end{aligned}$ | 40.1306 |  |  | Single Set - bagged Set of 50 - bagged | $\begin{array}{\|l} 40-8031 \\ 40-1314 \\ \hline \end{array}$ |
|  |  | INSULATING HARDWARE: <br> $\begin{array}{ll}\text { (2) } & \text { Mica Washers } \\ \text { (1) } \\ \text { Teflon Spacer } \\ \text { (1) } & \text { Terminal }\end{array}$ bagged | 40-8022 | RECTIFIERS: 1N3288 Series, $101 \mathrm{KL}, 150 \mathrm{~K}$ SCRs: 36RCS, 71RCS CASE STYLES:A-15, A-16, DO-8 | 3/8-24 | MOUNTING HARDWARE: $\left.\begin{array}{ll} \text { (1) } & \text { Nut } \\ \text { (1) } & \text { Flatwasher } \\ \text { (i) } & \text { Lockwasher } \end{array}\right\} \text { bogged }$ | 40-8040 |
|  |  | (100) Mica Washers - bagged <br> (50) Teflon Spacers - bagged <br> (50) Terminals - bagged | 40-1307 |  |  | (10) Nuts - bagged (10) Flatwashers - bagged (10) Lockwashers - bagged | 40-1313 |
|  |  | MOUNTING PLUS INSULATING HARDWARE COMBINED: | 40-8021 | RECTIFIERS: <br> 150L, 1N3085 Series SCRs: <br> 36/37, 71/72, 81/82 <br> Series <br> CASE STYLES: <br> A-13, A-14, DO-30 <br> TO-49, T0-83 TO-94 | 1/2-20 | MOUNTING HARBWARE: <br> $\left.\begin{array}{ll}\text { (1) } & \text { Nut } \\ \text { (i) } & \text { Flatwashers } \\ \text { (i) } & \text { Lockwasher }\end{array}\right\}$ bagged | $40-8050$ |
| ZENERS: <br> 50 watt | 1/4-28 | MOUNTING HARDWARE: <br> $\left.\begin{array}{ll}\begin{array}{l}\text { (1) }\end{array} & \begin{array}{l}\text { Nut } \\ \text { (1) } \\ \text { (1) } \\ \text { Flatwasher } \\ \text { Lockwasher }\end{array}\end{array}\right\}$ bagged | 40-8030 |  |  | (10) Nuts - bagged <br> (10) Flatwashers - bagged <br> (10) Lockwashers - bagged | 40-1311 |
| RECTIFIERS: <br> 40 to 70 amps |  |  |  | RECTIFIERS: $251 \mathrm{UL}, 300 \mathrm{U}$ 301U, 501 V SCRs: 101, 151, 250, 300350 Series CASE STY B-8, B-22 LES: TO-93, TO-118 | 3/4-16 | MOUNTING HARDWARE: |  |
| SCRs: <br> 10 to 22 amp . <br> 40 RCS |  | (50) Nuts - bagged <br> (50) Flatwashers - bagged <br> (50) Lockwashers - bagged | 40-1308 |  |  | $\left.\begin{array}{ll} \text { (1) } & \text { Nut } \\ \text { (1) } & \text { Flatwasher } \\ \text { (1) } & \text { Lockwasherer } \end{array}\right\} \text { begged }$ | 40-8060 |
| CASE STYLES: <br> A-8, C-8, DO. 5 <br> TO-48, TO-65 |  | INSULATING HARDWARE: (2) Mica Washers (1) Glask Mel Bush. (1) Terminal i | 40-8034 |  |  | (10) Nuts - bagged (10) Flitwasher -bagged (10) Lockwashers - bagged | 40-1310 |

## Opto-Electronic Devices



CARD/TAPE SENSOR PHOTOCELL ARRAYS
Designed for perforated tape and punched card data reading systems, analog-to digital encoders, and shaft positioning systems, these readout photocell arrays provide high speed response to light passing through punched cards or tape. Complete, high reliability readout assemblies using these arrays are also available inch of active area with load impedance of 1000 ohms, and 500 FC illumination.

IR PART NUMBER CODE

| OEVICE TYPE |  | $\begin{gathered} \text { NUMBER } \\ \text { OEGENTS } \\ \text { SEME } \\ (1-10) \\ \hline \end{gathered}$ | CENTER-TO-CENTER SPACING (In.) |  |  |  | $\begin{aligned} & \text { ADD } \\ & \text { EITHER } \\ & \text { OR BOTH } \end{aligned}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SAR | SPR |  | 08 |  | $0.100^{\prime \prime}$ |  |  |  |
| N-ON-P | P-ON-N |  | $0.087^{\prime \prime}$ |  |  |  |  |  |
| ELECTRICAL CHARACTERISTICS |  |  | TYPICAL | minimum | TYPICAL | MINIMUM |  |  |
| Short Circuin Current ( A ) |  |  | 250 | 225 | 315 | 250 |  | $\begin{array}{\|c\|c\|} \hline \text { PR } \\ \substack{\text { Piptait } \\ \text { Leads) }} \end{array}$ |
| Load Current ( $\mu \mathrm{A}$ ) |  |  | 180 | 145 | 270 | 200 |  |  |
| Load Voltage (mV) |  |  | 180 | 145 | 270 | 200 |  |  |
| Open Circuit Voltage (mV) |  |  | 325 | - | 325 | - |  |  |
| Response Time (usec) |  |  | 2.0 | 2.0 | 2.0 | 2.0 |  |  |
| Related at 500 FC , color temp. $2800{ }^{\circ} \mathrm{K}$ tungsten, $22^{\circ} \mathrm{C}$ ambient (0utline L-1) |  |  |  |  |  |  |  |  |

## SILICON LIGHT SENSOR

International Rectifier silicon photocells are employed in photometer, switching position detection, tape and disc EOT-BOT sensing, solar energy conversion, and other numerous applications.
Silicon photosensors with special geometries, spectral response, and switching character istics, are available on a custom basis, and are widely used in the optical
encoder, character recognition, and optical instrumentation fields.
IR PART NUMBER CODE


ELENIUM LIGHT SENSORS
Selenium Cells offer color response similar to human vision and are especially useful in ultraviolet range applications. Due to a slightly higher internal
impedance, selenium has a slower frequency response than silicon.
RECTANGULAR TYPES (OUTLINE L3) ROUND TYPES (OUTLINE L4)

| $\begin{aligned} & \text { IR } \\ & \text { PART } \\ & \text { NO. } \\ & \hline \end{aligned}$ | OUTPUT CURRENT 100 fc 100 OHMS (MICROAMPERES) | $\begin{aligned} & \text { Size (In). } \\ & \text { L\& W } \end{aligned}$ | $\begin{array}{\|l\|} \hline \text { IR } \\ \text { PART } \\ \text { NO. } \end{array}$ | OUTPUT CURRENT $100 f \mathrm{c} 100$ OHMS (MICROAMPERES) | DIAMETER ( (1n.) |
| :---: | :---: | :---: | :---: | :---: | :---: |
| B2 | 77 | $0.72 \times 0.44$ | A2 | 12 | 0.25 |
| 84 | 120 | $0.88 \times 0.54$ | A3 | 20 | 0.38 |
| ${ }^{85}$ | 250 | $1.44 \times 0.64$ | A5 | 250 | 1.33 |
| 810 | 380 | $1.69 \times 0.88$ | A10 | 600 | 1.75 |
| 817 | 710 | $6.00 \times 0.50$ | A15 | 770 | 2.00 |

MOUNTED CELLS

| $\begin{gathered} \text { IR } \\ \text { PART } \\ \text { PAR. } \\ \hline \end{gathered}$ | TYPICAL OUTPUICURRENT 100 OHMS 100 c c 100 OHMS (MICROAMPS) (MICROAMPS) | OUTLINE |
| :---: | :---: | :---: |
| B10.M | 320 | L.5 |
| A5-m | 220 | 1.6 |
| A15-M | 700 | L-6 |

moisture resistant cellis

Far pigtail leads, add "PL" at end of code.

Semiconductor Fuses

International Rectifier's fast-acting semiconductor protective fuses employ a high-grade alumina ceramic body to prevent charring and arcing under operating conditions. Allwelded construction rather than soldering is used to prevent internal fatigue from changing fuse parameters. These quality fast-acting fuses are competitively priced.
A complete range of European-style semiconductor fuses is also available.

| Max. VRMs (V) | 130 | 250 | 500 | 600 | 600 | 700 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Max. Arc Voltage (V) | 220 | 410 | 850 | 1,050 | 1,050 | 1,200 |
| Nominal RMSCurrent (A) |  |  |  |  |  |  |
| $\begin{array}{r} 5 \\ 10 \\ 15 \\ 20 \\ 25 \\ \hline \end{array}$ | SF13X5SF <br> SF $13 \times 13 \times 15$ SF $13 \times 20$SF $13 \times 25$ | $\begin{aligned} & \text { SF25x5 } \\ & \text { SF25 } 2 \times 10 \\ & \text { SF25x15 } \\ & \text { SF25 } 2520 \\ & \text { SF25 } 2525 \end{aligned}$ |  |  | SF60X5 <br> SF60010 <br> SF60×20 | SF70P10 SF70P15 SF70P25 |
| $\begin{aligned} & 30 \\ & 35 \\ & 40 \\ & 45 \\ & 50 \end{aligned}$ |  SF $13 \times 40$ SF $13 \times 50$ | SF25X30 <br> SF25×40 <br> SF $25 \times 50$ | SF50P35 SF50P40 SF50P50 | SF60C30 SF60C40 SF60C45 SF60C50 | SF60X30 SF60×35 SF60X40 <br> SF60×50 | $\begin{aligned} & \text { SF70P30 } \\ & \text { SF70P5 } \\ & \text { SF7OP40 } \\ & \text { SF70P50 } \end{aligned}$ |
| $\begin{gathered} 60 \\ 70 \\ 80 \\ 90 \\ 100 \\ \hline \end{gathered}$ | SF 13×60 SF $13 \times 80$ SF13×100 | SF25×60 SF25×80 SF25×100 | SF50P60 SF50P80 SF50P90 SF50P10 F50P1 | SF60C60 SF60C70 SF60c90 SF60C10 | SF60X60 SF60x70 SF60x90 SF60X10 | SF70P60 SF70P80 SF70P100 |
| $\begin{aligned} & 125 \\ & 150 \\ & 175 \\ & 200 \\ & 2225 \end{aligned}$ | SF $13 \times 125$ $\mathbf{S F} 13 \times 150$ <br> SF $13 \times 200$ |  | $\begin{aligned} & \text { SF50P125 } \\ & \text { SF50P50 } \\ & \text { SFF5P175 } \\ & \text { SF50P275 } \end{aligned}$ |  | SF60X125 SF60X150 SF60 SF60X200 | $\begin{aligned} & \text { SF70P } 125 \\ & \text { SFFTOP50 } \\ & \text { SFTOP175 } \\ & \text { SFFOPR200 } \end{aligned}$ |
| $\begin{aligned} & 250 \\ & 300 \\ & 350 \\ & 400 \\ & 450 \\ & \hline \end{aligned}$ | SF $13 \times 250$ SF $13 \times 300$ SF $13 \times 350$ SF $13 \times 400$ $\qquad$ |  | SF50P250 <br> SF50P350 <br> SF50P45 | SF6GC250 SF60C300 SF60C350 SF60ca0 SF60C450 | SF60×250 SF60X350 SF600400 SF60X450 | SF70P250 SF70P300 <br> SF70P400 |
| $\begin{aligned} & 500 \\ & 550 \\ & 500 \\ & 700 \\ & 800 \\ & \hline \end{aligned}$ | SF $13 \times 500$ SF $13 \times 600$ SF13×800 | SF25X500 <br> SF25×600 | SF50P5000 S550P550 SF50P600 S50P700 SF50P800 |  | SF60x500 <br> SF60×600 <br> - |  |



SEMICONDUCTOR FUSE DIMENSIONS All Dimensions in Inches

| PART NUMBER | FIG. | A | 8 | c | 0 | E | F | G | H |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SF13X5 to 30 SF13X35 to 60 SF13X70 to 400 SF13X500 to 800 | $2$ | $\begin{aligned} & 1.500 \\ & 2.00 \\ & 2.656 \\ & 3.500 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.406 \\ & 0.812 \\ & 2.062 \\ & 2.438 \end{aligned}$ | $\begin{aligned} & 0.375 \\ & 0.594 \\ & 1.156 \\ & 1.250 \end{aligned}$ | $\begin{gathered} - \\ 1.000 \\ 1.500 \\ \hline \end{gathered}$ | $\begin{gathered} \overline{-} \\ 0.125 \\ 0.250 \end{gathered}$ | $\begin{aligned} & 0.750 \\ & 1.000 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0 . \overline{0.212} \\ & 0.406 \end{aligned}$ | $\begin{aligned} & 0 . \overline{438} \\ & 0.406 \end{aligned}$ |
| SF25X5 to 30 SF25 $\times 40$ to 60 SF25 270 to 200 SF25 2225 to 600 | $\begin{aligned} & 2 \\ & 2 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.000 \\ & 3.188 \\ & 3.125 \\ & 3.844 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.562 \\ & 2.438 \\ & 2.315 \\ & 2.781 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.500 \\ & 1.562 \\ & 1.625 \\ & 1.578 \end{aligned}$ | $\begin{aligned} & 0.812 \\ & 1.218 \\ & 1.531 \end{aligned}$ | $\begin{aligned} & -\overline{0.125} \\ & 0.188 \\ & 0.250 \end{aligned}$ | $\begin{aligned} & 0 . \overline{19} \\ & \begin{array}{l} 0.000 \\ 1.000 \end{array} \end{aligned}$ | $\begin{aligned} & 0.344 \\ & 0.344 \\ & 0.406 \end{aligned}$ | ${ }_{0}^{0.406}$ <br> 0.406 <br> 0.469 |
| SF50P35 to 60 SF50P70 to 100 SF50P125 to 200 SF50P250 to 400 SF50P700 to 800 | $\begin{aligned} & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & \hline \end{aligned}$ | $\begin{aligned} & 3.188 \\ & 3.625 \\ & 3.625 \\ & 4.344 \\ & 4.469 \\ & 6.469 \\ & \hline \end{aligned}$ | $\begin{aligned} & 2.438 \\ & 2.875 \\ & 2.875 \\ & 3.281 \\ & 3.406 \\ & 4.469 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.563 \\ & 2.125 \\ & 2.125 \\ & 2.094 \\ & 2.219 \\ & 2.219 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.818 \\ & 0.947 \\ & 1.218 \\ & 1.525 \\ & 2.000 \\ & 2.500 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.125 \\ & 0.125 \\ & 0.188 \\ & 0.245 \\ & 0.250 \\ & 0.375 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.719 \\ & 0.750 \\ & 1.750 \\ & 1.000 \\ & 1.500 \\ & 2.000 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.344 \\ & 0.313 \\ & 0.344 \\ & 0.406 \\ & 0.406 \\ & 0.531 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.406 \\ & 0.375 \\ & 0.406 \\ & 0.469 \\ & 0.500 \\ & 0.720 \\ & \hline \end{aligned}$ |
| SF60C5 to 30 SF60C35 to 60 SF60C70 to 100 SF60C125 to 200 SF60C225 to 400 SF60C450 to 800 | $\begin{aligned} & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & 2 \\ & \hline \end{aligned}$ | 2.875 4.375 5.000 5.500 6.250 6.250 | $\begin{aligned} & 2.500 \\ & 3.625 \\ & 3.875 \\ & 4.000 \\ & 4.750 \\ & 4.750 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.875 \\ & 2.734 \\ & 2.875 \\ & 2.906 \\ & 3.000 \\ & 3.063 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.563 \\ & 0.813 \\ & 0.938 \\ & 1.531 \\ & 2.000 \\ & 2.500 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.063 \\ & 0.125 \\ & 0.125 \\ & 0.250 \\ & 0.250 \\ & 0.250 \end{aligned}$ | $\begin{aligned} & 0.406 \\ & 0.719 \\ & 0.750 \\ & 1.000 \\ & 1.500 \\ & 2.000 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.251 \\ & 0.250 \\ & 0.344 \\ & 0.406 \\ & 0.406 \\ & 0.563 \\ & 0.563 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.120 \\ & 0.250 \\ & 0.406 \\ & 0.625 \\ & 0.781 \\ & 0.625 \\ & 0.625 \\ & \hline \end{aligned}$ |
| SF60X5 to 30 SF60X35 to 60 SF $60 \times 70$ to 100 SF60 125 to 200 SF60X250 to 400 SF60X450 to 600 | $2$ | $\begin{aligned} & 5.000 \\ & 4.375 \\ & 4.406 \\ & 4.406 \\ & 5.094 \\ & 5.094 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.813 \\ & 3.625 \\ & 3.656 \\ & 3.656 \\ & 4.032 \\ & 4.032 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.625 \\ & 2.750 \\ & 2.906 \\ & 2.906 \\ & 2.844 \\ & 2.844 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.813 \\ & 1.000 \\ & 1.219 \\ & 1.532 \\ & 2.000 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.125 \\ & 0.125 \\ & 0.188 \\ & 0.250 \\ & 0.250 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.719 \\ & 0.750 \\ & 1.000 \\ & 1.000 \\ & 1.000 \\ & \hline 1.500 \end{aligned}$ | $\begin{aligned} & 0.344 \\ & 0.313 \\ & 0.344 \\ & 0.406 \\ & 0.406 \\ & \hline \end{aligned}$ | $0 . \overline{406}$ 0.375 0.406 0.459 0.500 |
| SF70P10 to 30 SF70P35 to 60 SF70P70 to 100 SF70P125 to 200 SF70P500 to 800 | $\frac{2}{2}$ | $\begin{aligned} & 2.000 \\ & 4.325 \\ & 4.406 \\ & 5.063 \\ & 5.063 \\ & 7.094 \\ & \hline \end{aligned}$ | 0.563 3.625 3.656 4.032 4.032 5.094 | $\begin{aligned} & 0.500 \\ & 2.750 \\ & 2.906 \\ & 2.844 \\ & 2.844 \\ & 2.844 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.818 \\ & 0.947 \\ & 1.525 \\ & 2.000 \\ & 2.500 \end{aligned}$ | $\begin{aligned} & 0.125 \\ & 0.125 \\ & 0.245 \\ & 0.250 \\ & 0.375 \end{aligned}$ | $\begin{aligned} & 0.719 \\ & 0.750 \\ & 1.000 \\ & 1.500 \\ & 2.000 \\ & \hline \end{aligned}$ | $\begin{aligned} & 0.344 \\ & 0.313 \\ & 0.406 \\ & 0.406 \\ & 0.531 \\ & \hline 0.531 \end{aligned}$ | 0.406 0.375 0.469 0.500 0.720 |

## Cross Reference

| COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE <br> PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2 N 681 | 2N681 | 2N2888 | 16RC20AS20 | 2N3896 | 2N3896 | 2N4379 | 72RA160 |
| $2 \mathrm{N682}$ | 2N682 | 2 N 2889 | 16RC30AS20 | 2N3897 | 2N3897 | 2N4441 | IR122F |
| $2 \mathrm{N6P3}$ | $2 \mathrm{N6B3}$ | 2 N 3099 | 2 N 3099 | 2N3898 | 2N3898 | 2N4442 | ${ }_{181228}$ |
| 2N684 | 2 N 684 | 2N3100 | 2N3100 | 2N3899 | 2N3899 | 2N4443 | 1R1220 |
| 2N685 | 2N685 | 2N3101 | 2 N 3101 | 2N3986 | 71R850 | 2N4444 | \|R122M |
| ${ }^{2} \mathrm{~N} 686$ | 2 N 686 | 2 N 3102 | 2 N 3102 | 2N3987 | 71RB60 | 2N5204 | 16RC60A |
| 2N687 | $2 \mathrm{N687}$ | 2N3103 | 2 N 103 | 2N3988 | $71 \mathrm{RB70}$ | 2N5205 | 16RC80A |
| ${ }^{2 N 688}$ | $2 \mathrm{N688}$ | 2N3104 | 2 N 3104 | 2N3989 | 71RB80 | 2N5206 | 16RC100A |
| $2 \mathrm{N689}$ | 2N689 | 2N3105 | ${ }^{2} \mathbf{N} 3105$ | 2N3990 | 71R890 | 2N5207 | 16RC120A |
| 2N690 | 2N690 | 2N3106 | 2N3106 | 2N3991 | $71 \mathrm{RB100}$ |  |  |
| 2N691 | 2N691 | 2 2,3353 | $301 \mathrm{RE5}$ | 2N3992 | 71R8110 |  |  |
| 2 N 692 | $2 \mathrm{N692}$ | 2N3354 | $301 \mathrm{RB10}$ | 2N4151 | 1 R 32 U |  |  |
| 2N1595 | 2N1595 | 2N3355 | $301 \mathrm{RB20}$ | 2N4152 | IR32F |  |  |
| 2N1596 | 2N1596 | 2N3356 | 301R830 | 2N4153 | 1 R 32 A |  |  |
| 2N1597 | 2N1597 | 2N3357 | $301 \mathrm{RB40}$ | 2N4154 | 1R328 | 802022 | \|R10681 |
| 2N1598 | ${ }^{2} \mathrm{~N} 1598$ | 2 2N3358 | $301 \mathrm{R850}$ | ${ }^{2}$ 2N4155 | ${ }_{1832 \mathrm{C}}$ | 802023 | \|R10681 |
| 2N18428 | 2N18428 | 2N3359 | $301 \mathrm{RB60}$ | 2N4156 | 1 P 32 D | 802025 | \|R106D1 |
| 2N1843B | 2 N 18438 | 2N3360 | $301 \mathrm{RB70}$ | ${ }^{2} \mathbf{N 4 1 5 7}$ | 1 R32E | 802026 | \|R106D1 |
| 2 N 1844 B | 2 N 18448 | 2N3361 | $301 \mathrm{RB80}$ | 2 N 158 | 1 R 32 M | 802051 | \|R12281 |
| 2N1845B | 2 N 18458 | 2N3362 | $301 \mathrm{R890}$ | 2N4159 | 1 P 32 U | 802052 | \|R12281 |
| 2N1846B | 2 N 1846 B | 2N3363 | 301R8100 | 2 N 1160 | 1832F | 802053 | \|R12201 |
| 2 N 18478 | 2 N 18478 | 2N3364 | 301 RB 120 | 2N4161 | IR32A | 802054 | \|R12201 |
| 2 N 1848 B | 2 N 18488 | 2N3530 | 304RA5 | ${ }^{2} \mathbf{N 4 1 6 2}$ | ${ }_{18328}$ | 804001 | $1 \mathrm{R5B}$ |
| 2 N 1849 B | 2 N 18498 | 2N3531 | 304RA10 | 2N4163 | ${ }_{1832 \mathrm{C}}$ | B04002 | IR5B |
| 2N1850B | 2 N 1850 B | 2 2N3532 | 304 RA 20 | 2N4164 | IR32D | B04003 | 1R6B |
| ${ }^{2 N} 2031$ | 2N2031 | 2 N 3533 | $304 \mathrm{RA30}$ | 2 N 4165 | 1 R 32 E | B04004 | 1 R 5 D |
| 2N2322 | 2 N 2322 | 2N3534 | 304RA40 | 2N4166 | IR32M | 804005 | IR5D |
| 2N2322A | 2 N 2322 A | 2N3535 | $304 \mathrm{RA50}$ | 2N4167 | 5RC10A | 804006 | IR6D |
| 2 N 2323 | 2 N 2323 | 2N3536 | 304RA60 | 2N4168 | 5RC10A | C5A | IR5A |
| 2N2323A | 2 N 2323 A | 2N3537 | 304 AR 70 | 2N4169 | $5 \mathrm{AC10A}$ | C58 | 1R58 |
| ${ }^{2 N} 2324$ | 2 N 2324 | 2 N 3538 | $304 \mathrm{RA80}$ | 2N4170 | 5RC20A | c5c | IR5C |
| 2 N 2324 A | 2 N 2324 A | 2 N 3539 | $304 \mathrm{RA90}$ | 2 N 4171 | 5 Sc 30 A | C5D | $1 \mathrm{R5D}$ |
| 2 N 2325 | ${ }^{2} \mathbf{N} 2325$ | 2 N 3540 | 304RA100 | 2N4172 | 5RC40A | C5F | \|R5F |
| 2 N 2325 A | 2 N 2325 A | 2N3541 | 304RA120 | 2 N 4173 | $5^{5 R C 50 A}$ | ${ }^{\text {c5G }}$ | IR5G |
| 2N2326 | 2 N 2326 | 2N3649 | 2 N 3649 | 2 N 4174 | 5 Fcg 6 A | ${ }^{\text {C5 }}$ | 1854 |
| 2 N 2326 A | 2 N 2326 A | 2 N 3650 | 2 N 3650 | 2N4175 | 5RC10A | C5U | IRSU |
| 2N2327 | 2 N 2327 | 2N3651 | 2N3651 | 2N4176 | 5RC10A | c6A | IRGA |
| 2N2327A | 2 22327A | 2N3652 | ${ }^{2 N} 3655$ | 2N4177 | 5RC10A | C6B | 1R6B |
| ${ }^{2 N} 23238$ | ${ }^{2 \mathrm{~N} 2328}$ | 2N3653 | $2 N 3653$ $2 N 3654$ | 2N4178 | $5_{58 C 20 A}$ | ${ }_{\text {c CbC }}^{\text {C6D }}$ | IR6C |
| 2N2328A | 2N2328A | 2N3654 | 2 N 3654 | 2N4179 | 5RC30A | C6D | $1 \mathrm{R6D}$ |
| 2 N 2344 | 2N2344 | 2 N 3655 | 2 N 3655 | ${ }^{2} \mathrm{~N} 4180$ | $5 \mathrm{FCC40A}$ | C6F | 1R6F |
| 2 N 2345 | 2 N 2345 | 2 N 3656 | 2 N 3655 | 2 N 4181 | 5RC50A | C6G | IR6G |
| 2N2346 | 2 N 2346 | 2N3657 | 2 N 3657 | 2N4182 | 5RC60A | $\mathrm{C6H}$ | $1 \mathrm{R6H}$ |
| 2 N 2347 | 2 N 2347 | 2N3658 | 2 2N3658 | 2N4361 | 71RA10 | c6u | IRGU |
| 2N2348 | 2 N 2348 | 2N3870 | 2N3870 | 2N4362 | 71 RA 20 | CIOA | 2N1772A |
| 2 N 2503 | $1518{ }^{155}$ | 2N38771 | 2 N 3877 | 2 N 4363 | 71RA40 | C10B | 2N1774A |
| 2N2504 | 1518 F 10 | 2N3872 | 2 N 3872 | 2N4364 | 71 RAGO | C10c | 2N1776A |
| 2N2505 2N2506 | 151RF20 151 RF 30 | 2N3873 | ${ }_{\text {251RA10 }}^{\text {2N373 }}$ | 2N4365 | 71 RABO | C10D | 2N1777A |
| 2N2506 2N2507 | 151RF30 | 2N3884 | $151 \mathrm{RA10}$ | ${ }^{2} \mathbf{N 4 3 6 6}$ | $71 \mathrm{RA100}$ | C10F | 2N1771A |
| 2N2507 | 151RF40 | 2N3885 | 151RA10 | 2N4367 | $71 \mathrm{RA120}$ | C10G | 2N1773A |
| 2N2542 | 151RC5A | 2 N 3887 | 151RA30 | 2N4369 | 71RA160 | clou ciou | ${ }_{2} \mathbf{2 N 1 7 7 0 A}$ |
| 2N2543 | 151RC10A | 2N3888 | 151 Ra40 | 2 N 4371 | 72RA10 | c11A | 2N1772 |
| 2N2544 | 151RC20A | 2N3889 | 151 RA 50 | 2 N 4372 | 72RA20 | c118 | 2 N 1774 |
| 2N2545 | 151RC30A | 2N3890 | 151 RA60 | 2N4373 | 72RA40 | Clic | 2 N 1776 |
| 2 N 2546 | 151RC40A | 2 N 3891 | 151 RA 70 | 2 N 4374 | 72RA60 | C110 | 2 N 1777 |
| 2N2547 | 151RC50A | 2N3892 | 151 RABO | ${ }^{2 N 4375}$ | 72RABO | C11E | 2N1778 |
| ${ }^{2 N 2548}$ | 151RC60A | 2 N 3893 | $151 \mathrm{RA90}$ | 2 N 4376 | 72RA100 | C11F | 2N1771 |
| 2N2549 | 151RC80A | 2N3894 | 151 RA 100 | 2N4377 | 72RA120 | c11G | 2N1773 |
| 2N2550 | 151RC100A | 2N3895 | 151RA120 | 2N4378 | 72RA140 | C11H | 2N1775 |




| COMPETITIVE <br> PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO PART NO. | SUGGESTEDIR REPLACEMENT | $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTED IR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| C394D | 550PB040 | C506E | 470PB50S57 | C28120PC | 254 RA 130 | E220.4 | 250 PA40 |
| C394E | 550P8050 | C506M | 470P860S57 | C28120s | 254RA70 | E220.6 | $250 P$ A60 |
| с394, | 550PB060 | C507A | 550 PB 10 | C28120T | 254RA90 | E220.8 | $250 P$ A80 |
| C395A | 550PBQ10564 | C5078 | 550 PB 20 | C29120E | 304RA50 | E220-10 | 250 PA 100 |
| С3958 | 550PBO20SE4 | C507C | 550 PB 30 | C29120M | 304RA60 | E220.12 | 250 PA 120 |
| C395C | 550PB030564 | C507D | $550 \mathrm{PB40}$ | C29120N | $304 \mathrm{RA80}$ | E220.14 | 250 PA140 |
| C3950 | 550PBO40S64 | C507E | $550 \mathrm{PB50}$ | C29120P | 304 RA 100 | E220-16 | 250PA160 |
| C395E | 550PBO50S64 | C507M | ¢50P860 | C29120PA | 304RA110 | E241A | 16RC5A |
| C395M | 550PB060564 | C507N | $550 \mathrm{PB80}$ | C29120PB | 304RA120 | E2418 | $16 \mathrm{RCl10A}$ |
| C398E | 420 PM 50 | C507P | 550PB100 | C29120S | 304RA70 | E241C | 16RC15A |
| C398M | 420 PM 60 | C507PA | 550P8110 | C29010T | $304 \mathrm{RA90}$ | E2410 | $16 \mathrm{RC20A}$ |
| C398N | $420 \mathrm{PM80}$ | C507PB | 550 PB 120 | C53.02 | \|R1228 | E241E | 16RC25A |
| C398P | 420 PM 100 | C507PC | 550PB130 | C53.03 | IR122C | E241F | 16 RC 30 A |
| C398PA | 420 PM 110 | C507PD | 550PB140 | C53.04 | 18122 D | E241H | 16RC40A |
| C398PB | 420 PM 120 | C507S | $550 \mathrm{PB70}$ | C53.05 | IR122E | E241K | 15RC50A |
| C398S | 420 PM 70 | C507T | $550 \mathrm{PB90}$ | C53.06 | \|R122M | E241M | $16 \mathrm{RC60A}$ |
| С3987 | 420 PM 90 | с509M | 500PB660 | C55-02 | 10RC20A | E241P | 16RC70A |
| C440E | $900 \mathrm{PB50}$ | C509n | 500p0880 | C55.04 | 10RC40A | E241S | 16RC80A |
| C440M | 900 PB60 | C509P | 500PB6100 | C55.06 | 10RC60A | E241V | 16RC90A |
| C440N | 900 PB80 | C509PA | 500 PB 0110 | C55.08 | 10RC80A | E2412 | 16RC100A |
| C440P | 900 PB 100 | C509PB | 500PB6120 | Cs5-10 | 10RC100A | E2412B | 16RC110A |
| C440PA | 900 PB 110 | c509s | 500 PBO 70 | C55-12 | 10RC120A | E241zD | 16RC120A |
| C440PB | 900 PB 120 | C509\% | 500Рво90 | C5220.08 | 250 A80 | E351A | 22RC5 |
| C440PC | 900 PB 130 | C510A | $550 \mathrm{PBQ10}$ | Cs220-10 | 250PA100 | E3518 | $22 \mathrm{RCl} 0_{0}$ |
| C440S | 900 PB 70 | C5108 | 550Р8020 | CS220.12 | 250 PA120 | E351C | $22 \mathrm{RC15}$ |
| C440T | 900PB90 | C510C | $550 \mathrm{POB3} 3$ | Cs220-14 | 250 PA140 | E3510 | 22 RC 20 |
| C441PA | 750 PB 110 | C5100 | 550 PB 040 | CS220-16 | 250 PA160 | E351E | 22 RC 25 |
| C441PB | $750 \mathrm{PB120}$ | C510e | 550 PB 050 | CS250.08 | 250 PABO | E351F | $22 \mathrm{RC30}$ |
| C441PC | $750 \mathrm{PB130}$ | c510M | 550PB060 | CS250-10 | 250 PA 100 | E351H | $22 \mathrm{RC40}$ |
| C441PD | $750 \mathrm{PB140}$ | C600e | $900 \mathrm{PB50}$ | CS250-12 | 250 PA120 | E351K | 22 RC 50 |
| C441PE | 750 PB 150 | c600m | $900 \mathrm{PB60}$ | CS250-14 | 250 PA140 | E351M | $22 \mathrm{RC60}$ |
| C441PM | 750 PB 160 | C600N | $900 \mathrm{PB80}$ | Cs250.16 | 250 PA 160 | E351P | $22 \mathrm{RC70}$ |
| C441PS | $750 \mathrm{PB170}$ | C600P | 900 PB 100 | C5400.08 | $550 \mathrm{PB80}$ | E352A | $22 \mathrm{RC5}$ |
| C444A | 701PBC10 | C600PA | 900PB110 | CS400-10 | 550PB100 | E3528 | $22 \mathrm{RC10}$ |
| C444B | 701 PBO 20 | C600PB | 900 PB 120 | CS400-12 | 550PB120 | E352C | $22 \mathrm{RC15}$ |
| C444C | 701 PBO 30 | c600S | 900 PB 70 | CS400-14 | 550P8140 | E3520 | 22 RC 20 |
| C444D | 70198040 | C600 | $900 \mathrm{PB90}$ | CS400.16 | 550 PB 160 | E352E | 22 RC 25 |
| C444E | 701PB650 | C601PA | $750 \mathrm{~PB}_{1110}$ | CS401-18 | 600P8180 | E352F | 22RC30 |
| C444M | 701P8060 | C601PB | 750 PB 120 | CS401-20 | 600PB200 | E352H | $22 \mathrm{RC40}$ |
| C445A | 700PBQ10 | C601PC | 750 PB 130 | CS401-21 | 600P8210 | E352K | $22 \mathrm{RC50}$ |
| ${ }^{\text {C445B }}$ | 700 PBO 220 | C601PD | 750 PB 140 | CS4401-22 | 600 PB 220 | E352M | $22 \mathrm{RC60}$ |
| C445C | 700 PB O30 | C601PE | $750 \mathrm{PB150}$ | CS401.23 | 600PB230 | E352P | $22 \mathrm{RC70}$ |
| C445D | 700 PB 040 | C601PM | 750 PB 160 | CS401.24 | 600 PB 240 | F400-2 | 420 PB 20 |
| C445E | 700PBESO | C601PS | 750PB170 | CS401.25 | 600 PB 250 | F400-4 | 420 PB 40 |
| C445M | 700 PB 860 | C602L | 600PB200 | CS550.08 | 750 P880 | F400.6 | $420 \mathrm{PB60}$ |
| C447E | 650 PB O50 | C602LA | 600 PB 210 | Cs550.10 | 750 PB100 | F400-8 | $420 \mathrm{PB80}$ |
| C447M | 650P8a60 | C602LB | 600P8220 | Cs550.12 | 750P8120 | F400-10 | $420 \mathrm{PB100}$ |
| C447N | 650PB080 | C602LC | 600 PB 230 | Cs550.14 | $750 \mathrm{PB140}$ | F400.12 | $420 \mathrm{PB1} 12$ |
| C447P | 650p8P100 | C602LD | 600 P8240 | Cs550-16 | 750PB160 | F400-14 | 420 PB 140 |
| C447PA | 650PBal10 | C602LE | 600 PB 250 | E151A | 10RC5A | F400-16 | 420 PB160 |
| C447PB | 650PBQ120 | C602PN | 600PB180 | E151B | 10RC10A | F500-2 | 420 PB 20 |
| C447S | 650P8070 | C602PS | $600 \mathrm{PB170}$ | E151C | 10RC15A | F500-4 | 420 P 40 |
| ${ }^{\text {C447T }}$ | 650P8090 | C602PT | $600 \mathrm{PB190}$ | E151D | 10RC20A | F500-6 | $420 \mathrm{PB60}$ |
| C448E | $651 \mathrm{PBa50}$ | c609m | 750 PB 060 | E151E | 10RC25A | ${ }^{\text {F500.8 }}$ | 420 P880 |
| C448M | 651 PB 060 | C609N | 750p8080 | E151F | 10RC30A | F500-10 | 420 PB 100 |
| C448N | 651 PBQ80 | C609P | $750 \mathrm{PBQ100}$ | E151H | 10RC40A | F500-12 | 420 PB 120 |
| C448P | 651 PB6100 | C609PA | $750 \mathrm{PBC1} 110$ | E151K | 1 IORC50A | F500-14 | $420 \mathrm{PB140}$ |
| C448PA | 651 PBO 110 | C609PB | 750 PB 120 | E151M | 10RC60A | F500-16 | 420 PB 160 |
| C448PB | $651 \mathrm{PBQ1} 20$ | C609S | 750 PB 970 | E151P | 10RC70A | F600-2 | 420 PB 20 |
| C448S | 651 PBQ70 | C609T | 750 PB 090 | E151S | 10RC80A | F600.4 | $420 \mathrm{PB40}$ |
| C448T | 651 PB090 | C701PA | 1000 PK110 | E151V | 10RC90A | F600-6 | $420 \mathrm{PB60}$ |
| C501N | $550 \mathrm{PB80}$ | C701PB | 1000 PK120 | E161A | 10RC5A | F6008 | $420 \mathrm{PB80}$ |
| C501P | 550 P8100 | C701PC | 1000 PK130 | E1618 | 10RCLIOA | F600-10 | 420 PB 100 |
| C501PA | 550P8110 | C701PD | 1000 PK140 | E161C | 10RC15A | F600.12 | 420 PB 120 |
| C501PB | 550 PB120 | C701PE | 1000 PK150 | E161D | 10RC20A | F600-14 | $420 \mathrm{PB140}$ |
| C501PC | 550 PB 130 | C701PM | 1000 PK160 | E161E | 10RC25A | F600-16 | $420 \mathrm{PB160}$ |
| C501PD | 550PB140 | C702L | 700PK200 | E180-2 | 2509 A20 | G400-2 | 420 PB 20 |
| C501PE | 550 PB 150 | C702LA | 700PK210 | E180-4 | 250 PA40 | G400-4 | 420 PB 40 |
| C501PM | 550 PB 160 | C702LB | 700PK220 | E1806 | 250 P A60 | G4006 | $420 \mathrm{PB60}$ |
| C501ps | 55098170 | C702LC | 700PK230 | E180.8 | 2509 PABO | G400-8 | $420 \mathrm{PBB0}$ |
| C501s | $550 \mathrm{PB70}$ | C702LD | 700PK240 | E180-10 | 250 PA100 | G400-10 | 420 PB 100 |
| C501T | $550 \mathrm{PB90}$ | C28120N | 254RABO | E180.12 | 250 PA120 | G400-12 | 420 PB 120 |
| C506A | 470 PB 10557 | C28120P | 254RA100 | E180-14 | 250PA140 | G400-14 | 420 PB 140 |
| C506C | 470 PB 30557 | C28120PA | 254 RA 110 | E180.16 | 250PA160 | G400-16 | 420 PB 160 |
| C506D | 470PB40S57 | C28120PB | 254RA120 | E220.2 | 250P A20 | G500-2 | 470 PB 20 |


| COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| G500-4 | 470 P840 | H1800-10 | 1000 PK100 | MCR2935-6 | $1 \mathrm{IR30D}$ | NLC36A | 10RC10 |
| G500.6 | 470 P860 | H1800-12 | 1000 PK 120 | MCR3818-1 | IR32U | NLC36B | 10RC20 |
| G500-8 | 470 P880 | MCR106-1 | \|R106Y1 | MCR3818-2 | IR32F | NLC36C | $10 \mathrm{RC30}$ |
| G500-10 | $470 \mathrm{PB100}$ | MCR106-2 | \|R106F1 | MCR3818.3 | IR32A | NLC36D | $10 \mathrm{RC40}$ |
| G500-12 | 470 P8120 | MCR106-3 | 18106A1 | MCR38184 | 1R328 | NLC36E | $10 \mathrm{RC50}$ |
| G500-14 | 470 PB140 | MCR106-4 | \|R106B1 | MCR3818-5 | IR32C | NLC36M | $10 \mathrm{RC60}$ |
| G500-16 | 477088160 | MCR106-5 | \|R106C1 | MCR3818-6 | IR32D | NLC36N | 10 RCs 0 |
| G650-2 | 470 PB20 | MCR1066 | \|R106D1 | MCR3918-1 | IR30U | NLC36S | $10 \mathrm{RC70}$ |
| G650-4 | 470 P B40 | MCR406-1 | \|R106Y1 | MCR3918-2 | IR30F | NLC37A | 10RC10A |
| G650.6 | $470 \mathrm{PB60}$ | MCR406-2 | \|R106F1 | MCR3919.3 | IR30A | NLC37B | 10 RC 20 A |
| G650-8 | $420 \mathrm{PB80}$ | MCR406-3 | \|R106A1 | MCR3918-4 | IR30B | NLC37C | 10RC30A |
| G650-10 | 470 PB100 | MCR406-4 | \|R106B1 | MCR3918.5 | IR30C | NLC37D | 10RC40A |
| G650-12 | 470 P8120 | MCR406-5 | \|R106C1 | MCR3818.6 | IR300 | NLC37E | 10RC50A |
| G650-14 | 470 P8140 | MCR406-6 | \|R106D1 | MCR3935-1 | 22RA2 | NLC37M | 10RC60A |
| G650-16 | 470 PB 160 | MCR407.1 | \|R106Y1 | MCR3935-2 | $22 \mathrm{RA5}$ | NLC37N | 10RC80A |
| 6850-2 | 550 PB 20 | MCR407-2 | \|R106F1 | MCR3935-3 | $22 \mathrm{RA10}$ | NLC37s | 10RC70A |
| G850-4 | 5509840 | MCR407-3 | \|R106A1 | MCR3935-4 | 22RA20 | NLC38A | $22 \mathrm{RC10}$ |
| G850.6 | $550 \mathrm{PB60}$ | MCR407-4 | \|R10681 | MCR3935-5 | 22RA30 | NLC38B | 22 RC 20 |
| 6850.8 | $550 \mathrm{PB80}$ | MCR407.5 | \|R106C1 | MCR3935-6 | 22RA40 | NLC38C | $22 \mathrm{RC30}$ |
| G850-10 | 550PB100 | MCR4076 | \|R106D1 | MCR3935-7 | 22RA50 | NLC38D | $22 \mathrm{RC40}$ |
| G850-12 | 550P8120 | MCR846-1 | 3RC2A | MCR3935-8 | 22 RAGO | NLC38E | $22 \mathrm{RC50}$ |
| G850-14 | 550 PB 140 | MCR846-2 | 3RC5A | NL511A | 16RC10AS60 | NLC38G | $22 \mathrm{RC15}$ |
| G850-16 | $550 \mathrm{PB160}$ | MCR846-3 | 3RC10A | NL511B | 16RC20AS60 | NLC38H | 22 RC 25 |
| G950.2 | 550 P820 | MCR846-4 | 3RC20A | NL511C | 16RC30AS60 | NLC45A | 37RC10A |
| 6950-4 | 550 P840 | MCR1308-1 | 10RC2A | NL5110 | 16RC40AS60 | NLC45B | 37RC20A |
| G950-6 | 550 P860 | MCR1308-2 | 10RC5A | NL511E | 16RC50AS60 | NLCA5C | 37RC30A |
| G950-8 | $550 \mathrm{PB80}$ | MCR1308-3 | 10RC10A | NL511M | 16RC60AS60 | NLC45D | 37RC40A |
| G950-10 | 550PB100 | MCR1308-4 | 10RC20A | NL511N | 16RC80AS60 | NLC45E | 37RC50A |
| G950-12 | $550 \mathrm{PB120}$ | MCR1308-5 | 10RC30A | NL511P | 16RC100AS60 | NLCA5G | 37RC15A |
| G950-14 | 550P8140 | MCR1308-6 | 10RCAOA | NL511PA | 16RC110AS60 | NLC45H | 37RC25A |
| G950-16 | 550PB160 | MCR1907-1 | 1 R 141 F | NL511PB | 16RC120AS60 | NLC45M | 37RC60A |
| H800-2 | 700PK20 | MCR1907-2 | IR141F | NL511S | 16RC70AS60 | NLCA5N | 37RC80A |
| H880.4 | 700 K K40 | MCR1907-3 | 1R141A | NL511T | 16RC90AS60 | NLCASS | 37RC70A |
| H800-6 | $7009 \mathrm{K60}$ | MCR1907-4 | 1R1418 | NL555A | 36RC10A | NLCAST | 37RC90A |
| H800-8 | 700PK80 | MCR1907-5 | 18141C | NL555B | 368 C 20 A | NLC46A | 36RCIOA |
| H800.10 | 700PK100 | MCR19076 | 181410 | NL555C | 36 RC 30 A | NLCA6B | 36 RC 20 A |
| H800-12 | 700PK120 | MCR2304-1 | ${ }_{1832 \mathrm{~L}}$ | NL555D | 36RC40A | NLC46C | 36RC30A |
| H800-14 | 700PK 140 | MCR2304-2 | 1R32F | NL555E | 36RC50A | NLCA6D | 36 RC 40 A |
| H800-16 | 700PK160 | MCR2304.3 | 1 1R32A | NL555M | 36RC60A | NLCA6E | 36RC50A |
| H1000-2 | 700PK20 | MCR2304.4 | 1R32B | NL555N | $36 \mathrm{RAB0}$ | NLCA6G | 36RC15A |
| H1000.4 | 700 PK40 | MCR2304.5 | ${ }^{1832 C}$ | NL555P | $36 R A 100$ | NLCA6H | 36RC25A |
| H1000-6 | 700PK60 | MCR2304-6 | 18320 | NL555PA | 36 RA110 | NLC46M | $36 \mathrm{RC60A}$ |
| H1000-8 | 700PK80 | MCR2305-1 | ${ }_{\text {IR30U }}$ | NL555PB | 36RA120 | NLC46N | 36RC80A |
| H1000-10 H1000-12 | 700PK 100 | MCR2305-2 | 1 R 30 F | NL555PC | $36 R$ A130 | Nlcags | 36RC70A |
| H1000-12 | 700PK120 | MCR2305-3 | IR30A | NL555PD | $36 \mathrm{RA140}$ | NLCAGT | 36RC90A |
| H1000-16 | 700PKK160 | MCR2305-4 | IR30B | NL555PE | $36 \mathrm{RA150}$ | NLC50A | 71RC10A |
| H1200-2 | 850PK20 | MCR2305-6 | IR300 | NL555S | ${ }_{36 R A 70}$ | NLC508 | 711RC30A |
| H1200-4 | 850 PK 40 | MCR2604-1 | 5RC2A | NL555T | $36 \mathrm{RA90}$ | NLC500 | 71RC40A |
| H1200.6 | 850PK60 | MCR2604-2 | 5RC5A | NL556A | 37RCIOA | NLC50E | 71RC50A |
| ${ }^{\text {H1200-8 }}$ | 850 KK80 | MCR2604.3 | 5RC10A | NL556B | $37 \mathrm{RC20A}$ | NLC50G | 71RC15A |
| H1200-10 | 850PK100 | MCR2604 4 | 5RC20A | NL556C | 37RC30A | NLC50H | 71RC25A |
| H1200-12 | 850PK120 | MCR2604-5 | $5 \mathrm{FC30A}$ | NL5560 | 37RC40A | NLC50M | 71RC60A |
| H1200-14 | 850PK 140 | MCR2604.6 | 5RC40A | NL556E | 37RC50A | NLCson | $71 \mathrm{RCB0A}$ |
| H1200-16 | 850PK 160 | MCR2604.7 | 5RC50A | NL556M | 37RC60A | NLC50S | 71RC70A |
| H1400-4 | 10000PK40 | MCR2604-8 | 5RC60A | NL556N | 37 RABO | NLC50T | 71RC90A |
| H1400-6 | 1000 PK60 | MCR2605-2 | 5RC2A 5RC5A | NL556P | 37RA100 37RA110 | NLC52A | 72RC10A |
| H1400.8 | 1000 PK 80 | MCR2605-3 | 5RC10A | NL556PB | $37 \mathrm{RA120}$ | NLC52C | 72RC30A |
| H1400-10 | 1000PK100 | MCR2605-4 | 5RC20A | NL556PC | 37 RA 130 | NLC520 | 72RC40A |
| H1400-12 | 1000 PK 120 | MCR2605-5 | 5RC30A | NL556PD | 37RA140 | NLC52E | 72RC50A |
| H1400-14 | 1000 PK 140 | MCR2605-6 | 5RC40A | NL556PE | 37RA150 | NLC52G | 72RC15A |
| ${ }_{\text {H1400-16 }}$ | 1000PK160 | MCR2605-7 | 5RC50A | NL556PM | 37RA160 | NLC52H | 72RC25A |
| H1600-2 H1600-4 | 1000 PK20 1000 PK40 | MCR2605-8 | 5RC60A | NL556S | 37 RA 70 | NLC52M | 72RC60A |
| H1600.4 | 1000 PK460 | MCA2835-1 | IR32U | NL556T | 37RA90 | NLC52N | $72 \mathrm{RC80A}$ |
| H1600.8 | 1000 PK80 | MCR2835-3 | IR32A | NLC35A | $16 R C 10 A$ 16 CL 20 A | NLC52S | 72RC700 |
| H1600-10 | 1000PK100 | MCR2835-4 | ${ }_{18328}$ | NLC36C | 16RC30A | NLC150E | 71 RA 50 |
| H1600-12 | 1000 PK 120 | MCR2835-5 | 1 1R32C | NLC35D | 16 RCAOA | NLC150M | 71 RA60 |
| H1600-14 | 1000 PK140 | MCR2835-6 | IR32D | NLC35E | 16RC50A | NLC150N | 71 RABO |
| H1600-16 | 1000 F K 160 | MCR2935-1 | IR30U | NLC35M | $16 \mathrm{RC60A}$ | NLC150P | 71RA100 |
| H1800-2 | 1000PK20 | MCR2935-2 | IR30F | NLC35N | 16RC80A | NLC150PA | 71 RA110 |
| H1800-4 | 1000PK 40 | MCR2935-3 | ${ }_{1830 A}$ | NLC35P | 16RC100A | NLC150PB | 71RA120 |
| H18006 | 1000PR60 | MCR2935-4 | ${ }_{\text {IR308 }}$ | NLC35S | 16RC70A | NLC150PC | 71 RA 130 |
| H1800-8 | 1000PK80 | MCR2935-5 | IR30C | NLC35T | 16RC90A | NLC150S | 71RA70 |


| COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. PART NO. | SUGGESTED IR REPLACEMENT | $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTED IR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| NLC150T | 71RA90 | NLCI85E | 151RF50 | NLCSOIP | 550PB100 | NLF158M | 81RLB60 |
| NLC151E | 81RL50 | NLC185M | 151RF60 | NLC501PA | 550P8110 | NLF158N | 81RLB80 |
| NLC151M | 81RL60 | NLC290A | 300RA10 | NLC501P8 | 550 PB 120 | NLF159P | 81RL8100 |
| NLC151N | $81 \mathrm{RL80}$ | NLC290B | 300RA20 | NLCS01PC | 550PB130 | NLF158S | 81RLB70 |
| NLC151P | B1RLI00 | NLC290C | 300RA30 | NLC501PD | 550P8140 | NLF158T | 81 L299 |
| NLC151S | $81 \mathrm{RL70}$ | NLC2900 | 300RA40 | NLC501PE | 550PB150 | NLF159A | 82RLB10 |
| NLC151T | 81 L.90 | NLC290E | 300RA50 | NLC501PM | 550PB160 | NLF1598 | 82RLB20 |
| NLC152E | 72RA50 | NLC290G | 300RA15 | NLC501PS | 550P8170 | NLF159C | 82RLB30 |
| NLC152M | 72RA60 | NLC290H | 300RA25 | NLC501s | 550PB70 | NLF159D | 82RLE40 |
| NLC152N | 72 RABO | NLC290M | 300RA60 | NLC501T | 550PB90 | NLF159E | $82 \mathrm{RLB50}$ |
| NLC152P | 72RA100 | NLC290N | $300 \mathrm{RAB0}$ | NLF150B | 81 RLA 20 | NLF159M | 82RLB60 |
| NLC152PA | 72RA110 | NLC290P | 300 RA 100 | NLF150C | 81RLA30 | NLF159N | 82RL880 |
| NLC152P8 | 72RA120 | NLC290PA | 300RA110 | NLF150D | 81RLA40 | NLF159P | 82RLB100 |
| NLC152PC | 72RA130 | NLC290PB | 300RA120 | NLF150E | 81RLA50 | NLF159S | 82RLB70 |
| NLC152S | 72 RA 70 | NLC290S | 300RA70 | NLF150M | 81RLA60 | NLF159T | 82 LL 890 |
| NLC152T | 72RA90 | NLC290T | 300RA90 | NLF150N | 81RLAB0 | NLF185A | 161RL10 |
| NLC153E | 82RL50 | NLC291A | $303 R A 10$ | NLF150P | 81RLA100 | NLF1858 | 161RL20 |
| NLC153M | 82 RL 60 | NLC291B | $303 R A 20$ | NLF150S | 81RLA 70 | NLF185C | 151RL30 |
| NLC153N | 82RL80 | NLC291C | 303RA30 | NLF150T | 81RLA90 | NLF1850 | 151RL40 |
| NLC153P | 82 RLL 100 | NLC2910 | 303RA40 | NLF151B | 81 RL20 | NLF185E | 161 RL50 |
| NLCI53S | 82 RL 70 | NLC291E | $303 \mathrm{RA50}$ | NLFI51C | $81 \mathrm{RL30}$ | NLF185M | 161 PL 60 |
| NLC153T | 82RL90 | NLC291G | 303 FA 15 | NLF1510 | 81 RL40 | NLF355A | 140 PAL10 |
| NLC154A | 91RM10 | NLC291H | $303 R$ A 25 | NLF151E | 81RL50 | NLF3558 | 140PAL20 |
| NLC154B | 91 Rm 20 | NLC291M | $303 R$ A60 | NLF151M | 81 RL60 | NLF355C | 140 PAL30 |
| NLC154C | 91RM30 | NLC291N | $303 \mathrm{RAB0}$ | NLF151N | 81 RL80 | NLF3550 | 140 PAL40 |
| NLC154D | $91 \mathrm{RM40}$ | NLC291P | 303 RA100 | NLF151P | 81 RLIOC | NLF355E | 140 PAL50 |
| NLC154E | 91 RM50 | NLC291PA | 303RA110 | NLF151S | 81RL70 | NLF355M | 140PAL60 |
| NLC154M | 91RM60 | NLC291PB | 303RA120 | NLF151T | 81RL90 | NLF358A | 125PALB10 |
| NLC155A | 91RL10 | NLC291S | 303 RA 70 | NLF1528 | 82RLA20 | NLF3588 | 125 PaLb 20 |
| NLC155B | 91RL20 | NLC291T | 3038 A90 | NLF152C | 82RLA30 | NFL358C | 125 PAL 330 |
| NLC155C | 91RL30 | NLC350A | 115 PA10 | NLF1520 | $82 \mathrm{RLA40}$ | NLF3580 | 125 PaLb40 |
| NLC155D | 91RL40 | NLC350B | 115 PA20 | NLF152E | 82RLA50 | NLF358E | 125PALB50 |
| NLC155E | 91RL50 | NLC350C | 115 PA30 | NLF152M | 82RLA60 | NLF358M | 125 PaLbe0 |
| NLC155M | 91RL60 | NLC3500 | 115 PA40 | NLF152N | 82RLAB0 | NLF358N | 125PALB80 |
| NLC156A | 92RM10 | NLC350E | 115 PA50 | NLF152P | 82 LLA100 | NLF358P | $125 P$ ALB100 |
| NLC1568 | $92 \mathrm{RM20}$ | NLC350M | 115 PA60 | NLF152S | B2RLA ${ }^{\text {a }}$ | NLF358PA | 125 PALB110 |
| NLC156C | 92RM30 | NLC350N | 115 PA80 | NLF152T | 82RLA90 | NLF358PB | 125PALB120 |
| NLC156D | $92 \mathrm{RM40}$ | NLC350P | 115 PA100 | NLF153B | 82RL20 | NLF358S | 125 PaLB70 |
| NLC156E | $92 \mathrm{RM50}$ | NLC350PA | 115 PA110 | NLF153C | 82RL30 | NLF358T | 125 PaLb90 |
| NLC156M | 92RM60 | NLC350PB | 115 PA120 | NLF153D | 82RL40 | PSO20 | 1832F |
| NLC157A | $92 \mathrm{RL10}$ | NLC350PC | 115 PA130 | NLF153E | 82RL50 | PS120 | IR32A |
| NLC1578 | 92RL20 | NLC350S | 115 PA 70 | NLF533M | 82RL60 | PS220 | IR328 |
| NLC157C | 92RL30 | NLC350T | $115 \mathrm{PA90}$ | NLF153N | 82RL80 | PS320 | IR32C |
| NLC157D | 92RL40 | NLC354A | 140PAM10 | NLF153P | 82RLI00 | PS420 | 18320 |
| NLC157E | 92 RL 50 | NLC354B | 140PAM20 | NLF153S | 82 RL 70 | S0301/S2 | $\mid \mathrm{R106Y} 1$ |
| NLC157M | $92 \mathrm{RL60}$ | NLC354C | 140PAM30 | NLF153T | 82RL.90 | S0301JS3 | IR106Y1 |
| NLC178A | 151 R810 | NLC354D | 140PAM40 | NLF154A | $91 \mathrm{RM10}$ | s0301MS1 | IRSF |
| NLC1788 | $1518 \mathrm{Bz20}$ | NLC354E | 140PAM50 | NLF154B | 91RM20 | s0301MS2 | IRSF |
| NLC178C | $151 \mathrm{RB30}$ | NLC354M | 140PAM60 | NLF154C | 91RM30 | s0301Ms3 | IR6F |
| NLC178D | $151 R 840$ | NLC355A | 140 PaLl0 | NLF154D | 91RM40 | S0303RS2 | \|R106Y1 |
|  | $151 \mathrm{RB50}$ | NLC3558 | $140 \mathrm{PAL20}$ | NLF154E | 91RM50 | S0303RS3 | 1R106Y1 |
| NLC178M | $151 \mathrm{RB60}$ | NLC355C | 140PAL30 | NLFF154M | 91RM60 | S0306RS2 | IR122Y |
| NLCl78N | $151 R 880$ | NLC3550 | 140 PAL40 | NLF155A | 91RL10 | S0306RS3 | IR122Y |
| NLC178P | $151 \mathrm{RB100}$ | NLC355E | 140PAL50 | NLF1558 | 91RL20 | s0308RS2 | 1R122Y |
| NLCC178PA | $151 \mathrm{RB110}$ | NLC355M | 140 PAL60 | NLF155C | 91RL30 | S0308RS3 | IR122Y |
| NLC178PB | 151R8120 | NLC380A | 250 PA 10 | NLF1550 | 91RL40 | S0325G | IR30F |
| NLC178S | $151 \mathrm{RB70}$ | NLC380B | 250 PA20 | NLF155E | 91RL50 | S0501 JS2 | \|R106Y1 |
| NLC178T | 151 R890 | NLC380C | 250 PA30 | NLF155M | 91RL60 | S0501JS3 | \|R106Y1 |
| NLC180A | 151RA10 | NLC3800 | 250 PA40 | NLF156A | 92RM10 | S0501MS1 | IRSF |
| NLC1808 | 151 RA20 | NLC380E | 250 PA50 | NLF156B | 92RM20 | S0501MS2 | IR5F |
| NLC180C | 151 RA30 | NLC380M | 250 PAGO | NLFI56C | 92RM30 | S0501MS3 | 1R6F |
| NLC1800 | 1511 A40 | NLC380N | $250 \mathrm{PA80}$ | NLF156D | 92RM40 | S0503RS2 | 1R106F1 |
| NLC180E | 1517A50 | NLC380P | 250 PA100 | NLF156E | $92 \mathrm{RM50}$ | S0503RS3 | IR106F1 |
| NLC180M | 151RA60 | NLC380PA | $250 \mathrm{PA110}$ | NLF156M | 92RM60 | S0506RS2 | IR122F |
| NLC180P | 151RA100 | NLL380P8 | 150PA120 | NLF157A | 92RL10 | S0506883 | 1R122F |
| NLC180PA | 151 RA 110 | NLC380S | 250PA70 | NLF157C | 92RL30 | S0508RS3 | IR122F |
| NLC180P8 | 151RA120 | NLC380т | $250 \mathrm{PA90}$ | NLF1570 | 92RL40 | s0525G | IR30F |
| NLLC180PC | 151RA130 | NLC385A | 250 PAL 10 | NLF157E | 92RL50 | S1001/S2 | IR106A1 |
| NLC180S | 151 RA70 | NLC385B | 250 PAL 20 | NLF157M | 92RL60 | S1001/J3 | IR106A1 |
| NLC180T | 151 RA90 | NLC385C | 250 PAL30 | NLF158A | $81 \mathrm{RLB10}$ | S1001MS1 | IR5A |
| NLC185A | 151RF10 | NLC3850 | 250 Pal40 | NLF158B | 81RL820 | S1001MS2 | IR5A |
| NLC1858 | 151RF20 | NLC385E | 250 PAL50 | NLF158C | 81RLB30 | S1001ms3 | IR6A |
| NLC185C | 151RF30 | NLC385M | ${ }^{250 p A L 60}$ | NLF1588 | $81 \mathrm{RLLb40}$ | S1003RS2 | IR106A1 |
| NLC1850 | 151RF40 | NLC501N | 550P880 | NLFI58E | 81RLb50 | S1003RS3 | IR106A1 |


| $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTED IR REPLACEMENT |
| :---: | :---: |
| S1006RS2 | IR122A |
| S1006RS3 | IR122A |
| S1008RS2 | 18122A |
| S1008RS3 | IR122A |
| S10256 | IR30A |
| S2001JS2 | 1810681 |
| S2001JS3 | \|R10681 |
| s2001MS1 | 1R58 |
| S2001MS2 | IR5B |
| S2001MS3 | \|R6B |
| S2003RS2 | 1R10681 |
| S2003RS3 | 1R10681 |
| S2006RS2 | 1R1228 |
| S2006RS3 | 1R1228 |
| S2008RS2 | 181228 |
| S2008RS3 | 1R1228 |
| S2025G | IR308 |
| S4001 JS2 | IR106D1 |
| S4001JS3 | 1R106D1 |
| S4001MS1 | IR50 |
| S4001MS2 | IR50 |
| S4001MS3 | $1 \mathrm{R6D}$ |
| S4003RS2 | IR106D1 |
| S4003RS3 | IR106D1 |
| S4006RS2 | 181220 |
| S4006RS3 | 181220 |
| S4008RS2 | IR1220 |
| S4008RS3 | 18122 D |
|  | $1 \mathrm{IR30D}$ |
| SPS08 | 2N1771A |
| SPS020 |  |
| SPSO35 SPS18 | 16 CLSA 2 N 1772 a |
| SPS18 SPS28 | 2N1772A 2 N 1774 A |
| SPS28 SPS38 | 2N1774A 2N1776A |
| SPS48 | 2N1777^ |
| SPS58 | 2N1776A |
| SPS68 | 2N2619A |
| SPS120 | IR30A |
| SPS135 | $16 \mathrm{RC10A}$ |
| ${ }^{\text {SPS } 220}$ | 1 I 308 |
| SPS235 | 16RC20A |
| SPS320 | $1 \mathrm{IR30C}$ |
| SPS335 | 16RC30A |
| SPS420 | 1 R 30 D |
| SPS435 | 16PC40A |
| ${ }^{\text {SPS535 }}$ | 168C50a |
| ${ }^{\text {SPS635 }}$ | 16RC60A |
| T1C106A1 | IR106A1 |
| T1C10881 | 1R10681 |
| T1C106C1 | 1R106C1 |
| T1C10601 | IR106D1 |
| T1C106F1 | \|R106F1 |
| T1C10601 | \|R10601 |
| T1C106U1 | 1810641 |
| T400002208 | 16RC5A |
| T400011008 | $10 \mathrm{RC10}$ |
| T400011608 | 10RCIOA |
| T400012208 | 16RC10a |
| T400021008 | 10RC20A |
| T400021608 | 10RC20A |
| T400022208 | 16RC20A |
| T400031008 | 10RC30A |
| T400031608 | 10RC30a |
| T400032208 | 16 RC 30 A |
| T400041008 | 10RC40A |
| T400041608 | 108C40a |
| T400042208 | 16 RC 40 A |
| T400051008 | 10RC50A |
| T400051608 | 10RC50A |
| T400052208 | $16 \mathrm{RC50A}$ |
| T400062208 | 16RC60A |
| T4040022 | IR140F |
| T4040122 | IR140A |
| T4040222 | IR140B |


| COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT |
| :---: | :---: | :---: | :---: |
| T4040322 | IR140C | T5020880 | 81aLb80 |
| T4040422 | 1R1400 | T50210×70 | 81RLB100 |
| T4050122 | $22 \mathrm{RC10}$ | T5021080 | 81RLB100 |
| T4050222 | 22RC20 | T50211×70 | 81 RLB110 |
| T4050322 | 22 RC 30 | T5021180 | 81 RLB110 |
| T4050422 | 22RC40 | T50212×70 | ${ }^{81 R L B 120}$ |
| T4050522 | $22 \mathrm{RC50}$ | T5021280 | 81RLB120 |
| T4050522 | 22RC60 | T502-×70820 | 81RM20S66 |
| T4070022 | IR141F | T502-×70830 | 81RM30566 |
| T4070122 | 18141A | T502.x70840 | 81RM40S66 |
| T4070222 | \|R141B | T502.X70850 | 81RM50566 |
| T4070322 | 1R141C | T502-×70860 | $8^{81 R m 60 S 66}$ |
| T4070422 | $1 \mathrm{R}^{1410}$ | T502-×70870 | 81RM70566 |
| T4080016 | 10RC5A | T502-×70880 | 81 RM80s66 |
| T4080116 | 10RC10A | T502. $\times 70890$ | 81RM90566 |
| T4080216 | 10RC20A | T502-X70C10 | 81RM100566 |
| T4080316 | 10RC30A | T502-×70C114 | 811RLB110S66 |
| T4080416 | 10RC40A | T502. ${ }^{\text {T }}$ 70C12 | 81RLB120S66 |
| T4080516 | $10 \mathrm{RC50A}$ | T504017074AA | 82RM10 |
| T500014005AA | $37 \mathrm{RA10}$ | T504017074AO | $81 \mathrm{RM10}$ |
| T500014005AO | 36RA10 | T504024064AA | 82RM20 |
| T500024005AA | 37Ra20 | T504024064AO | 81RM20 |
| T500034005AA | 37RA30 | T504027074AA | 82RM20 |
| T500034005AO | 36Ra30 | T504027074AO | 81RM20 |
| T500044005AA | 37RA40 | T504034064AA | 82RM30 |
| T500044005AO | 36RA40 | T504034064AO | 81RM30 |
| T500054005AA | 37RA50 | T504037074AA | 82RM30 |
| T500054005AQ | 36Ra50 | T504037074AA | 81RM30 |
| T500058005AA | 72RA50 | T504044064AA | 82RM40 |
| T500058005Aa | 71Ra50 | T504044064Aa | 81RM40 |
| T500064005AA | 37RA60 | T504047074AA | $82 \mathrm{Rm40}$ |
| T500064005AO | 36Ra60 | T504047074AO | $81 \mathrm{Rm40}$ |
| T500068005AA | 72Ra60 | T504054064AA | 82RM50 |
| T500068005AO | 71RA60 | T504054054AA | 82RM50 |
| T500074005AA | 37Ra70 | T504057074AA | 82RM50 |
| T500074005AO | 36RA70 | T504057074AO | 81RM50 |
| T500078005AA | 72Ra70 | T504064064AA | 82RM60 |
| T500078005Aa | 71RA70 | T504064064AO | 81RM60 |
| T500084005AA | 37Rabo | T504067074AA | 82RM60 |
| T500084005Aa | 36Raso | T504067074AA | $81 \mathrm{RM60}$ |
| T500088005AA | 72RA80 | T504074064AA | ${ }^{\text {82RM70 }}$ |
| T500088005AO | 71Rabo | T504074064Aa | 81RM70 |
| T500094005AA | 37RA90 | T504077074AA | 82RM70 |
| T500094005AQ | 36Ra90 | T504077074AO | $81 \mathrm{RM70}$ |
| T500098005AA | 72RA90 | T504084064AA | 82RM80 |
| T500098005Aa | 71RA90 | T504484064AA | ${ }^{81 R \mathrm{RM} 80}$ |
| T500104005AA | 37Ra100 | T504087074AA | ${ }^{\text {82Rm80 }}$ |
| T500104005AO | 36Ra100 | T504087074AA | $81 \mathrm{Rm80}$ |
| T500108005AA | 72RA100 | T504094054AA | 82RL90 |
| T500108005Aa | 71RA100 | T504094054AO | 81RL90 |
| T500114005AA | 37RA110 | T504097044AA | 82RLB90 |
| T500114005AO | $36 R$ A110 | T504097044AO | 81 LL 890 |
| T500118005AA | 72RA110 | T504104054AA | 82RL100 |
| T500118005AO | 71RA110 | T504104054AO | 81 RL 100 |
| T500124005AA | 37RA120 | T504107044AA | 82RLB90 |
| T500124005AQ | 36RA120 | T504107044AO | $81 \mathrm{RL890}$ |
| T500128005AA | 72RA120 | T504114034AA | 37RA110T60 |
| T500128005AO | 71RA120 | T509114034AA | 36Ra110t60 |
| T500134005AA | $37 \mathrm{Ra130}$ | T504117034AA T504117034A | 72R8110760 |
| T500134005Aa | 36RA130 |  |  |
| T500138005AA | 72RA130 | T504124034AA | 37RA120760 |
| T500138005Aa | 71RA130 | T504124034AO | 36RA120760 |
| T500144005AA | 37 RA 140 | T504127034AA | 72R8120760 |
| T500144005AQ | 36RA140 | TS04127034Aa | ${ }_{\text {71RB120T60 }}$ |
| T500148005AA | 721A140 | T505054005AA | 37REH50 |
| T500148005AO | 71RA140 | T505054005AO | ${ }^{\text {36REH50 }}$ |
| T500154005AA | 37RA150 | T505058005AA | 72REH50 |
| T500154005AQ | 36RA150 | T505058005AO | 71REH50 |
| T500158005AA | 72RA150 | T505064005AA | 37REH60 |
| T500158005AQ | 71RA150 | T505064005Aa | 36REH60 |
| T50205×70 | 81RLb50 | T505068005AA | 72REH60 |
| T5020580 | 81 RLE50 | T505068005AO | 71REH60 |
| T50206×70 | $81 \mathrm{RLP60}$ | T50574005AA | 37REH70 |
| T5020680 T50208 | $81 \mathrm{RLLB60}$ | T505074005AO | 36REH70 72REH70 |
| T50208×70 | 81RLB80 | T505078005AA | 72REH70 |


| $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTED IR REPLACEMENT |
| :---: | :---: |
| T505078005AO | 71REH70 |
| T505084005AA | 37REH80 |
| T505084005AO | 36REH80 |
| T505088005AA | 72REH80 |
| T505088005AO | 71REH80 |
| T505094005AA | 37REH90 |
| T505094005AO | 36REH90 |
| T505098005AA | 72REH90 |
| T505098005AO | 71REM90 |
| T505104005AA | 37REH100 |
| T505104005AO | 36REH100 |
| T505108005A | 72REh100 |
| T505108005AO | 71REH100 |
| T507018064AA | 82RM10 |
| T507018064AO | $81 \mathrm{Rm10}$ |
| T507028064AA | 82RM20 |
| T507028064AO | 81RM20 |
| T507038064AA | 82Rм30 |
| T507038064AO | 81Rм30 |
| T507048064AA | 82Rm40 |
| T507048064AO | $81 \mathrm{RM40}$ |
| T507058064AA | 82Rm50 |
| T507058064Aa | 81 RM50 |
| T507068064AA | 82Rm60 |
| $\begin{array}{\|l\|l\|} \text { T507068064AA } \\ \hline \text { T507078064AA } \end{array}$ | 81RM60 |
| T507079064AO | 81RM70 |
| T507088064AA | 82Rм80 |
| T507088064AO | 81Rm80 |
| T507098064AA | 82AM90 |
| T507098064AO | 81RM90 |
| T507108064AA | 82RM100 |
| T507109064Aa | 81RMico |
| T507118044AA | 82RLB110 |
| T507118044AQ | 81 RLB110 |
| T507128044AA | 82RLB120 |
| T507128044AO | 81RLB120 |
| T5200113050N | 115 PA 10 |
| T520021305DN | 115 PA20 |
| T520031305DN | 115 PA 30 |
| T5200413050 | $115 \mathrm{PA40}$ |
| T5200513050N | $115 P A 50$ |
| T5200613050N | $115 \mathrm{PA60}$ |
| T520071305DN | 115 PA 70 |
| T520081305DN | $115 \mathrm{Pa80}$ |
| T5200913050N | $115 \mathrm{PA90}$ |
| T520101305DN | 115 PA 100 |
| T5201113050N | 115 PA 110 |
| T520121305DN | 115PA120 |
| T520131305DN | 115 PA 130 |
| T5201413050N | 115 PA140 |
| T520151305DN | 115 PA 150 |
| T527011364DN | $125 P$ PM10 |
| T527021364DN | $125 P$ AM20 |
| T5270313640N | 125PAM 30 |
| T5270413640N | 125 PAM40 |
| T527051364DN | $125 \mathrm{PAM50}$ |
| T5270613640N | 125PAM60 |
| T527071364DN | $125 P$ AM70 |
| T5270813640N | 125 PAM80 |
| T527091364DN | 125 PAM 90 |
| T5271013640N | $125 P A M 100$ |
| T5271113440N | $125 P$ ALB110 |
| T527121344DN | $125 \mathrm{PALB120}$ |
| T600011304BT | $151 \mathrm{RB10}$ |
| T6000115048T | 151 RA 10 |
| T60001 18048T | $175 R$ A10 |
| Y600021304BT | 151R820 |
| T6000215048T | 151RA20 |
| T600021804BT | 175RA20 |
| T600031304BT | 151RB30 |
| T600031504BT | 1518A30 |
| T6000318048T | 175RA30 |
| T600041304BT | 151R840 |
| T600041504BT | 151RA40 |


| COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTEDIR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| T600041804BT | 175RA40 | T620123004DN | 300PA120 | T707072044BY | 250RM70 | T7601330 | 304RA130 |
| T600051304BT | 151R850 | T6201313040~ | 175PA130 | T7070725448Y | 250RM70 | T7601430 | 304 RA 140 |
| T6000515048T | 151Ra50 | T620132004DN | 250Pa130 | T707082044BY | 250RM80 | T7601530 | 304 RA 150 |
| T600051804BT | 175RA50 | T620141304DN | $175 P$ P140 | T707082544BY | 250Rm80 | T7601630 | $304 \mathrm{RA160}$ |
| T600061304BT | 151R860 | T6201420040N | 250PA140 | T707092044BY | 250RM90 | T7601730 | 304RA170 |
| T600061504BT | 151RA60 | T620151304DN | $175 P A 150$ | T707092544BY | 250RM90 | T9200506 | 700 PK50 |
| T600061804BT | 175RA60 | T620152004DN | 250PA150 | T707102044BY | 250RM100 | T9200507 | 700PK50 |
| T600071304BT | $151 \mathrm{RB70}$ | T624041564DN | 250PAL40 | T707102544BY | 250RM100 | T9200508 | $850 P K 50$ |
| T600071504BT | 151RA70 | T624051564DN | 250 PAL 50 | T7071120448Y | 250RM110 | T9200509 | 850 PK50 |
| T600071804BT | $175 R 270$ | T624061564DN | 250PAL60 | T7071125448Y | 250RM110 | T9200510 | 1000 PK50 |
| T6000813048T | 151R880 | T624071554DN | 240 PAL70 | T7071220448Y | 250RM120 | T9200606 | $7009 \mathrm{P60}$ |
| T600081504BT | 151RA80 | T524081554DN | 240PAL80 | T707122544B | 250RM120 | T9200607 | 700PK60 |
| T600081804BT | 175RA80 | T6240915440N | 240PAL90S68 | T7200535 | 420 PB 50 | T9200608 | 850 PK 60 |
| T600091304BT | 151R890 | T624101544DN | 240PAL100568 | T7200545 | 470 PB50 | T9200609 | 850PK60 |
| T600091504BT | 151RA90 | T624111524DN | 240PAL110T62 | T7200555 | 550 P850 | T9200610 | 1000 PK60 |
| T600091804BT | 1758 A 90 | T624121524DN | 240PAL120T62 | T7200635 | $420 \mathrm{PB60}$ | T9200806 | 700PK80 |
| T600101304BT | 151RB100 | T62701156 | 250PAL10 | T7200645 | 470 PB 60 | T9200807 | 700PK80 |
| T600101504BT | 151RA100 | T62701158 | 250 Pam 10 | T7200655 | $550 \mathrm{PB60}$ | T9200808 | 850 PK 80 |
| T600101804BT | $175 R \mathrm{~A} 100$ | T62702156 | 250 PAL20 | T7200835 | 420Р880 | T9200809 | 850 PK80 |
| T600111304BT | 151 RB110 | T62702158 | 250 PAM20 | T7200845 | 470 PB80 | T9200810 | 1000 PK80 |
| T600111504BT | 151RA110 | T62703156 | 250 PAL30 | T7200855 | $550 \mathrm{PB80}$ | T9201006 | 700PK100 |
| T6001118048T | $175 R$ al10 | T62703158 | 250Pam 30 | T7201035 | 420 PB 100 | T9201007 | 700PK 100 |
| T6001213048T | 151RB120 | T62704156 | 250PAL40 | T7201045 | $470 \mathrm{PB100}$ | T9201008 | 850PK 100 |
| T600121504BT | 151RA120 | T62704158 | 250 PAM40 | 77201055 | 550 PB 100 | T9201009 | 850PK100 |
| T600121804BT | 175RA120 | T62705156 | 250PAL50 | T7201135 | 420 PB 110 | T9201010 | 1000 PK100 |
| T600131304BT | ${ }^{\text {151RB130 }}$ | T62705158 | 250PAM50 | T7201145 | 470 P8110 | 79201106 | 700PK110 |
| T600131504BT | 151RA130 | T62706156 | 250PAL60 | T7201155 | 550 PB 110 | T9201107 | 700PK110 |
| T600141304BT | 151RB140 | T62706158 | 250PAM60 | T7201235 | 420 PB 120 | T9201108 | 850PK110 |
| T600141504BT | 151RA140 | T6600530 | $303 R A 50$ | T7201245 | 470 PB 120 | T9201109 | 850PK110 |
| T600151304BT | 151RB150 | T6600630 | 303 BA 40 | T7201255 | 550 PB 120 | T9201110 | 1000 PK110 |
| T600151504BT | 151RA150 | T6600830 | 303RA80 | T7201335 | 420 PB 130 | T9201206 | 700PK120 |
| T6040115648T | 151RF10 | T6601030 | 303 FA 100 | T7201345 | 470 PB 130 | T9201207 | 700PK120 |
| T6040215648T | 151RF20 | T6601130 | 303RA110 | T7201355 | 550 PB 130 | T9201208 | 850PK120 |
| T604031564BT | 151RF30 | T6601230 | $303 \mathrm{RA120}$ | T7201435 | 420 PB 140 | T9201209 | 850PK120 |
| T604041364BT | 151RF40 | T6601330 | 303RA130 | T7201445 | 470 PB140 | T9201210 | 1000PK120 |
| T604041564BT | 151RF40 | T6601430 | $303 \mathrm{RA140}$ | T7201455 | 550 PB 140 | T9201306 | 700PK130 |
| T604051364BT | 151RF50 | T6601530 | 303 RA 150 | 77201535 | $420 \mathrm{PB150}$ | T9201307 | 700PK130 |
| T604051564BT | 151RF50 | T6800530 | $303 \mathrm{RB50}$ | T7201545 | 470 PB 150 | T9201308 | 850PK130 |
| T6040613648T | 151RF60 | T680C630 | 303R860 | T7201555 | $550 \mathrm{PB150}$ | T9201309 | 850PK130 |
| T604061564BT | 151RF60 | T6800830 | $303 \mathrm{RB80}$ | T7201635 | $420 \mathrm{PB160}$ | T9201406 | 700PK140 |
| T604071354BT | 151RL70 | T6801030 | $303 \mathrm{RB100}$ | 7201645 | 470 PB160 | T9201407 | 700PK140 |
| T604081354BT | 151RL80 | T6801130 | $303 \mathrm{RB110}$ | T7201655 | $550 \mathrm{PB160}$ | T9201408 | 850PK140 |
| T6040913448T. | 151RL90S68 | T6801230 | $303 \mathrm{RB120}$ | 77201735 | $420 \mathrm{PB170}$ | T9201409 | 850PK140 |
| T604101344BT | 151RL100S68 | T6801330 | $303 \mathrm{RB130}$ | 77201745 | 470 PB 170 | T9201506 | 700PK150 |
| T620051304DN | 175 PA50 | T6801430 | 303RB140 | T7201755 | $550 \mathrm{PB170}$ | T9201507 | 700PK150 |
| T620052004DN | $250 P$ A50 | T6801530 | $303 \mathrm{RB150}$ | T727012574DN | 550PBQ10 | T9201508 | 850PK150 |
| T6200530 | 300PA50 | T7000525 | $250 \mathrm{RA50}$ | T727013574DN | 550PB010 | T9201509 | 850PK150 |
| T620053004DN | 300PA50 | T7000530 | 300RA50 | T7270225740N | 550РBO20 | T9201606 | 700PK160 |
| T620061304DN | $175 \mathrm{PA60}$ | T7000535 | 350RA50 | T7270235740N | $550 \mathrm{~PB} \mathbf{2 0}$ | T9201607 | 700PK160 |
| T620062004DN | $2508 \mathrm{Pa60}$ | T7000625 | 250 RAGO | T7270325740N | 550PB030 | T9201608 | 850PK160 |
| T6200630 | $3008 \mathrm{Pa60}$ | T7000630 | 300RA60 | T727033574DN | 550PB030 | T9201609 | 850PK160 |
| T620063004DN | 300PA60 | T7000635 | 350RA60 | T7270425740N | 550PBO40 | TC106A1 | IR106A1 |
| T6200713040N | $175 \mathrm{Pa70}$ | T7000825 | 250 RA 0 | T727043574DN | 550PB040 | TC10681 | \|R10681 |
| T620072004DN | 250PA70 | T7000830 | 300 RABO | T7270525740N | 555PBO50 | TC106C1 | IR106C1 |
| T6200730 | 300PA70 | T7000835 | 350 RA 80 | T727053574DN | 550PBO50 | TC106D1 | \|R106D1 |
| T620073004DN | 3008470 | T7001025 | $250 \mathrm{RA100}$ | T727062574DN | 550 PB660 | TC106F1 | \|R106F1 |
| T6200813040N | 175 PA80 | T7001030 | 300RA100 | T727063574DN | 550P8860 | TC10601 | \|R10601 |
| T620082004DN | $250 \mathrm{Pa80}$ | T7001035 | 350RA100 | T727072544DN | 420 РВм70 | TC106U1 | IR106U1 |
| ${ }^{T 6200830}$ | 300P A80 | T7001125 | 250 RA110 | T727073544DN | 420 РВМ70 |  |  |
| T6200930040N | 300PA80 | T7001130 | 300RA110 | T727082544DN | 420 PBM80 |  |  |
| T620091304DN | 175 PA90 | T7001135 | 350RA110 | T727083544DN | 420 PBM80 |  |  |
| T620092004DN | $250 \mathrm{Pa90}$ | T7001225 | 250RA120 | T727092544DN | 420РВМ90 |  |  |
| T6200930 | $300 \mathrm{Pa90}$ | 77001230 | 300RA120 | T7270935440N | 420РВМ90 |  |  |
| T620093004DN | 300 A990 | T7001235 | 350 RA 120 | T7271025440N | 420 PBM100 | $3 \mathrm{RC10}$ | 3RCIOA |
| T620101304DN | 175PA100 | T7001325 | 250RA130 | T727103544DN | 4208pm100 | $3 \mathrm{RC20}$ | 3RC20A |
| T6201020040N | 250 PA100 | T7001330 | 300RA130 | T7271125440N | 420 PBM110 | 3RC30 | 3RC30A |
| T6201030 | 300PA100 | T7001335 | 350 RA 130 | T7271135440N | 420Р8M110 | $3 \mathrm{RC40}$ | 3 RC 40 A |
| T6201030040N | 300Pa100 | T7001425 | 250RA140 | T727122544DN | 420Р8М 120 | 3RC50 | 3RC50A |
| T6201113040N | 175 PA 110 | T7001430 | 300RA140 | T7271235440N | 420 PBM120 | $3 \mathrm{RC60}$ | 3RC60A |
| T620112004DN | 250PA110 | T7001435 | 350RA140 | T7600530 | 304RA50 | 5RC10 | 5RCIOA |
| T6201130 | 300PA110 | T7001525 | 250RA150 | T7600630 | 304RA60 | 5RC20 | 5RC20A |
| T620113004DN | 300PA110 | T7001530 | 300RA150 | T7600830 | 304RABO | 5RC30 | 5RC30A |
| T6201213040N | 175PA120 | T7001535 | 350 RA 150 | T7601030 | 304RA100 | 5RC40 | 5RC40A |
| T620122004DN | 250 PA 120 | T7001630 | 300RA160 | T7601130 | 304RA110 | 5RC50 | $58 \mathrm{C50A}$ |
| T6201230 | 300PA120 | T7001730 | 300RA170 | T7601230 | 304RA120 | 5RC60 | 5RC60A |


| COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT | $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTEDIR REPLACEMENT | $\begin{aligned} & \text { COMPE TITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTEDIR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 10RC10 | 10RC10A | 36RE50 | 36RA50 | 70C40F | 72RCAOA | 72RE130 | 72RA130 |
| 10RC20 | 10RC20A | 36RE60 | $36 \mathrm{RAG0}$ | 70050 | 71RC50A | 72REA50 | 72RA50 |
| 1 ORC30 | 10RC30A | 36RE80 | 36 Ra 80 | 70C50F | 72RC50A | 72REA60 | 72RA60 |
| $10 \mathrm{CC40}$ | 10RC40A | $36 \mathrm{RE1} 100$ | $36 R A 100$ | $70 ¢ 60$ | 71RC60A | 72REA80 | T2RA80 |
| $10 \mathrm{RC5} 0$ | 10RC50A | 36RE110 | $36 R A 110$ | 70C60F | 72RC60A | 72REA100 | 72 RA100 |
| $10 \mathrm{RC60}$ | $10 \mathrm{RC60A}$ | $36 \mathrm{RE120}$ | $36 R A 120$ | 70 c80 | 71RC80A | 72REA110 | $72 \mathrm{RA110}$ |
| $10 \mathrm{RCB0}$ | 10RC80A | 36RE130 | 36 RA 130 | 70CB0F | 72RC80A | 72REA 120 | 72RA120 |
| 10 Cc 100 | 10RCLIOAA | 37RCF5A | 82RM5 | 70 Cl 100 | 71RA100 | 72REA 130 | 72 RA 130 |
| $10 \mathrm{RC110}$ | 10RCl10A | 37RCF10A | 82RM10 | 70C100F | $72 \mathrm{RA100}$ | $72 \mathrm{REB50}$ | 72 RB50 |
| 10RC120 | 10RC120A | 37RCF15A | 82RM15 | $70 \mathrm{Cl110}$ | 71 RA110 | 72REB60 | 72RB60 |
| 10RCF10A | IR140A | 37RCF20A | 82 RM 20 | 70C110F | 72RA110 | 72REB80 | 72RB80 |
| 10RCF20A | 1R1408 | 37RCF25A | 82RM25 | 70C120 | 71 RA120 | 72REB100 | $72 \mathrm{RB100}$ |
| 10RCF30A | IR140C | 37RCF30A | 82 Rm 30 | 70C120F | $72 \mathrm{RA120}$ | 72REB110 | $72 \mathrm{RB110}$ |
| 10RCF40A | 1R1400 | 377CF40A | 82RM40 | 70C130 | 71RA130 | 72REB120 | $72 \mathrm{RB120}$ |
| 10RCF50A | IR140E | 37RCF50A | $82 \mathrm{RM50}$ | 70C130F | $72 \mathrm{RA130}$ | 100C10 | 101 RCL 10 |
| $10 \mathrm{RCF60A}$ | IR140M | 377CF60A | 82RM60 | 70 Cl 40 | 71RA140 | 100C20 | 101 RC 20 |
| $16 \mathrm{CO25}$ | 22RA2 | 37RCF70A | $82 \mathrm{Rm70}$ | 70C140F | 72RA140 | 100C40 | $101 \mathrm{RC40}$ |
| $16 \mathrm{CO5O}$ | $22 \mathrm{RA5}$ | 37RCF80A | $82 \mathrm{RM80}$ | 70 C 150 | $71 \mathrm{RA150}$ | 130060 | 101 RC60 |
| $16 \mathrm{Cl10}$ | 22 RA 10 | $37 \mathrm{RE50}$ | $37 \mathrm{RA50}$ | 70C150F | $72 \mathrm{RA150}$ | 100480 | 101 RC80 |
| 16 C 20 | 22 RA 20 | 37RE60 | 37RA60 | $70{ }^{\text {c }} 160$ | 71 RA160 | 1000100 | 101 RA 100 |
| 16 c30 | 22RA30 | 37RE80 | 37 RABO | 70C160F | 72RA160 | 100C110 | 101 RA110 |
| $16 \mathrm{C40}$ | 22RA40 | 37 RE100 | $37 \mathrm{RA100}$ | 71RCF10 | $81 \mathrm{RM10}$ | 1000120 | 101RA120 |
| 16 C 50 | 22RA50 | $37 \mathrm{RE1} 10$ | $37 \mathrm{RA110}$ | 71RCF20 | 81RM20 | 100C140 | 101RA140 |
| $16 \mathrm{C60}$ | 22RA60 | $37 \mathrm{RE1} 20$ | 37 RA 120 | 71RCF30 | 81Rm30 | 100C160 | 101 RA 160 |
| 16 C 80 | 16 RC80A | 37RE130 | 37 RA130 | 71RCF40 | 81 RM40 | 101 RE50 | 101 RA50 |
| 16 Cl 100 | 16RC100A | 40coso | $40 \mathrm{RCS5}$ | 71RCF50 | 81RM50 | 101 RE60 | 101 RA60 |
| 16 C 110 | 16RC110A | 40 Cl 10 | 40 RCS 10 | 71 RCF60 | 81RM60 | 101RE80 | 101 RA80 |
| 16 C 120 | 16RCl20a | 40C20 | 40 RCS 20 | 71RCG5 | 81 RM5 | 101RE100 | 101 RA 100 |
| $16 \mathrm{RC10}$ | 16RC10A | 40.30 | 40RCS30 | 71RCG10 | 81 RM10 | 101RE110 | 101 RA110 |
| 16 RC 20 | 16RC20A | $40 \mathrm{C40}$ | $40 \mathrm{RCS40}$ | 71RCG15 | 81 RM15 | 101RE120 | 101RA120 |
| 16RC30 | 16 RC30A | $40 \mathrm{C50}$ | $40 \mathrm{RCS50}$ | 71RCG20 | 81 Rm 20 | 125 PL 10 | $125 \mathrm{PAL10}$ |
| $16 \mathrm{RC40}$ | $16 \mathrm{RC40A}$ | $40 \mathrm{C60}$ | $40 \mathrm{RCS60}$ | 71RCG25 | 81RM25 | 125 PL 20 | 125 PAL20 |
| $16 \mathrm{RC50}$ | 16RC50A | $40 \mathrm{C80}$ | $40 \mathrm{RCS80}$ | $71 R C G 30$ | 81 RM30 | $125 \mathrm{PL30}$ | 125 PAL30 |
| $16 \mathrm{RC60}$ | 16RC60A | 40C100 | 40RCS 100 | 71RCG40 | 81 RM40 | $125 P$ L40 | $125 \mathrm{PAL40}$ |
| $16 \mathrm{RC80}$ | 16RC80A | 40 C 110 | 40 RCS 110 | $71 \mathrm{RCG50}$ | 81 RM50 | $125 \mathrm{PL50}$ | 125 PAL50 |
| $16 \mathrm{RCl00}$ | 16RC100A | 40 Cl 20 | 40RCS120 | 71RCG60 | 81 MM60 | 125 P L60 | 125 PAL60 |
| $16 \mathrm{RC110}$ | 16RC110A | $55 \mathrm{Co50}$ | $36 \mathrm{RC5A}$ | 71RE60 | 71RA60 | 125 PL L80 | $125 \mathrm{PALB0}$ |
| $16 \mathrm{RC120}$ | 16RC120A | ${ }^{55 C 050 F}$ | 37 RCSA | 71 RE70 | 71 RA 70 | 125 PL 100 | 125PALI00 |
| 16 RCF 10 | 1R140A | ${ }_{55510}^{55 C 10 F}$ | $36 \mathrm{RC10A}$ | $71 \mathrm{RE8O}$ | $71 R A 80$ | 125 PL 120 | 125 PALI 120 |
| 16RCF20 | 121408 | 55 Cl 10 F | 37RC10A | 71RE90 | 71 Rago | 125PM10 | 125 PAM10 |
| 16RCF30 | 18140C | ${ }^{55 c 20}$ | ${ }^{36 R C 20 A}$ | 71RE100 | 71 RA100 | 125 PM 20 | 125PAM20 |
| 16 RCF 40 | $1 \mathrm{R1400}$ | ${ }^{55 C 20 F}$ | $37 \mathrm{RC20A}$ | 71 RE110 | 71 RA110 | $125 P$ M 30 | $125 \mathrm{PAM30}$ |
| $16 \mathrm{RCF50}$ | IR140E | ${ }^{55530}$ | $36 \mathrm{RC30A}$ | 71 RE120 | $71 \mathrm{RA120}$ | 125 Pm 50 | 125 PAM50 |
| $16 \mathrm{RCF60}$ | IR140M | 55C30F | $37 \mathrm{RC3} 30 \mathrm{~A}$ | 71 RE130 | $71 \mathrm{RA130}$ | 125PM60 | 125 PAM60 |
| 18RC10 | $16 \mathrm{RC10A}$ | 55C40 | $36 \mathrm{RC40A}$ | 71REA50 | 71RA50 | 125 PM 80 | 125 PAM 80 |
| $18 \mathrm{RC20}$ | 16 RC20A | $555 \mathrm{C40F}$ | $37 \mathrm{RC40A}$ | 71REA60 | $71 \mathrm{Ra60}$ | 125 PM 100 | 125PAM100 |
| 18 RC 30 | 16 RC 30 A | ${ }^{55550}$ | $36 \mathrm{RC50A}$ | 71REA8O | 71 RABO | 140PL10 | 140 PAL 10 |
| $18 \mathrm{RC40}$ | 16RC40A | ${ }^{55 C 50 F}$ | $37 \mathrm{RC50A}$ | 71REA100 | $71 \mathrm{RA100}$ | 140PL20 | 140PAL20 |
| $18 \mathrm{RC50}$ | 16RC50A | 55c60 | 36RC60A | 71 REA110 | 71 RA110 | 140PL30 | 140PAL30 |
| $18 \mathrm{RC60}$ | 16RC60A | 55560 F | $37 \mathrm{RC60A}$ | 71REA120 | $71 \mathrm{RA120}$ | 140 PL 40 | 140 PAL 40 |
| $18 \mathrm{RCB0}$ | $16 \mathrm{RCB0A}$ | 55680 | 367 CB 80 A | 71REA130 | 71RA130 | 140 PL 50 | $140 \mathrm{PAL50}$ |
| 18RC100 | 16RC100A | 55C80F | 37RC80A | 71 REB50 | 71RB50 | 140 LL60 | 140PAL60 |
| $23 \mathrm{CO25}$ | 22 RA 2 | 55 C 100 | $36 R$ A 100 | 71REB60 | 71Rb60 | 140PM10 | 140 PAM10 |
| $23 \mathrm{CO5O}$ | $22 \mathrm{Ra5}$ | 55C100F | $37 \mathrm{RA100}$ | 71REB80 | 71 Rbso | 140PM20 | 140PAM20 |
| 23 Cl 10 | 22 RA 10 | ${ }_{55 C 110}$ | 36 RA 110 | 71 REB100 | $71 \mathrm{RB100}$ | 140PM30 | 140 PAM 30 |
| 23 C 20 | 22 RA 20 | 55C110F | 37 RA 110 | 71REB110 | $71 \mathrm{RB110}$ | 140PM40 | 140 PAM 40 |
| 23630 | 22 RA 30 | ${ }^{55 C 120}$ | 36 RA 120 | 71REB120 | $71 \mathrm{RB120}$ | 140PM50 | 140PAM50 |
| ${ }^{23} 340$ | $22 \mathrm{RA40}$ | $55 \mathrm{Cl20F}$ | $37 \mathrm{RA120}$ | 72RCF5A | 82RM5 | 140PM60 | 140PAM60 |
| 23 C 50 | $22 \mathrm{RA50}$ | 55C130 | 36RA130 | 72RCF10A | 82RM10 | 150 Cl 10 | 151RCIOA |
| ${ }^{23 C 60}$ | $22 \mathrm{RA60}$ | ${ }^{55 C 130 F}$ | 37 RA 130 | 72RCF15A | 82RM15 | 150 C 20 | 151RC20A |
| 233880 | 16RCB0A | ${ }_{5}^{55 C 140}$ | 36 RA 140 | 72RCF20A | $82 \mathrm{RM20}$ | $150 C 40$ | 151RC40A |
| 23 Cl 100 | 16RC100A | 55C140F | $37 \mathrm{RA140}$ | 72RCF25A | 82 RM 25 | $150 \mathrm{C60}$ | 151RC60A |
| $23 \mathrm{Cl110}$ | 16RCIIOA | ${ }_{55 C 150}$ | $36 R A 150$ | 72RCF30A | 82 Rm 30 | 150180 | 151RC80A |
| ${ }_{36 \text { 23C120 }}^{23}$ | 16RC120A | ${ }^{55 C 150 F}$ | $37 \mathrm{RA150}$ | 72RCF40A | 82RM40 | 1500100 | 151RA100 |
| 3 36RCF5A | 81RM5 | 55C160 | 36 RA 160 | 72RCF50A | 82RM50 | $150 C 110$ | 151RA110 |
| 36RCF15A | 81RM15 | 55C160F 700050 | ${ }_{\text {71RC5A }}$ | 72RCF60A 72RCF70A | 82RM60 82RM70 | 150 C 120 | 151RA120 |
| 36RCF20A | $81 \mathrm{RM20}$ | 70C050F | $72 \mathrm{RC5A}$ | 72RCF80A | $82 \mathrm{Rm80}$ | $151 \mathrm{C160}$ | 151 RA160 |
| 36RCF25A | 81RM25 | $70 \mathrm{Cl0}$ | 71RC10A | $72 \mathrm{RE60}$ | 72RA60 | $150 \mathrm{RC10}$ | 151 RC10 |
| 36RCF30A | 81 RM30 | 70C10F | 72RC10A | 72RE70 | 72RA70 | 150RC20 | 151 RC 20 |
| 36RCF40A | 81 RM40 | 70020 | $71 \mathrm{RCL20A}$ | 72RE80 | $72 \mathrm{RA80}$ | 150RC30 | $151 \mathrm{RC3} 30$ |
| 36RCF50A | 81 RM50 | 700620F | 72RC20A | 72RE90 | 72RA90 | 150RC40 | $151 \mathrm{RC40}$ |
| 36RCF60A | 81 RM60 | 70030 | $71 \mathrm{RC30A}$ | 72RE100 | 72 RA 100 | 150RC50 | 151RC50 |
| $36 \mathrm{RCFF70A}$ 36RCF80A | 81 RM 70 81 RM80 | 70C30F 70040 | 72RC30A $71 \mathrm{RC40A}$ | 72RE110 72RE120 | 72RA110 | 150RC60 | $151 \mathrm{RC60}$ |
| 36RCF80A | 81RM80 | 70040 | 71RC40A | 72RE120 | 72RA120 | 150RC70 | 151RC70 |



| COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT |
| :---: | :---: |
| 254ZK | 71RA150 |
| 254ZM | 71RA160 |
| 260 K | $175 R$ A50 |
| 260 M | $175 R$ A60 |
| 260P | 175 RA 70 |
| 2605 | 1758 PA 80 |
| 260 V | $175 R$ A90 |
| $260 z$ | 175 RA100 |
| 2602B | 175 RA110 |
| 260ZD | 175RA120 |
| 261 K | 151 RA50 |
| 261 M | 151RA60 |
| 2615 | 151 RA80 |
| 2612 | 151 RA100 |
| 26128 | 151 RA110 |
| 2612 D | 151 RA120 |
| 2612 F | 151RA130 |
| 2612 H | 151 RA140 |
| 2612K | 151 Ra150 |
| 261ZM | 151 RA160 |
| 262 K | $175 P A 50$ |
| 262 M | 175 PA60 |
| 2625 | $175 \mathrm{PA80}$ |
| 2622 | 175 PA 100 |
| 26278 | 175 PA110 |
| 2622 D | 175 PA120 |
| 2622F | 175 PA130 |
| 2622 H | 175 PA140 |
| 2622 K | 175PA150 |
| 262ZM | 175 PA160 |
| 263 K | 115 PA 50 |
| 263 M | $115 \mathrm{PA60}$ |
| 2635 | $115 \mathrm{PA80}$ |
| 2632 | $115 P A 100$ |
| 26328 | 115 PA110 |
| 2632 D | 115 PA120 |
| 2632 F | 115 PA 130 |
| 2632 H | 115 PA 140 |
| 263ZK | 115 PA150 |
| 2632M | 115 PA 160 |
| 270 K | 350RA50 |
| 270M | 350RA60 |
| 2708 | 350RABO |
| 2702 | 350 RA 100 |
| 270zB | 350 RA 110 |
| 2702 D | $350 \mathrm{RA120}$ |
| 270ZF | 350RA130 |
| 270ZH | 350RA140 |
| 2702K | 350RA150 |
| 270ZM | 350 RA160 |
| 270zP | 350RA170 |
| 270-Y30860 | 300RA60 |
| 270-Y30870 | 300RA70 |
| 270-Y30880 | 300RA80 |
| 270-Y30890 | 300 RA 90 |
| $270 . Y 30 \mathrm{Cl} 10$ | 300 RA 100 |
| 270-Y30C11 | 300RA110 |
| 270-Y30C12 | 300RA120. |
| 270-Y30C13 | 300RA130 |
| 270-Y30C14 | 300RA140 |
| 270-Y3015 | 300RA150 |
| 270-Y30C16 | 300RA160 |
| $270 \cdot \mathrm{Y} 30 \mathrm{C} 17$ | 300 RA 170 |
| 272 K | 300 PA50 |
| 272M | 3009 A60 |
| ${ }^{272 \mathrm{~S}}$ | 300 PAB0 |
| 2722 | 300PA100 |
| 27228 | 300 PA 110 |
| 2727 D | 300 PA 120 |
| 273k | $175 P A 50$ |
| 273 M | 175 PA60 |
| 2738 | $175 \mathrm{PA80}$ |
| 2732 | 175 PA100 |
| 27328 | $175 P$ A110 |
| 2732 D | 175 PA 120 |


| COMPETITIVE PART No. | SUGGESTEDIR REPLACEMENT |
| :---: | :---: |
| 2732F | 175PA130 |
| 273ZH | 175 PA140 |
| 273zk | 175 PA150 |
| 2732M | 175 PA160 |
| 276K | 300RA50 |
| 276M | $300 \mathrm{RA60}$ |
| 2765 | 300RA80 |
| 2762 | 300RA100 |
| 27628 | $300 \mathrm{RA110}$ |
| 276ZD | 300RA120 |
| 276ZF | 300RA130 |
| 2762H | 300RA140 |
| 2762 K | 300RA150 |
| 2762M | 300RA160 |
| 276ZP | 300RA170 |
| 278K | $303 \mathrm{RB5C}$ |
| 278M | $303 \mathrm{RB60}$ |
| 278P | $303 \mathrm{RB70}$ |
| 2788 | зозRв8о |
| 278 V | $303 \mathrm{RB90}$ |
| 2782 | $303 \mathrm{RB100}$ |
| 27828 | 303RB110 |
| 2782 D | $303 \mathrm{RB120}$ |
| 282 K | $550 \mathrm{PB50}$ |
| 282M | $550 \mathrm{PB60}$ |
| 2828 | 550 P880 |
| 2822 | 550PB100 |
| 28278 | 550PB110 |
| 28270 | 550PB120 |
| 2822 F | $550 \mathrm{PB130}$ |
| 2822 H | 550P8140 |
| 2822k | 550PB150 |
| 282ZM | $550 \mathrm{PB160}$ |
| 2822P | 550PB170 |
| 282-Y40860 | $420 \mathrm{PB60}$ |
| 282-Y40870 | 420 PB 70 |
| 282-Y40880 | $420 \mathrm{PB80}$ |
| ${ }^{282-Y 40890}$ | $420 \mathrm{PB90}$ |
| 282-Y40C10 | 420 PB 1100 |
| 282-Y40C11 | 420 PB 110 |
| 282-Y40C12 | 420 PB 120 |
| 282-Y40C13 | 420 PB 130 |
| $282-\mathrm{Y} 40 \mathrm{C} 14$ | $420 \mathrm{PB140}$ |
| 282-Y40C15 | $420 \mathrm{PB150}$ |
| 282-Y40C16 | 420 PB 160 |
| 282 - 400 C 17 | $420 \mathrm{PB170}$ |
| 283 H | $470 \mathrm{PB40}$ |
| 283k | 470 PB50 |
| 283M | $470 \mathrm{PB60}$ |
| 2835 | 470 PB80 |
| 2832 | 470 PB100 |
| 28378 | $470 \mathrm{PB110}$ |
| 2832 D | 470 PB120 |
| 2832 F | 470PB130 |
| 2832 H | 470 PB140 |
| 2832k | $470 \mathrm{PB150}$ |
| 283ZM | 470PB160 |
| 283ZP | $470 \mathrm{PB170}$ |
| 286K | 304RA50 |
| 286 M | 304RA60 |
| ${ }^{2865}$ | $304 \mathrm{RAB0}$ |
| 2862 | 304RA100 |
| 28678 | 304RA110 304 A |
| 2862F | 304RA130 |
| 286ZH | 304RA140 |
| 286zK | 304Ra150 |
| 286ZM | 304RA160 |
| 2862 P | 304 RA 170 |
| 286-Y30860 | $304 \mathrm{RA60}$ |
| 286-Y30870 | 304 RA 70 |
| 286-Y30880 | 304 RABO |
| 286-Y30890 | $304 \mathrm{RA90}$ |
| 286-Y30C10 | 304RA100 |
| 286-Y30C11 | 304RA110 |


| $\begin{aligned} & \text { COMPETITIVE } \\ & \text { PART NO. } \end{aligned}$ | SUGGESTEDIR REPLACEMENT |
| :---: | :---: |
| 286-Y30C12 | 304RA120 |
| 286-Y30C13 | 304RA130 |
| 286-Y30C14 | $304 \mathrm{RA140}$ |
| 286-Y30C15 | 304RA150 |
| 286-Y30C16 | 304RA160 |
| 286-Y30C17 | $304 \mathrm{RA170}$ |
| 2888 | $303 \mathrm{RA10}$ |
| 2880 | 303 RA 20 |
| 288F | $303 \mathrm{RA30}$ |
| 288 H | 303 RA 40 |
| 288K | $303 \mathrm{RA50}$ |
| 288M | $303 \mathrm{BA60}$ |
| 288P | 303 BA 40 |
| 2885 | $303 \mathrm{BAB0}$ |
| 288 V | $303 \mathrm{RA90}$ |
| 2882 | 303RA100 |
| 28828 | $303 \mathrm{RA110}$ |
| 2882 D | 303RA120 |
| 2882F | 303RA130 |
| 2882 H | 303 RA 140 |
| 2882 K | 303RA150 |
| 2882M | 303RA160 |
| 301c10 | $300 \mathrm{PAC10}$ |
| $301 \mathrm{C20}$ | $300 \mathrm{PAC20}$ |
| 301c30 | 300PAC30 |
| $301 \mathrm{C40}$ | 300PAC40 |
| $301 \mathrm{C50}$ | $300 \mathrm{PAC50}$ |
| $301 \mathrm{c60}$ | $300 \mathrm{PAC60}$ |
| 301 c80 | $300 \mathrm{PA80}$ |
| 3016100 | 300 PA100 |
| 3016110 | 300 PA110 |
| $301 \mathrm{Cl20}$ | 300 PA 120 |
| 420PL60 | $420 \mathrm{PBL60}$ |
| $420 \mathrm{PL80}$ | $420 \mathrm{PbL80}$ |
| 420 PL100 | 420 PbL 100 |
| 420 PL110 | $420 \mathrm{PBL110}$ |
| 420PL120 | 420PBL120 |
| 420PM60 | 420 P вм 60 |
| 420PM80 | 420Рвм 80 |
| 420PM100 | 420РВМ100 |
| 420PM110 | 420 PBM110 |
| 420PM120 | 420 РВм120 |
| $470 \mathrm{PA50}$ | $550 \mathrm{PB50}$ |
| $470 \mathrm{Pa60}$ | 5509860 |
| 470 PA80 | 5509880 |
| 470 PA100 | 550P8100 |
| 470PA110 | 550PB110 |
| 470 PA120 | ${ }^{550 P 8120}$ |
| 470PA130 | 550PB130 |
| 470PA140 | 550P8140 |
| 470PA150 | 550P8150 |
| 470PA160 | 550P6160 |
| 470 PA 170 | 550PB170 |
| 700PA50 | 700PK50 |
| $700 \mathrm{Pa60}$ | $700 \mathrm{PK60}$ |
| 700P A80 | 700PK80 |
| 700Pa100 | 700PK 100 |
| 700PA110 | 700PK110 |
| 700pal20 | 700PK120 |
| 700Pal30 | 700PK130 |
| 700pal40 | 700PK140 |
| 700PA150 | 700PK150 |
| 700PK160 | 700PK160 |
| 700PK170 | 700PK170 |
| 809B | 71RCIOA |
| 809D | 71RC20A |
| 809F | 71RC30A |
| 809H | $71 \mathrm{RC40A}$ |
| 809 K | $71 \mathrm{RC50a}$ |
| 809M | 71RC60A |
| 8095 | $71 \mathrm{RC80A}$ |
| 850PA50 | 850 PK 50 |
| 850P A60 | 850 PK60 |
| 850PAB0 850 A A100 | ${ }^{\text {850PK } 80}$ |
| 850PA100 | 850PA100 |


| COMPETITIVE PART NO. | SUGGESTEDIR REPLACEMENT |
| :---: | :---: |
| 850PA110 | 850PK110 |
| 850PA120 | 850PK120 |
| 850PA130 | 850PK130 |
| 850PA140 | 850PK140 |
| 850PA150 | 850PK150 |
| 850PA160 | 850PK160 |
| 850PA170 | 850PK170 |
| 1000PA50 | 1000 PK50 |
| 1000Pa60 | 1000 PK60 |
| 1000 PA80 | 1000 PK80 |
| 1000 PA100 | 1000 PK 100 |
| 1000 PA 110 | 1000 PK 110 |
| 1000PA120 | 1000PK120 |
| 1000 PA 130 | 1000PK130 |
| 1000 Pa 140 | 1000PK140 |
| 1000PA150 | 1000 PK 150 |
| 1000PA160 | 1000 PK 160 |
| $1000 \mathrm{PA170}$ | 1000 PK 170 |
| 1600 PA50 | 1600 PN50 |
| 1600PA60 | 1600 PN60 |
| 1600PA80 | 1600 PNB0 |
| 1600 PA 100 | 1600 PN100 |
| 1600 PA 110 | 1600 PN 110 |
| 1600PA120 | 1600PN120 |
| 2181 K | 151RF50 |
| 2181 M | 151 RF60 |
| 2182 K | 151 RL50 |
| 2182M | 151 RL60 |
| 2182 S | $151 \mathrm{RL80}$ |
| 21827 | 151 RL 100 |
| 21827B | 151 RL 110 |
| 21822 D | 151RL120 |
| 2191 K | 91RM50 |
| 2191M | $91 \mathrm{RM60}$ |
| 2192K | 81 RM50 |
| 2192M | 81 RM60 |
| 2201 K | 250RM50 |
| 2201 M | ${ }^{250 R M 60}$ |
| 22015 | ${ }^{2508 M 80}$ |
| 22012 | 250RM100 |
| 220178 | $250 \mathrm{RM110}$ |
| 2201 zD | 2508 M 120 |
| 2202 K | 250RM50 |
| 2202 M | 250RM60 |
| 22025 | $250 \mathrm{RM80}$ |
| 22022 | 250RM100 |
| 220278 | $250 \mathrm{RM110}$ |
| 220230 | 250RM120 |
| ${ }^{2248 \mathrm{~K}}$ | $3038 B 550$ |
| 2248M | $303 \mathrm{RB60}$ |
| 22485 | $303 \mathrm{RB80}$ |
| 22482 | $303 \mathrm{RB100}$ |
| 224878 | $303 \mathrm{RB110}$ |
| 22482 D | $303 \mathrm{RB120}$ |
| 2248ZF | $303 \mathrm{RB130}$ |
| 2248ZH | $303 \mathrm{RB140}$ |
| 22482 K | $303 \mathrm{RB150}$ |
| 2248ZM | $303 \mathrm{RB160}$ |
| 2248ZP | $303 \mathrm{RB170}$ |
| 2451 K | 81 RM50 |
| 2451M | 81 Rm 60 |
| 24515 | $81 \mathrm{Rm80}$ |
| 2451 Z | 81 RMM100 |
| 2452 K | 81 RM50 |
| 2452M | 81 RM60 |
| 2452 S | $81 \mathrm{Rm80}$ |
| 24522 | 81 RM100 |
| 2505 K | 71REH50 |
| 2505M | 71REH60 |
| 2505P | 71 REH70 |
| 25055 | 71REH80 |
| 2505 V | 71REH90 |
| 25052 | 71REH100 |
| 2515 K | 36REH50 |
| 2515M | 36REH60 |


| COMPETITIVE <br> PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT | COMPETITIVE PART NO. | SUGGESTED IR REPLACEMENT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 2515 P | 36REH70 | 25412 | 81 RM100 | 2543D | 91 RM 20 | 40743 | ${ }^{\text {IR300 }}$ |
| 2515 S | $36 \mathrm{REH80}$ | 2542A | 81RM5 | 2543F | 91RM30 | 40744 | 10RC60A |
| 2515 V | 36REH90 | 25428 | $81 \mathrm{RM10}$ | 2543H | 91RM40 | 40749 | IR32A |
| 25152 | 36REH100 | 2542 D | 81RM20 | 2543K | 91RM50 | 40750 | ${ }_{18328}$ |
| 2541 A | 81 RM5 | 2542F | 81 RM30 | 2543M | $91 \mathrm{RM60}$ | 40751 | IR32D |
| 25418 | $81 \mathrm{RM10}$ | 2542 H | 81RM40 | 40735 | 10RC60A | 40752 | 10RC60A |
| 25410 | 81RM20 | 2542K | 81 RM50 | 40737 | IR32A | 40753 | IR30A |
| 2541F | 81 Rмз ${ }^{\text {a }}$ | 2542M | 81 RM60 | 40738 | IR328 | 40754 | IR308 |
| 2541H | 81 RM40 | 2542S | 81 RM80 | 40739 | IR32D | 40755 | IR30D |
| 2541 K | 81RM50 | 25422 | 81RM100 | 40740 | 10RC60A | 40756 | 10RC60A |
| 2541M | $81 \mathrm{RM60}$ | 2543 A | 91RM5 | 40771 | IR30A |  |  |
| 2541 S | 81RM80 | 25438 | 91RM10 | 40742 | IR308 |  |  |

(1) MECHANICAL DIFFERENCE

| Peak Repotitive Reverse Voltrge | $\begin{aligned} & \text { GE } \\ & \text { NATL } \end{aligned}$ | w |  | IR |  | Peak Repotitive Reverse Voltage | $\begin{aligned} & \text { GE } \\ & \text { NATL } \\ & \hline \end{aligned}$ | w |  | IR |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{array}{r} 15 \\ 25 \\ 30 \\ 30 \\ 100 \\ \hline \end{array}$ | $\begin{aligned} & \hline \mathrm{O} \\ & \mathrm{U} \\ & \mathrm{Y} \\ & \mathrm{~F} \\ & \mathrm{~A} \\ & \hline \end{aligned}$ | $\begin{aligned} & \bar{U} \\ & \bar{A} \\ & B \end{aligned}$ |  | $\begin{array}{r} -2 \\ -2 \\ 10 \end{array}$ | $\begin{gathered} - \\ \overline{05} \\ 1 \end{gathered}$ | 1500 1600 1700 1800 2000 | PE <br> PM <br> PS <br> PN <br> L | $\begin{aligned} & \text { ZK } \\ & \text { ZM } \\ & \text { ZP } \\ & \text { ZS } \end{aligned}$ | $\begin{aligned} & \mathrm{C} 15 \\ & \mathrm{C} 16 \\ & \mathrm{C} 17 \end{aligned}$ | 150 160 170 180 200 | 15 16 17 18 20 |
| $\begin{aligned} & 150 \\ & 200 \\ & 250 \\ & 300 \\ & 400 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \text { G } \\ & \text { B } \\ & \mathbf{H} \\ & \mathbf{C} \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline \text { C } \\ & \text { D } \\ & \text { E } \\ & \text { H } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 15 \\ & 20 \\ & 25 \\ & 30 \\ & 40 \\ & \hline \end{aligned}$ | $\begin{aligned} & \hline-2 \\ & \hline \\ & \hline \\ & \hline \end{aligned}$ | $\begin{aligned} & 2100 \\ & 2200 \\ & 2300 \\ & 2400 \\ & 2500 \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { LA } \\ & \text { LC } \\ & \text { LD } \\ & \text { LE } \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { = } \\ & \hline \end{aligned}$ |  | $\begin{aligned} & 210 \\ & 220 \\ & 230 \\ & 240 \\ & 250 \\ & \hline \end{aligned}$ | $\begin{aligned} & 21 \\ & 22 \\ & 23 \\ & 24 \\ & 25 \end{aligned}$ |
| 500 600 700 800 900 | $\begin{aligned} & E \\ & M \\ & \text { S } \\ & N \\ & \hline \end{aligned}$ | $\begin{aligned} & \mathrm{K} \\ & \mathrm{M} \\ & \mathrm{p} \\ & \mathrm{~s} \\ & \mathrm{v} \\ & \hline \end{aligned}$ | 850 <br> 880 <br> 870 <br> 880 <br> 890 <br> 8 | $\begin{aligned} & 50 \\ & 60 \\ & 70 \\ & 80 \\ & 90 \\ & \hline \end{aligned}$ | $\begin{aligned} & 5 \\ & 6 \\ & 7 \\ & 7 \\ & 9 \end{aligned}$ | 2600 2700 2800 2900 3000 | $\begin{aligned} & \overline{=} \\ & \text { = } \end{aligned}$ | $\begin{aligned} & \text { I } \\ & \text { I } \end{aligned}$ |  | $\begin{aligned} & 260 \\ & 270 \\ & 280 \\ & 2890 \\ & 300 \end{aligned}$ | = |
| 1000 1100 1200 1300 1400 | $\begin{aligned} & \hline P \\ & P A \\ & P B \\ & P B \\ & P C \\ & P D \\ & \hline \end{aligned}$ | Z ZB ZD ZE ZE ZH | C10 C111 C12 C13 C14 C14 | $\begin{aligned} & 100 \\ & 110 \\ & 120 \\ & 130 \\ & 140 \\ & \hline \end{aligned}$ | $\begin{aligned} & 10 \\ & 11 \\ & 12 \\ & 13 \\ & 14 \\ & \hline \end{aligned}$ |  |  |  |  |  |  |

IR replacement numbers indicate the nearest IR equivalent, and in most instances are exact replacements. Occasionally, however, devices differ
in size, electrical parameter, or manufacturing method. For this reason, IR cannot guarantee that the suggested type will, in every instance, in size, electrical parameter, or manufacturing method. For this reason, 1R cannot guarantee that the esuggested type w
serve as an exact replacement, and therefore assumes no responsibility for any consequences in the use of the replacements
IR further suggests that examining the application may reveal that the qualities of another IR device may better fit the needs of the circuit than
the simple replacement of a competitive device.

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[^1]:    Static Characteristics
    The characteristics of an SCR

[^2]:    Average vs. RMS Current Ratings
    A problem with "simple" con-

[^3]:    *These two particular thyristors were chosen because the low frequency ratings are approximately equal.

