NORTHERN ALBERTA INSTITUTE OF TECHNOLOGY
EDMONTON ALBERTA

ELECTRONICS DEPARTMENT

THEORY, CHARACTERISTICS AND APPLICATIONS OF SILICON UNILATERAL, AND BILATERAL SWITCHES

The SUS/SBS are constructed as simple integrated circuits which perform as gated or voltage sensitive switches. Device theory and operation are explained plus circuit applications in the areas of power thyristor triggering and logic. Devices illustrated include the MUS 4987-88 and the MBS 4991-92.

ET/A/49

THEORY, CHARACTERISTICS AND APPLICATIONS OF SILICON UNILATERAL, AND BILATERAL SWITCHES

INTRODUCTION

The silicon unilateral switch (SUS) and silicon bilateral switch (SBS) are advanced semiconductors having negative resistance switching characteristics similar to the 3-layer diode, 4-layer diode and unijunction transistor (UJT). The latter devices have seen wide application, especially in triggering circuits where they can supply the fast rising, high-current gate pulse necessary for the proper operation of power thyristors. In such applications, the SUS and SBS can improve circuit performance and reduce cost at the same time.

These devices are not just an improved version of a pnpn diode. They are actually fabricated as simple integrated circuits consisting of transistors, diodes and resistors.

A third lead, designated the Gate, has been brought out for increased circuit flexibility. Since these devices are a regenerative switch, they may also be designed into many low power latching circuits.

THEORY AND CHARACTERISTICS

The equivalent circuit diagram of an SUS and its symbol are shown in Figure 1. The device is actually a simple IC and consists of a pnp and an npn transistor, a 6.8 volt zener diode and a 15 kΩ resistor, R_B. Unlike existing 4-layer diodes which use a stacked structure, the SUS employs annular techniques in its construction. The result is a device with better stability and control of its electrical parameters.

Electrical characteristics are shown in Figure 2 and the parameters are defined as follows: V_S, the switching voltage, is the maximum forward voltage the device can sustain without switching to the conducting state; I_S, the switching current, is the current through the device when V_S is applied; V_F, the forward voltage, is the voltage drop across the device when it is in the conducting state and passing a specified current; I_H, the holding current, is the current through the device necessary to sustain conduction; I_B, the leakage current through the device with 5 volts bias; V_R, the maximum reverse voltage, is that voltage which, if exceeded, can permanently damage the device.

Operation of the SUS can be best understood while referring to Figures 1 and 2. Consider an adjustable source of voltage with a current limiting resistor in series supplying a voltage to a device anode that is 5 volts positive with respect to its cathode. Since this voltage is less than the sum of V_{BE} of the pnp transistor and V_Z of the 6.8 volt zener diode, only a very small leakage current will flow and the device is in the OFF or blocking state. As the supply voltage is increased, a point will be reached (near V_S) where a small increase in voltage results in a substantial increase in current flow. The pnp transistor purposely has high current gain and most of this increased current flows out of its collector and produces a voltage drop across R_B.

The two transistors are connected in a positive feedback loop similar to the equivalent circuit for an SCR where the

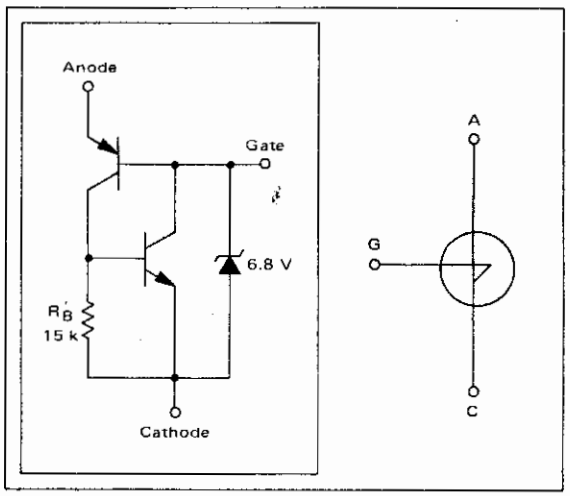

FIGURE 1 – SUS Equivalent Circuit and Symbol

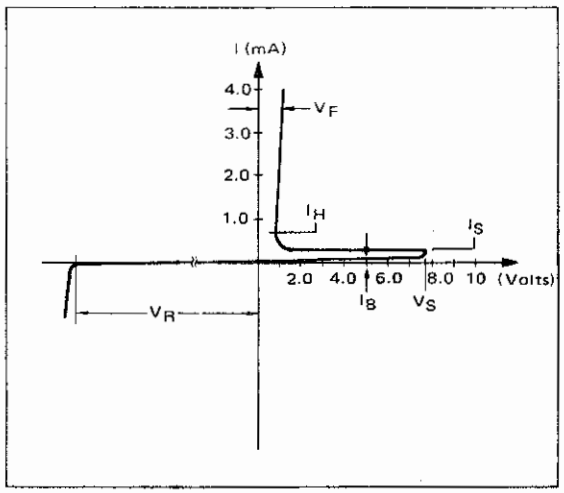

FIGURE 2 – SUS Anode-Cathode V-I Characteristics

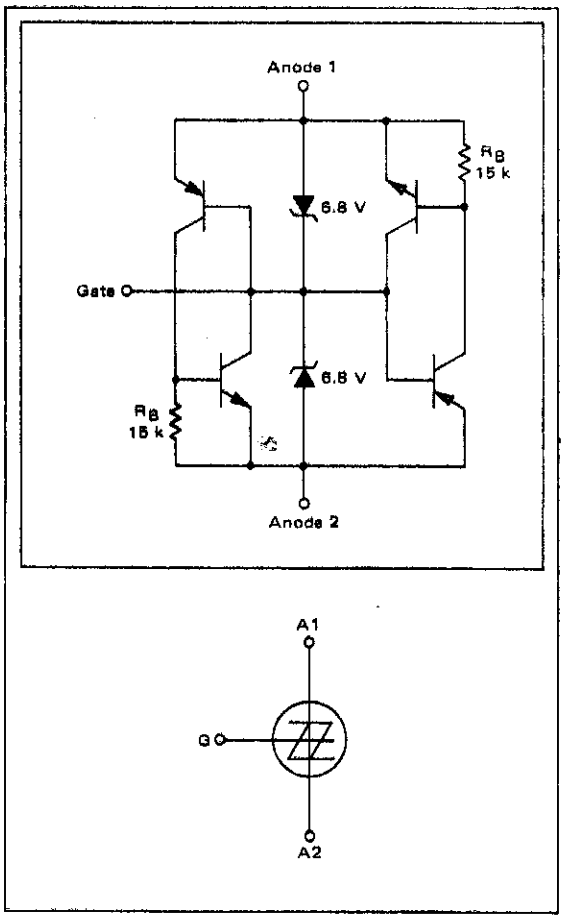

FIGURE 3 – SBS Equivalent Circuit and Symbol

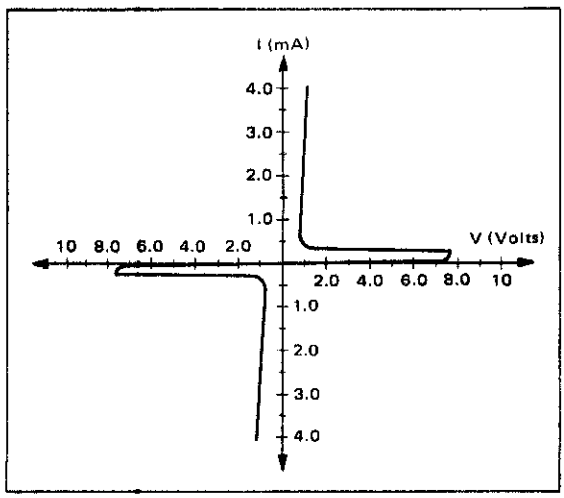

FIGURE 4 – SBS Anode 1 - Anode 2 V-I Characteristics

collector current of one is the base current for the other. When the voltage across R_B is sufficient to turn the npn transistor ON and the loop gain exceeds unity, both transistors are driven into saturation, the voltage across the device abruptly drops and the current through it is limited mainly by the external circuitry. The device has now switched to the ON or conducting state.

The 6.8 volt zener diode has a positive temperature coefficient of voltage which is opposite to that of V_{BE} of the pnp transistor. The net result is good temperature stability of V_S, typically +0.02%/°C.

V_F, the forward voltage across the device, remains relatively low even if the current through it is greatly increased, rising approximately 3 volts/ampere. The device will remain ON until the current through it is reduced to zero or at least below the holding current value. One method of insuring turn-off is to apply a reverse voltage less than V_R, the maximum reverse voltage. After a few microseconds (turn-off time) has elapsed, the transistors will have recovered from saturation and the device will again block a forward voltage up to V_S.

A third lead, the gate, can be used to modify the characteristics of the SUS. As an example, connecting a 3.9 volt zener diode from gate to cathode would lower V_S to approximately 4.6 volts. Connecting a 20 kΩ resistor from gate to anode and a similar resistor from gate to cathode will lower V_S to approximately 4 volts at the expense of increased current around the device prior to switching. Also, if a voltage less than V_S is applied to an SUS, it can be "gated" ON by drawing a small current out of the gate lead.

The SBS is a bilateral version of the SUS. Figure 3 shows the equivalent circuit diagram and symbol for the device. It is actually two SUS's on the same chip with metallization connecting the anode of one to the cathode of the other and having a common gate lead. Figure 4 shows the symmetry of the electrical characteristics. Since the device is fabricated as an IC, the components are well matched resulting in an asymmetry, or difference of positive V_S and negative V_S, of less than 0.5 volts. Other electrical characteristics are the same as for the SUS except that the SBS does not have a V_R rating.

Like other regenerative switches, the SUS and SBS have a tendency to switch to the ON state in the presence of rapidly rising anode voltage. The dv/dt rating of the SUS is difficult to define and the method of measurement may produce erroneous results. A test ramp of voltage with adjustable dv/dt as shown in Figure 5a may be applied to the device if not repeated more frequently than every 10 seconds. The device may switch to the ON state when the dv/dt is in the range of 1 to 10 volts/microsecond. The repetitive waveform of Figure 5b may be applied much more frequently (convenient for an oscilloscope display) providing only that the time interval between turn-off and the next ramp is longer than the turn-off time of the device. The turn-on pulse in Figure 5b is necessary to discharge internal capacitance which can accumulate a charge and give false indication of very high dv/dt capability.

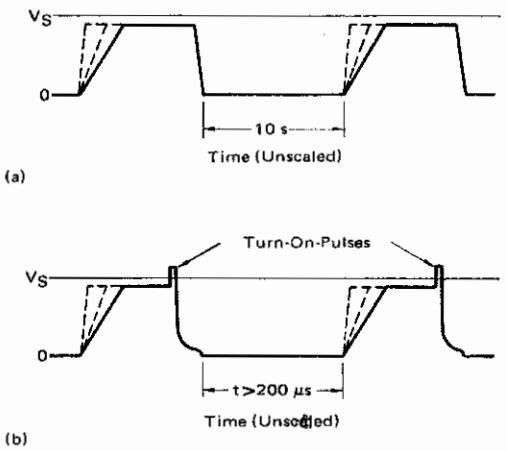

FIGURE 5 – Waveforms for dv/dt Test

Sweeping an SBS in either direction will yield results similar to the above. However, when an SBS has been conducting in one direction and the anode voltage is rapidly reversed, the dv/dt must be limited to approximately 0.1 volt/microsecond. This is necessary because if the transistors in the conducting half of the device have not recovered from saturation, they will provide a path for a current to turn the opposite side ON.

APPLICATIONS

Power thyristors such as the silicon controlled rectifier (SCR) and triac are used in many ac power controller circuits (See AN-240). It is important that the trigger circuitry be capable of supplying a fast rising, high current gate pulse to the power thyristors in order to prevent di/dt failure, especially when they are subjected to high inrush load currents (See AN-173). Because of the regenerative switching action and low dynamic ON resistance of the SUS and SBS, they are ideally suited for use in this type of circuitry.

Several circuits follow which are only indicative of the many potential uses for the SUS and SBS. In some applications the device switches ON at V_S while in others it is turned ON by drawing a small current out of the gate lead. Also included are circuits which utilize the bi-stable nature of the device to perform counting and memory functions.

Lamp Dimmers

Figure 6 is the schematic diagram of a low cost full range lamp dimmer. Shunting the SBS with two 20 kΩ resistors minimizes the "flash-on" or hysteresis effect. V_S of the SBS is reduced to about 4 volts, and since this is below the operating voltage of the internal zener diodes, the temperature sensitivity of the device is increased.

An improved full range power controller suitable for lamp dimming and similar applications is shown in Figure 7. For settings such that no power is delivered to the load, the timing capacitor would never discharge through the SBS. The result is an abnormal amount of apparent phase shift caused by the capacitor starting to charge toward a source of voltage with a residual charge of the opposite sign. This is the cause of the hysteresis effect and is eliminated in this circuit by the addition of the two diodes and 5.1 kΩ resistor connected to the SBS gate. At the end of each positive half cycle when the applied voltage drops below that of the capacitor, gate current flows out of the SBS and it switches ON discharging the capacitor to near zero volts.

Another full range power controller is shown in Figure 8. A load requiring pulsating dc may be connected between the bridge rectifier and SCR. If the load requires an alternating voltage, it may be connected in series with either side of the ac power line. Again the addition of the diode and 10 kΩ resistor across the SCR will guarantee the discharge of the capacitor near the end of each half cycle as in the previous circuit.

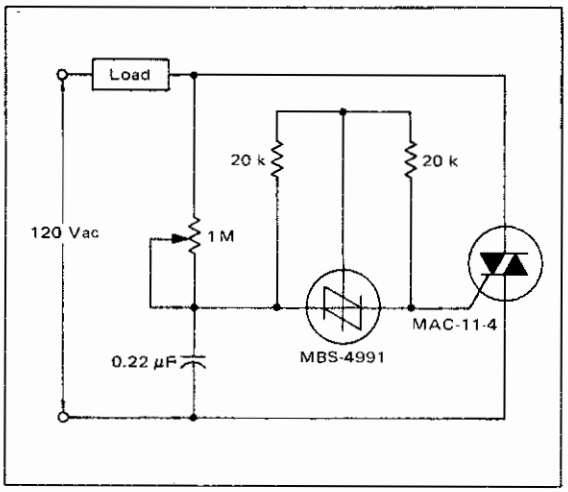

FIGURE 6 – Low Cost Lamp Dimmer

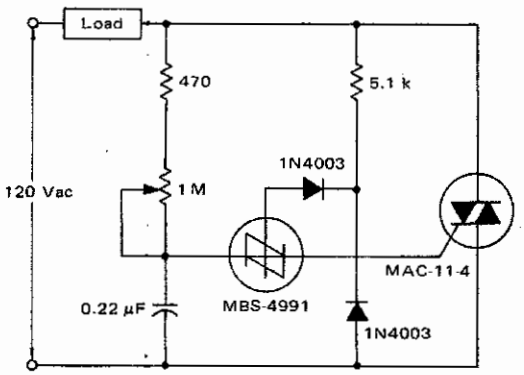

FIGURE 7 – Hysteresis-Free Power Controller

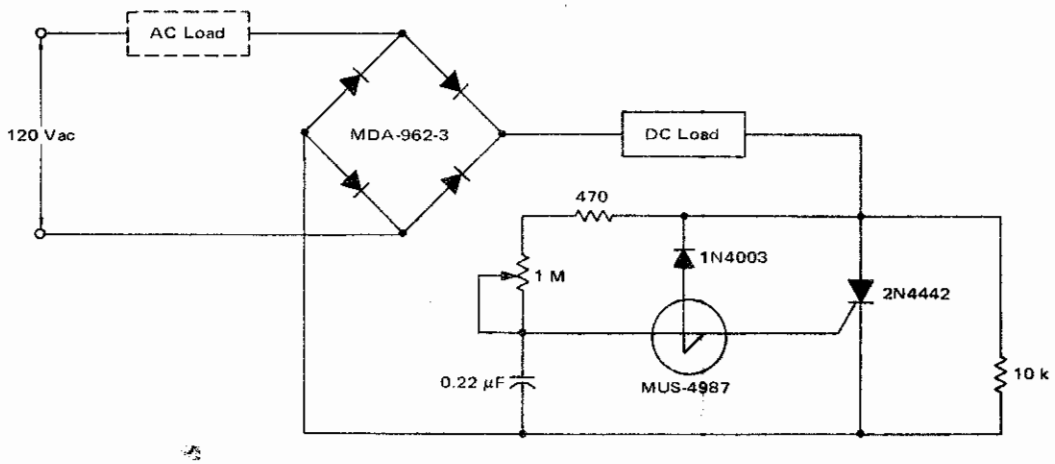

FIGURE 8 – SCR Full Range Power Controller

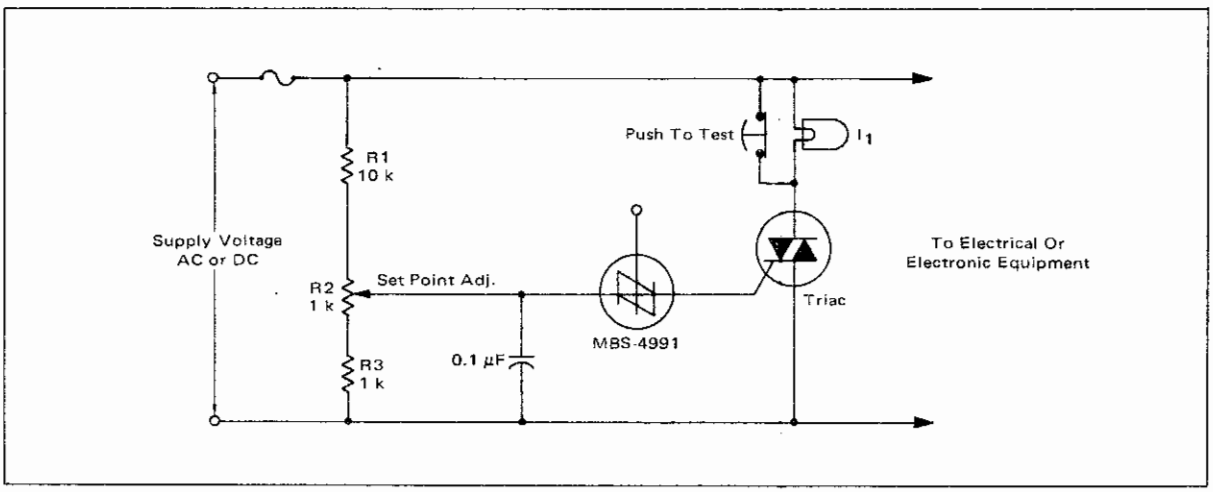

FIGURE 9 – Electronic Crowbar

Electronic Crowbar

Occasionally the need arises for positive protection of expensive electrical or electronic equipment against excessive supply voltage. Such overvoltage conditions can occur due to improper switching, wiring, short circuits or failure of regulators. Where it is economically desirable to shut down equipment rather than allow it to operate on excessive supply voltage, an electronic "crowbar" circuit such as the one shown in Figure 9 can be employed to quickly place a short circuit across the power lines, thereby dropping the voltage across the protected device to near zero and blowing a fuse. Since the triac and SBS are both bilateral devices, the circuit is equally useful on ac or dc supply lines. With the values shown for R1, R2 and R3, the crowbar operating point can be adjusted over the range of 60 to 120 volts dc or 42 to 84 volts ac. The resistor values can be changed to cover a different range of supply voltages. The voltage rating of the triac must be greater than the highest operating point as set by R2. I_1 is a low power incandescent lamp with a voltage rating equal to the supply voltage. It may be used to check the set point and operation of the unit by opening the test switch and adjusting the input or set point to fire the SBS. An alarm unit such as the Mallory Sonalert may be connected across the fuse to provide an audible indication of crowbar action. Note that this circuit may not act on short, infrequent power line transients.

Single Pulser

The schematic diagram of a manually operated single pulse generator is shown in Figure 10 and is very useful for testing digital circuitry. A simple switch and source of voltage is generally not suitable for this type of testing since the mechanical bounce of the contacts will actually produce a long series of pulses. The circuit shown overcomes this problem since it can produce only a single pulse for each operation of S1. The 0.5 μF energy storage capaci-

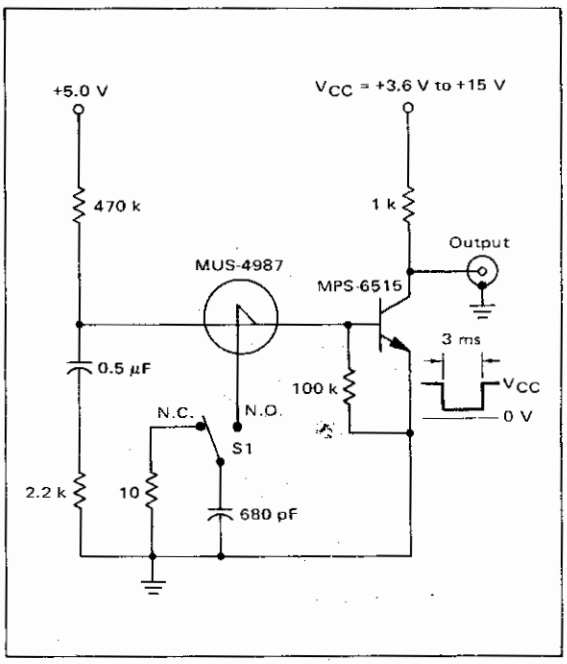

FIGURE 10 – Single Pulse Generator

tor is normally charged to 5 volts, below V_S of the SUS. Switching the 680 pF capacitor to the SUS gate will result in a surge of current flowing out of that electrode and the device switching on. The SUS will remain ON, keeping the output transistor saturated until the energy storage capacitor has discharged to a point where the current flowing is below the holding current of the device.

The output is a clean pulse of 3 millisecond duration. V_{CC} for the output transistor may be set to +3.6 volts to +15 volts in order to match the requirements of the logic being tested. An additional inverter stage may be used if necessary.

Bi-Stable Switch

A circuit having bi-stable or memory characteristics is shown in Figure 11. Initially both SUS's are in the OFF state since the supply voltage is less than V_S of the devices. A momentary contact in either of the normally open switches will gate its SUS ON. That device will remain in the ON state and its anode voltage less than 1 volt positive until the other device is gated ON. The negative anode swing of the SUS turning ON is coupled through the commutating capacitor and reverse biases the other device turning it OFF. The mechanical switches may be replaced, of course, by other solid state devices or a negative going pulse referenced to the supply line.

Ring Counter

Another interesting circuit which utilizes the latching feature of the SUS is the 4-stage ring counter shown in Figure 12. When power is applied to the circuit, the SUS in stage "0" will be switched ON due to the surge of gate current required to charge the 5 μF capacitor connected to it. The MPS 6565 transistor is saturated and its collector near ground. Therefore, most of the supply voltage appears across the 1 kΩ cathode resistor in stage "0". This voltage determines the current level through MPS 6512 and the light emitting diode, MLED 600, is ON indicating a count of "0". Each stage is connected to the next through a 0.1 μF capacitor. The capacitor connecting stage "0" to stage "1" will be essentially discharged since the voltage at each side is near the supply. Each of the other 3 coupling capacitors is charged to approximately supply voltage. An event to be counted must be shaped to a 1 volt negative square wave with a duration of 30 to 50 microseconds and fed to the counter input. Each input pulse will turn off the MPS 6565 transistor and the 100 ohm resistor will allow its collector to rise to the supply voltage. During this interval there is no voltage across the SUS in stage "0" and it will return to the OFF state. When the MPS 6565 is driven into saturation following the first input pulse, only the coupling capacitor between stages "0" and "1" will require charging and most of the required current must flow out of the SUS gate in stage "1", turning it ON with the MLED 600 in that stage indicating a count of "1". In this manner each succeeding input pulse is able to advance the count around the ring a stage at a time. Opening the normally closed RESET switch will cause any stage to return to the OFF state and only stage "0" will be gated ON when it is closed. The 4.7 ohm resistor and 100 μF capacitor limit the dv/dt of the supply line to prevent stages other than the first from switching ON when the RESET switch is closed. Any number of stages may be cascaded.

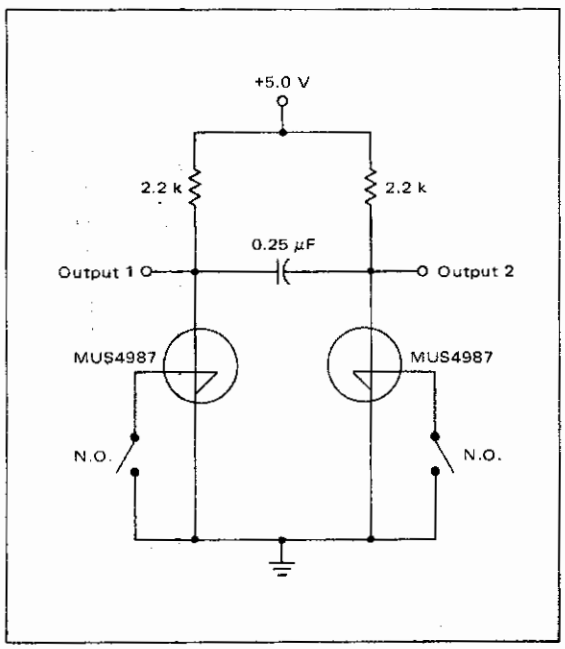

FIGURE 11 – Memory Circuit

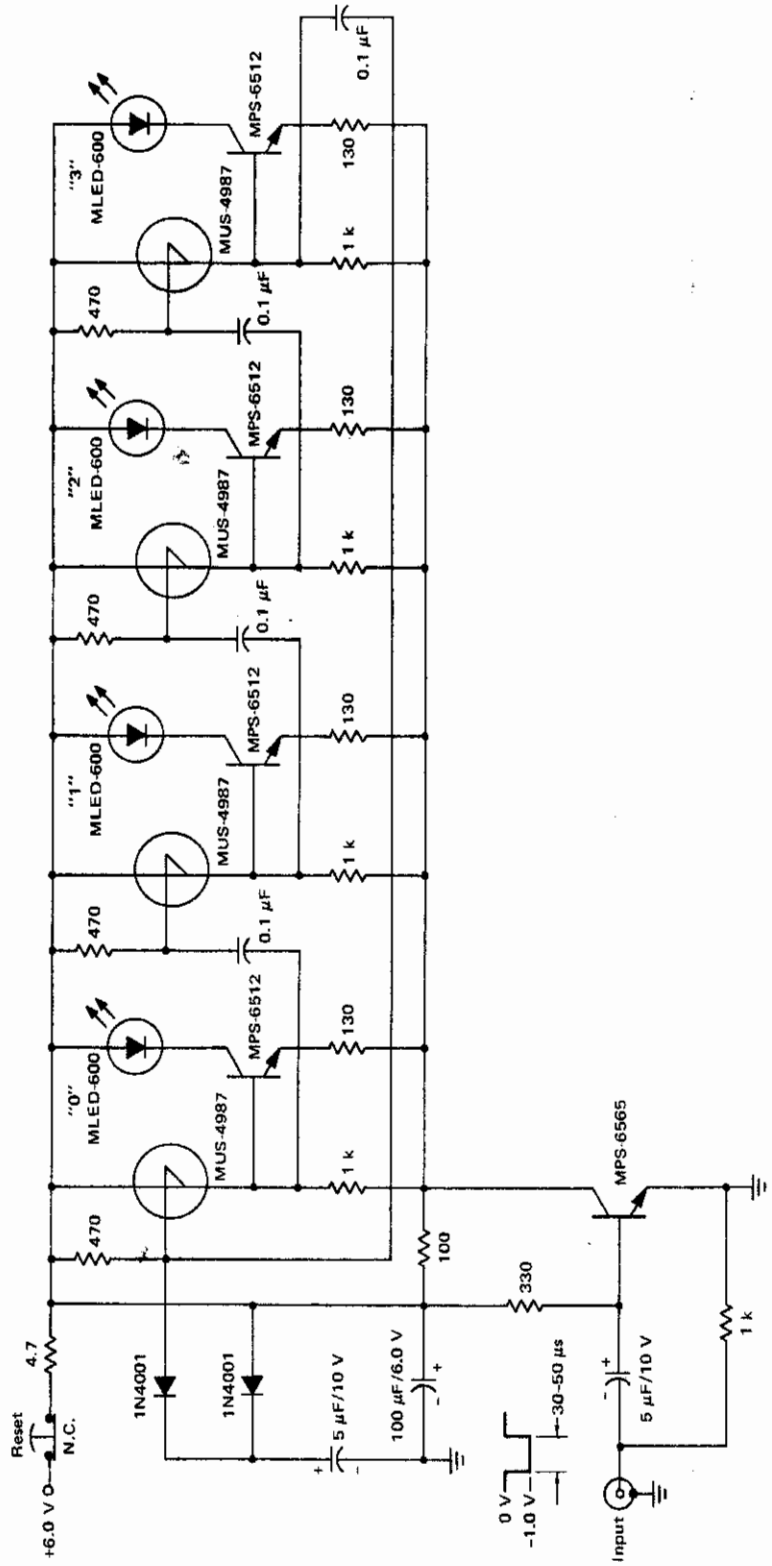

FIGURE 12 – 4-Stage Ring Counter

SUMMARY

The SUS and SBS have been shown to be ideal trigger devices for power thyristors. Since the devices exhibit a switchback of over 5 volts and a dynamic ON resistance of 2 to 3 ohms, they are capable of supplying more output current than a UJT, the current from the latter being limited by the conductivity modulated portion of the interbase resistance. This is an important advantage in applications where the supply voltage for the trigger circuitry must be limited to a low value. Fabricated as simple IC's, these devices will be less expensive than multilayer diodes and also have more stable and predictable electrical characteristics. Their low switching voltage and dynamic ON resistance are conducive to the design of simple, low cost and reliable triggering circuits.

The bi-stable nature of the devices, plus the availability of a gate electrode, make them very useful in certain types of logic circuits. Having some characteristics similar to an SCR, they may be designed into dc latching circuits but should not be considered as a substitute for an SCR in ac circuits because of the limited dv/dt capability.

15V DIAC THREE LAYER LATERAL TRIGGERS

Cat. No. 276-1078

ARCHER TECHNICAL DATA

AN EXCLUSIVE RADIO SHACK SERVICE TO THE EXPERIMENTER

'his device is two termi-
al, three layer diode
/hich exhibits symetrical
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ng characteristics. The
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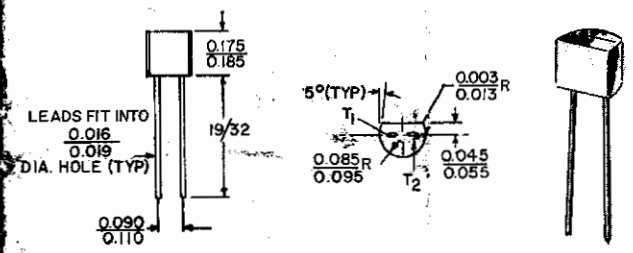
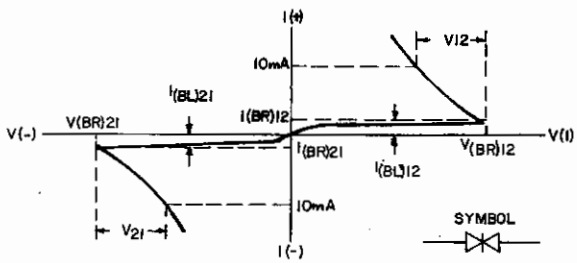
uits, lamp drivers and
notor speed controls.

eatures
- Low switching current
- Large switchback voltages
- Reliable

BILATERAL TRIGGER

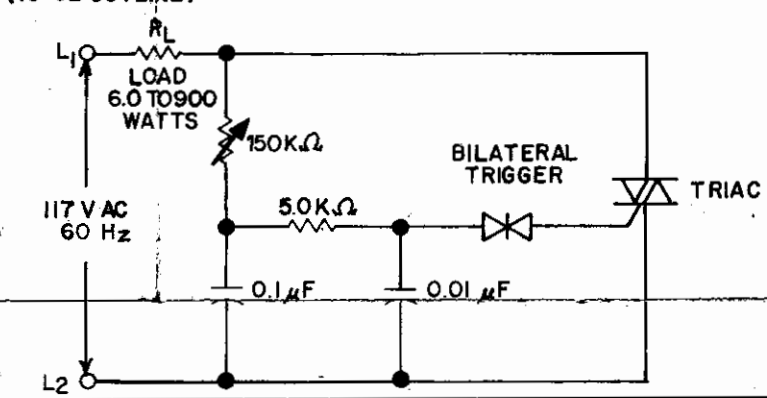


VOLT-AMPERE CHARACTERISTICS*



CASE 29B
(TO-92 OUTLINE)

TYPICAL CONTROL CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Typ	Unit
Breakover (Switching) Voltage — both directions	$V_{(BR)12}$ & $V_{(BR)21}$	32	Volt
Breakover (Switching) Current — both directions	$I_{(BR)12}$ & $I_{(BR)21}$	20	Amp
Switchback (Delta) Voltage — both directions	V_{12} & V_{21}	10	Volt
Peak Blocking Current — both directions Voltage Applied = 18 V	$I_{(BL)12}$ & $I_{(BL)21}$	0.5	A
Breakover (Switching) Voltage Temperature Coefficient, T_A = -40°C to +100°C		0.03	%/°C

*These devices have symmetrical characteristics and as such the terminal leads are interchangeable. For purposes of symbol clarification, the leads have arbitrarily been designated 1 and 2. A 12 designation indicates that terminal 1 is positive with respect to terminal 2, vice versa for a 21 designation.

15V DIAC THREE LAYER BILATERAL TRIGGERS

Cat. No. 276-1078

ARCHER TECHNICAL DAT

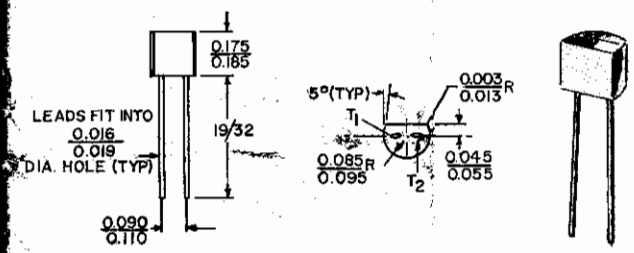
AN EXCLUSIVE RADIO SHACK SERVICE TO THE EXPERIMENTER

This device is two terminal, three layer diode which exhibits symetrical negative resistance switching characteristics. The diac is ideally suited for use in SCR triggering circuits, lamp drivers and motor speed controls.

Features

- Low switching current
- Large switchback voltages
- Reliable

BILATERAL TRIGGER



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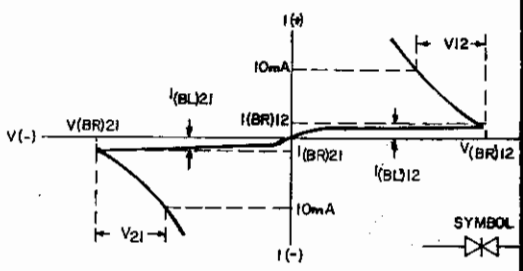

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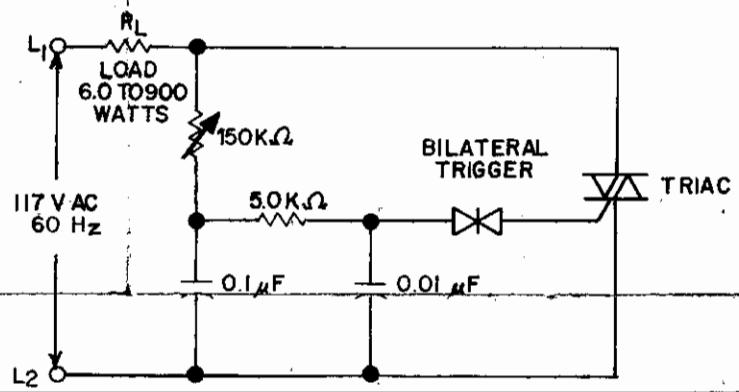

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Transistor array converts to fast-switching thyristors

by H.S. Kothari
Central Electronics Engineering Research Institute, Pilani, India

An ordinary monolithic transistor array can be wired to perform as multiple four-layer silicon-controlled switches by making use of the terminal to the array's substrate. For example, a seven-transistor array having common emitters can be used to implement a seven-stage ring counter.

As shown in (a), the npn transistor array has a separate connection to its p-type substrate. The array is easily wired as shown in (b), with the substrate being employed as a common anode to form pnpn structures that can be regarded as silicon-controlled switches. And since the geometry of each transistor is very small, switching times can be on the order of a few nanoseconds.

The schematic of the ring counter is drawn in (c). The first stage is turned on by the trailing edge of the reset pulse. Now, when a clock pulse is applied to the input transistor, the voltage at this transistor's collector drops, and the other counter stages are turned off. In this way, a trigger pulse is transferred from the first stage to the second stage. The next clock pulse causes a trigger pulse to go from the second to the third stage. This process continues and repeats when the seventh counter stage triggers on the first counter stage.

The hold-on current for any stage can be between 50 microamperes and 1 milliampere. The negative voltage amplitude of the reset pulse should be large enough to lower the voltage of the anode gate of the first stage so that this stage is sure to fire. The anode-gate voltage, therefore, is made negative with respect to the anode voltage.

The length of the triggering delay is determined by the capacitance value selected. Voltage amplitudes can be made as large as the collector-emitter breakdown limit of each transistor by increasing the supply voltage, as well as the zener voltage, to some suitable maximum level. □

Wiring transistors as thyristors. Integrated seven-transistor array (a) can be wired as silicon-controlled switches by making use of their common substrate connection. The transistors can then be operated as four-layer devices (b) that have switching times on the order of a few nanoseconds. One application for the pnpn switch array is illustrated in (c)—a seven-stage ring counter.