



SiGe PROCESSES
CAN GIVE ANALOG-
CIRCUIT DESIGNERS
FAST, HIGH-VOLT-
AGE TRANSISTORS
WITH LOW NOISE,
WHEREAS BICMOS
SiGe FITS INTO CMOS
PROCESS FLOWS.

BY PAUL RAKO • TECHNICAL EDITOR

SILICON GERMANIUM

FAST, QUIET, and

POWERFUL

CMOS (complementary-metal-oxide-semiconductor) processes have consistently surprised the semiconductor industry. CMOS prices decreased and CMOS speeds increased, a scenario that primarily benefits digital-IC designers. A digital-IC designer does not care that a part is running on 1V or less, as long as there is enough SNR (signal-to-noise ratio) to discriminate a one from a zero. Analog-circuit designers, on the other hand, have

a much harder time making the myriad trade-offs necessary for a pure-analog-signal or a mixed-signal part. One of the fundamental problems with fine-line CMOS is the high cost of its mask set. That drawback makes the technology available only to large-market ICs that can amortize the cost. Analog-IC designers have alternatives, however: Bipolar SiGe (silicon germanium) and BiCMOS (bipolar-CMOS) SiGe. In addition, germanium-strained-silicon CMOS creates fast PMOS (positive-

channel-MOS) transistors that allow for fast, complementary low-leakage digital design.

In germanium-strained silicon, manufacturers implant germanium into the channel of the PFETs (positive-channel field-effect transistors). The presence of the larger germanium atom stretches the silicon lattice, providing faster carrier mobility (Figure 1). This process is thus inherently more complementary, with similar-sized transistors for both the

negative- and the positive-channel devices. In the hands of a good IC designer, the performance of fast PNP (positive/negative/positive) transistors, even in digital designs that ignore the transistor-level-circuitry benefit, can improve because the technology reduces both die area and cost. Although electronics professors still teach students that the drive currents of NFETs (negative-channel FETs) are three times those of PFETs, some industry observers dispute that idea. "That [assumption] is no



longer true for modern processes,” says Ric Borges, senior marketing manager for TCAD (technology-computer-aided design) at Synopsys. “There are even cases where the drive current of the PMOS device is higher than that of the NMOS [negative-channel-MOS] device, due to the strained silicon.”

When op-amp or RF designers discuss SiGe, they are generally referring to bipolar SiGe (Figure 2). Because bipolar SiGe is not a CMOS process, the bipolar transistors can provide high performance. “SiGe HBTs [heterojunction-bipolar transistors] have SiGe alloys of nanoscale thickness—say, 20% SiGe over 50 nm—embedded in their base regions, which are compositionally graded to boost their performance metrics in a tunable way,” says John D Cressler, the Ken Byers Professor at the Georgia Institute of Technology. This alloy results in higher gain, higher frequency, higher maximum frequency, lower-resolution bandwidth, lower noise floor, lower flicker noise, and higher output resistance than a similarly doped silicon-only bipolar transistor, he says. The presence of fast, complementary PNP transistors allows this process to make operational amplifiers with gain-bandwidth products greater than 1 GHz. Just as important, SiGe’s lower noise figure helps the amplifier deliver remarkable performance, and its operating volt-

AT A GLANCE

- ❑ SiGe (silicon germanium) can be a purely bipolar process, a BiCMOS (bipolar-complementary-metal-oxide-semiconductor) process, or a strained-silicon process in CMOS PFETs (positive-channel field-effect transistors).
- ❑ In strained-CMOS PFETs, the germanium increases the mobility of carriers in the P channel.
- ❑ In bipolar or BiCMOS processes, the germanium resides in an epitaxial film to create the base region.
- ❑ Bipolar SiGe changes the band-gap in the base area and allows higher dopant concentrations.
- ❑ SiGe processes use normal fab flows, requiring only the addition of the epitaxial reactor.
- ❑ SiGe ICs can use available tool flows.
- ❑ SiGe has a niche in analog and RF parts that benefit from the low cost and integration of silicon but do not need the performance of III-V-semiconductors—those combining an element from the third column of the periodic table with an element from the fifth column.

age can be higher than that of CMOS processes, increasing SNR in RF receivers. This higher voltage is an essential

feature of RF-power amplifiers. SiGe also provides better linearity, which is essential in modern modulation schemes in which the RF envelope contains the information (Reference 1).

“Even in the industrial [market], where you want higher-voltage parts, SiGe is an enabling technology due to the increased beta [current-gain] and early-voltage benefits,” says Tim Kalthoff, a TI fellow and chief technologist for high-performance analog at Texas Instruments. “You get higher gain and better precision with better distortion characteristics because of SiGe,” he says. SiGe transistors are superior to other bipolar transistors in almost every figure of merit. SiGe exhibits many of the same trade-offs as silicon transistors, but, because its performance metrics are all on a higher baseline, you can tune a SiGe process to surpass the performance of silicon transistors in almost any specification without letting any other specification fall below best in class for silicon. In addition, the process can use not only trench isolation, but also full dielectric isolation for low stray capacitance and maximum speed (Figure 3).

These processes are ideal for mixed-signal parts that need the blazing speed of SiGe and the signal-processing control of CMOS. Because the CMOS in these processes is generally two generations old, the line widths are 135 nm or more. This width can provide benefits such as higher-voltage operation, but it also provides a significant cost penalty for the digital part of the chip. For this reason, designers of low-cost, high-volume digital circuits prefer to stick with CMOS if possible and move the RF or analog to a separate chip if they cannot design it in CMOS.

HISTORY OF A PROCESS

In the 1950s, Herbert Kroemer, a professor of physics at the University of California—Santa Barbara, proposed the HBT. Russian physicist Zhores I Alferov, who in 2002 shared the Nobel Prize with Kroemer, independently invented the heterotransistor. Kroemer’s research focused on III-V compounds, such as GaAs (gallium arsenide), which are semiconductors that combine an element from the third column of the periodic table and an element from the

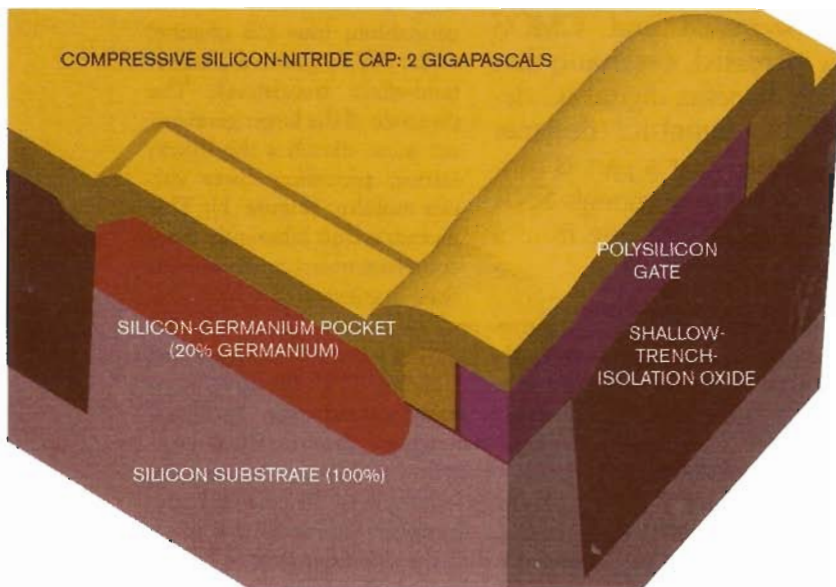


Figure 1 A strained-silicon PFET has germanium in the channel region to increase carrier mobility and, thus, speed (courtesy Synopsys).

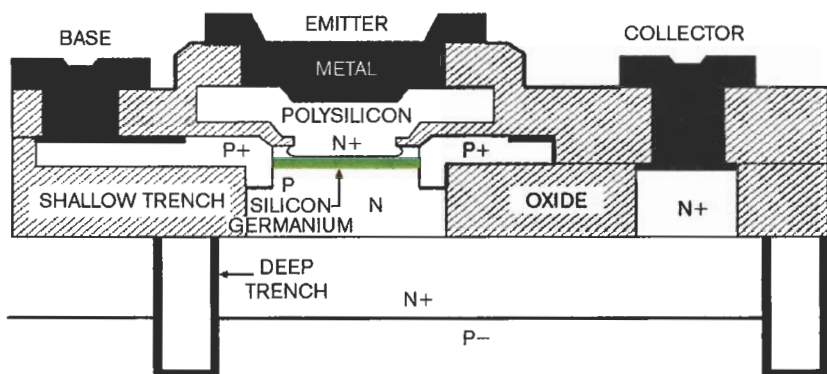


Figure 2 This silicon-germanium NPN HBT has trench-isolated devices on a junction-isolated substrate (courtesy John Cressler, Georgia Institute of Technology).

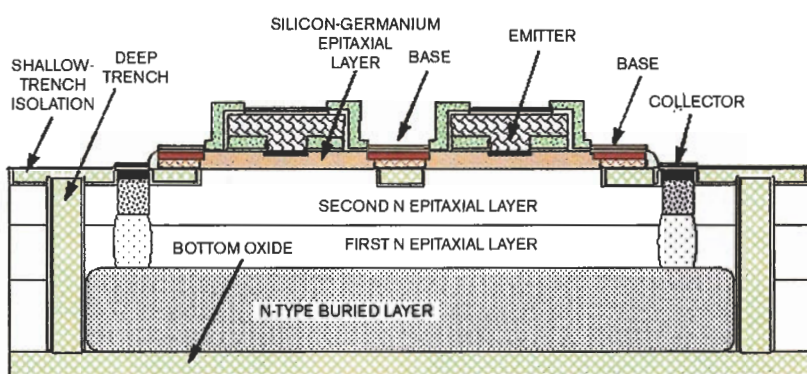


Figure 3 In addition to trench isolation between devices, SiGe processes can use a bottom oxide to achieve full dielectric isolation (courtesy Texas Instruments).

fifth column. By 1987, seeking a process to use in mainframe computers, IBM adapted the HBT to silicon processes (Reference 2).

Engineers at the company knew that they could achieve higher speeds with SiGe, but CMOS designs offered lower power consumption—critical to that era's mainframe computers. Knowing that SiGe produced superior transistors, IBM repurposed the SiGe process for use in analog- and mixed-signal RF ICs, using a high-vacuum-deposition system, according to Jeff Babcock, principal integration-device engineer at National Semiconductor (Figure 4). Universities, including the Georgia Institute of Technology, are assisting in the development of SiGe processes. Georgia Tech's Professor Cressler has dedicated an entire lab to pursuing this transistor technology to its limits.

Soon, other semiconductor companies started to see the potential for SiGe in their analog designs. Analog Devices in 1993 formed an alliance with IBM,

and Texas Instruments developed several similar processes for op amps and RF designs. National Semiconductor also uses multiple SiGe processes, including bipolar SiGe, which finds use in amplifiers, and BiCMOS SiGe, which finds use in interface and mixed-signal products. Maxim Integrated Products is using SiGe to assist in its expansion into RF ICs. Several fabs, including Jazz, NEC, and austriamicrosystems, also offer SiGe processes (Reference 3). IBM has not rested on its laurels, either, having recently announced SiGe transistors that have unity-gain frequencies approaching 300 GHz at low temperatures. Researchers expect by the end of the decade to have 500-GHz SiGe as well as 300-GHz unity-gain frequency at room temperature.

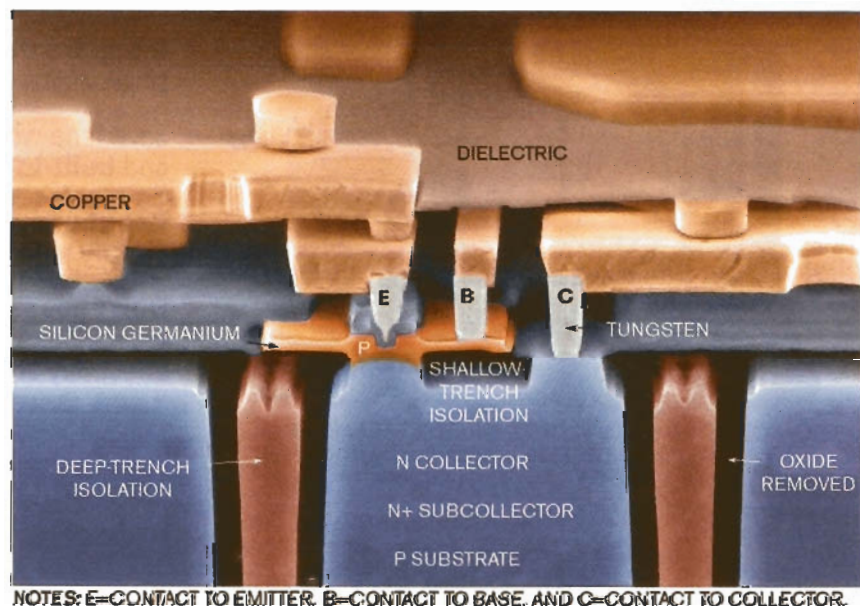
The HBT uses fundamental physics and quantum mechanics to achieve speeds in the hundreds of gigahertz. CMOS processes can achieve speed only by reducing device geometries, so operating voltages must be lower to prevent

breakdown across the transistors. For digital circuitry, that approach is acceptable because the transistors must convey only on and off states. But for analog, the SNR with this approach soon becomes unacceptable. To even approach 100 GHz, CMOS devices must decrease to sizes that will withstand a power-supply voltage of only 1V or less. "The real limitation of CMOS is the ever-dropping voltage," says Jean-Marc Mourant, senior scientist of IC design at Maxim Integrated Products. CMOS is the purview of low-performance applications in which cost and integration are primary, he says.

As the name *heterojunction* implies, the base of a SiGe transistor is the area that combines silicon and the germanium that an epitaxial reaction deposits. If you want to add SiGe to a CMOS line, you have to purchase only one epitaxial reactor, and the rest of the fab flow remains the same. The germanium in the silicon lattice provides far more benefits to a bipolar transistor than it does to the germanium-implanted channel of a strained-silicon-CMOS process. Like with the strained silicon, the mobility increases, but you derive more benefit from the change in the bandgap. For this reason, HBT processes benefit from bandgap engineering.

Germanium allows higher dopant concentrations in the base region. "You are lowering the base resistance without killing the current gain," says Derek Kimpton, parasitics-product-line manager at TCAD-simulation-software manufacturer Silvaco. "The lower base resistance of the SiGe HBT also has the added benefit of creating a low-noise device, an important criterion for RF-circuit designers." The whole idea behind SiGe, like any other HBT, is that you can use more dopant for the base because a bandgap exists between the base and the emitter, so emitter-injection efficiency remains stable, according to Robb Johnson, PhD, director of technology at fabless-components company Inphi. "You can dope the base higher without killing the device performance, and, at the same time, you can make the base narrower and speed up the transit time," he says.

Using SiGe also increases the f_T , the unity-gain frequency of a transistor's short-circuit current gain. The doping concentration creates a field that accelerates the electrons in the devices (Figure 5). In a conventional silicon transistor, higher doping would lower the current gain and allow leakage back to the collector. In a SiGe transistor, the bandgap potentials maximize the current



NOTES: E—CONTACT TO EMITTER, B—CONTACT TO BASE, AND C—CONTACT TO COLLECTOR.

Figure 4 After dielectric etching, a color-enhanced micrograph of a SiGe transistor showcases the device. A real device has no air or vacuum between regions (courtesy Subramanian S Iyer, IBM).

gain and minimize leakage. The higher dopant concentration makes the silicon act more like a metal and less like an insulator. The base is more conductive, and the base resistance decreases, making the noise factor in SiGe transistors better than that of pure-silicon devices. As with all other analog processes, however, you must make trade-offs: lower emitter resistance or reduced leakage, for example. You achieve all these performance enhancements on a process line that differs little from that of any other silicon fab.

"If you increase the base dopant in a regular transistor, you can reduce the base resistance and improve the Early voltage, but you usually kill the current gain," says Marco Corsi, a fellow at Texas Instruments. *Early voltage* takes its name from its discoverer, US engineer James M Early. The Early Effect is the variation in the width of the base in a BJT (bipolar-junction transistor) due to a variation in the applied base-to-collector voltage. "You can't run the transistor at high current density if you don't have any current gain," says Corsi. "The SiGe improves the current gain, which allows you to run higher base dopings."

Mike Maida, National Semiconductor's chief technologist, adds: "By putting germanium into the silicon, you get a variable bandgap as a function of distance. This [approach] gives you another handle to tweak the current gain." According to Maida, you needn't trade off current gain versus base resistance. The thermal noise of the base resistance appears as a noise term, and higher base resistance also degrades the maximum frequency. Brad Scharf, a fellow at Analog Devices, explains that factors that decrease base resistance also derive from factors such as geometry shrinkage that do not directly relate to adding germanium. "The beta Early-voltage product is also an indication that the base resistance in the transistor is

Go to www.edn.com/080918df and click on Feedback Loop to post a comment on this article.

For more feature articles, go to www.edn.com/features.

lower with SiGe than it would be in an otherwise-comparable silicon transistor," says Scharf.

All of these benefits yield better transistors, according to David Hame, a fellow and director of derivative- and value-added-technology development at IBM. Developers of HBTs build the devices vertically, whereas CMOS' developers base the devices on lateral scaling and lithography. "The SiGe allows you to improve the overall figure of merit," says TI's Corsi. "Particularly with the PNP, it allows you to make the transis-

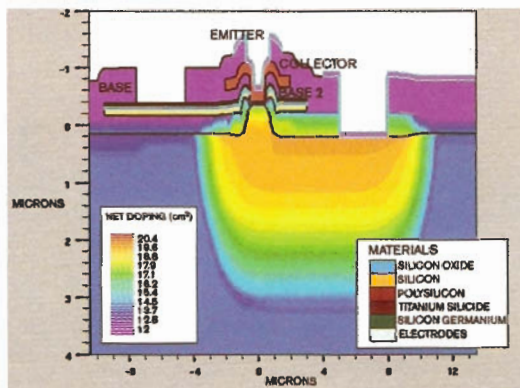


Figure 5 Varying the doping concentration across the base of a SiGe transistor creates an electric field that accelerates the electrons and speeds up the device (courtesy Silvaco).

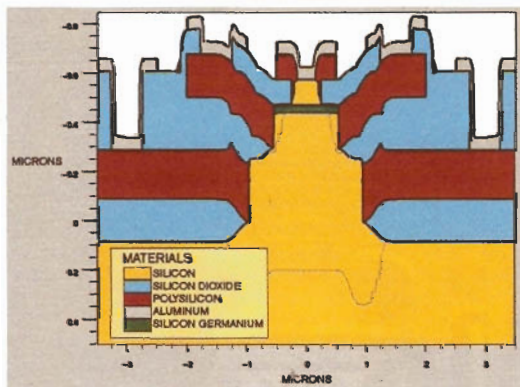


Figure 6 By modeling the physical transistor, a CAD tool can help derive design rules and device characteristics (courtesy Silvaco).

tor much closer to the performance of the NPN. This ... symmetrical process is great for building amplifiers and linear circuits." In short, using SiGe processes yields speed, along with low noise, higher voltage, lower power, and all the further benefits of the improved specs.

NO ROSE-COLORED GLASSES

Not everything in the SiGe world is perfect. Almost every analog-semiconductor company has a horror story about moving a process from one fab to another and losing the process, sometimes for years. Adding a machine cannot reduce capitol costs or improve yield. "The fact that you have more process steps has to hurt the yield; 10% more process steps automatically give you a few percentage points less yield," says Artur Balasinski, process-technology-development-engineering manager at Cypress Semiconductor. BiCMOS SiGe involves other cost implications, as well. Because the BiCMOS processes have wider lines and larger geometries, the dice are larger than those using the latest CMOS processes. And, even though the BiCMOS mask set is cheaper, the process makes little sense for high-volume parts with predominantly digital content. "Going back two generations to implement something that is merely 'faster' but doesn't provide you with much other competitive advantage and is also faster in a domain that you may not care about much makes BiCMOS a hard sell," says Balasinski.

The trade-offs favoring SiGe depend on each company's experience, capabilities, and strategy. National Semiconductor's use of SiGe BiCMOS in its interface parts makes sense because a serializer or a deserializer needs a handful of fast transistors to handle the 5- or 10-Gbps serial-data stream, which is an analog signal. Once inside the chip, the parallel-data flow runs at speeds that conventional CMOS can handle. Because these parts have few digital-processing needs, the benefits of SiGe outweigh the geometry hit of a BiCMOS process.

An advantage of SiGe models is that they can work with available tools. "Models for analog devices require a high degree of sophistication," says Subramanian S Iyer, a distinguished engineer and chief technologist at IBM. "A bipolar transistor definitely has a more complex model. We have [provided]

ALMOST EVERY ANALOG-SEMICONDUCTOR COMPANY HAS A HORROR STORY ABOUT MOVING A PROCESS FROM ONE FAB TO ANOTHER AND LOSING THE PROCESS, SOMETIMES FOR YEARS.



and will continue to provide a robust, accurate model. We have been so successful in our analog- and mixed-signal effort [because of the] attention we have paid to generating, testing, and verifying these models."

This observation does not dismiss the issues of adding bipolar SiGe to a CMOS flow, however. "With CMOS, you have a limited number of device models," says Cypress' Balasinski. "You have a particular number of transistors, and interpolation doesn't always work. More often than not, for analog you have discrete models. If you throw in the modeling complexity of BiCMOS, then it kind of kills you right away because you have so much more to maintain to build similar kinds of devices. You have 20 to 50 transistor models, and this number then doubles because you have to have a model for each variation of a bipolar transistor." Calibrating, developing, maintaining, verifying, and testing these models; keeping the line up for model validity; and ensuring that the models don't diverge take a lot of effort, he notes. Getting those models into a product is even more work. For example, you may want to transfer your models to TSMC (Taiwan Semiconductor Manufacturing Co). "You can have them copy exactly, but [TSMC] needs to keep track of your models, and matching them is no small task because the company may have totally different tool sets." Further complicating these issues, all analog processes are highly sensitive to change. "We are talking about subtle things that may work in one fab and not in another," he says.

The same situation holds true for strained silicon in CMOS: "In general, selective SiGe is a sensitive process," says Sri Samavedam, manager of 32-nm bulk integration at Freescale Semiconductor. "Any time you tweak or make any process change you have to recharacterize all the parameters."

Marc Goldfarb, a design engineer with Analog Devices, points out that trench and dielectric isolation also affects the models, meaning that you must consider thermal effects. "Trench and dielectric isolation result in slightly different thermal profiles," he says.

The need for sophisticated tools is not so much a function of the SiGe itself as the fact that, if you are using SiGe, you are probably designing a high-performance IC that needs sophisticated tools to ensure that the part will work properly. SiGe models can plug into midrange Spice tools, such as Cadence/Orcad's PSpice, as well as Synopsys' industry-standard HSpice. SiGe ICs most likely operate at nearly RF frequencies, however, so it also makes sense to have a field solver in the tool flow to ensure that crosstalk and interactions between circuits are not objectionable (Reference 4). In addition, fast chips are incorporating spiral inductors to make tank circuits. You may also want a tool set that can do the physics modeling, which helps you establish design rules so that your device behaves as it should after layout. "We are using a computational grid—a mesh," says Synopsys' Borge. "On that grid, we are solving the semiconductor equations. It is first-principle physics, and, more recently, we have had to include quantum-mechanical effects, particularly for the channels in the PMOS devices." Full-featured SiGe tools include a Spice engine, a field solver for the RF, and a physics modeler for the transistors (Figure 6).

The future of SiGe is good in view of its main competition, the III-V semiconductors, including gallium arsenide and indium phosphide. Although III-V compounds are even faster than SiGe, they are also more costly. Worse yet, the lack of an effective oxide layer in III-V semiconductors makes them less appealing for integration of entire subsystems on a die. Furthermore, the fabs that make these ICs all have smaller wafers;

FOR MORE INFORMATION

Analog Devices
www.analog.com

austriamicrosystems
www.austriamicrosystems.com

Cadence
www.cadence.com

Cypress Semiconductor
www.cypress.com

Freescale Semiconductor
www.freescale.com

Georgia Institute of Technology
www.gatech.edu

IBM
www.ibm.com

Inphi
www.inphi-corp.com

Jazz Semiconductor
www.jazzsemi.com

Maxim Integrated Products
www.maxim-ic.com

National Semiconductor
www.national.com

NEC
www.nec.com

Silvaco
www.silvaco.com

Synopsys
www.synopsys.com

Taiwan Semiconductor Manufacturing Co
www.tsmc.com

Texas Instruments
www.ti.com

6-in. wafers are common. The specialized needs of these devices mean that you cannot fabricate them on any variant of a CMOS-fab flow. SiGe's benefits really pay off in RF amplifiers. "SiGe RF-power amps have a big advantage," says National Semiconductor's Maida. "You can integrate them with CMOS so you no longer need an expensive, esoteric, gallium-arsenide die that sits by itself." EDN

REFERENCES

1 Rako, Paul, "Heads and tails: Design RF amplifiers for linearity and efficiency," *EDN*, April 3, 2008, pg 31. www.edn.com/article/CA6544734.

2 Iyer, Subramanian S, GL Patton, SS Delage, S Tiwari, and JMC Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," International Electron Devices Meeting, 1987, http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1487536.

3 Kempf, Paul, "Silicon germanium BiCMOS technology," Jazz Semiconductor, www.jazzsemi.com/docs/SiGe_BiCMOS_Technology.pdf.

4 Rako, Paul, "Beyond Spice," *EDN*, Jan 18, 2007, pg 41. www.edn.com/article/CA6406716.

You can reach
Technical Editor
Paul Rako at
1-408-745-1994
and paul.rako@edn.com.

