24 LINE PARALLEL INTERFACE

The Wenzel Associates Model 20-24 Parallel Interface is a general purpose, programmable I/O board for use with the IBM Personal Computer. Its 24 I/O lines are available on a 25 pin D connector and may be programmed as inputs, outputs, or both. These lines are TTL compatible, and have the added feature that most lines can source I ma at 1.5 volts to directly drive I)arlington type drivers and high-voltage displays.

The parallel interface requires 4 bytes of addres  and may be jumpered to recognize one of 64 address groups beginning with &H200, ending with &H2FC.

The Model 20-24 Interface is controlled by an 8255A Programmable Peripheral Interface I.C. that may be used in three modes of operation. In the basic mode, MODE 0, the 24 I/O lines are divided into two eight line groups and two four line groups. Each group may be configured in software as all inputs or all outputs by writing a configuration command to the control register. MODE 1 separates the 24 lines into two eight line groups, with the eight remaining lines providing control or "handshaking" functions for each group. Data direction is set through the control register. The third mode, MODE 2, creates a true bi-directional bus on eight of the I/O Lines. Five additional lines provide status and control information for the bus.

In all modes, data may be transferred to and from these I/O lines with the BASIC "OUT" and "INP" commands. Machine language programmers may use 8088 port commands.

The Model 20-24 Parallel Interface may be used to interface almost any peripheral equipment to the IBM personal computer through software control, without the need for additional external logic circuitry.

Operational Description

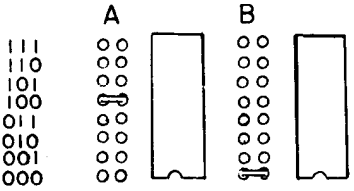
A programming model of the 20-24 parallel interface contains three ports and a control register.
Lines A, and A, on the internal bus, in conjunction with input and output commands, control selection of one of these registers.
Please note that the control word register can ONLY be written into. No read operation of the control word is allowed.

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A ⇒ DATA BUS
0	1	0	1	0	PORT B ⇒ DATA BUS
1	0	0	1	0	PORT C ⇒ DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS ⇒ PORT A
0	1	1	0	0	DATA BUS ⇒ PORT B
1	0	1	0	0	DATA BUS ⇒ PORT C
1	1	1	0	0	DATA BUS ⇒ CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS ⇒ 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS ⇒ 3-STATE

The addressing jumpers are set at the factory such that

&H210 accesses PORT A
&H211 accesses PORT B
&H212 accesses PORT C
&H213 accesses the CONTROL register

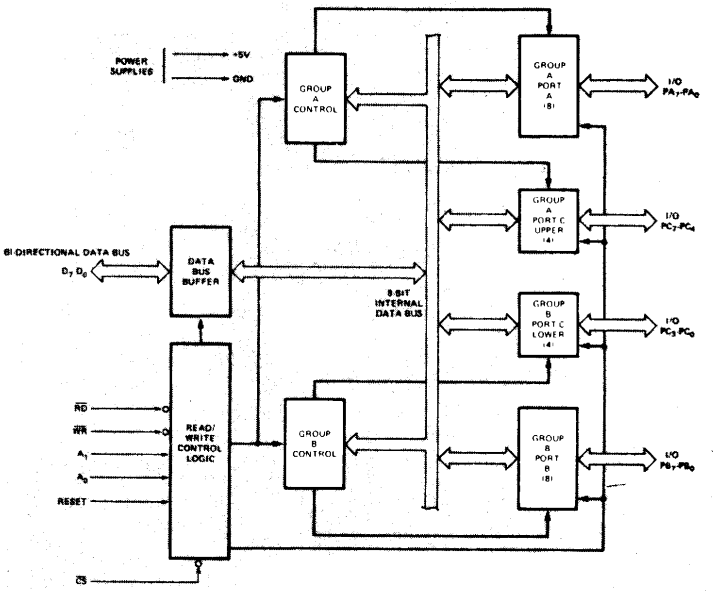
Other address groups may be selected by replacing the addressing jumpers.



A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	B	B	B	A	A	A	X	X

010 0001 0000 = 210 HEX

Group A and B Controls



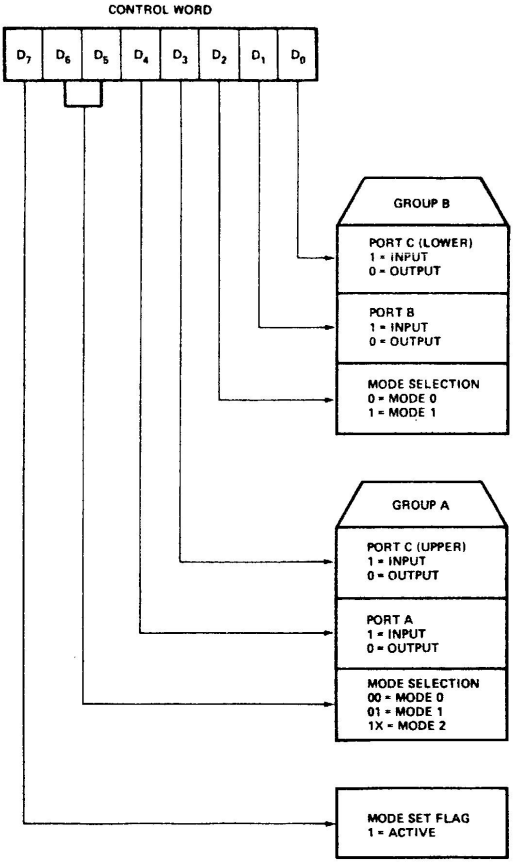
8255A Block Diagram

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic Input/Output
Mode l - Strobed Input/Output
Mode 2 - Bi-Directional Bus

When the IBM computer is powered up, or a system reset occurs, all ports will be set to input mode.

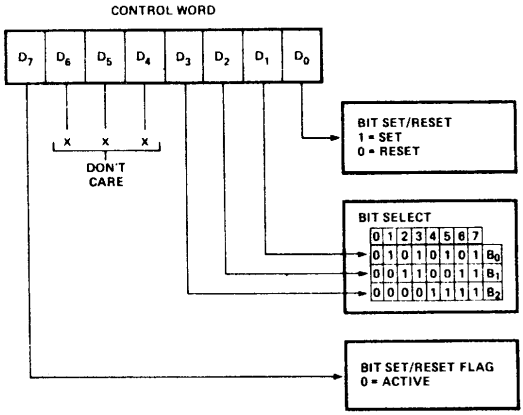
The modes for Port A and Port B can be separately defined, while Port C is divided into two portions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance, Group B can be programmed in Mode O to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Mode Definition Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be set or reset using a single OUTPUT instruction. When Port C is being used as status/control for Port A or B these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.



Bit Set/Reset Format

Interrupt Control Functions

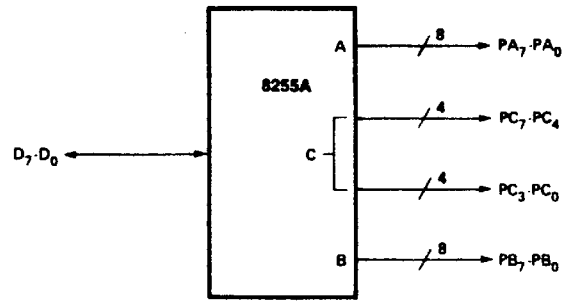
When the 8255A is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C can be inhibited or enabled by setting or resetting the associated INTE flip-flop using the bit set/reset function of Port C. Bit set enables interrupt and Bit reset disables the interrupt.

Operating Modes

Mode 0 provides simple input and output operations for each of the three ports. Data is simply written to or read from a specified port.
MODE 0 Basic Functional Definitions:
· Two 8 bit ports and two 4 bit ports
· Any port can be input or output
· Inputs are not latched
· 16 different I/O configurations are possible

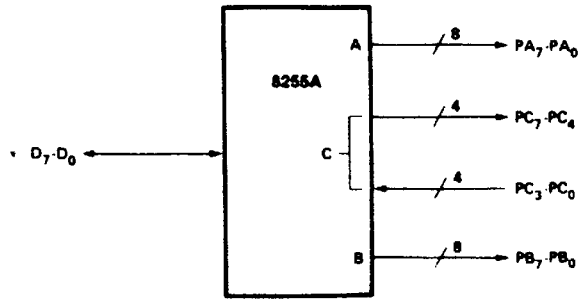
CONTROL WORD #0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



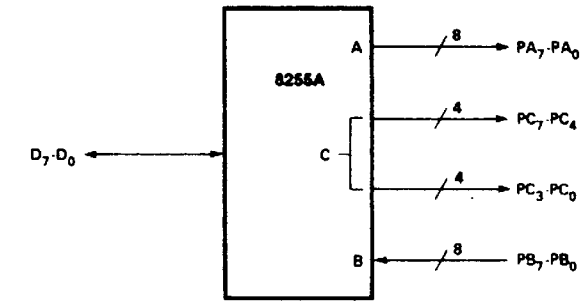
CONTROL WORD #1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



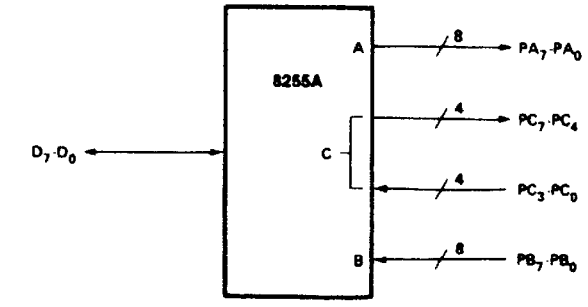
CONTROL WORD #2

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



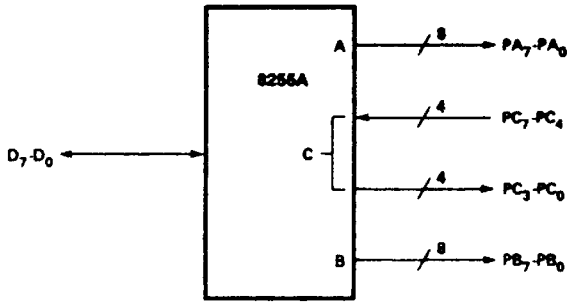
CONTROL WORD #3

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



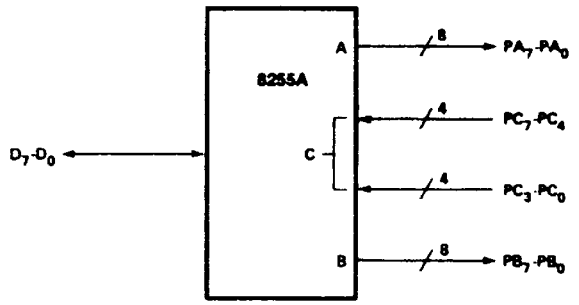
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



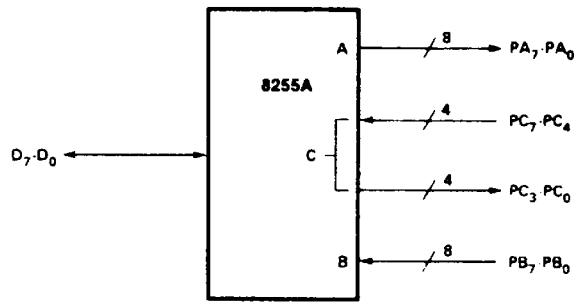
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



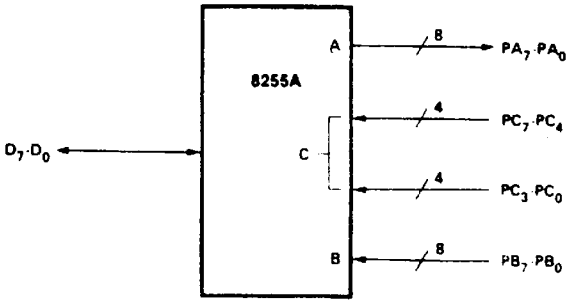
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



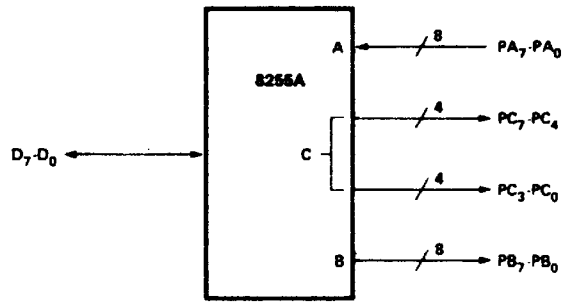
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



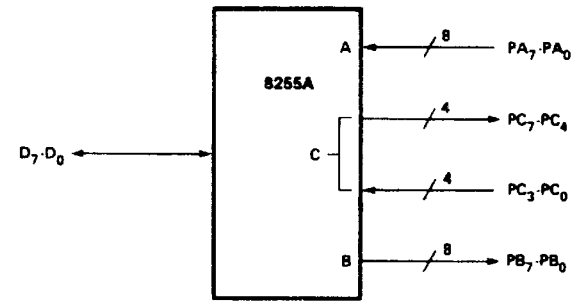
CONTROL WORD =8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



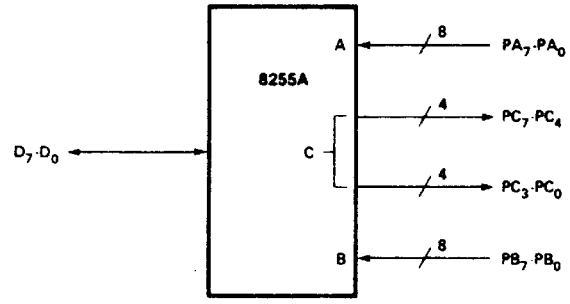
CONTROL WORD =9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



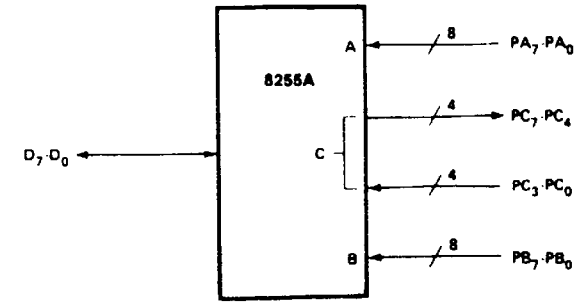
WORD =10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



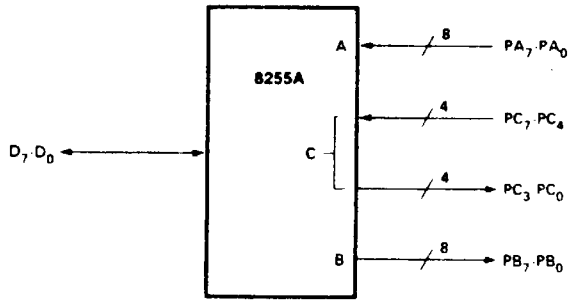
CONTROL WORD =11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



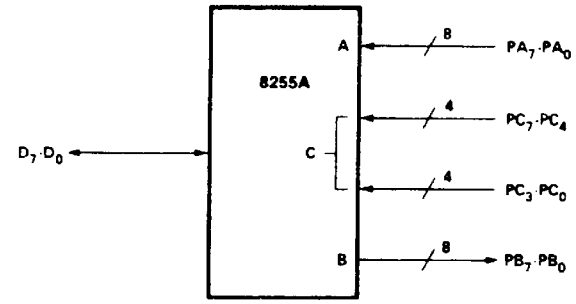
CONTROL WORD =12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



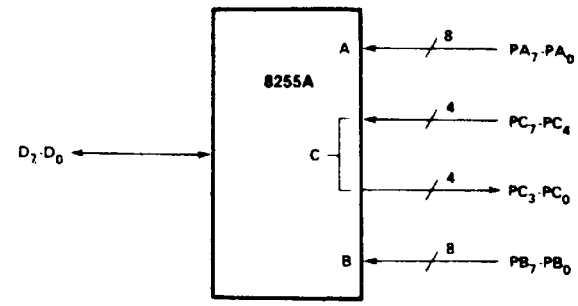
CONTROL WORD =13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



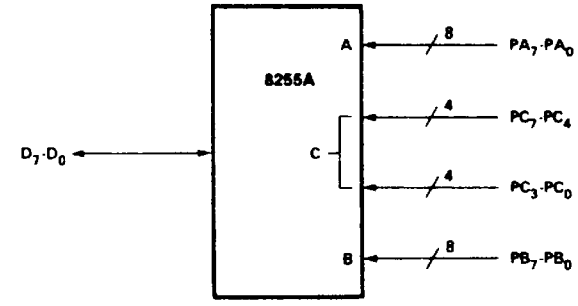
CONTROL WORD =14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



CONTROL WORD =15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Mode 1 provides a means for transferring I/O data to or from a specified port in conjunction with strobe or "handshaking" signals.

MODE 1 Basic Functional Definitions:

- Two Groups, A and B
- Each group contains one 8 bit data port and one 4 bit control/data port
- The 4 bit port is used for control and status of the 8 bit port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

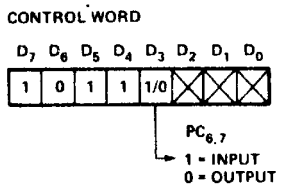
A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

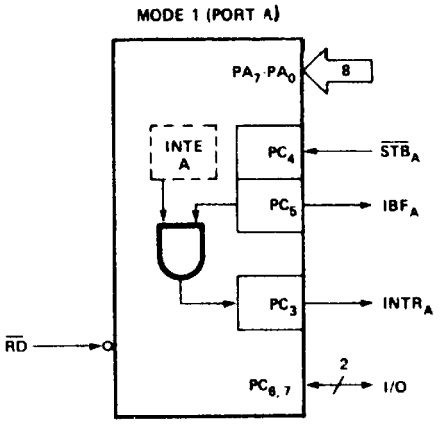
INTE A

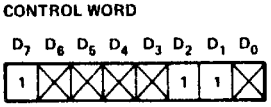
Controlled by bit set/reset of PC_4.

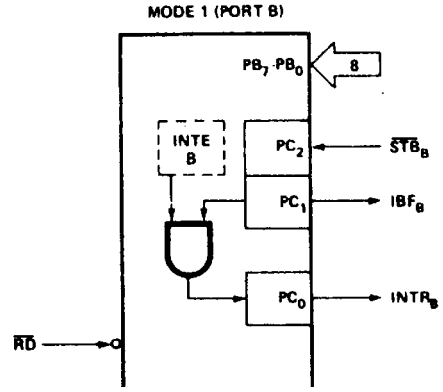
INTE B

Controlled by bit set/reset of PC_2.









Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

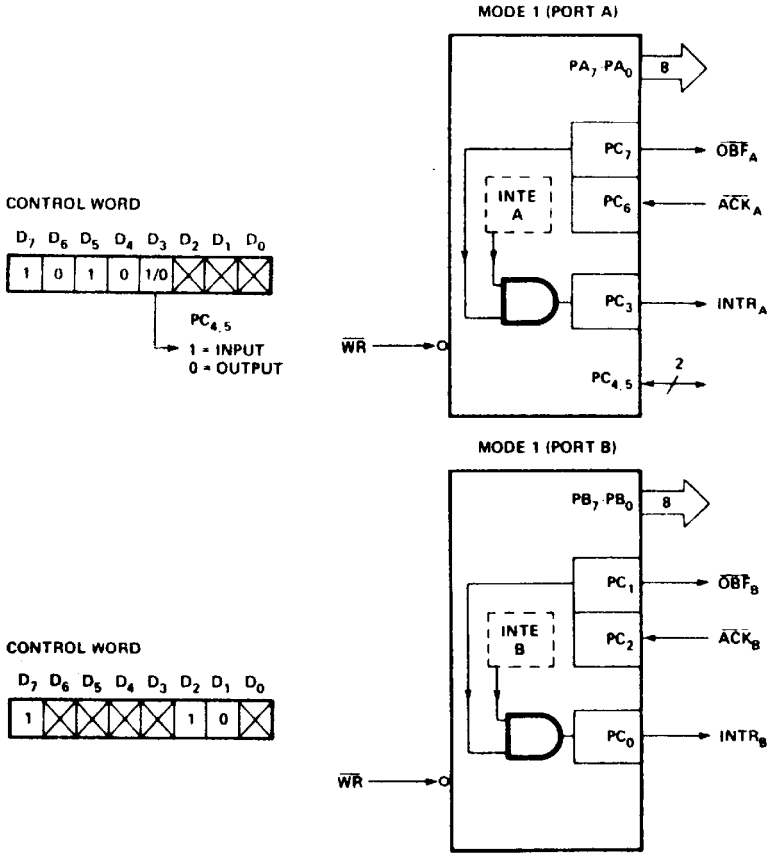
INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.



Mode 2 provides a means for communicating with a peripheral device or structure on a single 8 bit bus. Handshaking signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only
- One 8 bit bi-directional bus (Port A) and a 5 bit control port (Port C)
- Both inputs and outputs are latched
- The 5 bit control port is used for control and status for the bi-directional bus port

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

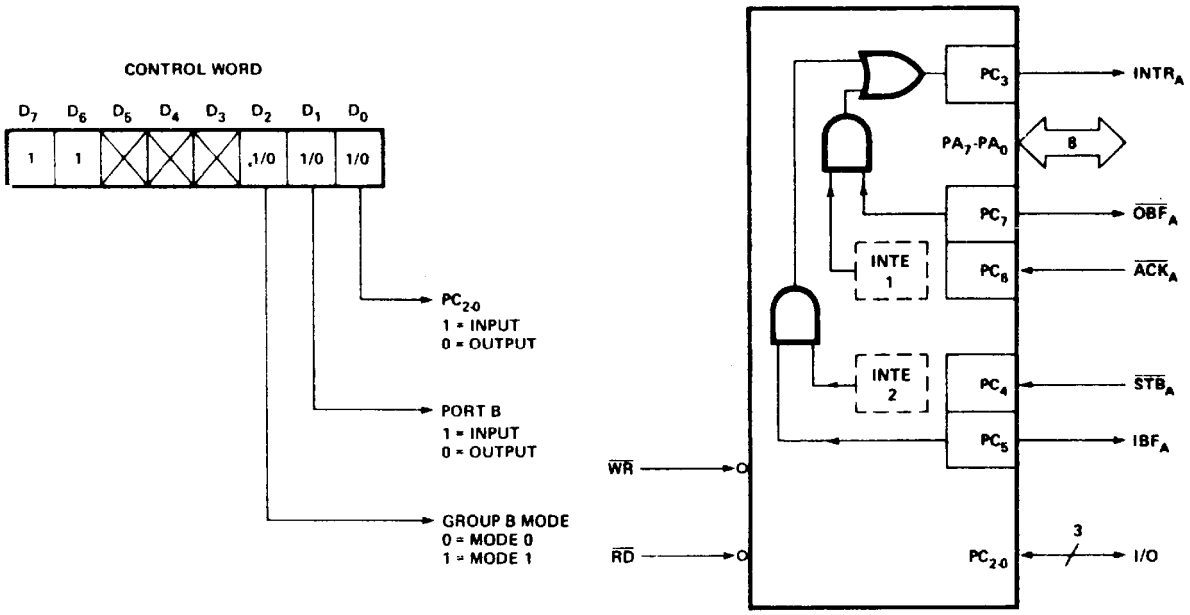
INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

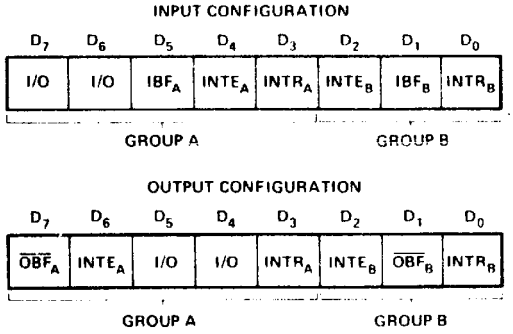
INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.



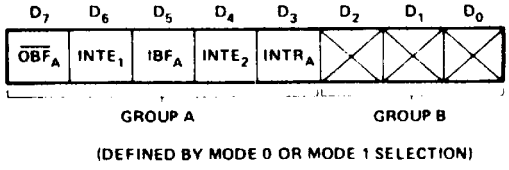
There are several combinations or modes when not all of the bits in Port C of an 8255A are used for control or status.
If programmed as inputs, all input lines can be accessed during a normal Port C read. If programmed as Outputs, bits PC7 to PC4 must be individually accessed using the Bit set/reset function.
Bits PC0 to PC4 can be accessed using the set/reset function or as a threesome by writing to Port C.

Any set of eight output buffers selected randomly from Ports B and C of an 8255A can source 1 ma at 1.5 volts.

Port C generates or accepts hand-shaking signals with the peripheral device in Modes 1 or 2. Reading the contents of Port C in these modes allows the programmer to test the status of the device.

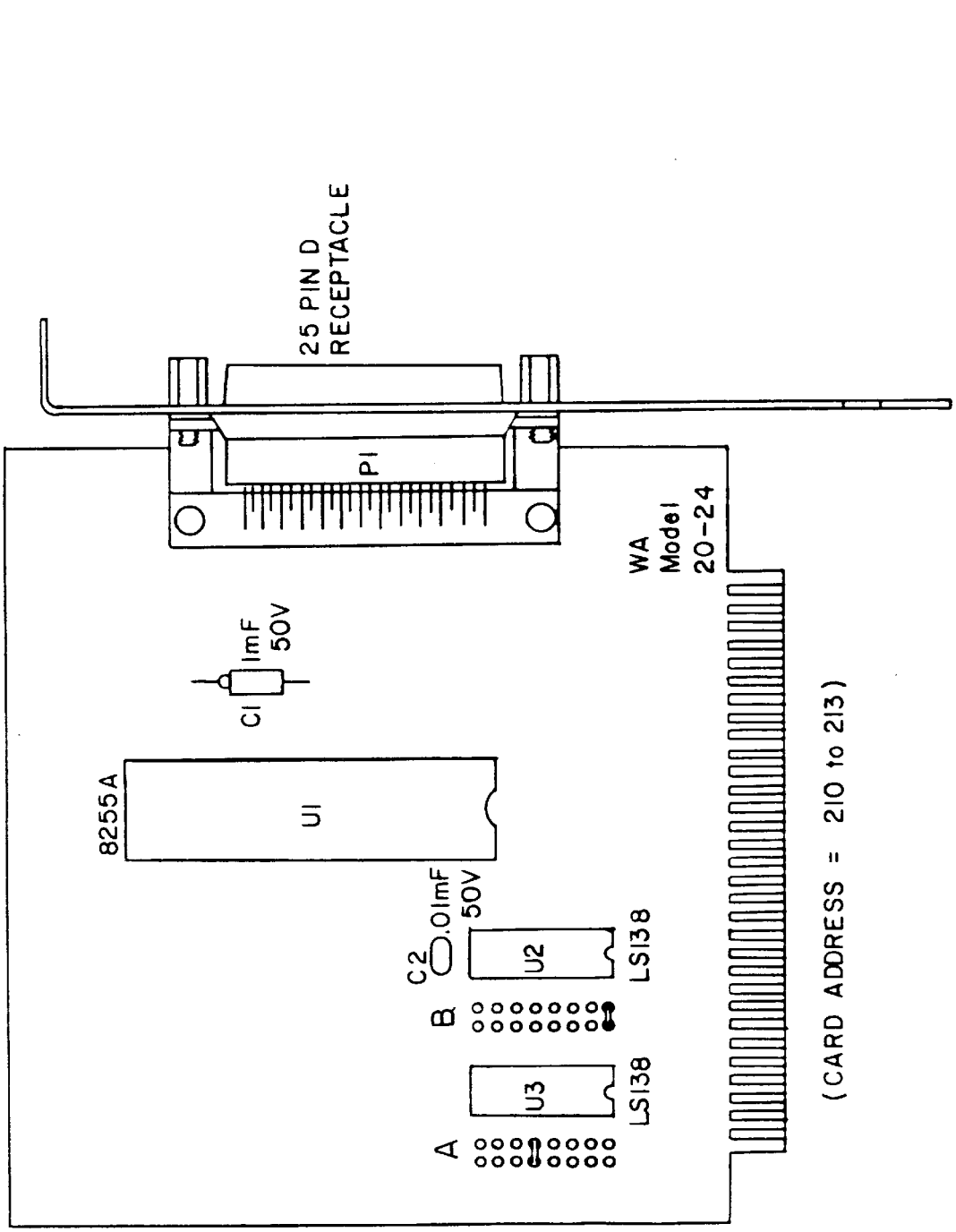


MODE 1 Status Word Format

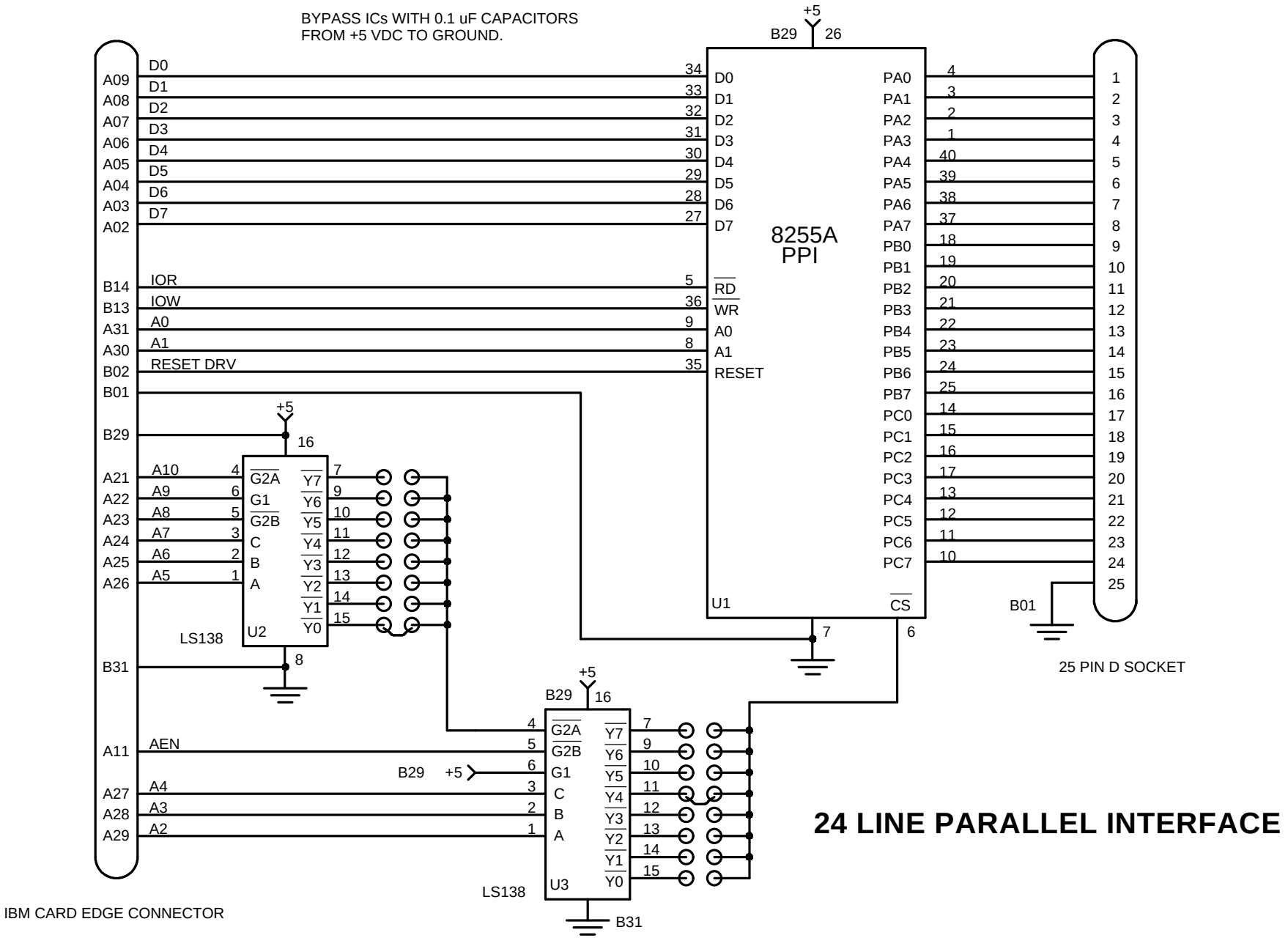


MODE 2 Status Word Format

24 LINE PARALELL INTERFACE



24 LINE PARALLEL INTERFACE


BYPASS ICs WITH 0.1 uF CAPACITORS
FROM +5 VDC TO GROUND.
+5
B29
26
8255A
PPI
U1
D0
D1
D2
D3
D4
D5
D6
D7
RD
WR
A0
A1
RESET
CS
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
A09
A08
A07
A06
A05
A04
A03
A02
B14
B13
A31
A30
B02
B01
IOR
IOW
A0
A1
RESET DRV
B29
B31
A21
A22
A23
A24
A25
A26
A10
A9
A8
A7
A6
A5
G2A
G1
G2B
C
B
A
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0
U2
LS138
16
8
A11
A27
A28
A29
AEN
A4
A3
A2
U3
B01
25 PIN D SOCKET
IBM CARD EDGE CONNECTOR
24 LINE PARALLEL INTERFACE

Mode 0: Get data from interface, send to terminal

```
20 OUT(&H213),&H9B                              :REM all inputs
30 PRINT CHR$(12)                               :REM clear screen
40 A=INP(&H210) : B=INP(&H211)                  :REM get data
50 LOCATE 1,1 : PRINT A + B*256,"      "        :REM convert and display
60 GOTO 40                                      :REM repeat
```

Mode 0: Get data from terminal, send to interface

```
20 OUT(&H213),&H80                              :REM all outputs
30 INPUT X                                      :REM get data
40 B=INT(X/256) : A=INT(X-B)                    :REM convert to 2 binary digits
50 OUT(&H210),A                                 :REM send to port A
60 OUT(&H211),B                                 :REM send to port B
70 GOTO 30                                      :REM repeat
```