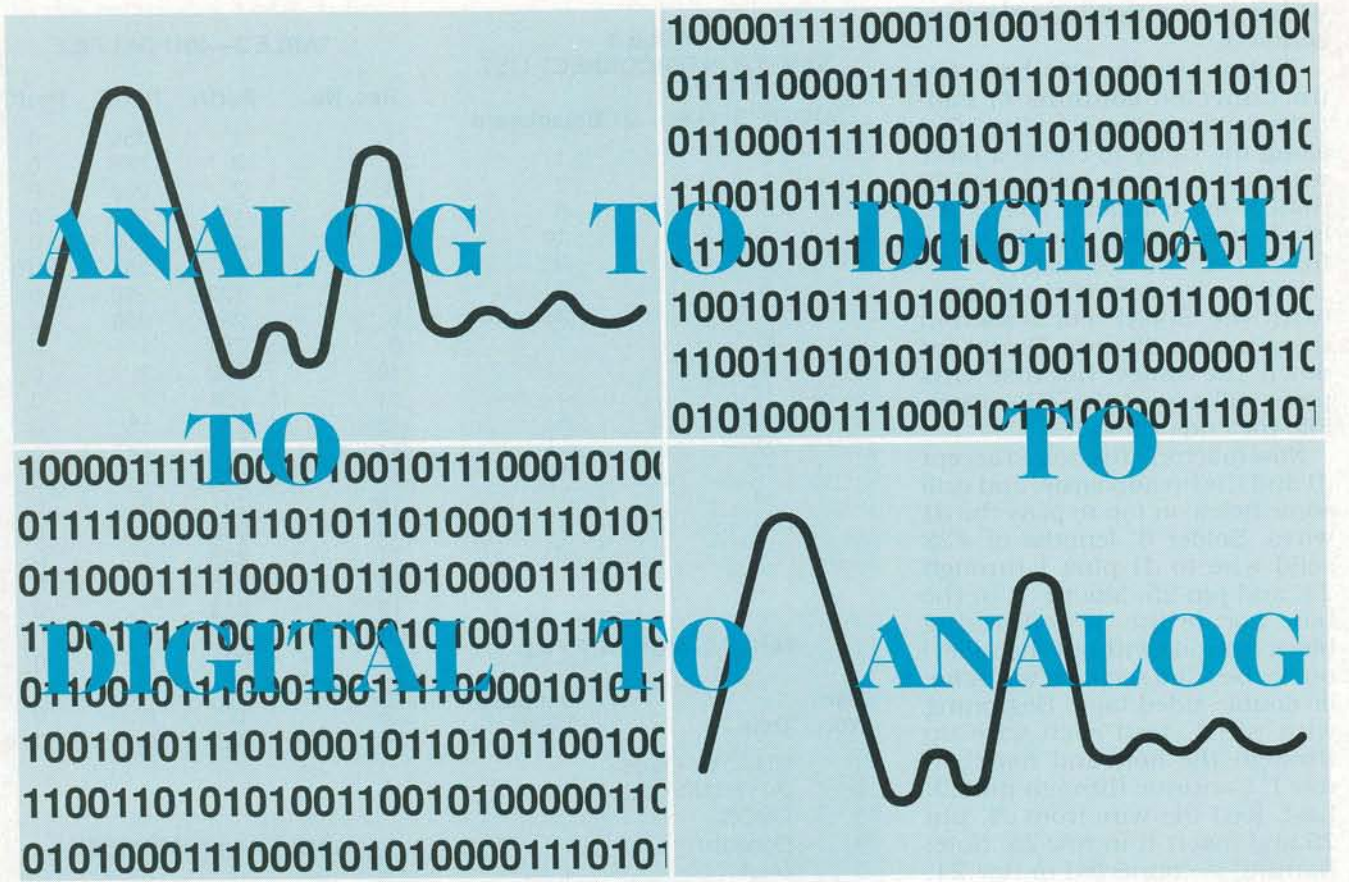


CONVERTERS

Discover the basics of some of the most widely used D/A and A/D conversion techniques.

STEPHEN J. BIGELOW

WE LIVE IN A WORLD OF CONTINUALLY varying analog dimensions, whether we're dealing with sight, sound, temperature, voltage, or current. Most physical and electrical parameters that we perceive change in a continuous manner, taking on an infinite number of values. Although our real-world consists mostly of analog signals, they can be difficult to manipulate. Digital signals, on the other hand, can be controlled by simple logic circuits, or by microprocessors. Complex operations can be more easily performed by digital rather than analog circuits. When digital circuits need inputs from the analog world or must output data to it, digital-to-analog (D/A) and analog-to-digital (A/D) converters become an essential interface.

We will explain some basic techniques of D/A and A/D conversion, as well as the important characteristics of certain types of approaches. We'll also show you some simple circuits with inexpensive, off-the-shelf parts you can easily build yourself.

Digital-to-analog converters

Digital-to-analog converters (DAC's) translate binary words from computers or other discrete circuitry into proportional analog-voltage levels. D/A converters can be used to drive analog devices such as meters, motor controllers, or audio circuitry. Perhaps the most dramatic example of D/A conversion is in a compact disk (CD) player. A DAC is used to convert the digital data recorded on the CD into the high-fidelity audio signal that you hear. Let's look at important D/A concepts.

The resolution of a D/A converter is the number of individual analog voltage levels that the output is capable of generating. That is directly related to the number of input bits that forms the binary word. A 4-bit DAC has 4 input bits with a resolution of 4. The number of distinct and different analog output levels the IC is capable of generating will be 2^n (2^4) or 16 levels. That means the analog output can be represented by up to 16 voltage levels. An 8-bit DAC can provide an analog output at up to 2^8 or 256 discrete levels. A 12-bit DAC can represent a digital word in 2^{12} or 4096 levels. As you can see, the more bits an A/D converter provides, the more accurately it can generate an analog signal, as shown in Fig. 1.

Settling time is the term used for the time required for the ana-

log output to stabilize after the binary input changes. It is usually specified as the time taken for the output to stabilize within ± ½ the least significant bit (LSB) of the expected value after the binary input changes. What that means in practical terms relates to the actual value of the LSB itself. If an 8-bit DAC has a 0 to 10-volt output range, then the LSB is worth $10/2^8$ or 0.039 volts. Half of that value is 0.0195 volts. The settling time would be the time required for the output to reach 0.0195 volts of the expected value. Settling time is typically under 10 μs.

Accuracy is another important factor in D/A converters. In simplest terms, the accuracy of a DAC is usually specified as ± anywhere from ½ to 2 times the LSB. Let's consider that more closely. For a DAC with an accuracy of ± one times the LSB, the voltage output can vary by as much as + or − the value of one bit. If the DAC has a 0- to 5-volt output with 12 bits of resolution, the LSB would be $5/2^{12}$ or 0.00122 volts. For any binary input, the output voltage may be higher or lower than the expected value by 0.00122 volts. If that same DAC has ± ½ times the LSB accuracy, an output could only deviate ± $0.00122/2$ or ±0.00061 volts. The smaller an accuracy value is, the more closely the output will match the expected output.

Several methods have been developed over the years to deal with digital-to-analog conversion. We will look at two generally accepted methods: binary weighted and binary ladder D/A.

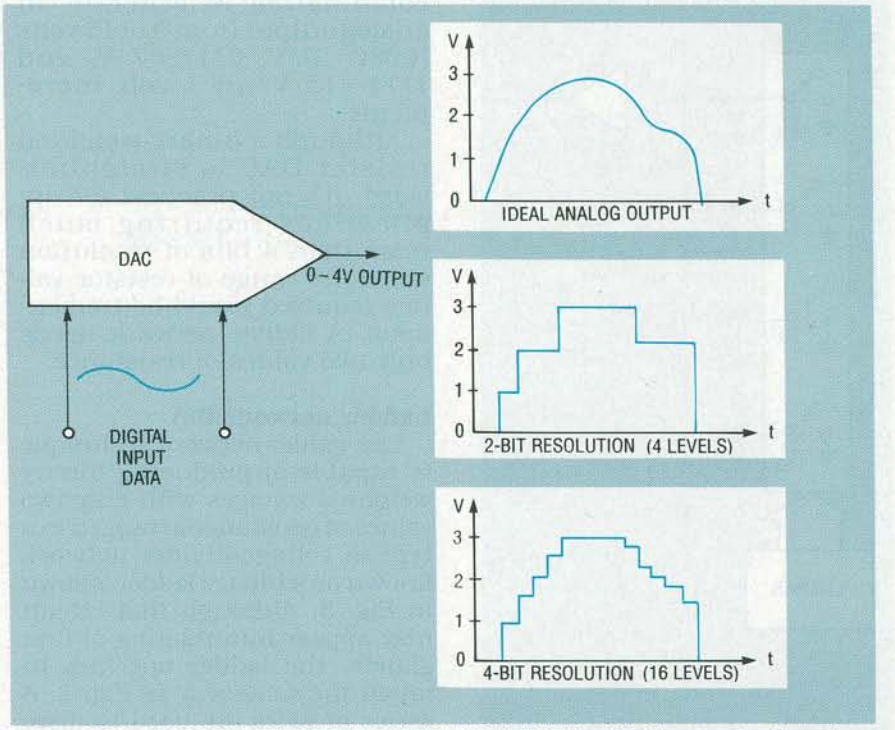


FIG. 1—FINER RESOLUTION OF THE OUTPUT VOLTAGE in a DAC is provided by using a larger number of bits.

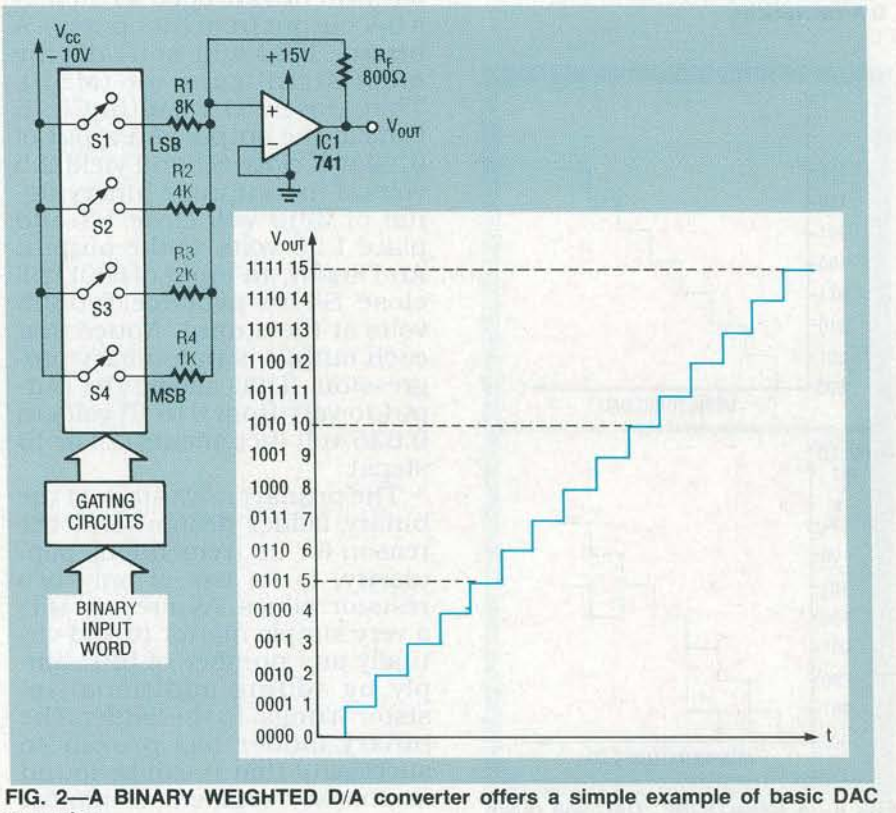


FIG. 2—A BINARY WEIGHTED D/A converter offers a simple example of basic DAC operation.

Binary-weighted resistor D/A

The binary-weighted technique is the oldest and simplest method of converting digital bits into an analog signal. For the circuit in Fig. 2, a binary word is applied to a series of gates that drive analog switches. When a binary ØØØØ is applied to the gates, all analog switches are open so no voltage is applied to the op-amp. The output is then 0 volts. When a binary ØØØ1 is applied, S1 closes and −10 volts is applied to R1. Since the op-amp input represents a virtual ground, there is effectively 10 volts across the 8K resistor. That causes 10 V/8000 Ω, or 1.25 mA, to flow through the 800-ohm feedback resistor, R_F. By Ohm's law, the voltage across R_F would be 800 ohms × 1.25 mA, or 1 volt.

When the binary word changes to ØØ1Ø, S1 opens and S2 closes. That causes 2.5 mA (10 V/4000 Ω) to flow through R2. The voltage across R_F is then 800 ohms × 2.5 mA, or 2 volts. A binary Ø1ØØ would result in 4 volts at the output, and a binary 1ØØØ would cause 8

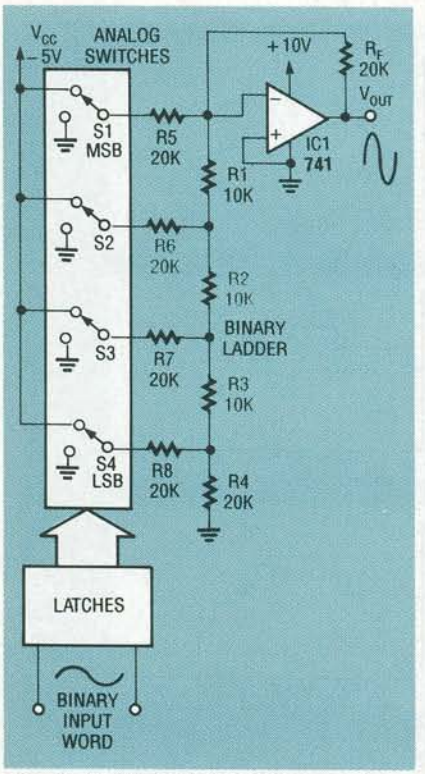


FIG. 3—A-BINARY LADDER provides a simple, reliable, and accurate method of D/A conversion.

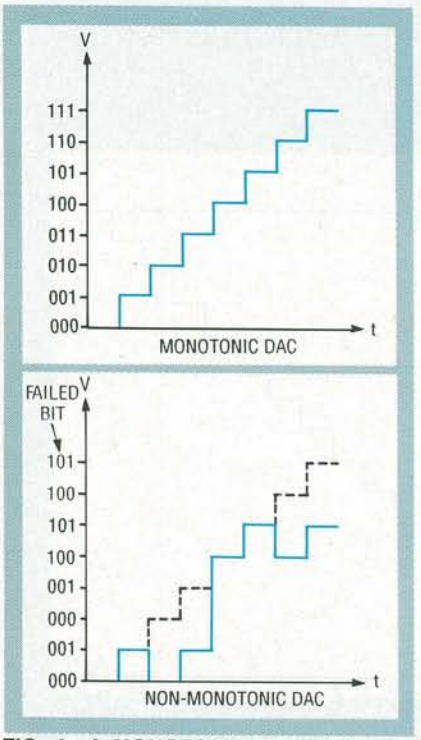


FIG. 4—A MONOTONIC DAC will reach every analog step correctly for each digital input word.

volts at the output. Notice how the value of input and feedback resistors are carefully chosen to create a binary progression. Each switch can be closed in combination to generate an analog output from 0 to 15 volts (ØØØØ = 0 V, Ø111 = 7 V, and 1111 = 15 V) in 1 volt increments.

Although a binary-weighted resistor DAC is straightforward, it's not practical for applications requiring much more than 4 bits of resolution since the range of resistor values required would be tremendous. A ladder network needs only two values of resistance.

Ladder network D/A

The ladder-network technique is capable of producing binary weighted voltages with only two values of resistance arranged in a type of voltage-divider network known as a binary ladder, shown in Fig. 3. Although that circuit may appear intimidating at first glance, the ladder operates in much the same way as Fig. 2. A series of gates are used to drive analog switches. When a binary ØØØØ is sent to the gates, all analog switches are open so there is a 0-V output from the op-amp. A binary 1ØØØ will activate the most significant bit (MSB). That closes S1 resulting in 5 volts at the output. An input of ØlØØ will close S2 and yield 2.5 volts at the output. A binary signal of ØØlØ will close S3 and place 1.25 volts at the output. And finally, an input of ØØØ1 will close S4 to produce 0.0625 volts at the output. Notice that each output is in a binary progression. That allows the output to vary from 0 to 10 volts in 0.625-volt increments (24 or 16 steps).

The primary advantage of the binary ladder design (and the reason for its tremendous popularity) is its use of only two resistor values. As a result, it is a very simple matter to add virtually any number of bits simply by adding additional resistor "rungs" to the ladder. The binary ladder has proven so successful that it can be found as the key segment of almost every DAC manufactured today.

Binary ladders also tend to be more accurate than binary weighted circuits since it's much easier to find precision resistors in two values (such as 10K and 20K) than the many diverse values that would be required in a binary weighted circuit. Conventional D/A converters integrate resistors and amplifiers onto a single IC, such as Precision Monolithic's DAC-08.

Now that we've discussed the basic approaches of DAC operation, we can examine a final important specification of monotonicity. As you know, the analog output voltage of a DAC will progress in steps as the binary input word increments, as shown in Fig. 4. Ideally, each increment in the binary input will cause a known, predictable step in the output voltage. In some devices, however, the switching and amplifier components do

TERMS AND DEFINITIONS

- **Accuracy—A figure indicating how closely the converter's output represents the input information, usually expressed as a portion of the LSB.**
- **Binary Coded Decimal (BCD)—A binary numbering system using binary codes 0 through 9 only, instead of 0 through F. That allows a closer relationship between digital data and decimal numbers.**
- **Comparator—An op-amp circuit used in ADC's to compare the analog input signal to a reference voltage.**
- **Conversion Time—An ADC term used to indicate the amount of time required for the analog input voltage to be converted to a digital word.**
- **Integrator—An op-amp circuit used in some ADC's to provide stable voltage-ramp performance for slope conversion.**
- **Least Significant Bit (LSB)—A digital bit which carries the least binary weight in the digital word.**
- **Monotonicity—A DAC term used to indicate that each analog output step will be correct for every corresponding digital input word.**
- **Most Significant Bit (MSB)—A digital bit which carries the greatest binary weight in a digital word.**
- **Quantizing Error—Error introduced into an A/D conversion when the analog input changes during the conversion cycle. The amount of error depends on the rate of signal change and the conversion time.**
- **Resolution—The number of discrete digital states (usually expressed as 2^n bits) that are used to express an analog signal.**
- **Settling Time—A DAC term used to express the amount of time required for the analog output to stabilize after the digital input has changed.**

not allow enough current to flow under all conditions. That can cause the DAC to "skip" steps at certain bit levels. While a monotonicity problem on a low-weight bit may have little impact on the output, the effects become more significant as the weight of the bit increases. A DAC is said to be monotonic if it does not miss any steps across the entire range of binary inputs. Now let's look at more involved A/D converters.

Analog-to-digital converters

An analog-to-digital converter (ADC) is used to translate a continuous analog signal into a finite number of digital bits. The resulting digital "word" becomes the binary representation of the analog level at the moment it was converted.

The resolution of an ADC is very much like its DAC counterpart—it is the number of bits with which the ADC will represent the analog signal. An ADC with 4 bits will have a resolution of 4 bits, and can represent an analog signal with up to 2^4 or 16 binary words. An 8-bit ADC can represent an analog signal with up to 2^8 or 256 discrete words. A 12-bit ADC can represent an analog signal with as many as 2^{12} or 4096 individual binary words. You probably get the picture. The more bits of resolution by now an A/D converter can provide, the more accurately it will represent the analog signal, as shown in Fig. 5.

Conversion time is another important aspect of A/D converters. As you will see, the conversion of an analog signal into a digital word is not an event, but a precise, deliberate process. As a result, it requires some finite amount of time to sample the analog input, digitize it, then make the binary result available at the output. The conversion time is the period of time required to complete that process. It can range anywhere from microseconds (for very fast converters) to milliseconds (for slower devices). Since A/D conversion is a precise synchronized process, a clock source is also needed in most devices.

Sampling theory

Since an ADC requires a certain amount of time to perform a conversion, there are only just so many samples of a signal a converter can digitize in any given time. For example, if an ADC makes one conversion in 1 ms, it could then theoretically make 1000 conversions in 1 second (1/.001 s). The maximum conversion rate is equal to the reciprocal of the conversion time.

To digitize a faithful representation of the analog input, the converter takes samples at a minimum of twice the maximum frequency component of the analog input signal. That sampling rate is also known as the Nyquist rate. Consider an analog sine wave of 10 Hz applied to an ideal ADC in Fig. 6. The minimum sampling rate is 2*f*, or 20 Hz, which yields two digital-data points for each cycle. When the digital data is reconstructed by a DAC, the new analog signal bears a resemblance to the original. (A filter on the DAC output smooths

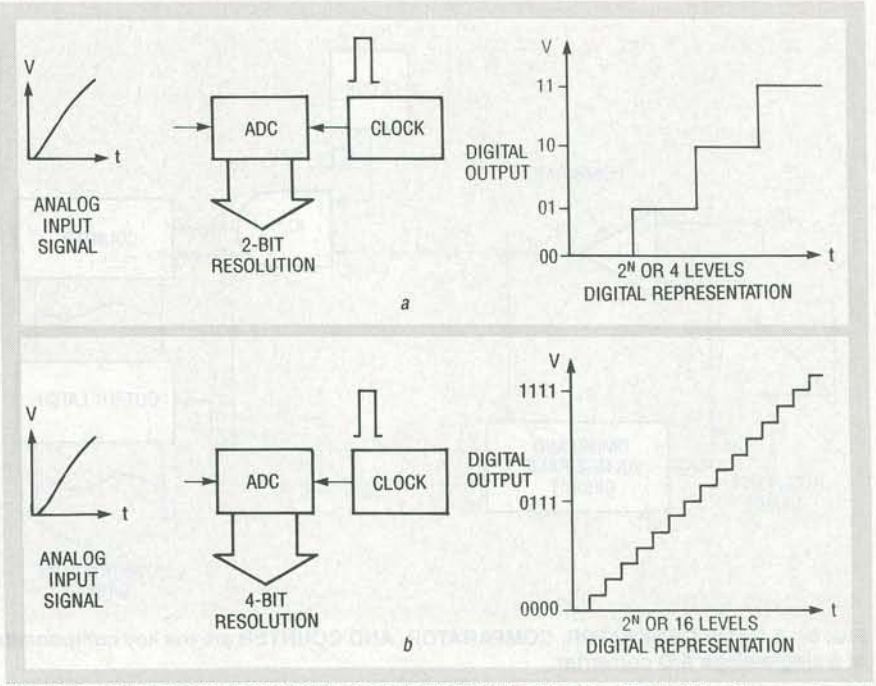


FIG. 5—THE RESOLUTION OF A/D CONVERTERS is directly affected by the number of bits.

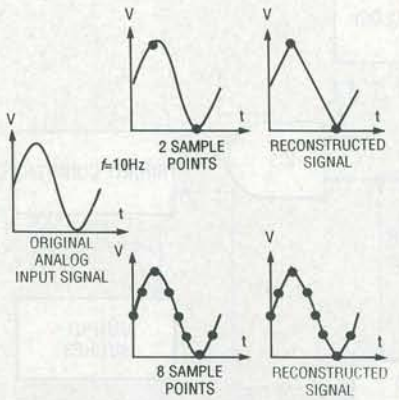
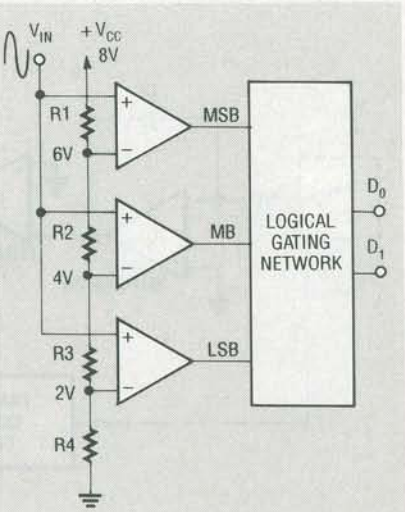


FIG. 6—THE MORE SAMPLE POINTS taken from an analog signal, the more closely a reconstructed signal will resemble the original.



V_{IN}	BINARY OUTPUT		COMPARATOR OUTPUT		
	D_1	D_0	MSB	MB	LSB
0–2V	0	0	0	0	0
2–4V	0	1	0	0	1
4–6V	1	0	0	1	1
6–8V	1	1	1	1	1

FIG. 7—THE FLASH A/D CONVERTER offers speed and simplicity of operation at low resolutions.

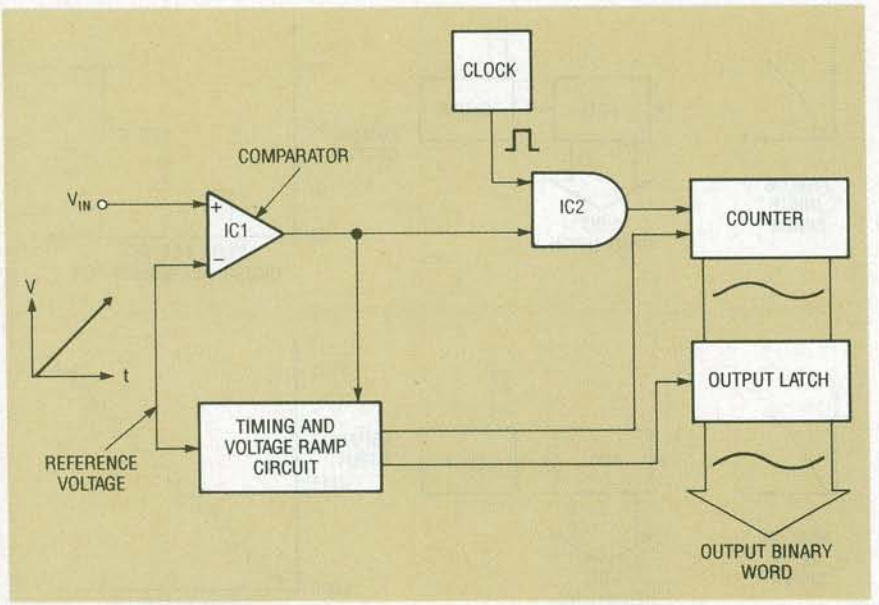


FIG. 8—A RAMP GENERATOR, COMPARATOR, AND COUNTER are the key components of a single-slope A/D converter.

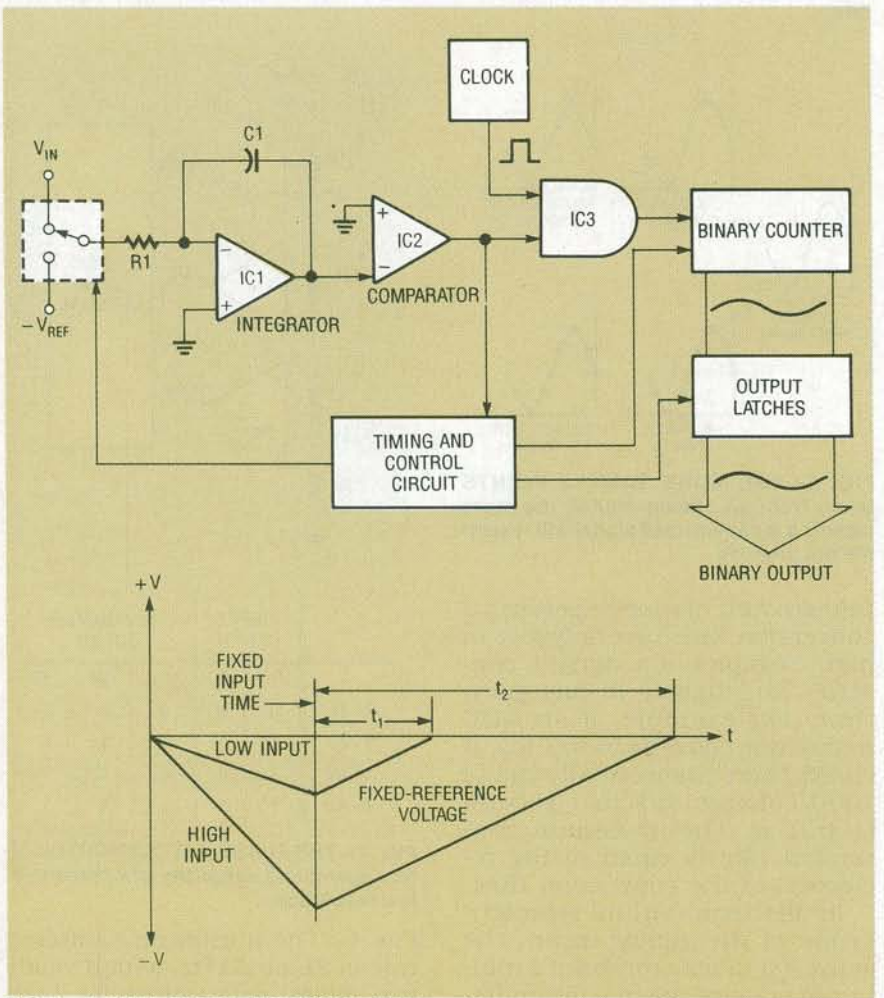


FIG. 9—A DUAL-SLOPE A/D CONVERTER provides much more stable operation than the single-slope converter.

the sharp peaks of the reconstructed signal.) If 10 Hz is the maximum frequency entering the ADC, the maximum allowable conversion time is 1/20 Hz, or 500 ms. If the maximum input frequency is raised to 10 kHz, the ADC needs to sample at 2*f*, or 20 kHz to maintain the same two data points per cycle. That means the converter has to perform conversions in 1/20,000 Hz, or 500 μs just to keep up with the input signal.

To improve the fidelity of the digitized signal, we could take more samples in the same period of time. A sample rate of 8 points per cycle requires a sample rate of 8 times the maximum frequency component of the input signal. An input of 10 Hz must be sampled at 80 Hz, so the converter would have to convert a point in 1/80 Hz or 12.5 ms. A 100-kHz signal needs to be sampled at 800 kHz. The ADC then converts a sample in 1/800,000 Hz, or 1.25 μs. That is extremely fast for most A/D converters, although there are some types which can approach 1-μs conversion times. If the ADC cannot sample fast enough to keep up with the signal, information contained in the analog input signal will be lost.

The relationship between input frequency, conversion time, and sample rate is a very important one. A variety of methods have been developed over the years to perform the digitizing of analog signals. Many are still in use today in one form or another. We will examine six of those techniques: flash, single slope, double slope, single counter, tracking counter, and successive approximation.

Flash conversion

The flash converter is the fastest type of A/D converter that is available (Fig. 7). It uses a bank of parallel comparators to process the analog input. Flash converters are also referred to as parallel converters. A series of resistors form a voltage-divider network across each comparator. The maximum input voltage that can be translated depends on the value of V_{CC}. The output signal from each comparator is either on or off, and is compatible with digital logic.

With no input voltage, the output of each comparator is logic low. As the input voltage increases, the output of each comparator will cascade high as the input exceeds each reference

voltage set by the voltage-divider network. A network of digital gates is used to convert the array of comparator signals into a binary word which is made available at the converter's output.

Our example in Fig. 7 provides only two bits of resolution. A 2-bit ADC is not very practical for most applications, but it demonstrates the key concepts needed to build a flash converter. As you may have noticed from the circuit in Fig. 7, it takes 2^{n-1} comparators to support the resolution of the converter. Our 2-bit ADC example requires 2^2-1, or 3 comparators; a 4-bit converter needs 2^4-1, or 15 comparators; an 8-bit flash ADC needs 2^8-1, or 255 comparators, and so on. This vastly increasing complexity is a great disadvantage in flash devices—not only in the need for additional comparators, but also in the unwieldy gating circuitry as well.

The main advantage to flash converters, of course, is simple speed. Since the analog input is applied to every comparator simultaneously, the conversion time is merely equal to the propagation delay of the comparators and gating circuitry. A flash conversion can be accomplished in just a few microseconds.

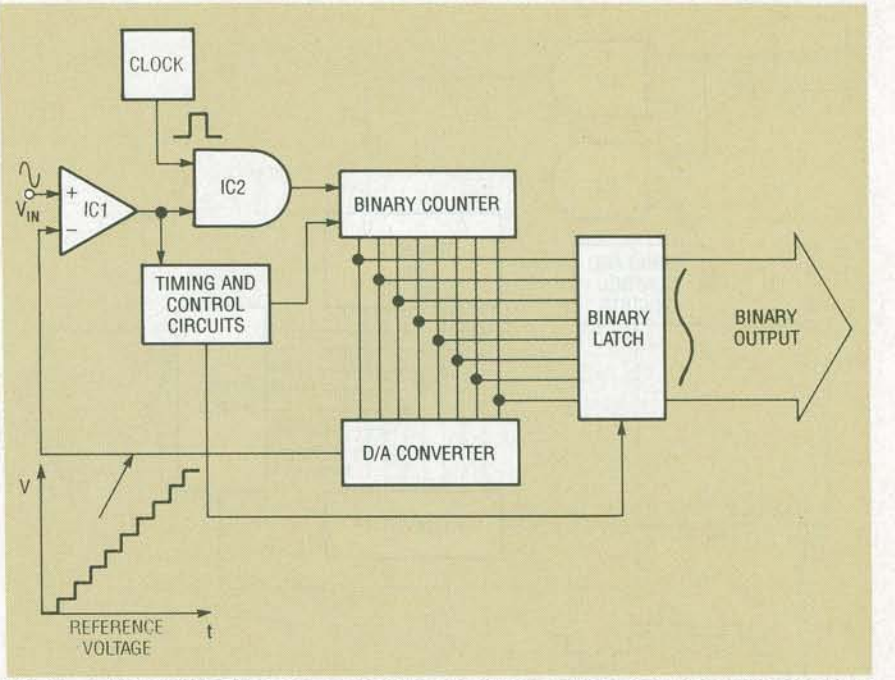


FIG. 10—A D/A CONVERTER can be used to provide the voltage ramp needed to operate a single-counter A/D converter.

Single-slope ADC

A more efficient method of A/D conversion is the single-slope A/D, also known as the single-ramp A/D (Fig. 8). In the single-slope circuit, the cycle begins with the counter reset and the ramp voltage at zero. The comparator's output at that point is low, so no clock signals are allowed to reach the counter. When an input voltage is applied to the converter, the comparator's noninverting input (+) will exceed the voltage at the inverting (−) input, so it's output will be high. That will enable the AND gate, which will allow clock pulses to reach the binary counter. At the same time, a timing circuit drives the voltage ramp up, which quickly increases the reference voltage on the comparator's inverting input. When the reference-ramp voltage just exceeds the input voltage, the comparator's output falls low again. The clock pulses stop and the timing circuit latches the count at the binary counter and resets the counter for the next conversion.

The single-ramp circuit is little more than a controlled counter with a voltage-feedback loop. The circuit is timed in such a way that when the reference-ramp voltage equals the applied input voltage, the binary count existing on the counter at that moment is the digitized value of the analog signal. Note that the speed of the clock and the rate of the voltage ramp must both be set correctly for the counter to function properly.

The time required to perform a conversion will depend upon the level of the analog input. Since the counter and reference ramp both start from zero at each conversion, it will take longer to match a higher level of analog input than a low level. The sequence of operations can take place very quickly. The reference-ramp voltage can change faster than 1 volt per ms to reach the input voltage. For example, if an input of 2 volts is applied to the circuit in Fig. 8, it would take 2×1 volt/ms, which equals 2 ms for the ramp voltage to equal the input. The actual binary count after 2 ms depends on the speed of the clock. A faster clock speed will yield a higher count, and vice versa.

Since the clock can operate independent of the voltage ramp, unique opportunities for other outputs besides straight binary become available. Some customized instrument IC's use single-slope techniques to convert an analog input directly to binary coded decimal (BCD) to drive 7-segment displays. That type of flexibility is a strong advantage. The primary disadvantage of using single-slope techniques is the tendency toward unstable operation over time. Without some form of synchronization between the clock and ramp generator, any drift in clock speed or ramp voltage performance will cause errors in the output word. That's why single-slope converters are not used in high precision applications.

Dual-slope ADC

The dual-slope conversion technique offers the advantage of conversion stability at the expense of conversion speed. The reference-ramp generator circuit eliminates the effects of component drift over time (Fig. 9).

The input signal of a dual-slope converter is fed into an integrator. When a positive input signal is applied, the integrator's output voltage ramps in the negative direction. The negative voltage forces the output of the comparator high. That in turn activates the clock input to the counter which will begin to incre-

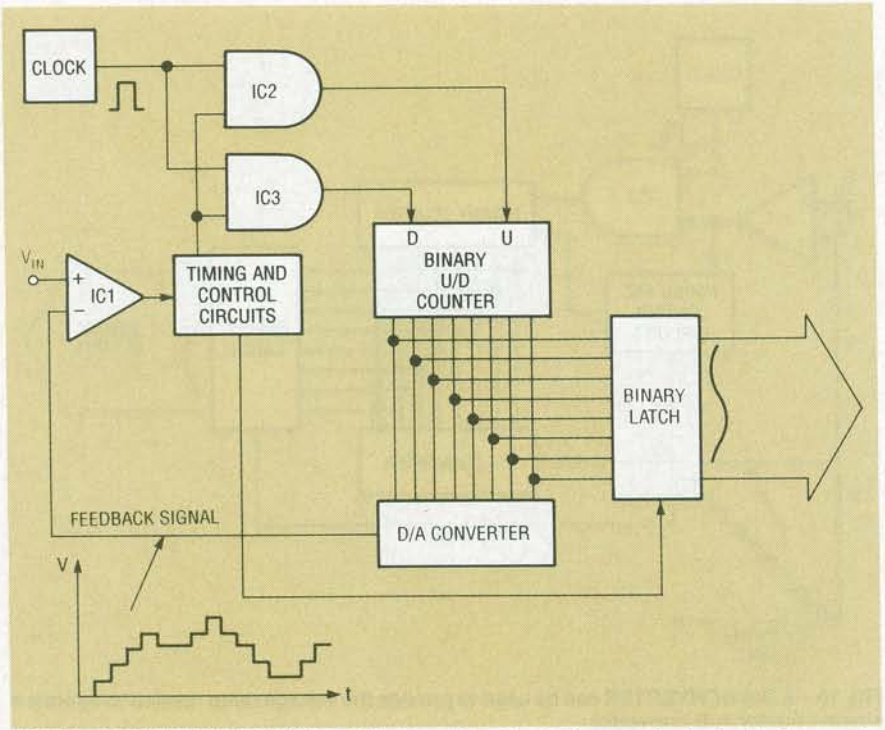


FIG. 11—A BINARY UP/DOWN COUNTER enables the A/D converter to track changes in the analog input for the tracking-counter A/D.

ment. The integrator will ramp for only a fixed period of time. After that fixed "input-time," the control circuit clears the counter and switches the converter's input to a fixed negative-reference voltage ($-V_{REF}$). With a negative voltage now applied to the integrator, its output ramps back in the positive direction. The counter begins a new series of counts until the integrator's output reaches zero. At that point, the comparator's output becomes low. That action shuts off the clock pulses to the counter. Control circuitry detects that change and latches the count to the output, then clears the counter. As with the single-slope converter, the final digital count represents the analog-input voltage.

The rate of integration depends on the magnitude of the input voltage, as well as the value of R1 and C1, so a low input voltage will reduce the integrator's output less than a high input voltage during the same fixed-input period of the conversion cycle. When a fixed negative reference voltage is applied (the values of R1 and C1 remaining constant), the time required for the integrator to return to zero is then directly proportional to the original magnitude of the input voltage. Any variations, therefore, in the integrator circuit due to time or temperature will automatically be canceled out. That allows the dual-slope converter much more stability for high-precision applications. Similar to the single-slope technique, dual-slope converters can be used to convert the input signal directly to BCD (or any other viable code) as well as regular binary. Most quality digital voltmeters use dual-slope conversion to translate the input directly to BCD.

The disadvantage of dual-slope conversion is the extended period of time needed to make a conversion. A dual-slope converter may require more than 100 ms to translate a high input voltage.

D/A feedback converters

D/A converters may also be used to provide the reference feedback signal to the comparator. There are two basic types that we will examine: single-counter and tracking-counter types. Let's take a brief look at each one.

The single-counter A/D converter is a variation of the single-slope approach. Its operation is identical in all aspects but one—a D/A converter is used to read the count from the binary counter and provide a feedback voltage to the comparator instead of an integrator or other voltage-ramp source (Fig. 10).

When an analog input is applied to the comparator, its output becomes high. That allows clock signals to reach a binary counter. As the counter increments, the voltage output of the DAC increases at the negative input to the comparator. When the DAC level just exceeds the input, the comparator shuts down. A control circuit latches the binary count to the output, as well as resets the counter for the next conversion.

Although single-counter conversion is a faster method than the dual-ramp approach, it does require the use of a high-precision DAC to provide a steady, accurate feedback signal to the comparator. It also requires the counter to start from zero at each conversion. That can waste a bit of time through each cycle, especially if the voltages to be converted are near their maximum levels.

The tracking-counter technique can yield conversions much faster than the single-counter. That is possible by the use of a binary up/down (U/D) counter instead of just an up counter like the ones used in our previous examples. The counter can increment or decrement depending on the state of the comparator's output. That permits the binary word to literally track the changes in the analog signal (Fig. 11).

The cycle begins with an analog signal to the comparator. The count on the binary U/D counter may be at any value. That means that the DAC feedback voltage may be greater or less than the analog input. If the feedback voltage is greater than the analog input, the comparator's output will be low and the control circuits will gate the clock pulses to the count-down input of the counter. That will decrement the binary counter's output and reduce the feedback voltage at the comparator. When feedback voltage drops below the analog input, the comparator's output will go high and control circuits will cause the binary count to latch to the output. Gating will send clock signals to the up input of the counter (which is not reset) and cause it to begin counting up

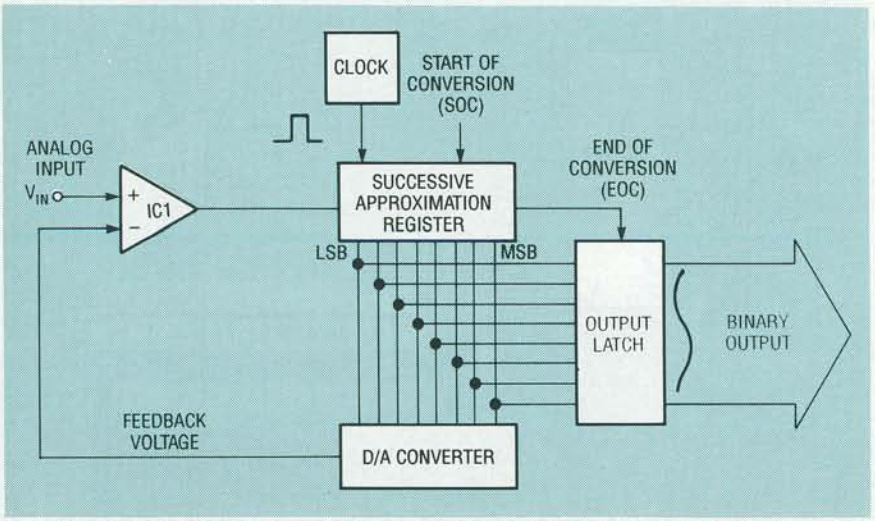


FIG. 12—A SUCCESSIVE APPROXIMATION REGISTER (SAR) speeds up the process of A/D conversion.

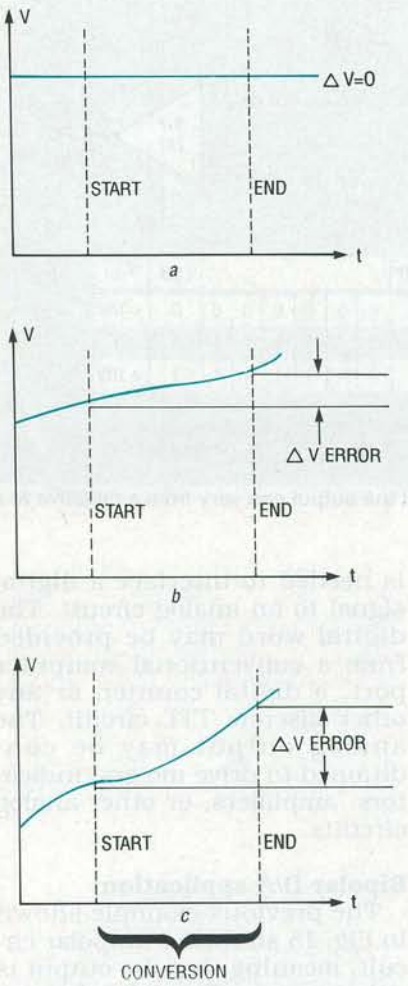


FIG. 13—QUANTIZING ERROR can enter the A/D conversion as the analog signal changes during the conversion cycle. No quantizing error exists for a DC voltage (*a*) because there is no change in voltage, some quantizing error occurs with low-frequency signals (*b*), and a higher degree of quantizing error is produced with high-frequency signals (*c*).

again looking for another change of state. If the input signal remains constant, the output word will tend to oscillate by 1 × LSB as the converter tries to center itself. That potential oscillation problem is the greatest disadvantage of tracking-counter ADC's.

As you might imagine, this type of converter can be much faster than the single-counter technique, but it is best suited for digitizing fast-changing analog inputs. Signals which change quickly are less likely to allow the converter to oscillate.

Successive-approximation ADC

Of all the techniques that we have covered up to now, the successive approximation (SA) approach has become the technique of choice for low-cost, moderate-resolution, high-speed A/D converters. Successive approximation is a clever and powerful technique that can be used to digitize an analog signal quickly and efficiently with no oscillation. The process of conversion is a bit more involved than the counter techniques that we have discussed.

The heart of the SA converter is a device called the successive approximation register (SAR). This serves a very different purpose than the counters we have seen (Fig. 12).

The conversion cycle begins when an analog signal is applied to the converter and a start conversion pulse is placed on the SAR. The first clock pulse into the SAR turns on the MSB output. That in turn sets the DAC output to 50% of its voltage output. The SAR looks at the comparator's output to see if the DAC output is greater or less than the analog input. If the DAC voltage is greater, the comparator will be off, so the SAR will turn off the MSB and call it a zero. If the DAC voltage is less than the analog input, the comparator will remain on, so the SAR will leave the MSB on and call it a one. It does all of this in one clock pulse. On the next clock pulse, the SAR will turn on the second most significant bit and re-check the results from the comparator. Once again, if the new DAC signal is greater than the input voltage, the comparator output will be off, so the SAR will turn off the bit and call it zero. If the new DAC signal is less, the comparator will remain on, and the SAR will leave the bit on as a one.

The SAR will examine each bit in this fashion (MSB to LSB) until all bits have been examined. Since one bit is evaluated in one clock pulse, an 8-bit ADC will process the conversion in only 8 clock pulses. When the LSB is finally processed, the SAR will send out an end of conversion (EOC) signal which will latch the

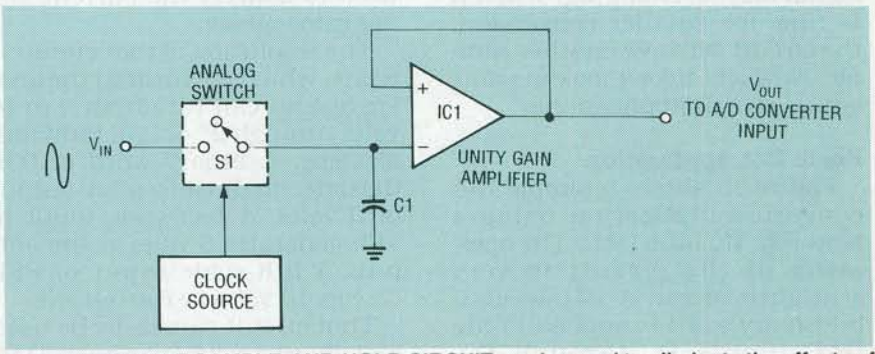


FIG. 14—A SIMPLE SAMPLE-AND-HOLD CIRCUIT can be used to eliminate the effects of quantizing error.

resulting binary word directly to the output.

Successive approximation converters are perhaps the most efficient type of A/D converters available. They are capable of extremely fast conversions at high resolutions. Many converters of this type can process 12 bits of resolution in less than 10 μs.

Quantizing error

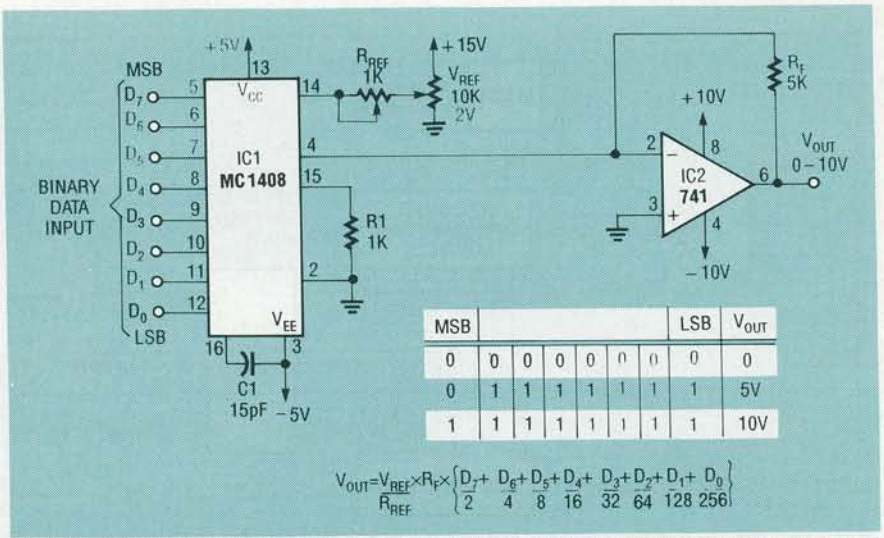
Now that you have a better idea of how A/D converters operate, we will discuss the characteristic of quantizing error. Quantizing error is caused by changes in the analog-input level during the conversion process.

Remember that the analog signal of an ADC is applied to a comparator. When a cycle is started, it requires some finite amount of time (microseconds to milliseconds) to produce a digital output. If the input voltage changes during the conversion, the final binary output will represent the voltage level at the end of the cycle instead of the beginning. When there is no change in input voltage, such as in a DC voltage, no quantizing error enters into the conversion, as shown in Fig. 13-a. The faster the signal change, or "slew rate," the greater the quantizing error will be (Figs. 13-b, 13-c).

One common way of avoiding quantizing error is to use a sample and hold circuit before the analog input to the comparator. Figure 14 shows such a circuit. An electronic switch is closed to take a rapid sample of the analog input signal. The sample capacitor C1 charges to the value of the input signal and the electronic switch will open. That eliminates the effects of quantizing error since the capacitor will retain the value of the analog sample regardless of how the overall analog signal may be changing. When it is time for another conversion, the circuit will take another sample. Now lets take a look at some actual circuit applications.

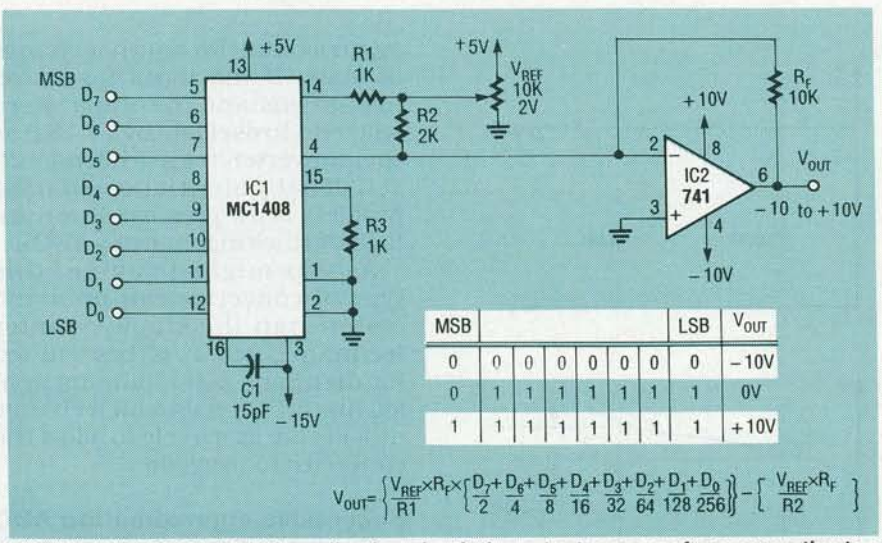
Basic D/A application

Figure 15 shows a simple D/A converter application using a Motorola MC1408 DAC. The operation of the circuit is very straightforward. A TTL-level 8-bit binary word is applied to the DAC inputs D_0 through D_7.



MSB							LSB	V_{OUT}
0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	5V
1	1	1	1	1	1	1	1	10V

FIG. 15—A UNIPOLAR D/A application circuit. An 8-bit binary word is applied to the DAC input. A binary ladder is used in the MC1408 to translate the signal into a current output, an op-amp is then used to convert the current into a voltage signal.



MSB							LSB	V_{OUT}
0	0	0	0	0	0	0	0	−10V
0	1	1	1	1	1	1	1	0V
1	1	1	1	1	1	1	1	+10V

FIG. 16—IN A BIPOLAR D/A application circuit the output can vary from a negative to a positive voltage.

Since no clock or outside timing is required, the conversion takes only the settle time of the MC1408 (about 300 ns). The MC1408 uses a binary ladder to switch and translate the signal into a current output. An op-amp, such as the LM741, can be used to convert the current signal into voltage.

The resolution of that circuit is 8 bits, which means that the analog output can vary from 0 to 10 volts through 2^8 or 256 individual steps. A binary word of 00h (hexadecimal) causes an output of 0 volts. A half-scale input of 7Fh generates 5 volts at the output. A full-scale input of FFh causes 10 volts at the output.

That circuit can easily be used just about anywhere a basic DAC is needed to interface a digital signal to an analog circuit. The digital word may be provided from a conventional computer port, a digital counter, or any other discrete TTL circuit. The analog output may be conditioned to drive meters, indicators, amplifiers, or other analog circuits.

Bipolar D/A application

The previous example shown in Fig. 15 showed a unipolar circuit, meaning that the output is only in one polarity. If a bipolar output is needed (one that varies from a negative to a positive voltage) the circuit can be changed as shown in Fig. 16.

Connecting the input of the op-amp to the reference resistor R2

TABLE 1—POPULAR 8-BIT CONVERTERS

Component	Type	Description	Resolution	Conversion Time	Settling Time	Supply Voltages	Price*
MC14433P	A/D	Dual Slope	3½ Digits	40ms	—	+5, +8	$7.00
MC14443P	A/D	Single Slope	8 bits	300ms	—	+5, +8	$4.00
MC14447P	A/D	Single Slope	8 bits	300ms	—	−5, +8	$4.00
MC14559BCP	A/D	Successive Approximation	8 bits	—	—	±3 to ±18	$7.00
ADC0803	A/D	Successive Approximation ±½ LSB	8 bits	100μs	—	+5V	$5.00
ADC0808	A/D	Successive Approximation ±½ LSB	8 bits	100μs	—	+5V	$5.00
ADC0809	A/D	Successive Approximation ±1 LSB	8 bits	100μs	—	+5V	$4.00
ADC0817	A/D	Successive Approximation ±1 LSB, 16-Channel Multiplexer	8 bits	100μs	—	+5V	$8.00
ADC0820	A/D	Flash Conversion Track/Hold Function		1.18μs	—	+5V	$8.50
MC1408P8	D/A	Multiplying	8 bits	—	300ns	+5, −15	$1.50
MC1408	D/A	Multiplying	8 bits	—	300ns	+5, −5 to −15	$1.50
DAC08	D/A	High-Speed	8 bits	—	150ns	±4.5 to ±18	$3.00
DAC0800	D/A	High-Speed Current Output	8 bits	—	100ns	±4.5 to ±18	$3.00
DAC0808	D/A	High-Speed	8 bits	—	150ns	±4.5 to ±18	$1.50
DAC0830	D/A	Double-Buffered Multiplying	8 bits	—	1μs	+5 to +15	$5.00

*All prices listed are approximate. Contact your local distributor for current prices and product specifications.

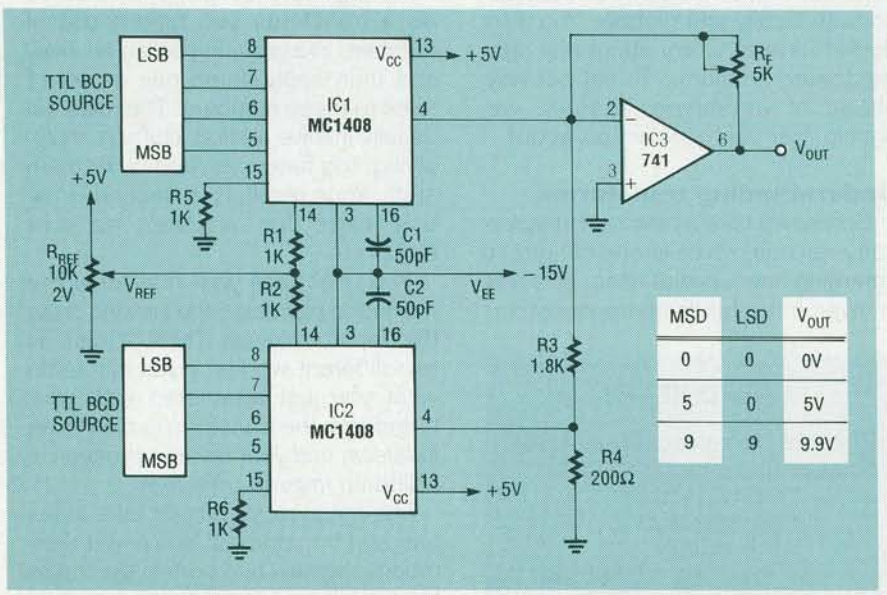


FIG. 17—A 2-DIGIT BCD-to-analog converter circuit can be made using an array of DAC's.

changes the circuit's frame of reference so that the amplifier's output will swing from −10 volts to +10 volts. In order to do that, the values of R1, R2, and R_F must be chosen very carefully. When a 00h is sent to the MC1408, its current output will be 0 mA, but the biasing of the op-amp will make the voltage output −10 volts. As the binary input increments to 7Fh, the analog output will rise to 0 volts. A binary word of FFh will raise the output to +10 volts.

The circuit in Fig. 16 represents a basic D/A sub-circuit. It can be used in just about any situation where 8 bits of resolution and 300 ns of settling time are appropriate, and a bipolar output is required.

continued on page 76

AC TO DC CONVERTERS

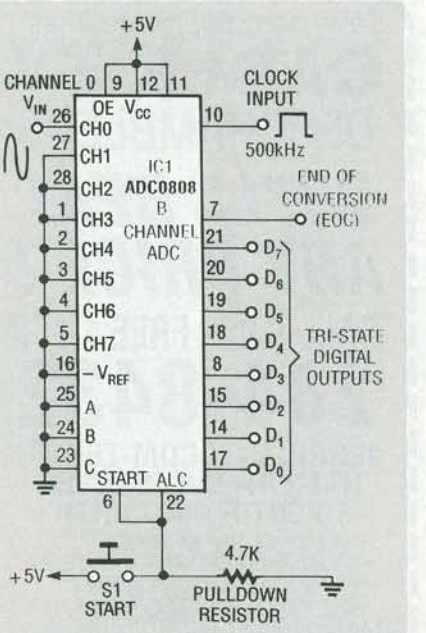
continued from page 67

BCD-to-analog converter

The input signal to the MC1408 does not have to be pure binary. An array of DAC's can be configured to convert a 2-digit BCD input into a corresponding analog output voltage. Figure 17 shows a circuit that can be used as a BCD-to-analog converter.

Notice that only the lower four bits of each DAC are used to accept the BCD signal. The four most significant bits are grounded. The TTL signal can be provided through discrete sources (such as thumbwheel switches) as well as BCD counters or other binary circuits. The most significant digit DAC drives the op-amp directly. The output from the least significant digit DAC is divided by 10 through a resistor network and added to the signal from the most significant digit to produce the 0- to 10-volt output. The value of the feedback resistor R_F can be adjusted to vary the output range from 0 up to 10 volts.

A BCD input of 00 will yield 0 volts out. As the BCD input increases to 50, the output voltage will climb to 5 volts. An input of 99 will give an output of 10 volts. Since the input range is now only 100 steps (00 to 99), the analog output will travel from 0 to 10 volts over 100 steps instead of the 256 steps that all 8 bits would normally offer. Although a BCD to analog convertor sacrifices some resolution, it can provide interesting advantages where special inputs are required.



V_{IN}	TTL OUTPUT							
	MSB							LSB
0V	0	0	0	0	0	0	0	0
2.5V	0	1	1	1	1	1	1	1
5V	1	1	1	1	1	1	1	1

FIG. 18—AN A/D converter circuit using the successive approximation technique.

Basic A/D application

A basic A/D converter can be built using a Texas Instruments ADC0808 as shown in Fig. 18. That is also a generic circuit which can be used to interface an analog voltage to a computer port or other digital circuit.

The ADC0808 uses the successive approximation method of A/D conversion. In normal operation, an analog voltage (from 0 to +5 volts) is applied to the IC at V_{IN}. When a conversion is required, a TTL-level start conversion signal is applied to the converter. In that case, a momentary pushbutton is used to provide the pulse. Any other TTL logic pulse may be used to start the conversion as well. A fast square-wave clock source (of about 500 kHz) steps the ADC quickly through its conversion process. When the conversion is complete, the IC will latch the digital result onto the output pins and generate an end of conversion signal.

Since that is a 0 to +5-volt ADC, a 0-volt input will generate a binary 00h at the output. An input of 2.5 volts output 7Fh, and a full 5-volt input output FFh. **R-E**