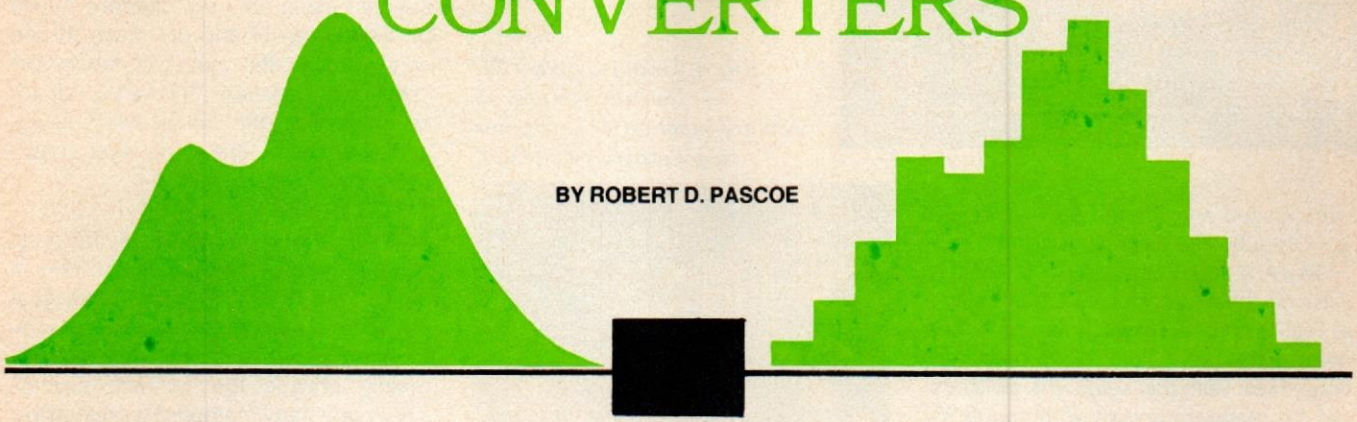
The HOW's & WHY's of D/A and A/D CONVERTERS



BY ROBERT D. PASCOE

New devices and circuits reduce complexity and lower cost in interfacing analog and digital signals.

THE DIFFERENT worlds of analog and digital electronics must frequently be interfaced. In the past, the means for accomplishing this was extremely complex and quite expensive. During the last few years, however, new devices and circuits for interfacing the two types of circuits have made it possible to reduce complexity and bring down cost considerably.

There are essentially two types of circuits or devices that can be used to interface analog and digital circuits. One is for converting analog signals into digital signals and is known as an analog-to-digital (A/D) converter. The other converts digital signals into analog signals and is called a digital-to-analog (D/A) converter. Here is how both types of circuits operate.

D/A and A/D. The diagram shown in Fig. 1A illustrates a D/A converter. This circuit can accept a number of input lines whose signal voltages are a combination of 1's (high) and 0's (low) and transforms them into equivalent analog voltages at the output. As an example, a digital value of 1111 (15 in decimal) might represent an analog output of 15 volts, while 0000 might represent 0 volt. Any digital value between 0000 and 1111 can, hence, be used to generate between 0 and 15 volts at the output in 1-volt steps. In this example, the resolution of our four-bit D/A converter would be 1 volt.

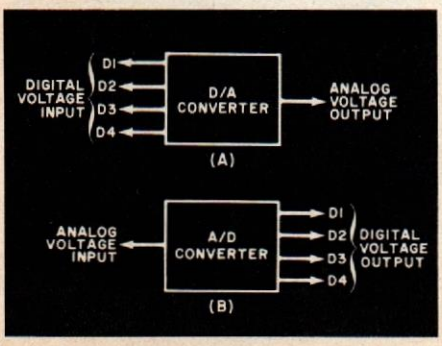


Fig. 1. Digital-to-analog (D/A) and analog-to-digital (A/D) converters are just opposites.

The A/D converter shown in Fig. 1B transforms an analog voltage to an equivalent digital value. Using our four-bit example from above, the A/D converter would change a 15-volt input into the digital value of 1111 (all highs on the output lines), down to 0 volt with a digital value of 0000 (all lows on the output lines).

The two diagrams shown in Fig. 1 illustrate the basic principles of operation of the D/A and A/D converters. Now, let us take a look at how this conversion is actually accomplished.

D/A Converters. While there are a number of ways by which D/A conversion can be accomplished, we will limit our discussion to only the two most popular. The first approach is illustrated by the circuit in Fig. 2, where a resistor network and op-amp voltage amplifier are employed. In this circuit, the digital inputs are represented by switches *S1* through *S4*. If a switch is open, a logic 0 is generated; if it is closed, a logic 1 is generated. Note that in this case, a 1 is the value of V, while a 0 is represented by no voltage being applied (by the given switch) to the inverting (−) input of the op amp.

If we assume a value of 500,000 ohms for *R* and 5 volts for *V*, the following calculations can be made: 1) If *S1* is closed and *S2*, *S3*, and *S4* are open, I_{in} = 5 volts/500,000 ohms = 10 μA and $-V_{out}$ (don't forget that the op amp is operated as an inverter) = 10 μA × 100,000 ohms (the value of the feedback resistor, which is *R*/5 = 500,000 ohms/5 = 100,000 ohms) = −1 volt. 2) If *S4* is closed and *S1*, *S2*, and *S3* are open, I_{in} = 5 volts/62,500 ohms (500,000 ohms/8) = 80 μA and $-V_{out}$ = 80 μA × 100,000 ohms = −8 volts.

More than one switch can be closed at any given time, of course. If *S1* and *S4*

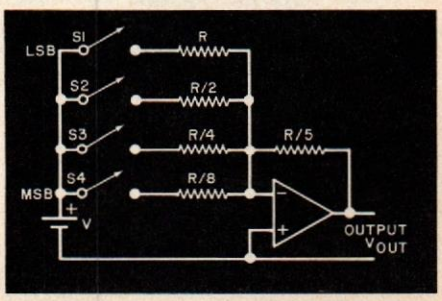


Fig. 2. This 4-bit D/A converter uses a resistor network and an op amp circuit.

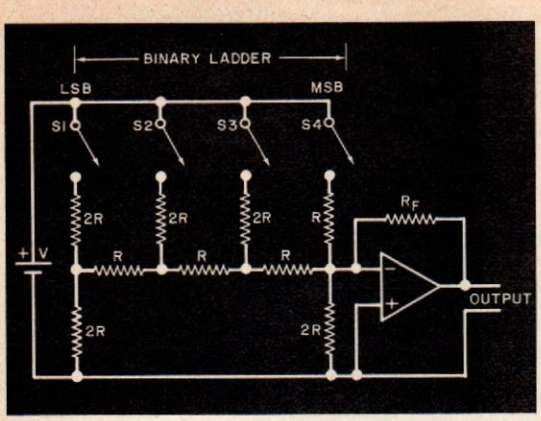
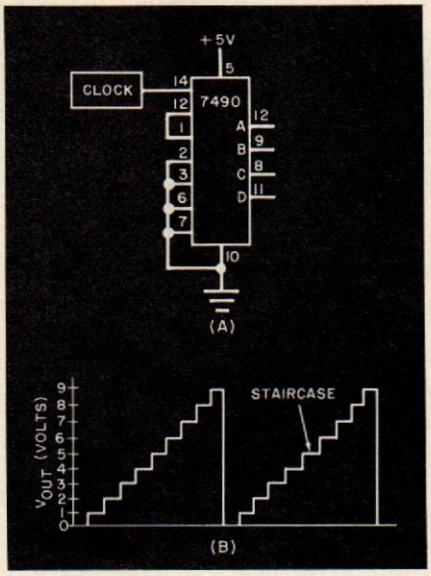


Fig. 3. In this D/A binary ladder only two different values of resistors are used.

Fig. 4. Using a 7490 TTL decade counter to replace mechanical switches to get staircase output.



were closed and *S2* and *S3* were open, I_{in} = 10 μA + 80 μA = 90 μA and $-V_{out}$ = 90 μA × 100,000 ohms = −9 volts.

Since there are four switches shown in Fig. 2 and each switch can be either open or closed, a total of 16 combinations exist. With this setup, the switches can be made to provide an output from the op amp of from 0 to −15 volts in 1-volt steps.

Instead of using mechanical switches, the input terminals, here the switch sides of the resistors in the network, can be connected to the outputs of binary bistable multivibrators or TTL decade counters. In the case of the 7490 decade counter, the A, B, C, and D outputs replace *S1* through *S4*, respectively. Since the 7490 counts to 9 and then resets to 0, the D/A converter circuit will generate 0 to −9 volts at its output. The logic-1 output of the 7490, or any other logic element tied to the D/A converter's input, may not be exactly 5 volts, which means that the value of the feedback resistor will have to be changed to compensate for the lower input level to retain the 0-to-9 volt output.

The advantage of the resistor-network approach is that the network uses only one resistor for each bit of information. However, the digital bit that has the most "weight" (*S4*) would have to supply much more current than any of the other switches. To illustrate, if a 10-bit D/A converter were constructed, the most-significant bit (MSB) would have to supply 1024 times more current than the least-significant bit (LSB).

To summarize, the weighted resistor network is constructed with N number of resistors whose values are *R*, *R*/2, *R*/4 . . . *R*/2^N, with each device connected to the network "seeing" a different resistance value. The LSB device would supply a current of V/*R*, while the MSB device would supply a current of N(V/*R*). Each digital input, however, requires only one resistor.

Another type of D/A converter, shown in Fig. 3, is commonly referred to as a "binary resistance ladder." In this converter, each digital bit supplies the same amount of current. It can be determined mathematically that the resistance "seen" by each digital bit is 3*R*. Hence, each digital bit supplies the same magnitude of current. The ladder is made up of only two resistance values—*R* and 2*R*.

If the voltage output of the op amp in Fig. 3 is the same as in Fig. 2, the value of feedback resistor R_f must be selected so that, in conjunction with the *R* and 2*R* combinations, it causes the op amp to have a gain of 24/5. Thus, if V were 5 volts, the combination of digital inputs would produce the same output range as in Fig. 2.

Switches *S1* through *S4* in Fig. 3 can be replaced with solid-state devices, as in the previous circuit. For example, if the outputs of a 7490 were connected to the inputs of the binary ladder and the 7490 were clocked, the circuit shown in Fig. 4A would produce the ladder output shown in Fig. 4B.

Two important terms used to describe the behavior of a D/A converter are *monotonicity* and *linearity*. Monotonicity is simply a continuously increasing output voltage for an increasing digital value up to the maximum for the ladder or resistor network. Linearity is the linear change in output voltage for increasing values of digital inputs. (The ladder steps should be equal.)

To sum up, the binary ladder is constructed using only two different values of resistance—*R* and 2*R*. Each device connected to the inputs of the ladder "sees" a constant 3*R* value of resistance. The Nth bit, or MSB, is required to supply the same level of current as the LSB.

A/D Converters. Perhaps the most common use of the A/D converter is in digital multimeters, where an analog input voltage must be converted to a digital signal to drive the circuits that ultimately provide the numeric display. There are many methods for making this conversion, four of which will be discussed here.

A simple four-bit, 0-to-9-volt DMM concept is illustrated in Fig. 5. The circuit employs a binary ladder, four-bit decade counter, decoder, seven-segment LED numeric display, and an op amp as a comparator. In the following discussion, we will assume that the reset clock generates a short pulse every 20 ms, while the clock generates a count pulse every 0.01 ms (10 μs). The binary ladder is

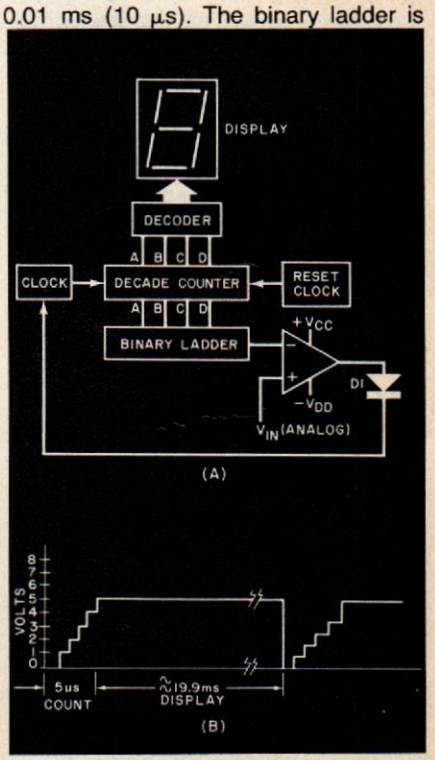


Fig. 5. At (A) is simple 0-9-volt digital voltmeter with its output waveform shown below at (B).

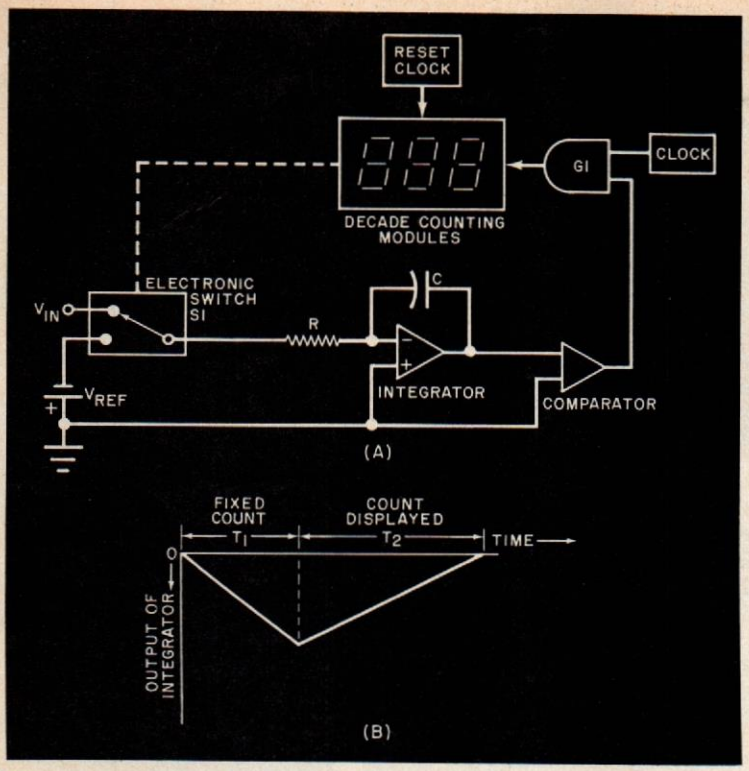


Fig. 6. The dual-slope converter integrates in both directions. An integrator (op amp with capacitor in feedback) is used as input to op amp comparator.

similar to that shown in Fig. 3 so that the output voltage from it is incremented by 1 volt for increasing digital values with a range of 0 to 9 volts.

Because the counter is clocked through all 10 states in 100 ms, it can count in a maximum time of 100 μs and the analog value is displayed for 19.9 ms (20 ms − 0.1 ms). For this particular circuit, the maximum time for conversion, or the time the counter takes to convert the maximum analog value and display it, is 100 μs. The average time for conversion is 100 μs/2 = 50 μs, while the update, or display time, is approximately 19.9 ms. This means that every 19.9 ms, a new conversion occurs.

In Fig. 5A, let us assume that an analog potential of 5 volts is applied to the noninverting (+) input of the op amp and that a reset pulse has been generated. At this instant, the output of the D/A converter is 0 volt (see Fig. 5B). The output from the op amp is maximum positive (supply voltage) and is passed through the forward-biased *D1* diode to activate the clock generator. The clock begins operating and supplies count pulses to the decade counter. The ABCD outputs of the decade counter start "piling" up a voltage in the binary ladder until at the count of 0101 (5 decimal), the binary ladder potential to the inverting input of the op amp very slightly exceeds, by a few millivolts, that of the reference voltage on the noninverting input. At this instant, the op amp slews very rapidly to a maximum negative output and forces the clock to stop working. The counter remains at the 0101 count until a reset pulse is generated, at which time, the counter stops and the cycle repeats. This process is illustrated in Fig. 5B. Because the display time is far longer than the count time, the display on the readout does not flicker.

For the device shown in Fig. 5, it is important to understand that the accuracy of the system is 10%, or 1 volt. This is because the D/A ladder is a four-bit system that has a least-significant value of 1 volt. For greater resolution and, hence, greater accuracy, more bits can be added to the system. The greater the number of bits, therefore, the better the resolution and the higher the accuracy.

As a point of interest, the Fig. 5 circuit has a display for one full digit. It can be converted to provide a three-digit display by "weighting" the outputs of a number of counters. Then, the three full digits would display values from 000 to 999.

The circuit shown in Fig. 6 is a dual-slope converter. It employs an integrator (an op amp with a capacitor in the feedback loop) as the input device to an op-amp comparator. If we assume that the analog input potential is 5 volts and that the counter has just been reset, the output of the circuit is at point 0 in Fig. 6B.

In this circuit, the decade counter has 1000 possible states. Electronic switch *S1* normally connects the input analog voltage to the integrator, which starts to charge the feedback capacitor in a linear fashion until the decade counter has cycled through its 1000 counts. At this instant, the MSB changes from a 9 to a 0, causing *S1* to change the integrator input from the analog voltage being measured to a reference voltage, V_{ref}. This is time T1 in Fig. 6B.

The integrator now integrates the negative reference voltage until it reaches 0 volt. At this time, T2, the comparator switches states and turns off the clock via AND gate *G1* to prevent any further change in state in the decade counters. The counter then remains at this particular count until the next reset pulse is generated to start a new cycle. The total conversion time is the sum of T1 and T2, hence the reason for calling this system "dual slope."

The analog input voltage is $V_{in} = (N/1000)V_{ref}$, where N is the display count. If N were 185 and V_{ref} were 10 volts, $V_{in} = (185/1000) \times 10 = 1.85$ volts.

The great advantage of dual-slope conversion is its simplicity. Needless to say, dual-slope conversion is very popular in the design of many types of digital multimeters.

The A/D converters discussed so far must be clocked through their states, which could possibly be 2^N states, where N is the number of bits. If a counter like that shown in Fig. 5 used 10 bits, the total number of states would be 2^{10}, or 1024. If the clock pulses occurred every 1 μs, the maximum conversion time would be $2^{10} \times 1$ μs, or approximately 1 ms. While 1 ms does not appear to be a very long time, in some applications it could prove excessive.

One method of reducing the conversion time is to use a circuit called a "successive approximation counter," the logic for which is shown in Fig. 7. This system has a conversion time equal to the clock-pulse time times the number of bits. Using the example above, the conversion time for this circuit would be 10 × 1 μs = 10 μs. Comparing this to 1 ms, you can see that the successive approximation counter's conversion time is considerably shorter than for other types of A/D converters.

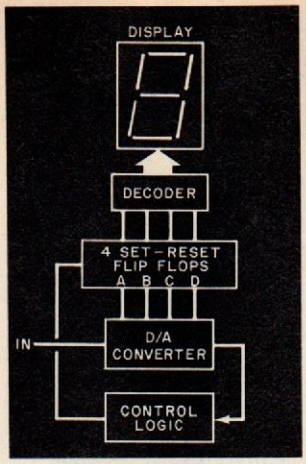


Fig. 7. Successive approximation converter uses bit-comparison technique and is faster than ladder.

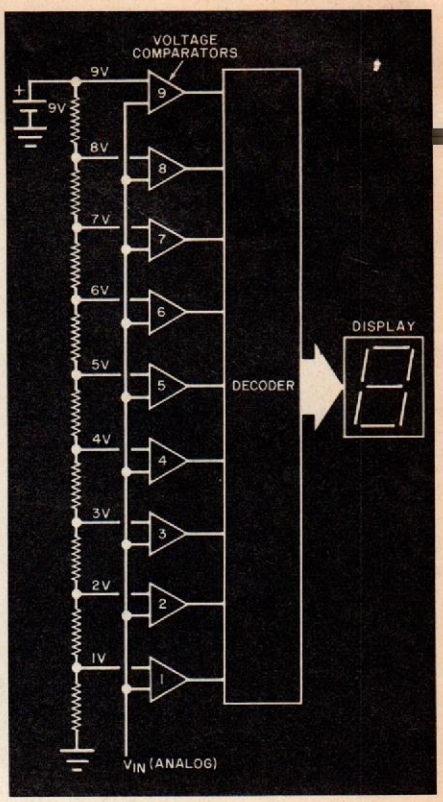


Fig. 8. Simultaneous A/D converter is fast but requires several comparators and resistors.

In the Fig. 7 circuit, the analog voltage at the input is transformed by the D/A converter by comparing the input voltage to the voltage generated by the binary ladder at a rate of one bit at a time. The MSB is compared first, followed by each successively lower significant bit, until the LSB is compared. As an example, assume that a four-bit successive approximation counter is used. The four flip-flops (8,4,2,1) would be turned on and off, starting with the MSB and ending with the LSB. Now, let us assume a 5-volt analog input. The MSB is turned on, which causes the output of the ladder to be 8 volts. Because 8 volts is greater than 5 volts, this flip-flop turns off. This starts the cycle.

The cycle continues with the next significant bit's flip-flop being turned on. Since this flip-flop generates a 4-volt output, which is less than 5 volts, this flip-flop remains on. The next lower bit, 2, is turned on, causing the output of the ladder to be 6 volts (4 volts + 2 volts). Because 6 volts is greater than 5 volts, the 2 flip-flop is turned off. Finally, the LSB flip-flop, 1, turns on, making the ladder output 5 volts (4 volts + 1 volt). Since the 5-volt output of the ladder is the same as the 5-volt input to the system, this last bit is left on. The output states of the four flip-flops are 0101, which represents 5 volts. Note here that the converter used a comparison of only four bits to convert the input voltage.

The circuitry for the successive approximation counter is more complex than for other types of A/D converters.

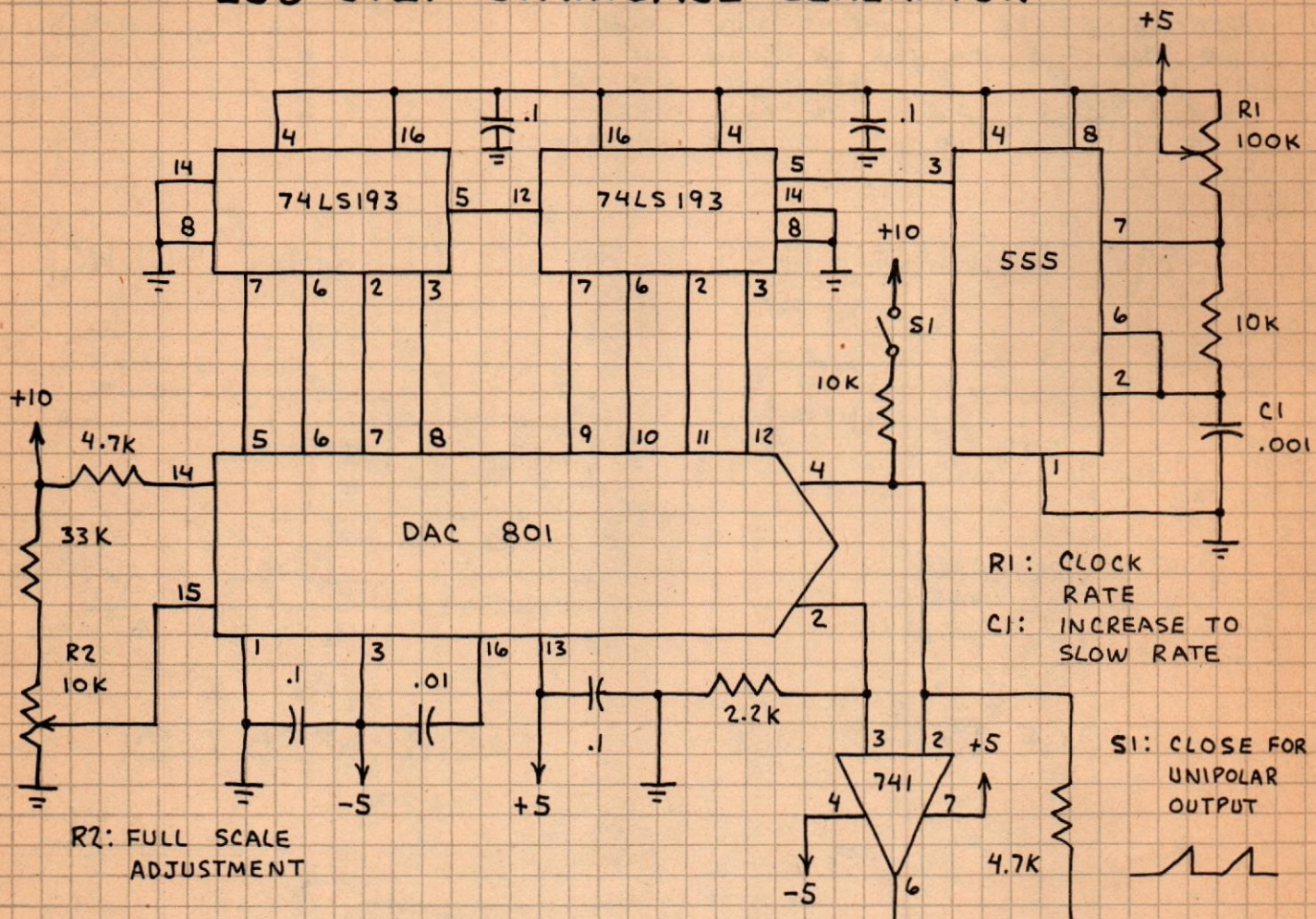
Simultaneous A/D conversion, shown in Fig. 8, falls into the "big-bang" school because everything happens simultaneously. Note that this circuit uses a number of op-amp comparators with one input of each comparator tied to decreasing dc voltages on a resistor network. The upper comparator here is referenced to 9 volts and the resistors are selected so that each comparator going down the line is referenced 1 volt lower. The outputs of all comparators are fed to a decoder that drives a 0-to-9 display.

If the analog input is 5 volts, comparators 1 through 5 would have a positive output, while the other comparators would have a 0 (or negative) output. The decoder converts this combination of 1's and 0's as required to display on the readout a numeral 5.

The disadvantage of using simultaneous A/D conversion is the large number of comparators and the associated resister network and decoder required.

In Conclusion. In this article, we have discussed a number of methods commonly used to interface the analog and digital worlds of electronics. Needless to say, we have only scratched the surface of A/D and D/A conversion techniques. However, the circuits and systems we have discussed should give you a basic understanding of how A/D and D/A converters in general work. ◇

256-STEP STAIRCASE GENERATOR

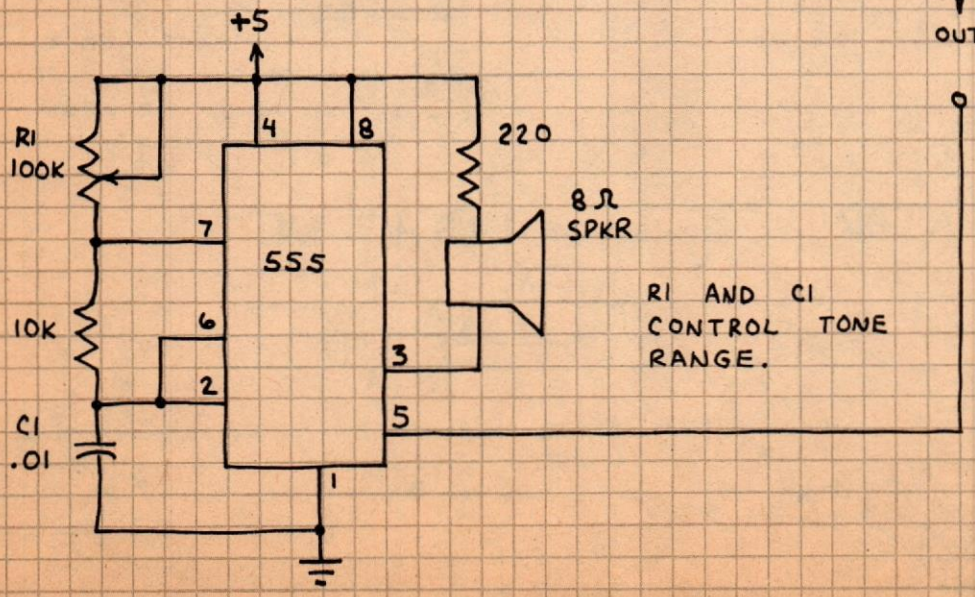


R1: CLOCK RATE
C1: INCREASE TO SLOW RATE

S1: CLOSE FOR UNIPOLAR OUTPUT

R2: FULL SCALE ADJUSTMENT

DAC 801 TONE GENERATOR



R1 AND C1 CONTROL TONE RANGE.

CHANGE OR OMIT ONE OR MORE INPUTS TO DAC 801 TO MAKE UNIQUE WAVEFORMS.

NOTE: +10V REFERENCE CAN BE +5 TO +10V IN NON-PRECISION ROLES (e.g. TONE GENERATION).

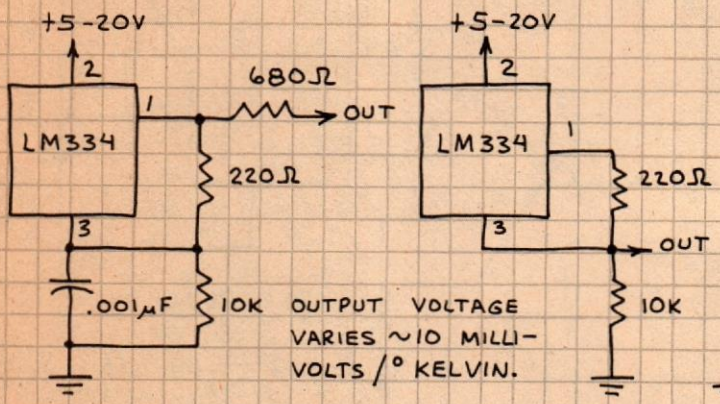
TEMPERATURE SENSOR AND ADJUSTABLE CURRENT SOURCE

L 334 (276-1734)

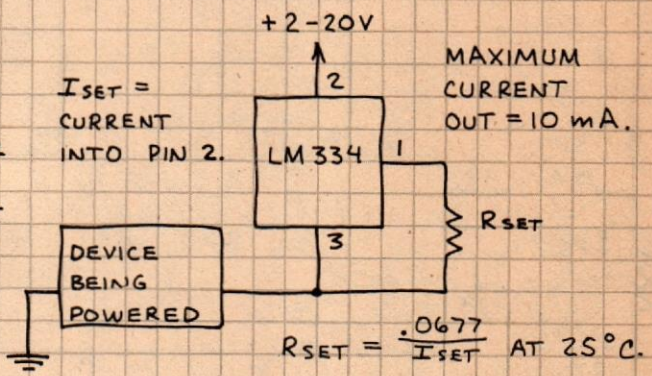
1 = R
2 = +V
3 = -V (GND)

VERSATILE 3-LEAD COMPONENT THAT LOOKS MORE LIKE A TRANSISTOR THAN AN IC. CAN BE USED AS A TEMPERATURE SENSOR, CURRENT SOURCE FOR LEDs AND OTHER COMPONENTS OR CIRCUITS, VOLTAGE REFERENCE, ETC.

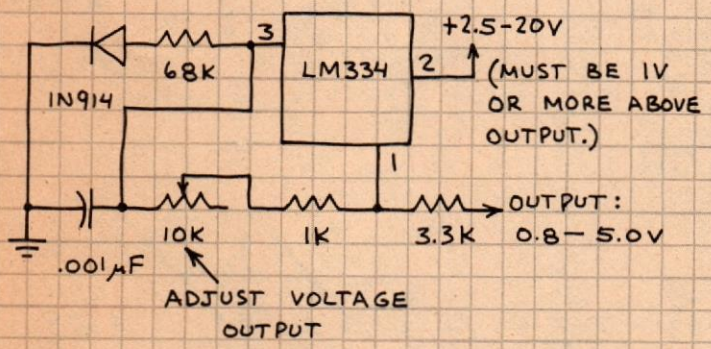
BASIC THERMOMETERS



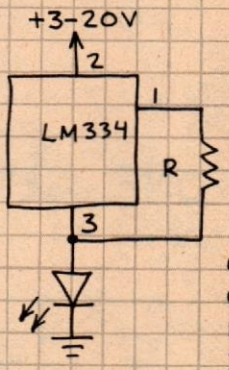
BASIC CURRENT SOURCE



VOLTAGE REFERENCE



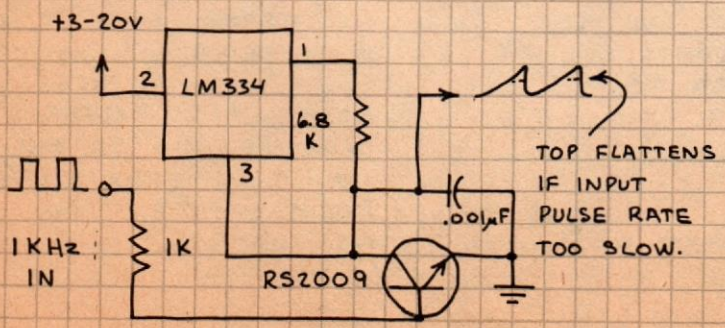
CALIBRATED LED



R	LED CURRENT
10 Ω	6.4 mA
15 Ω	4.3 mA

CONSTANT LED OUTPUT FOR ANY INPUT BETWEEN 3-20 VOLTS.

RAMP GENERATOR



LIGHT METER