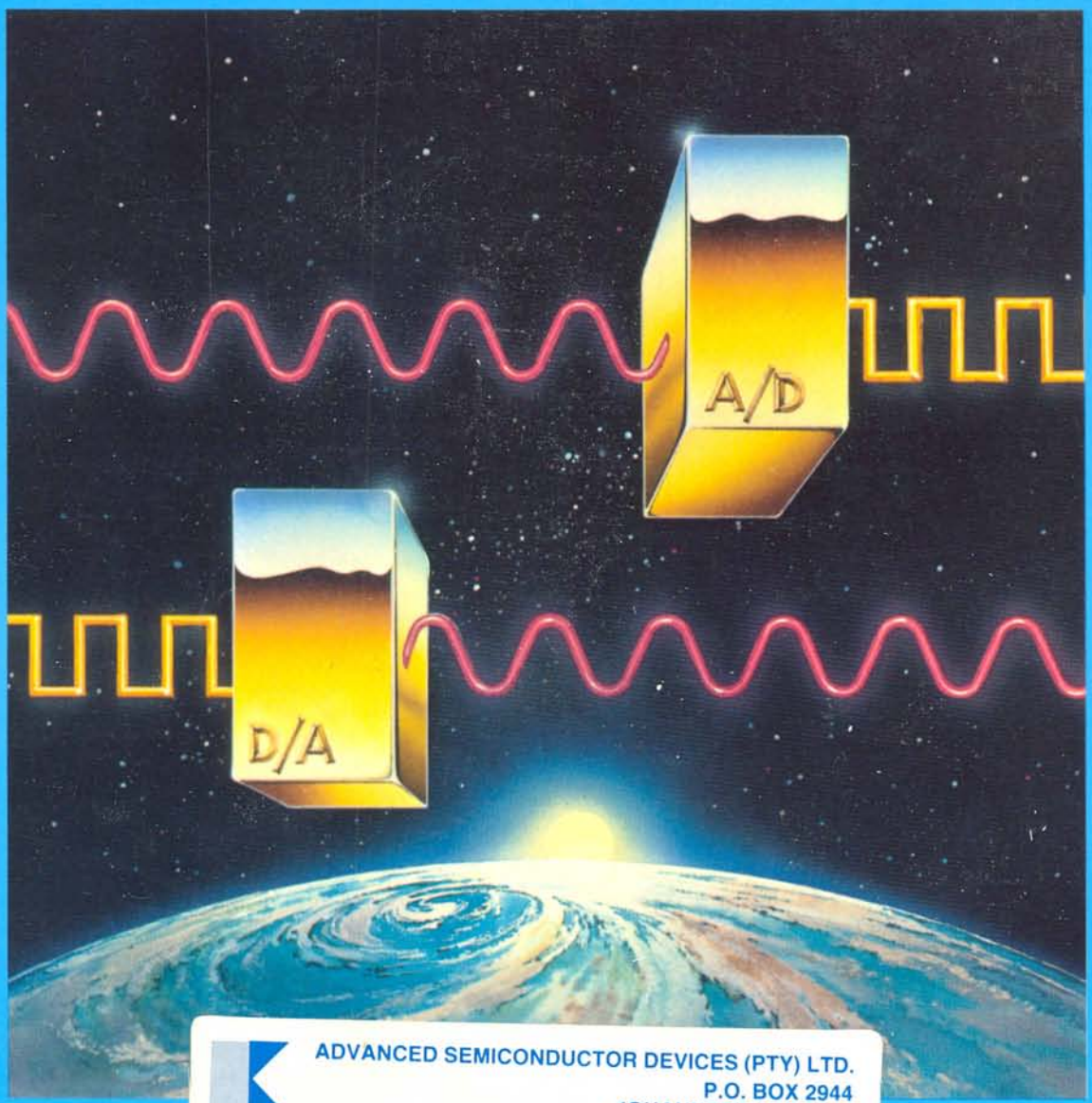
DLE400RI/D

MOTOROLA Semiconductors



A/D AND D/A CONVERSION MANUAL

MOTOROLA

ANALOG/DIGITAL AND DIGITAL/ANALOG CONVERSION MANUAL

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MOTOROLA

ANALOG/DIGITAL AND DIGITAL/ANALOG CONVERSION MANUAL

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ANALOG\DIGITAL AND DIGITAL\ANALOG CONVERSION MANUAL

INTRODUCTION

This data conversion handbook is a compilation of data sheets and application notes from Motorola designed to help to data conversion circuit designers. It also includes a selector guide that gives the minimum technical basis on the A/D and D/A conversion.

The introduction of monolithic digital to analog conversion (DAC) IC's has opened a new area for circuit designers. The cost barriers that have in the past limited the use of the DAC to only the most sophisticated system have now been broken down.

Not only have designers found that there is a cost saving to be realized in present applications, but more important, they have found that the new economy of monolithic DAC's allows their use in numerous new applications such as microprocessor based system. As an added bonus, monolithic DAC's are superior to modular units in most performance specifications.

Motorola range of products for high speed D/A conversion include the MC1408 and the DAC08, 8-bit multiplying converters.
These circuits have broken the cost barrier that up to now caused system designers to use alternate and often less efficient techniques.

For very high speed D/A conversions, a circuit is now available: the 8-bit D/A converter MC10318 operating at speeds above 25 MHz in MECL technology. It is aimed at the video, TV, radar, storage oscilloscope and communication markets. The MC10320, a triple 4-bit color palette video DAC is also to be introduced at time of printing.

The MC144110 and MC144111 are hex and quad static D/A converters realized in CMOS technology. Each converter featuring 6-bit resolution, consists of a 6-bit shift register, 6-bit latch and a static D/A converter.

In addition, Motorola offers ''building block'' subsystems useful for implementation of the A/D conversion (ADC) function. These low cost devices allow the construction of high performance ADC's at a fraction of the cost of comparable modular units.

The MC14433 is a high performance, low power 3 1/2 digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

A precision band gap voltage reference for critical instrumentation and D/A converter is also available. This is the MC1503; low temperature drift is a prime design consideration. The output voltage is 2.5 V with a temperature coefficient of 10 ppm (typ).

There are also the MC1504, a series available with 5.0 V, 6.25 V, 10 V output voltages and trimmable output. This voltage reference family is extended with the MC1500 series available with 2.5, 5, 6.25 and 10 V output voltages with very low temperature coefficient (5 ppm/°C typ) and the TL431 programmable precision references, and the LM385 micropower voltage reference diodes.

Motorola also has microprocessor based A/D Converter linear subsystem. The MC14443 and MC14447 devices are 6 channel, single slope, 8-10-bitA/D converters. Each device contains a 1 to 8 decoder, an 8 channel analog multiplexer, a buffer amplifier, a precision voltage to current converter, a ramp start circuit and a comparator.

Motorola announces availability of the MC145040/MC145041 analog to digital converters with serial interface. The device are low cost 8-bit A/D converters with serial interface parts that are compatible with SPI, Microwire and other similar interfaces.

The MC10319, an 8-bit parallel high-speed flash A/D converter with overrange is now available. Applications include video display and radar processing, high-speed instrumentation, and TV broadcast video encoding. An 8-bit MPU compatible A/D converter, the MC6108, has also been introduced for use in servo control or process systems and medium speed signal processing or wave form storage.

Moreover, the MC10321, a 7-bit low cost derivative of the MC10319 for consumer-like applications, is to be introduced at time of printing.

TABLE OF CONTENTS

SECTION 1 – TECHNOLOGY AND SELECTOR GUIDES

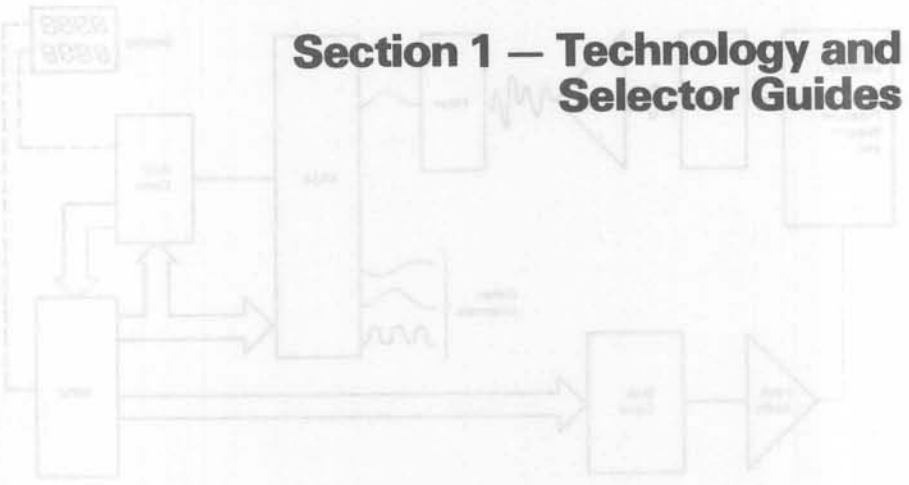
SECTION 2 – DATA SHEETS

SECTION 3 – APPLICATION NOTES

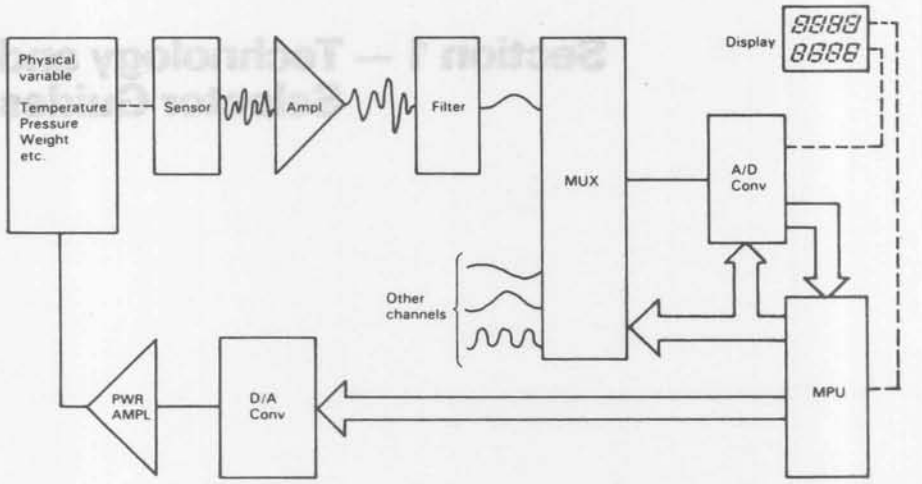
TABLE OF CONTENTS (continued)

SECTION 3 – APPLICATION NOTES (continued)

Section 1 — Technology and Selector Guides



TYPICAL ACQUISITION/CONTROL SYSTEM



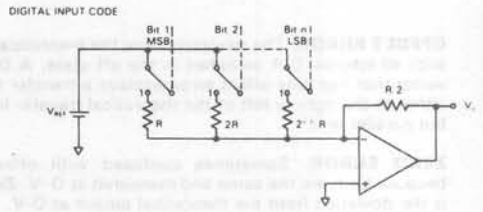
How to choose a converter - check list.
Before selecting a converter, the following questions have to be answered.

- Which resolution is needed (6, 8, 10,... bit)?
- Which accuracy is needed?
- Which linearity?
- Which logic level (input, output)?
- Which type of reference voltage, fixed, variable, internal, external?
- Which speed is necessary?
- Which settling time?
- Which power supply stability?
- Which operating temperature range is needed?
- Which is the best performance/cost ratio?

D/A CONVERTERS

A - BASIC D/A CONVERTER

$$V_O = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{AN}{2^N}\right)$$



Where A_N = "1" if A_N is a high level
A_N = "0" if A_N is a low level

A basic D/A converter consists of a reference, a set of binary-weighted precision resistors and a set of switches.
A way to reduce the resistance range is to use a limited number of repeated values with suitable attenuation - carrying this reduction of resistance values all the way, one arrives at the R-2R ladder.

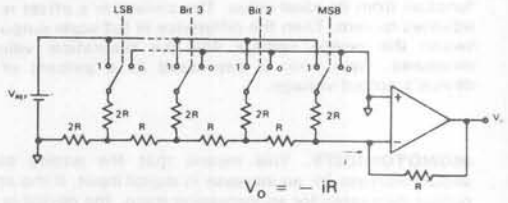
B - D/A CONVERTER USING R-2R LADDER NETWORK

If all bits but the «MSB» are off, the output voltage is:

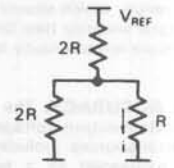
$$V_O = -\frac{R}{2R} V_{REF} = -\frac{V_{REF}}{2}$$

If all bits but bit 2 are off, the output voltage is:

$$V_O = \frac{1}{2}(-P/2R)\, V_{REF} = -\frac{1}{4} V_{REF}$$



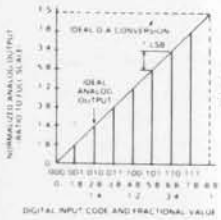
The lumped resistance of all the LSB circuitry (to the left of bit 2) is 2R - Since the grounded MSB series resistance, 2R, has virtually no influence, because the amplifier summing point is virtual ground, the equivalent circuit is:



The same line of thinking can be employed to show that the N^{th} bit produces an increment of output equal to $2^{-N} V_{REF}$.

C - KEY PARAMETERS

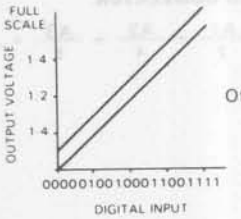
Offset error
Zero error
Gain error
Linearity error
Monotonicity
Absolute accuracy



IDEAL
D/A conversion

1

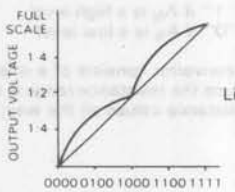
OFFSET ERROR. The deviation from the theoretical output with all internal D/A switches in the off state. A D/A converter that has only offset error displays a transfer function either to the right or left of the theoretical transfer function, but parallel to it.



Offset error

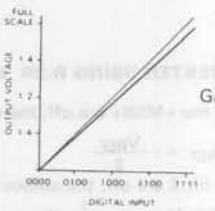
ZERO ERROR. Sometimes confused with offset error because both are the same and measured at 0-V. Zero error is the deviation from the theoretical output at 0-V.

LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of straightness of the actual transfer function from the ideal straight line. It's normally spec'd in parts of an LSB, with 1/2 = LSB maximum error the criterion for a good device.



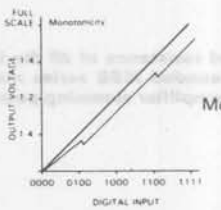
Linearity error

GAIN ERROR. The deviation of the slope of the transfer function from its ideal value. The converter's offset is first adjusted to zero. Then the difference in full scale output between the device voltage and the theoretical value is measured. Gain error is expressed as a percent of the device's output voltage.



Gain error

MONOTONICITY. This means that the analog output should increase for an increase in digital input. If the analog output decreases for an increasing input, the device is non-monotonic. Monotonicity is usually spec'd over a particular temperature range, which should at least equal the operating range. If integral linearity (see linearity error) is ± 1/2 LSB, over temperature monotonicity is guaranteed.



Monotonicity

ABSOLUTE ACCURACY. The deviation of actual output voltage from ideal output voltage for a given digital input, it includes all error sources, including gain, offset and linearity. It's usually expressed as a percent of fullscale range. Relative accuracy, which often appears on spec sheets, is equivalent to integral linearity, not absolute accuracy.

D/A CONVERTER SELECTOR GUIDE

Resolution (bits)	Motorola Part Number	Max. Linearity in % (@ 25°C)	Settling Time ns (typ)	Internal Reference	Supplies (Volts)	Inputs	Package (Pins) L: Ceramic P: Plastic D: Soic	Temp. Range (°C)	Function
6	MC144110	NA	NA	No	+4,5 to +15	CMOS, NMOS	18, P	0 to +65	Hex static D/A
	MC144111						14, P		Quad static D/A
8	MC1408	0.19	300	No	+5, −5 to −15	TTL, CMOS	16, L, P	0 to +70	Multiplying
	MC1508	0.19					16, L	−55 to +125	
8	DAC-08H	0.10	85	No	+5, −15	TTL. CMOS ECL	16, L, P	0 to +70	High Speed Multiplying
	DAC-08Q	0.19					16, L	−55 to +125	
	DAC-08E	0.19					16, L, P, D	0 to +70	
	DAC-08C	0.39					16, L, P, D	0 to +70	
8	MC10318	0.19	10	No	−5.2	ECL	16, L	0 to +70	Very High Speed Multiplying
3 × 4	MC10320 (see Note)	1.56	3	Yes	+5 or ±5	TTL, ECL	28, L	0 to 70	Video DAC

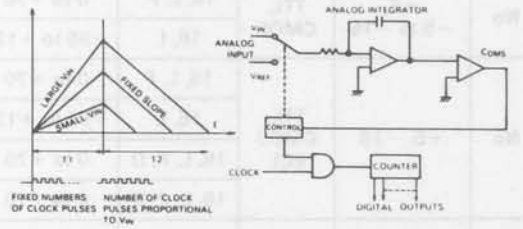
Note: Device to be introduced at printing date.

Technology and selector guide

1

There are many techniques of A/D conversion, each having different characteristics and each favoring different applications. The dual ramp technique of A/D conversion provides an inexpensive method of obtaining high accuracy which makes it ideal for DVM applications.

A - THE DUAL SLOPE TECHNIQUE - THEORY AND PRACTICE



The dual ramp conversion cycle consists of two basic time periods - time period T1 results from the input unknown voltage being integrated for a fixed time interval. This integration results in the output voltage of the integrator being proportional to the input unknown voltage. At the end of the time period T1, the voltage reference (V_{REF}) is applied to the integrator, causing the integrator output voltage to decrease. This integration continues until the output voltage again reaches the zero reference level. This time period, T2, is the down ramp time period.

Time period T1 is constant for each conversion time. The time interval T2 is dependent upon the input unknown voltage.

V on capacitor is equal in T1 and T2.

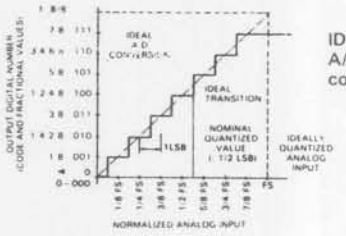
$$\frac{1}{RC}\int_{T1}^{T2} V_{IN}\,DT = \frac{1}{RC}\int_{T2}^{T3} V_{REF}\,DT$$

$$T2 = T1\,\frac{Vin}{VREF} \qquad V_{IN}\,T1 = V_{REF}\,T2$$

Looking at the four variables in the relationship, T1 is a fixed time period, T2 is measured from the start of the ramp down time period until the zero level is reached and V_{REF} is calibrated into the system. The only remaining variable in the equation is V_{IN}, which is the analog input to be determined. Thus by counting out a time period T1, measuring the down ramp time interval T2, and calibrating the reference voltage, the dual ramp A/D conversion technique determines the value of an analog input voltage.

B - KEY PARAMETERS

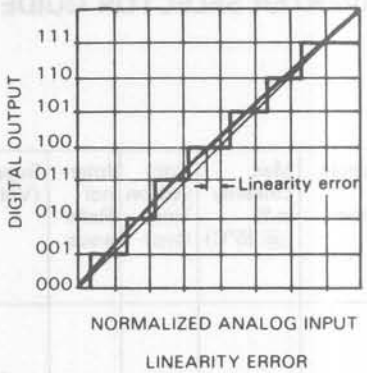
Quantization error
Linearity
Differential non linearity
Relative accuracy
Gain error
Gain temperature coefficient
Offset error
Offset temperature



IDEAL A/D conversion

QUANTIZATION ERROR. This is the fundamental error associated with dividing a continuous (analog) signal into a finite number of digital bits. A 10 bit converter, for example, can only identify the input voltage to 1 part in 2^{10}, and there is an unavoidable output uncertainty of ± 1/2 LSB (Least Significant Bit).

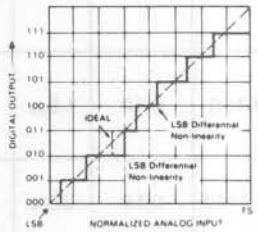
LINEARITY. The maximum deviation from a straight line drawn between the end points of the converter transfer function. It's usually expressed as a fraction of LSB size. A good converter has + 1/2 LSB.



Linearity error

LINEARITY ERROR

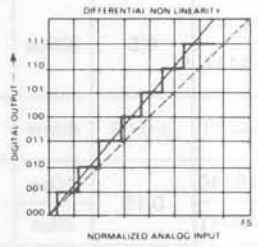
DIFFERENTIAL NON-LINEARITY. This describes the variation in the analog value between adjacent pairs of digital numbers, over the full range of the digital output. If each transition is equal to 1 LSB, the differential non-linearity is clearly zero. If the transition is 1 LSB ± 1/2 LSB, then there is a differential linearity error of ± 1/2 LSB, but no possibility of missing codes. If the transition is 1 LSB ± 1 LDB, then there is the possibility of missing codes. This means that the output may jump from, say 011... 111 to 100... 001, missing out 100... 000.



Differential non-linearity

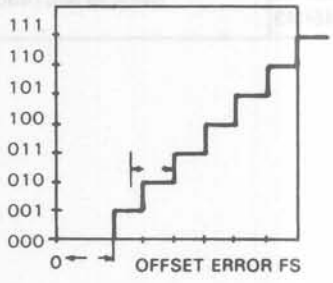
RELATIVE ACCURACY. The input to output error as a fraction of full scale, with gain and offset errors adjusted to zero. Relative accuracy is a function of linearity, and is usually specified at less than ± 1/2 LSB.

GAIN ERROR. The difference in slope between the actual transfer function and the ideal transfer function, expressed as a percentage. This error is generally adjustable to zero by adjusting the input resistor in a current-comparing successive approximation A/D.



Gain error

OFFSET ERROR. The mean value of input voltage required to set zero code out. This error can generally be trimmed to zero at any given temperature, or is automatically zeroed in the case of a good integrating design.



Offset error

A/D CONVERTER SELECTOR GUIDE

1

Resolution (bits)	Motorola Part Number	Max. Linearity in % (@ 25°C)	Conversion Time (typ)	Internal Reference	Supplies (Volts)	Output Logic Levels	Package (Pins) L: Ceramic P: Plastic FN: Plastic quadpack	Temp. Range (°C)	Function
8	MC10319	0.19	40ns	No	−3 to −6 +5	TTL	24, L	0 to +70	8 bit high speed A/D flash converter + overrange bit for direct 9 bit stack
8	MC6108	0,10	1.8μs	Yes	−5.2 +5	TTL	28, P	0 to +70	8 bit A/D converter MPU compatible
8	MC14442	0,19	32μs	No	4.5 to 5.5	TTL, CMOS, NMOS	28, P, FN	−40 to +85	MPU bus compatible
8-10	MC14443 MC14447	0,5	300μs	No	+4.5 to +18	NMOS, CMOS	16, P	−40 to +85	MPU based A/D converter linear subsystem
3/2 digits	MC14433	±0.05	40ms	No	±4.5 to ±8	CMOS, TTL	24, P, FN	−40 to +85	3 1/2 Digit A/D converter
8	MC145040	0,19	10μs	No	4.5 to 5.5	CMOS, TTL, NMOS	L	−55 to +125	11 channels serial data interface
	MC145041		20μs				20 P, FN	−40 to +85	
8	MC145042 MC145043	Same as MC145040/41 but with 19 Analog Inputs and 28 pin package.							

VOLTAGE REFERENCE SELECTOR GUIDE

Output Voltage	Motorola Part Number	Voltage Tolerance max. T_A = 25°C	Output Volt. Temp. Coeffic. over Temp. Range PPM/°C max.	Max. Output Volt. Change over Temp. Range mV	Line Regulation mV	Load Regulation 0≤10≤ 10 mA mV	Input Voltage Range (V)	Temp. Range Available	Package U Ceramic G Metal D Soic
2.5	MC1403	±1%	40	7.0	4.5	10	4.5 to 40	0 to 70	8, U, D
	MC1503		55	25				−55 to +125	8, U
2.5	MC1403A	±1%	25	4.4	4.5	10	4.5 to 40	0 to +70	8, U
	MC1503A			11				−55 to +125	
Adj. 2.5V to 36V	TL431	±2%	50	17			2.5 to 37	0 to +70 −40 to +85 −55 to +125	TO 92 8, P 8, U 8, D
1.235V	LM385	±1%	20	10			1.25 to 40	0 to +70	TO 92 8, D
2.5V								−40 to +85	

Section 2 — Data Sheets

2

2

Section 2 – Data Sheets

MOTOROLA

DAC-08

Advance Information

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

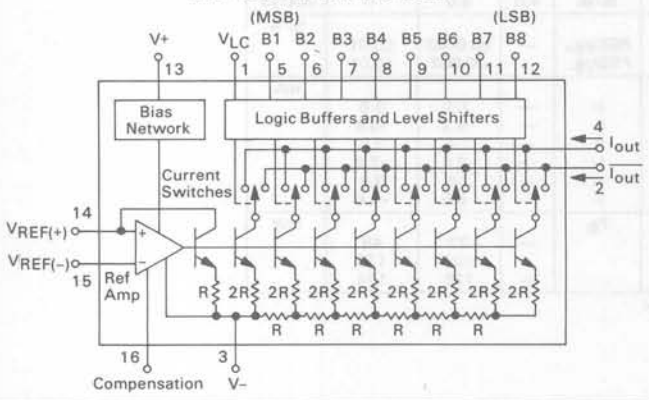
Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC}, (pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (±1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics, along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high-speed modems, and high-speed analog-to-digital converters.

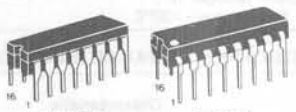
- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs –10 V to +18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost

DAC-08 EQUIVALENT CIRCUIT



HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



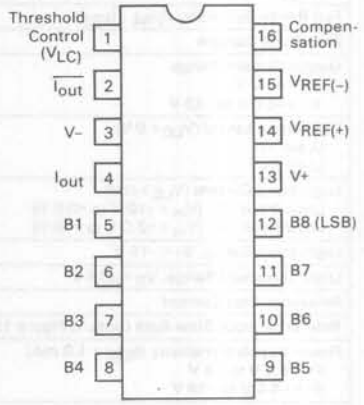
Q SUFFIX
CERAMIC PACKAGE
CASE 620-02

P SUFFIX
PLASTIC PACKAGE
CASE 648-06

D SUFFIX
PLASTIC PACKAGE
CASE 751B-01
SO-16*

*Surface Mount pin-out is different than standard package pin-out for this device.

PINOUT DIAGRAM



ORDERING INFORMATION

Device	Nonlinearity	Temperature Range	Package
DAC-08Q	±0.19%	–55°C to +125°C	Ceramic
DAC-08HQ	±0.1%	0°C to +70°C	Ceramic
DAC-08EQ	±0.19%	0°C to +70°C	Ceramic
DAC-08HP	±0.1%	0°C to 70°C	Plastic
DAC-08EP	±0.19%	0°C to +70°C	Plastic
DAC-08CP	±0.39%	0°C to +70°C	Plastic

DS9681

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V+ Supply to V–Supply	—	36	V
Logic Inputs	—	V– to V– Plus 36	V
Logic Threshold Control	V_{LC}	V– to V+	V
Analog Current Outputs	I_{out}	See Figure 7	mA
Reference Inputs (V14, V15)	V_{REF}	V– to V+	V
Reference Input Differential Voltage (V14 to V15)	$V_{REF(D)}$	±18	V
Reference Input Current (I14)	I_{REF}	5.0	mA
Operating Temperature Range DAC-08 Q DAC-08HQ, EQ, HP, EP, CP	T_A	 –55 to +125 0 to +70	°C
Storage Temperature	T_A	–65 to +150	°C
Power Dissipation Derate above 100°C	P_D $R_{\theta JA}$	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = –55°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08 Min	DAC-08 Typ	DAC-08 Max	Unit
Resolution	—	8	8	8	Bits
Monotonicity	—	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.19	%FS
Settling Time to ±1/2 LSB, Figure 24 (All Bits Switched On or Off, T_A = 25°C, Note 1)	t_s	—	85	150	ns
Propagation Delay, Note 1, T_A = 25°C Each Bit All Bits Swtiched	 t_{PLH} t_{PHL}	 — —	 35 35	 60 60	ns
Full Scale Tempco	TCI_{FS}	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	–10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ, T_A = 25°C)	I_{FR4}	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±1.0	±8.0	μA
Zero Scale Current	I_{ZS}	—	0.2	2.0	μA
Output Current Range V– = –5.0 V V– = –8.0 V to –18 V	 I_{OR1} I_{OR2}	 0 0	 — —	 2.1 4.2	mA
Logic Input Levels (V_{LC} = 0 V) Logic "0" Logic "1"	 V_{IL} V_{IH}	 — 2.0	 — —	 0.8 —	V
Logic Input Current (V_{LC} = 0 V) Logic Input "0" (V_{in} = –10 V to +0.8 V) Logic Input "1" (V_{in} = +2.0 V to +18 V)	 I_{IL} I_{IH}	 — —	 –2.0 0.002	 –10 10	μA
Logic Input Swing, V– = –15 V	V_{IS}	–10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	–10	—	+13.5	V
Reference Bias Current	I_{15}	—	–1.0	–3.0	μA
Reference Input Slew Rate (Note 1) Figure 19	di/dt	4.0	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA) V+ = 4.5 V to 18 V V– = –4.5 V to –18 V	 $PSSI_{FS+}$ $PSSI_{FS-}$	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	%/%
Power Supply Current V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, –15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	 I+ I– I+ I– I+ I–	 — — — — — —	 2.3 –4.3 2.4 –6.4 2.5 –6.5	 3.8 –5.8 3.8 –7.8 3.8 –7.8	mA
Power Dissipation V_S = ±5.0 V, I_{REF} = 1.0 mA V_S = +5.0 V, –15 V, I_{REF} = 2.0 mA V_S = ±15 V, I_{REF} = 2.0 mA	P_D	 — — —	 33 108 135	 48 136 174	mW

Note 1 Parameter is not 100% tested; guaranteed by design.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{REF} = 2.0 mA, T_A = 0°C to 70°C, unless otherwise noted.)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to +70°C	NL	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time to ±1/2 LSB (All Bits Switched On or Off, T_A = 25°C, Note 1) Figure 24	t_s	—	85	135	—	85	150	—	85	150	ns
Propagation Delay, Note 1, T_A = 25°C											ns
Each Bit	t_{PLH}	—	35	60	—	35	60	—	35	60	
All Bits Swtiched	t_{PHL}	—	35	60	—	35	60	—	35	60	
Full Scale Tempco	TCI_{FS}	—	±10	±50	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 megohm typ.	V_{OC}	-10	—	+18	-10	—	+18	-10	—	+18	V
Full Range Current (V_{REF} = 10.000 V; R14, R15 = 5.000 kΩ) T_A = 25°C	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	μA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	μA
Output Current Range											mA
V- = -5.0 V	I_{OR1}	0	—	2.1	0	—	2.1	0	—	2.1	
V- = -8.0 V to -18 V	I_{OR2}	0	—	4.2	0	—	4.2	0	—	4.2	
Logic Input Levels (V_{LC} = 0 V)											V
Logic "0"	V_{IL}	—	—	0.8	—	—	0.8	—	—	0.8	
Logic "1"	V_{IH}	2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current (V_{LC} = 0 V)											μA
Logic Input "0" (V_{in} = -10 V to +0.8 V)	I_{IL}	—	-2.0	-10	—	-2.0	-10	—	-2.0	-10	
Logic Input "1" (V_{in} = +2.0 V to +18 V)	I_{IH}	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing, V- = -15 V	V_{IS}	-10	—	+18	-10	—	+18	-10	—	+18	V
Logic Threshold Range, V_S = ±15 V	V_{THR}	-10	—	+13.5	-10	—	+13.5	-10	—	+13.5	V
Reference Bias Current	I_{15}	—	-1.0	-3.0	—	-1.0	-3.0	—	-1.0	-3.0	μA
Reference Input Slew Rate (Note 1) Figure 19	dI/dt	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/μs
Power Supply Sensitivity (I_{REF} = 1.0 mA)											%/%
V+ = 4.5 V to 18 V	$PSSI_{FS+}$	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	—	
V- = -4.5 V to -18 V	$PSSI_{FS-}$	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	—	
Power Supply Current											mA
V_S = ±5.0 V, I_{REF} = 1.0 mA	I+	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	
	I-	—	-4.3	-5.8	—	-4.3	-5.8	—	-4.3	-5.8	
V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA	I+	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I-	—	-6.4	-7.8	—	-6.4	-7.8	—	-6.4	-7.8	
V_S = ±15 V, I_{REF} = 2.0 mA	I+	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I-	—	-6.5	-7.8	—	-6.5	-7.8	—	-6.5	-7.8	
Power Dissipation	P_D										mW
V_S = ±5.0 V, I_{REF} = 1.0 mA		—	33	48	—	33	48	—	33	48	
V_S = +5.0 V, -15 V, I_{REF} = 2.0 mA		—	108	136	—	108	136	—	108	136	
V_S = ±15 V, I_{REF} = 2.0 mA		—	135	174	—	135	174	—	135	174	

Note 1. Parameter is not 100% tested; guaranteed by design.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT

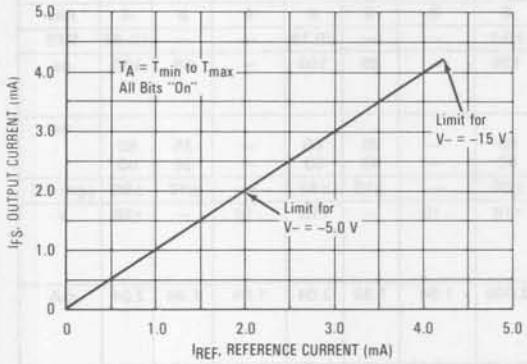
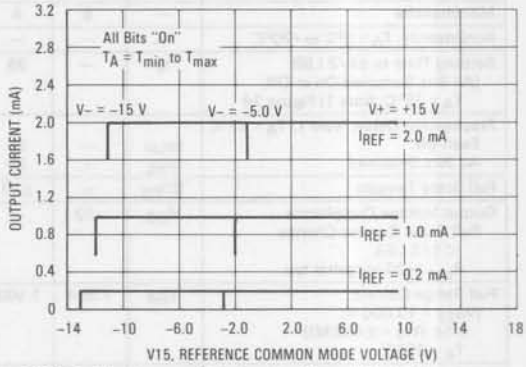
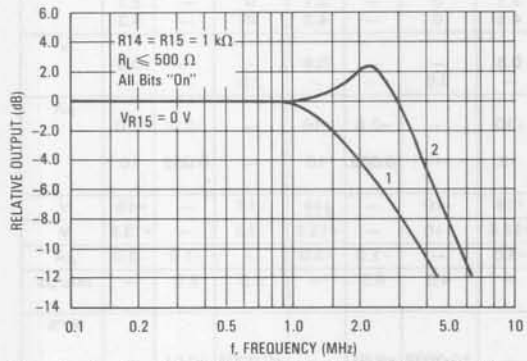


FIGURE 2 — REFERENCE AMP COMMON MODE RANGE



NOTE: Positive Common Mode Range is Always (V+) –1.5 V

FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE



Curve 1 — C_c = 15 pF, V_{in} = 2.0 V p-p Centered at +1.0 V (Large-Signal)
Curve 2 — C_c = 15 pF, V_{in} = 50 mV p-p Centered at +200 mV (Small-Signal)

FIGURE 4 — LSB PROPAGATION DELAY versus I_{FS}

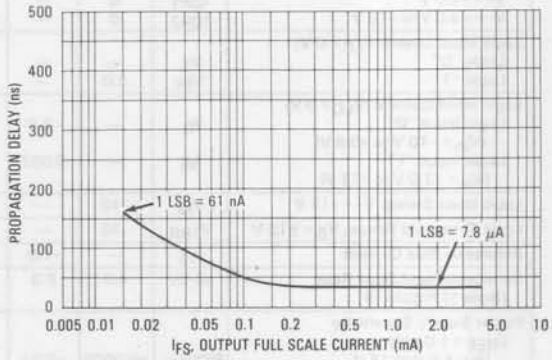


FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

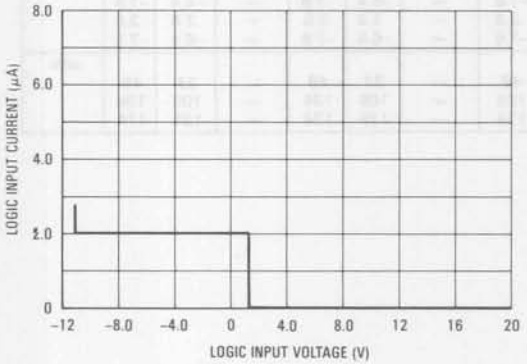
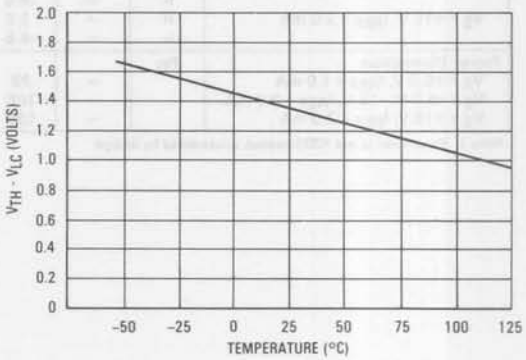


FIGURE 6 — V_{TH} - V_{LC} versus TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Voltage Compliance)

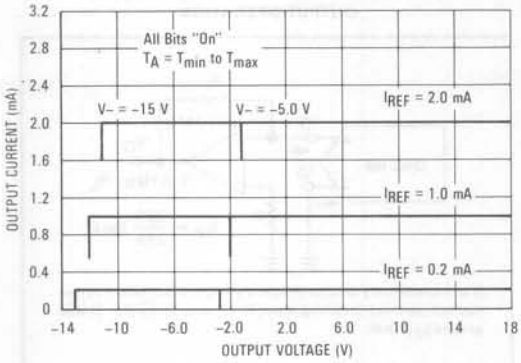


FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE

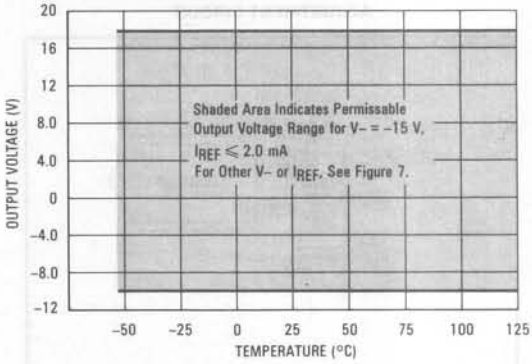
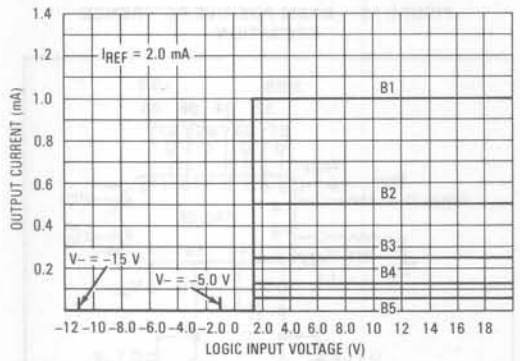


FIGURE 9 — BIT TRANSFER CHARACTERISTICS



NOTE: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range (V_{LC} = 0 V).

FIGURE 10 — POWER SUPPLY CURRENT versus V+

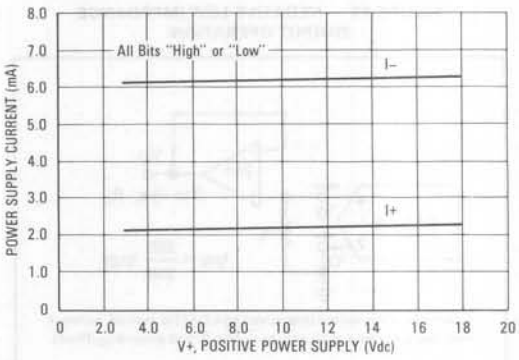


FIGURE 11 — POWER SUPPLY CURRENT versus V–

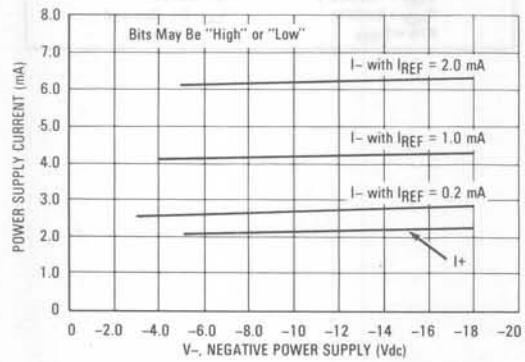
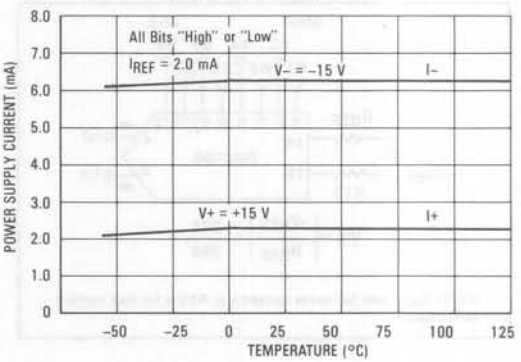


FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE



2

BASIC CIRCUIT CONFIGURATIONS

FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

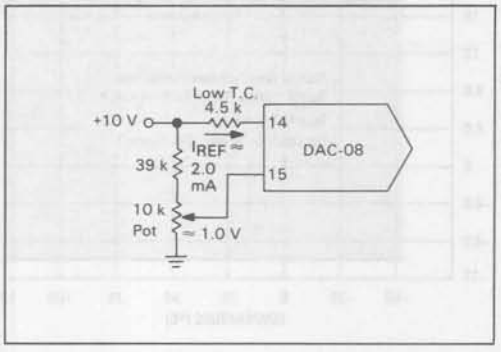
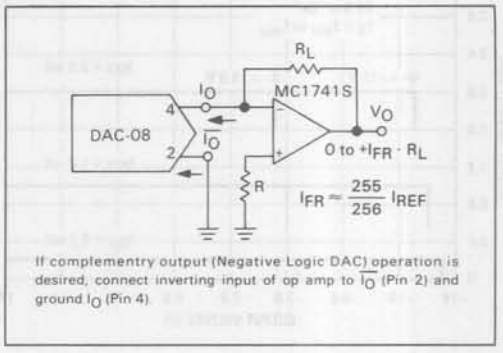
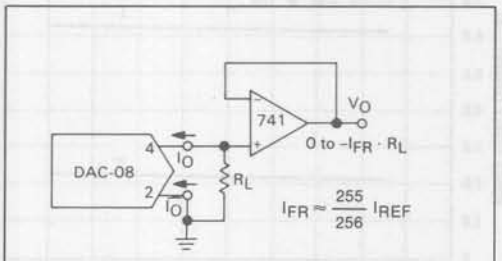


FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION



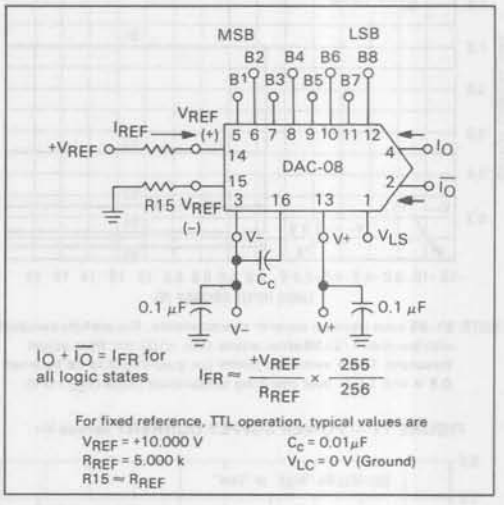
If complementry output (Negative Logic DAC) operation is desired, connect inverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4).

FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



If complementry output (Negative Logic DAC) is desired, connect noninverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4).

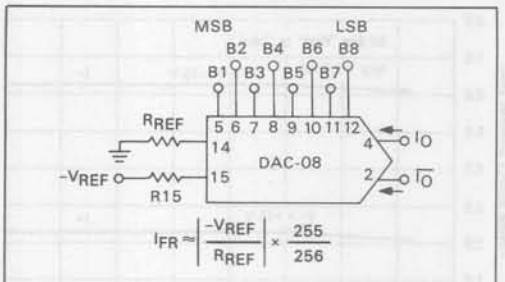
FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION



For fixed reference, TTL operation, typical values are

V_{REF} = +10.000 V	C_C = 0.01 μF
R_{REF} = 5.000 k	V_{LC} = 0 V (Ground)
R15 ≈ R_{REF}	

FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION



NOTE: R_{REF} sets full scale current I_{FR}; R15 is for bias current cancellation.

BASIC CIRCUIT CONFIGURATIONS

FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES

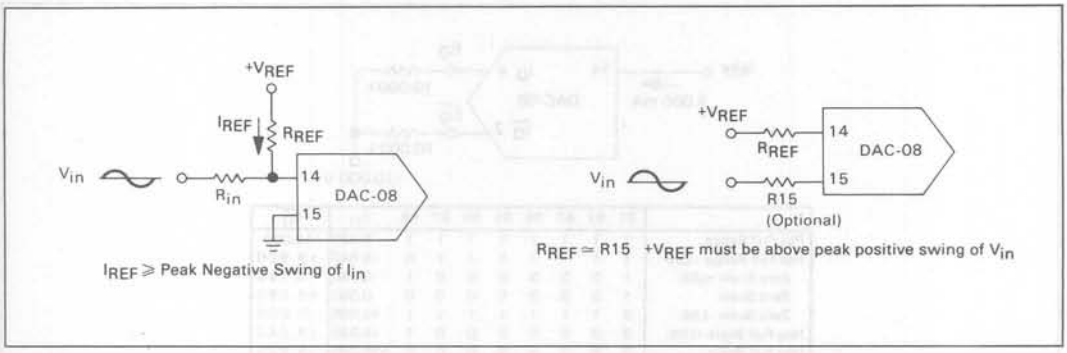


FIGURE 19 — PULSED REFERENCE OPERATION

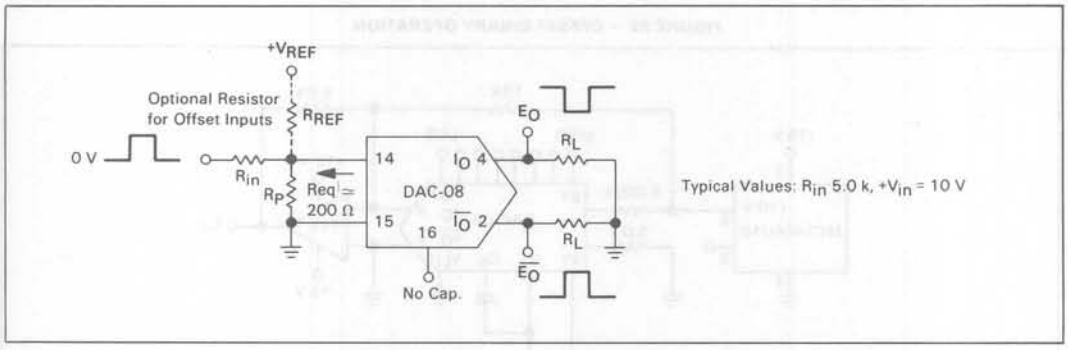
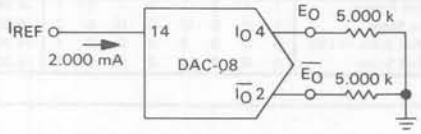


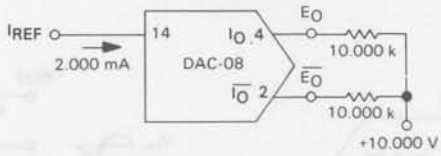
FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Range	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	-0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

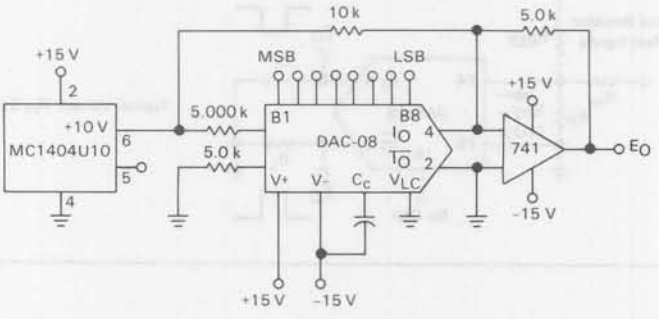
BASIC CIRCUIT CONFIGURATIONS

FIGURE 21 — BASIC BIPOLAR OUTPUT OPERATION



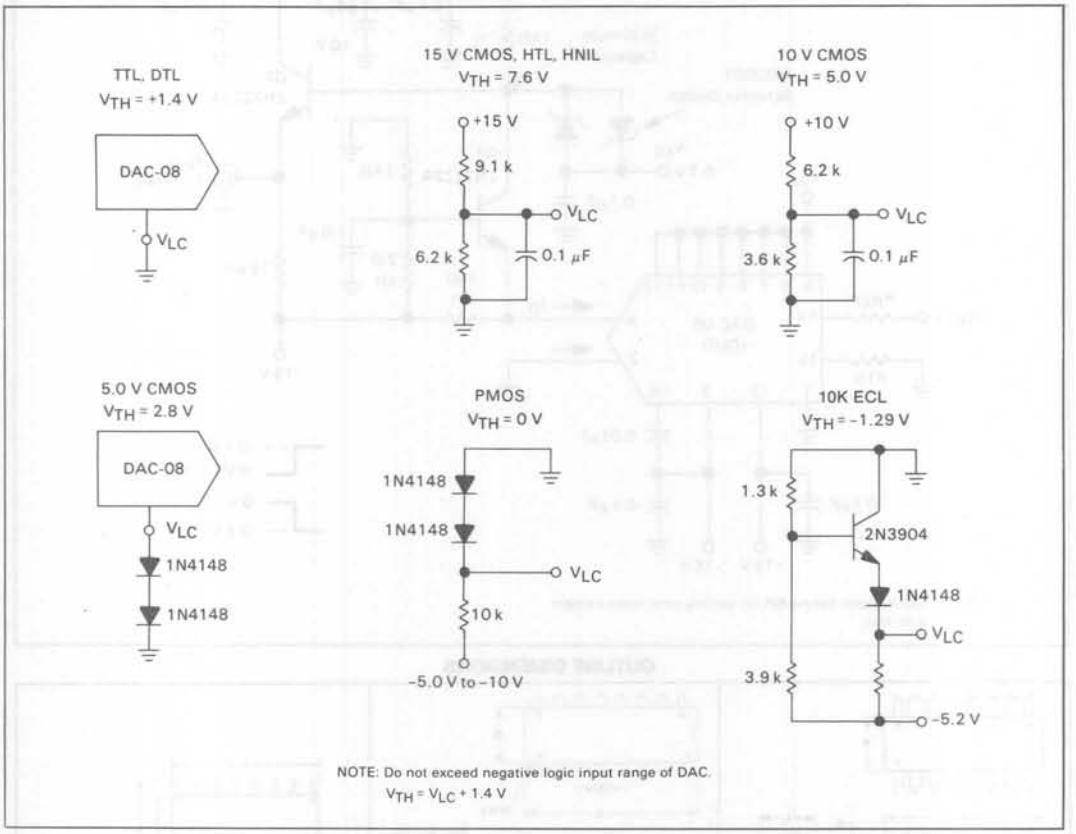
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos Full Range	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos Full Range -LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale +LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale -LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale +LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

FIGURE 22 — OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Range	1	1	1	1	1	1	1	1	-4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale +1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

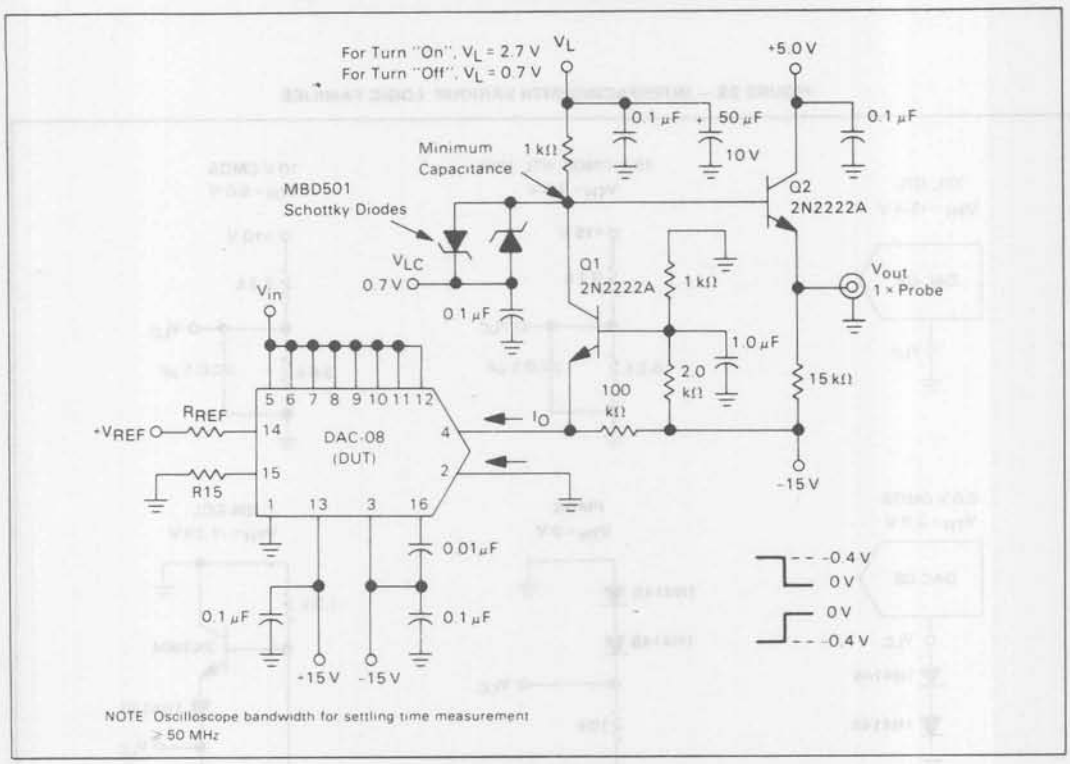
FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE: Do not exceed negative logic input range of DAC.
$V_{TH} = V_{LC} + 1.4$ V

2

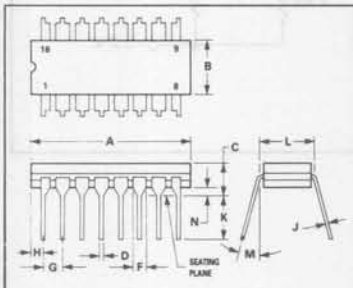
FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT



NOTE Oscilloscope bandwidth for settling time measurement ≥ 50 MHz

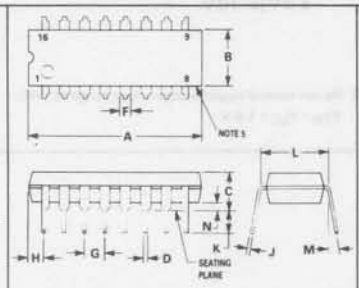
2

OUTLINE DIMENSIONS



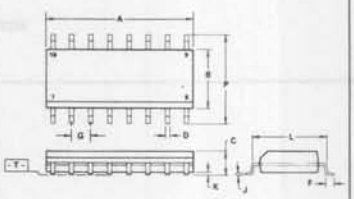
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

Q SUFFIX
CERAMIC PACKAGE
CASE 620-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

P SUFFIX
PLASTIC PACKAGE
CASE 648-06



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.01	0.385	0.394
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.009
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

D SUFFIX
PLASTIC PACKAGE
CASE 751B-01
SO-16

MOTOROLA

LM285
LM385

MICROPOWER VOLTAGE REFERENCE DIODES

The LM285/LM385 series are micropower two-terminal bandgap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

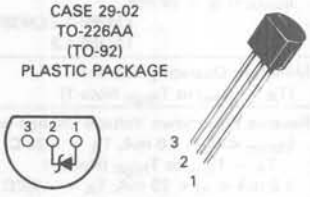
The LM285/LM385 series are packaged in a low cost TO-226AA (TO-92) plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Available in 1.235 and 2.500 Volt Versions

MICROPOWER VOLTAGE REFERENCE DIODES

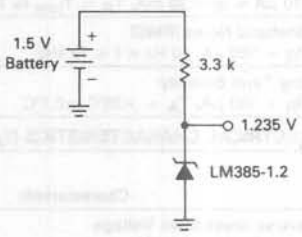
SILICON MONOLITHIC INTEGRATED CIRCUIT

Z SUFFIX
CASE 29-02
TO-226AA
(TO-92)
PLASTIC PACKAGE

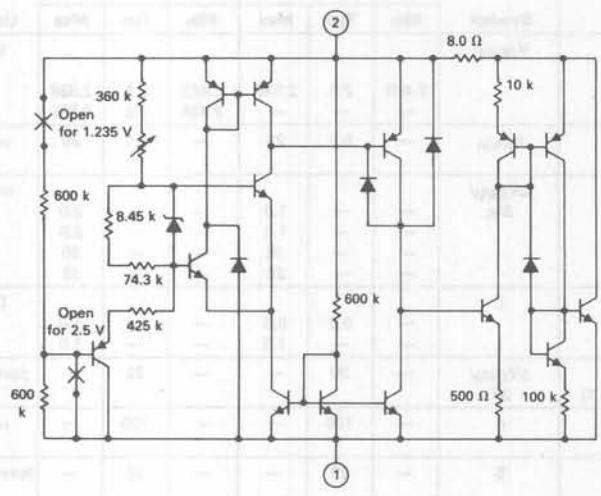


(Bottom View)

STANDARD APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temp. Range	Reverse Breakdown Voltage	Tolerance
LM285Z-1.2	−40 °C to +85°C	1.235 Volts	±1.0%
LM285Z-2.5		2.500 Volts	±1.5%
LM385BZ-1.2	0°C to +70°C	1.235 Volts	±1.0%
LM385Z-1.2		1.235 Volts	±2.0%
LM385BZ-2.5		2.500 Volts	±1.5%
LM385Z-2.5		2.500 Volts	±3.0%

DS9633

2

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise noted)

Characteristic	Symbol	LM285-1.2 Min	LM285-1.2 Typ	LM285-1.2 Max	LM385-1.2/LM385B-1.2 Min	LM385-1.2/LM385B-1.2 Typ	LM385-1.2/LM385B-1.2 Max	Unit
Reverse Breakdown Voltage $I_{Rmin} \le I_R \le 20$ mA	$V_{(BR)R}$							V
LM285-1.2/LM385B-1.2		1.223	1.235	1.247	1.223	1.235	1.247	
LM385-1.2		—	—	—	1.205	1.235	1.260	
Minimum Operating Current ($T_A = T_{low}$ to T_{high} Note 1)	I_{Rmin}	—	2.5	10	—	2.5	15	μA
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)}/\Delta I_R$							mV
$I_{Rmin} \le I_R \le 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	1.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance	Z							Ω
I_R = 100 μA, T_A = +25°C		—	0.2	0.6	—	0.4	1.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
Average Temperature Coefficient 10 μA $\le I_R \le$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	20	—	—	20	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	60	—	—	60	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ±0.1°C	S	—	20	—	—	20	—	ppm/kHR

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise noted)

Characteristic	Symbol	LM285-2.5 Min	LM285-2.5 Typ	LM285-2.5 Max	LM385-2.5/LM385B-2.5 Min	LM385-2.5/LM385B-2.5 Typ	LM385-2.5/LM385B-2.5 Max	Unit
Reverse Breakdown Voltage 20 μA $\le I_R \le$ 20 mA	$V_{(BR)R}$							V
LM285-2.5/LM385B-2.5		2.462	2.5	2.538	2.462	2.5	2.538	
LM385-2.5		—	—	—	2.425	2.5	2.575	
Minimum Operating Current $T_A = T_{low}$ to T_{high} (Note 1)	I_{Rmin}	—	5.0	20	—	5.0	20	μA
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)}/\Delta I_R$							mV
20 μA $\le I_R \le$ 1.0 mA, T_A = +25°C		—	—	1.0	—	—	2.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	2.5	
1.0 mA $\le I_R \le$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance	Z							Ω
I_R = 100 μA, T_A = +25°C		—	0.2	0.6	—	0.4	1.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
Average Temperature Coefficient 20 μA $\le I_R \le$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	20	—	—	20	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	120	—	—	120	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ±0.1°C	S	—	20	—	—	20	—	ppm/kHR

NOTES: 1. T_{low} = −40°C for LM285-1.2, LM285-2.5
= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5
T_{high} = +85°C for LM285-1.2, LM285-2.5
= +70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

FIGURE 1 — REVERSE CHARACTERISTICS

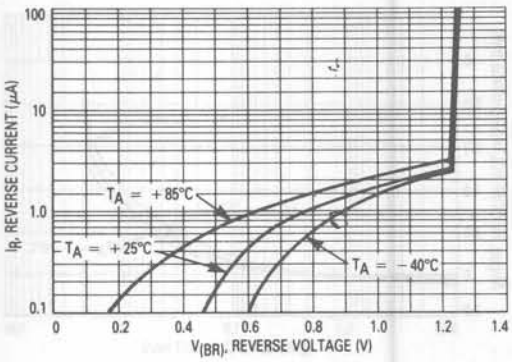


FIGURE 2 — REVERSE CHARACTERISTICS

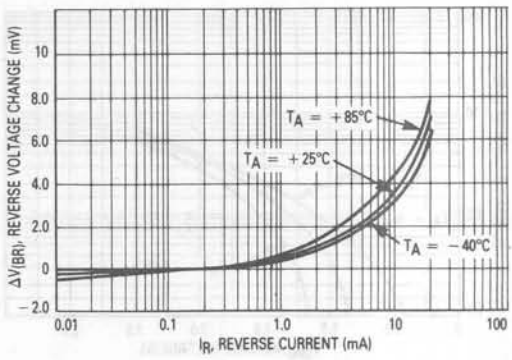


FIGURE 3 — FORWARD CHARACTERISTICS

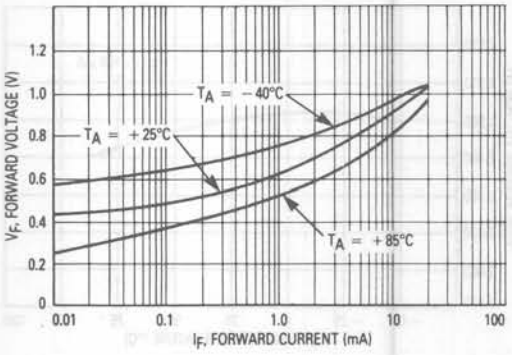


FIGURE 4 — TEMPERATURE DRIFT

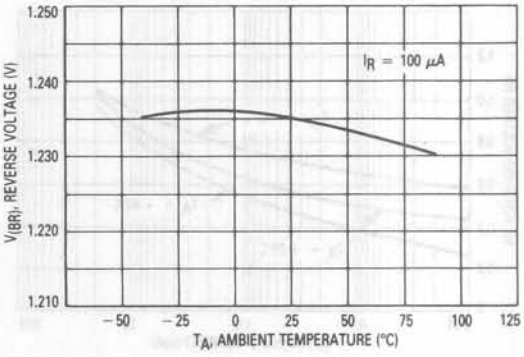


FIGURE 5 — NOISE VOLTAGE

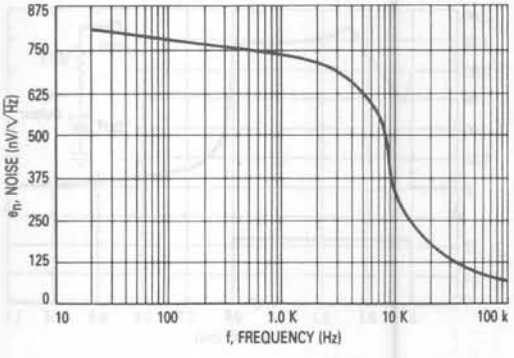
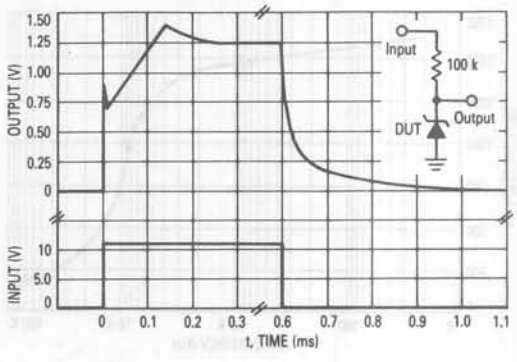


FIGURE 6 — RESPONSE TIME



TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

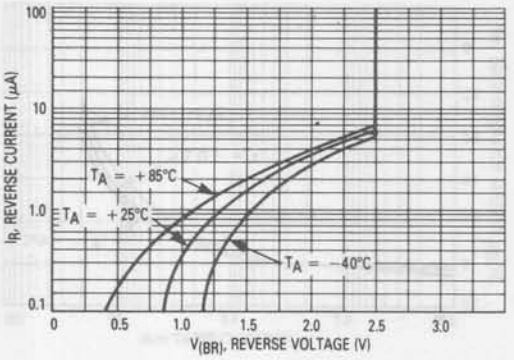


FIGURE 8 — REVERSE CHARACTERISTICS

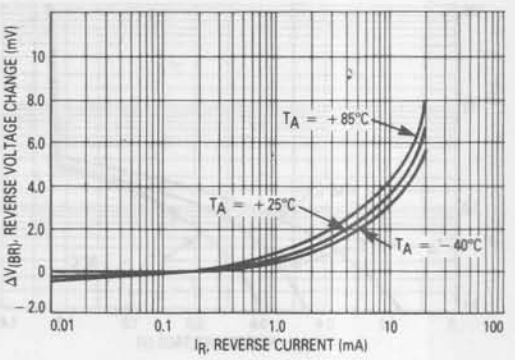


FIGURE 9 — FORWARD CHARACTERISTICS

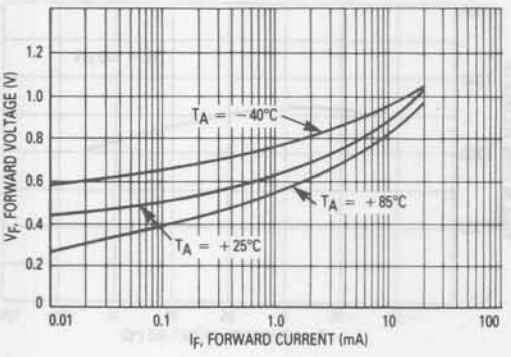


FIGURE 10 — TEMPERATURE DRIFT

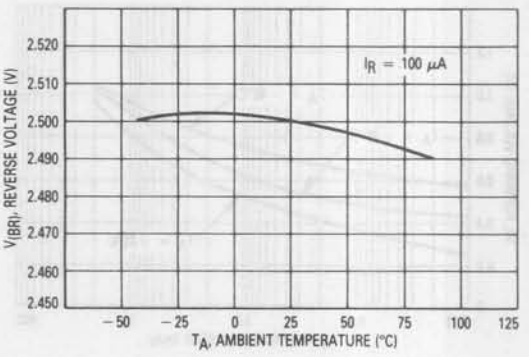


FIGURE 11 — NOISE VOLTAGE

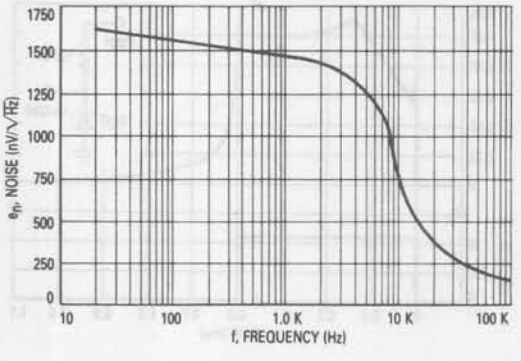
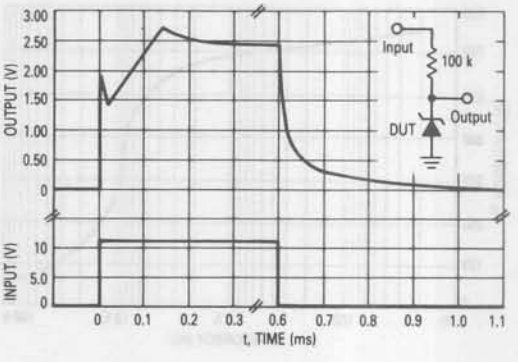


FIGURE 12 — RESPONSE TIME



MOTOROLA

MC1403,A
MC1503,A

LOW-VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1506, MC1508, and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

- Output Voltage = 2.5 V ±25 mV
- Input Voltage Range = 4.5 V to 40 V
- Quiescent Current = 1.2 mA typ
- Output Current = 10 mA
- Temperature Coefficient = 10 ppm/°C typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP Package

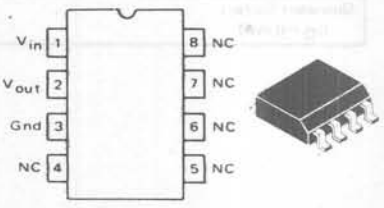
Typical Applications

- Voltage Reference for 8-12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

PRECISION LOW-VOLTAGE REFERENCE

LASER TRIMMED SILICON MONOLITHIC INTEGRATED CIRCUIT

U SUFFIX
CERAMIC PACKAGE
CASE 693



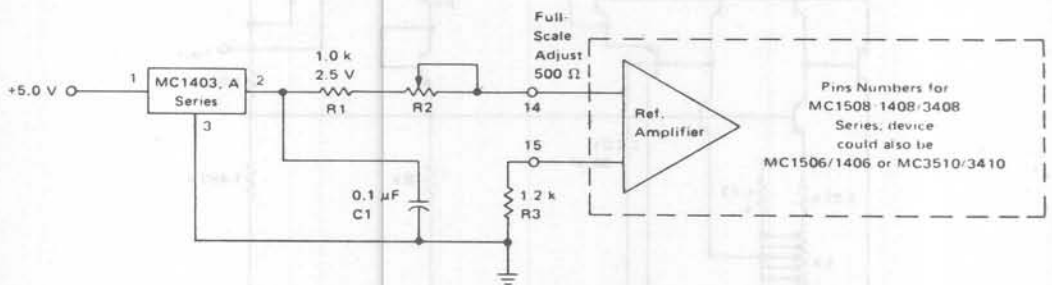
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	-65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temeprature Range MC1503,A MC1403,A	T_A	 -55 to +125 0 to +70	 °C °C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	-55 to +125°C	Ceramic DIP
MC1503AU	-55 to +125°C	Ceramic DIP
MC1403U	0 to +70°C	Ceramic DIP
MC1403AU	0 to +70°C	Ceramic DIP

FIGURE 1 – A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1406/1506, MC1408/1508, MC3410/3510 and MC3408 D/A converters all require a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

DL 9468

ELECTRICAL CHARACTERISTICS (V_I = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O	2.475	2.50	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		–	–	55	
MC1503A		–	–	25	
MC1403		–	10	40	
MC1403A		–	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503 } -55°C to +125°C		–	–	25	
MC1503A } -55°C to +125°C		–	–	11	
MC1403 } 0°C to +70°C		–	–	7.0	
MC1403A } 0°C to +70°C		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15 V ≤ V_I ≤ 40 V)		–	1.2	4.5	
(4.5 V ≤ V_I ≤ 15 V)		–	0.6	3.0	
Load Regulation ($0 mA < I_O < 10 mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_I	–	1.2	1.5	mA

FIGURE 2 – MC1403/1503 SCHEMATIC

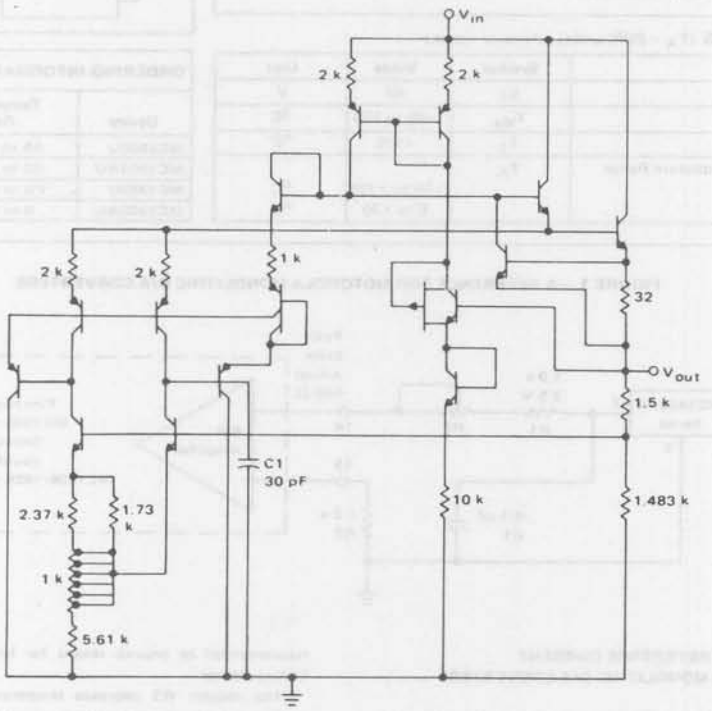


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in}
(NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

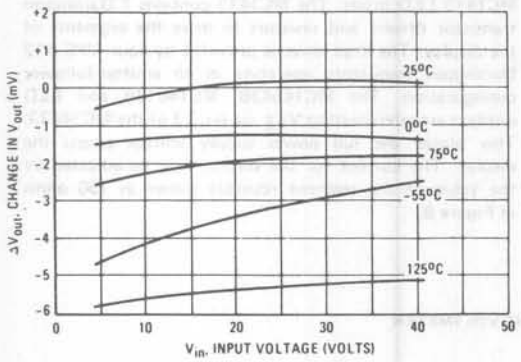


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE
versus LOAD CURRENT
(NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

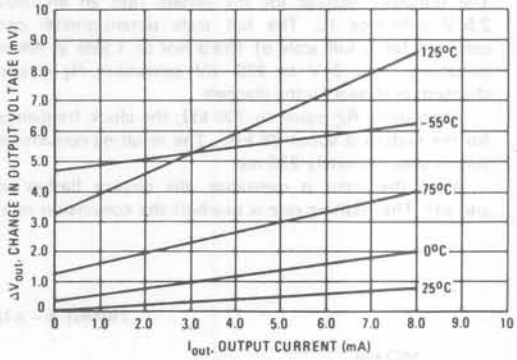


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE
(V_{in} = 15 V, I_{out} = 0 mA)

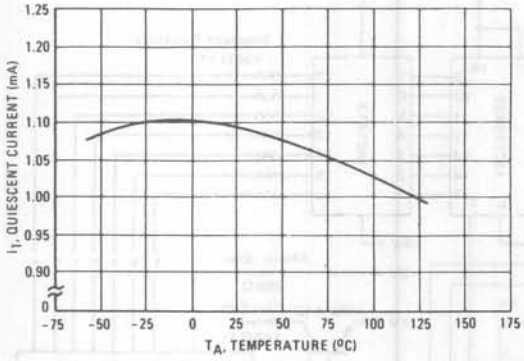


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO V_{out} @ V_{in} = 15 V)

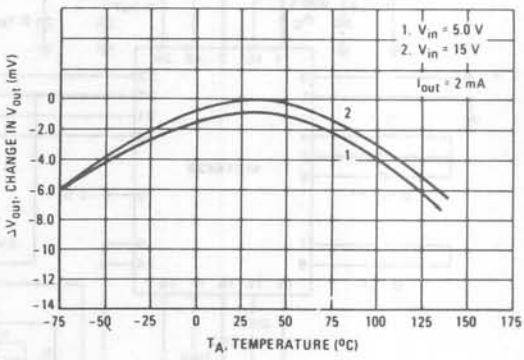
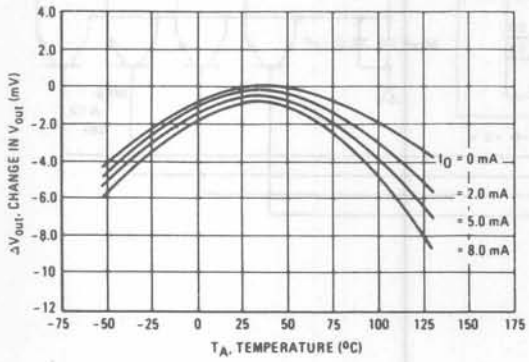
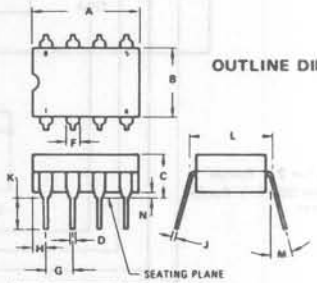


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO T_A @ V_{in} = 15 V, I_{out} = 0 mA)



OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 693

3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

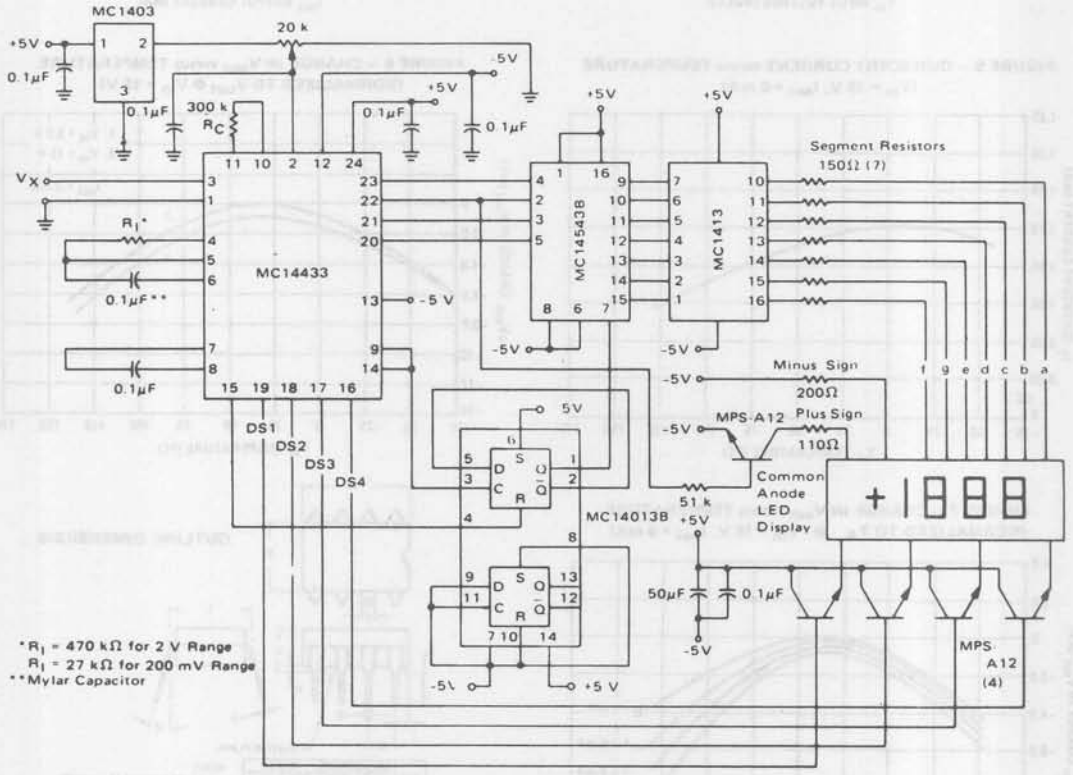
An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

FIGURE 8 – 3-1/2-DIGIT VOLTMETER



MOTOROLA

MC1408
MC1508

Specifications and Applications Information

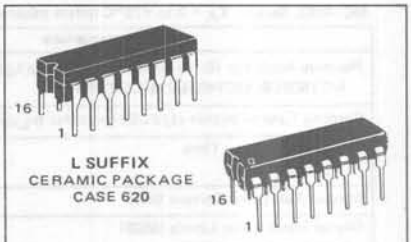
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

2

FIGURE 1 – D-to-A TRANSFER CHARACTERISTICS

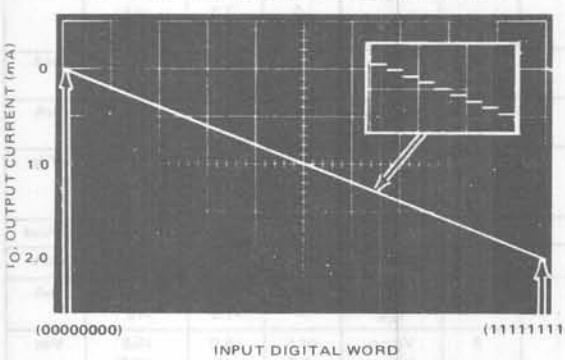
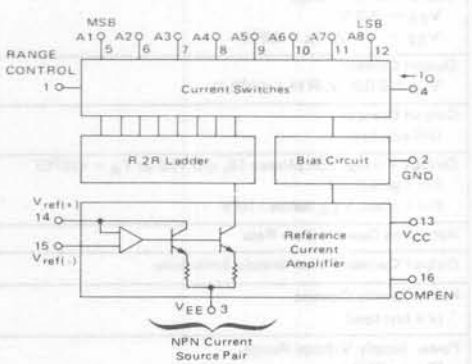


FIGURE 2 – BLOCK DIAGRAM



TYPICAL APPLICATIONS

- Tracking A-to-D Converters
- Successive Approximation A-to-D Converters
- 2 1/2 Digit Panel Meters and DVM's
- Waveform Synthesis
- Sample and Hold
- Peak Detector
- Programmable Gain and Attenuation
- CRT Character Generation
- Audio Digitizing and Decoding
- Programmable Power Supplies
- Analog-Digital Multiplication
- Digital-Digital Multiplication
- Analog-Digital Division
- Digital Addition and Subtraction
- Speech Compression and Expansion
- Stepping Motor Drive

DS 9238 R1

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

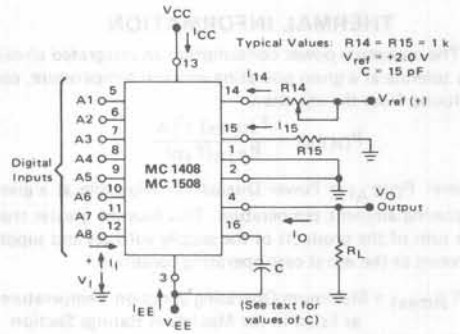
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L8: T_A = -55°C to +125°C, MC1408L Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8	4	E_r	–	–	±0.19	%
Settling Time to within ±1/2 LSB [includes t_{PLH}] (T_A=+25°C) See Note	5	t_S	–	300	–	ns
Propagation Delay Time T_A = +25°C	5	t_{PLH},t_{PHL}	–	30	100	ns
Output Full Scale Current Drift		TCI_O	–	-20	–	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 –	 – –	 – 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 – –	 0 -0.4	 0.04 -0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	–	-1.0	-5.0	μA
Output Current Range V_{EE} = -5.0 V V_{EE} = -15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{ref} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All bits low)	3	$I_{O(min)}$	–	0	4.0	μA
Output Voltage Compliance ($E_r \leq 0.19\%$ at T_A = +25°C) Pin 1 grounded Pin 1 open, V_{EE} below -10 V	3	V_O	 – –	 – –	 -0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	–	4.0	–	mA/μs
Output Current Power Supply Sensitivity		PSRR(–)	–	0.5	2.7	μA/V
Power Supply Current (All bits low)	3	I_{CC} I_{EE}	– –	+13.5 -7.5	+22 -13	mA
Power Supply Voltage Range (T_A = +25°C)	3	V_{CCR} V_{EER}	+4.5 -4.5	+5.0 -15	+5.5 -16.5	Vdc
Power Dissipation All bits low V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc All bits high V_{EE} = -5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 – – – –	 105 190 90 160	 170 305 – –	mW

Note All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left\{\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

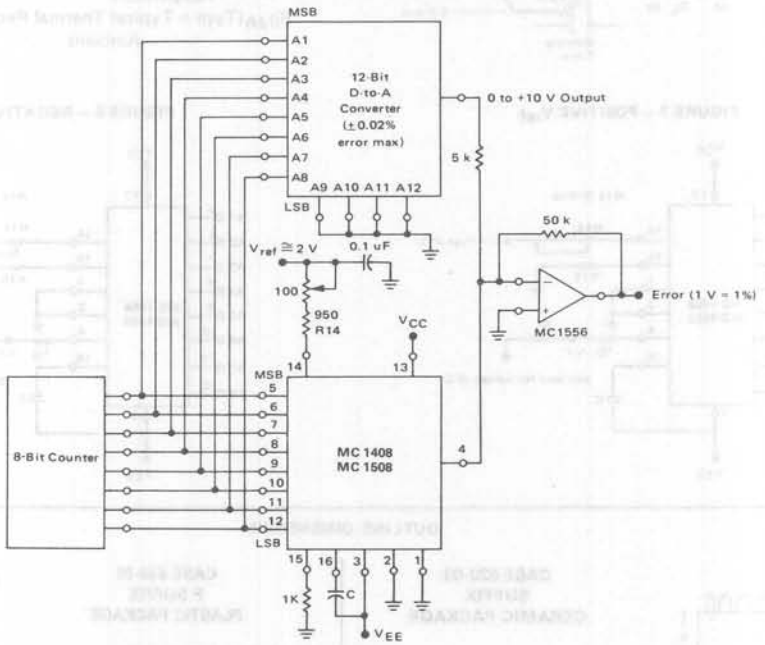
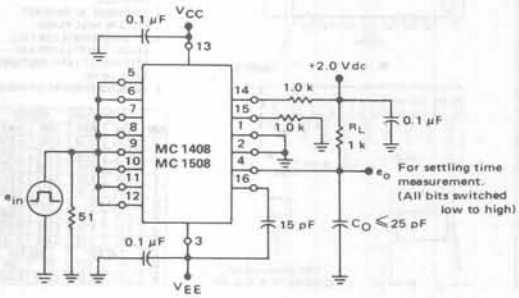
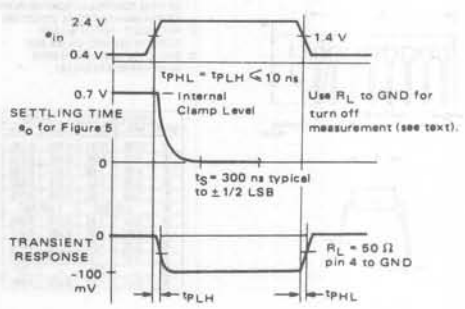


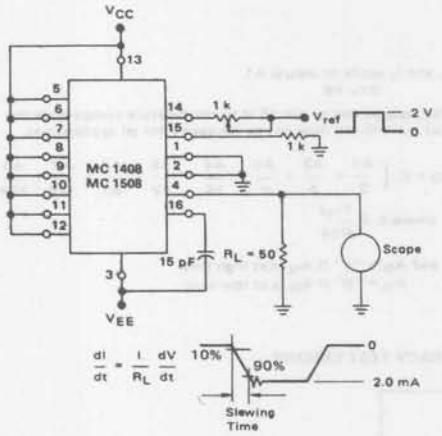
FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME





TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT



THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 7 – POSITIVE V_{ref}

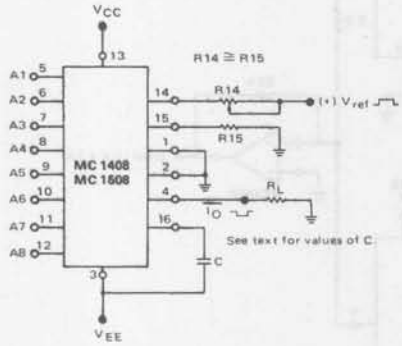
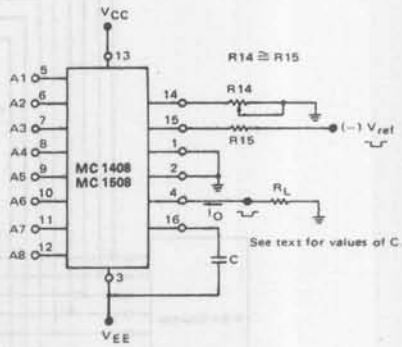


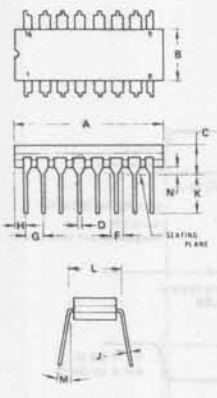
FIGURE 8 – NEGATIVE V_{ref}



2

OUTLINE DIMENSIONS

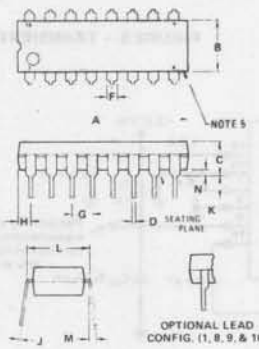
CASE 620-02
SUFFIX
CERAMIC PACKAGE



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.85	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

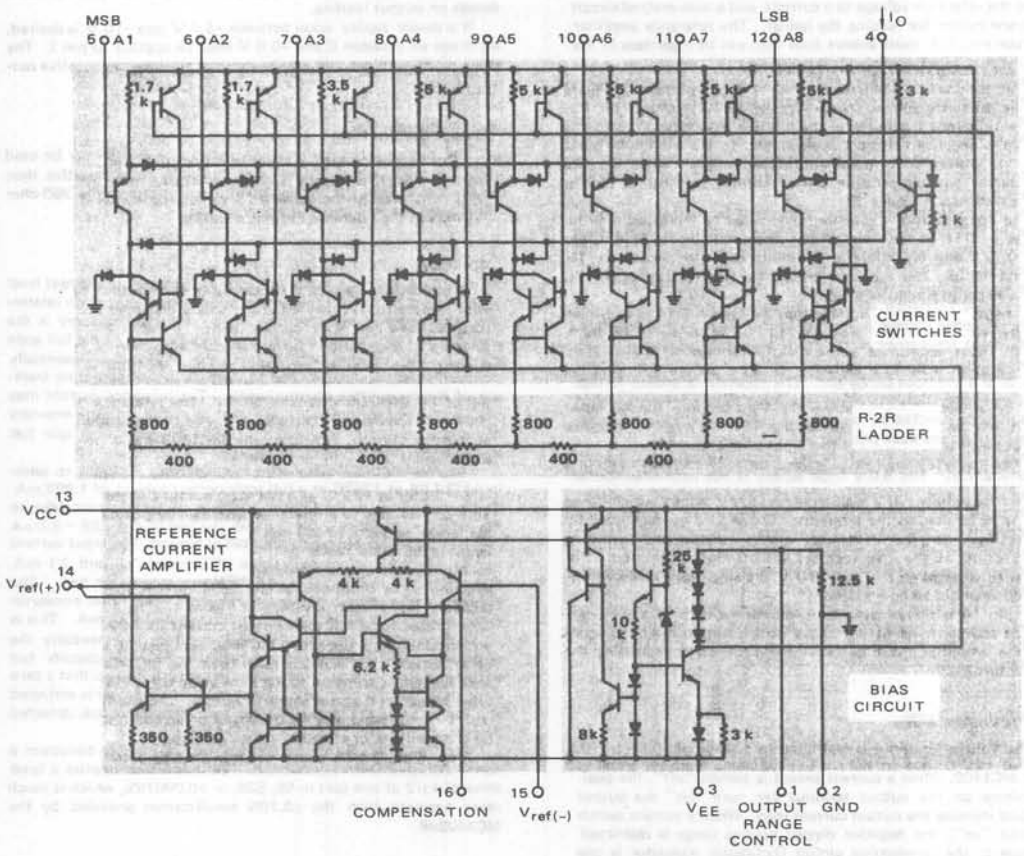
CASE 648-05
P SUFFIX
PLASTIC PACKAGE



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. ROUNDED CORNERS OPTIONAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	4.06	5.08	0.160	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.51	1.02	0.020	0.040

FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leq 500$ ohms and $C_O \leq 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

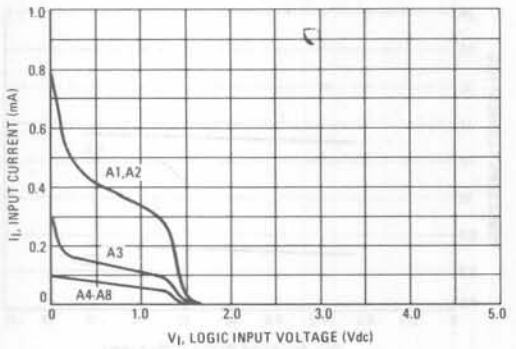


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE
(A5 thru A8 thresholds lie within range for A1 thru A4)

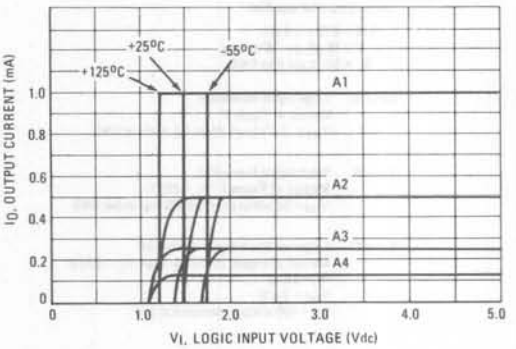


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE
(See text for pin 1 restrictions)

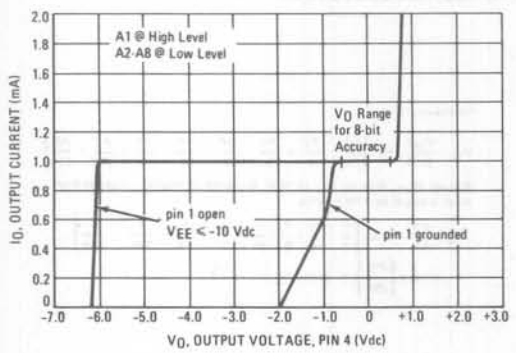
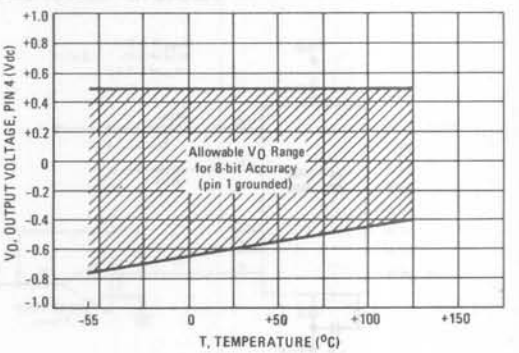


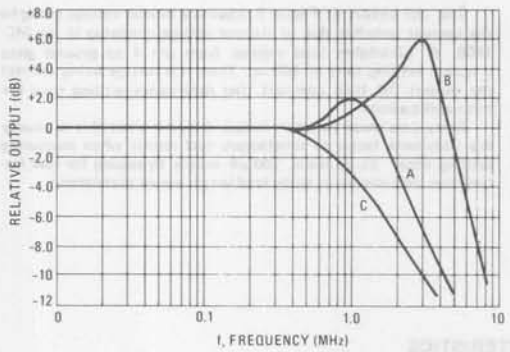
FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE
(Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

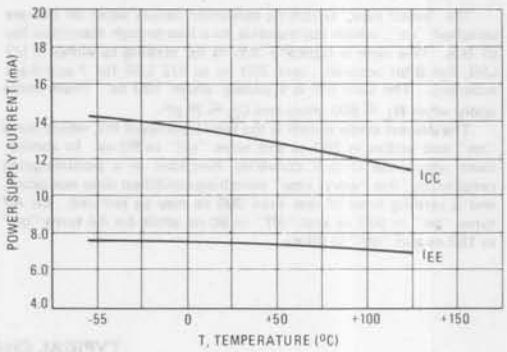
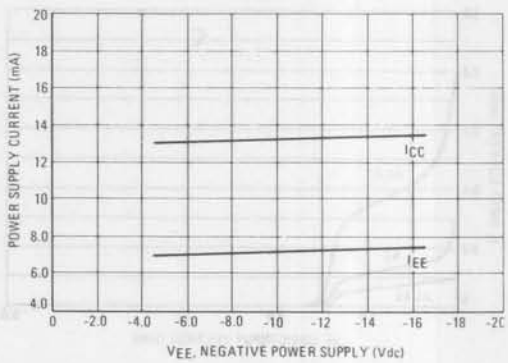
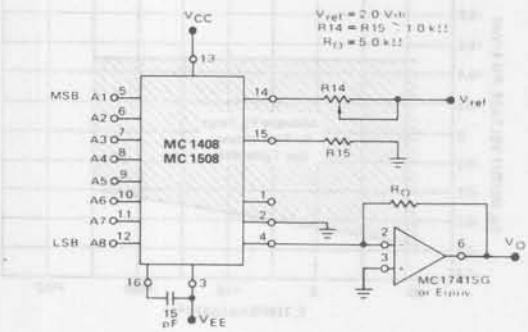


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

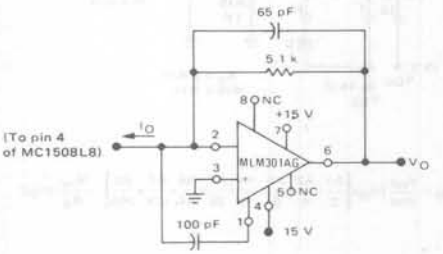
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

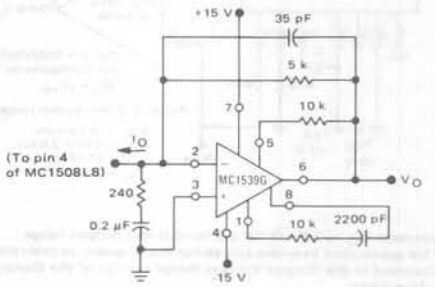
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



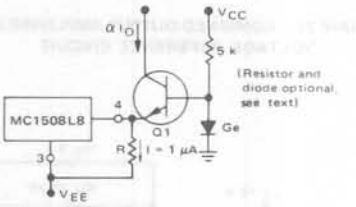
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

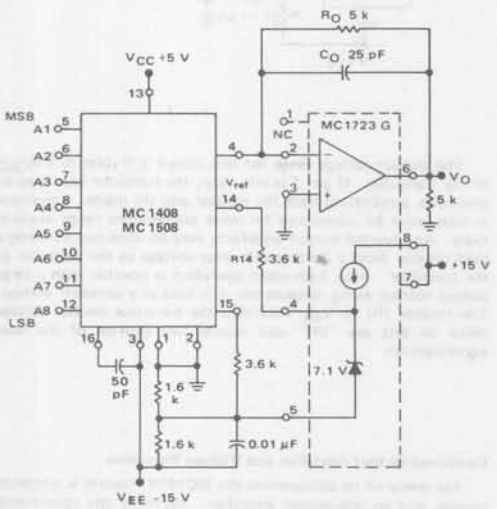
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

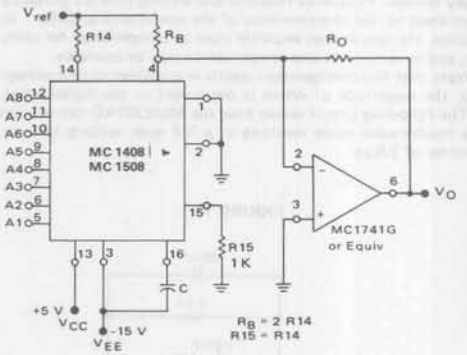
FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



Bipolar or Negative Output Voltage

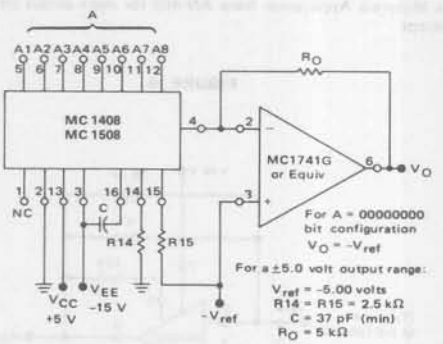
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]-\frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



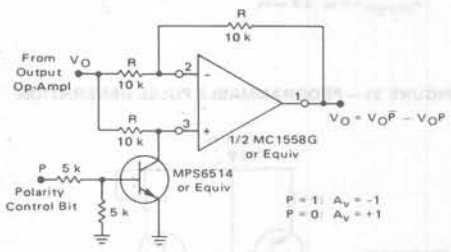
Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT
(8-Bit Magnitude Plus Sign D-to-A Converter)



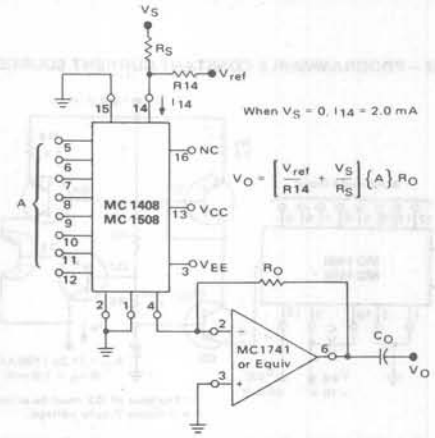
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

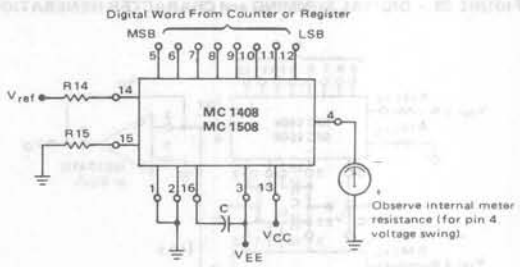
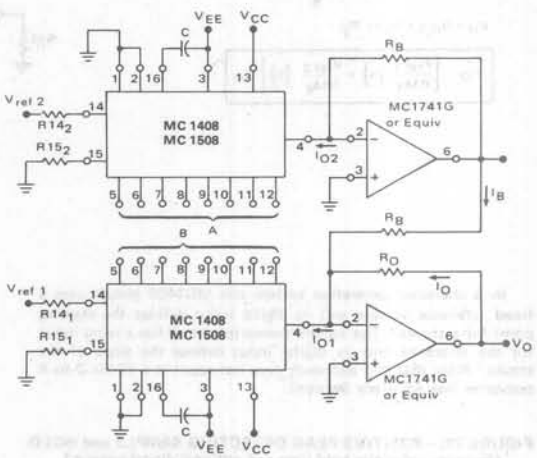


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



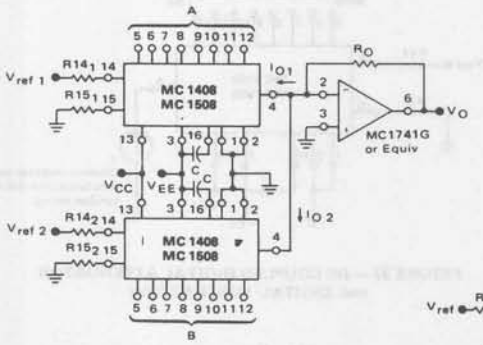
2

APPLICATIONS INFORMATION (continued)

This digital subtraction application is useful for indicating when one digital word is approaching another in value. More information is available than with a digital comparator.

Bipolar inputs can be accepted by using any of the previously described methods, or applied differentially to $R14_1$ and $R14_2$ or $R15_1$ and $R15_2$. V_O will be a bipolar signal defined by the above equation. Note that the circuit shown accepts bipolar differential signals but does not have a negative common-mode range. A very useful method is to connect $R14_1$ and $R14_2$ to a positive reference higher than the most positive input, and drive $R15_1$ and $R15_2$. This yields high input impedance, bipolar differential and common-mode range.

FIGURE 28 – DIGITAL SUMMING and CHARACTER GENERATION



In a character generation system one MC1408 circuit uses a fixed reference voltage and its digital input defines the starting point for a stroke. The second converter circuit has a ramp input for the reference and its digital input defines the slope of the stroke. Note that this approach does not result in a 16-bit D-to-A converter (see Accuracy Section).

FIGURE 29 – POSITIVE PEAK DETECTING SAMPLE and HOLD (Features indefinite hold time and optional digital output.)

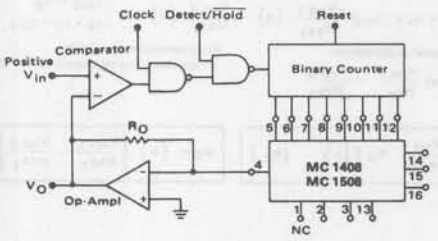


FIGURE 30 – NEGATIVE PEAK DETECTING SAMPLE AND HOLD

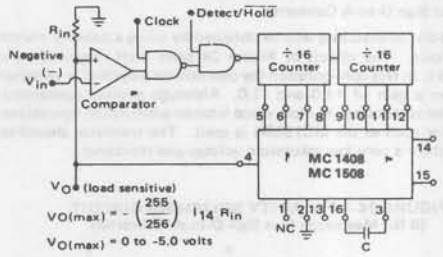
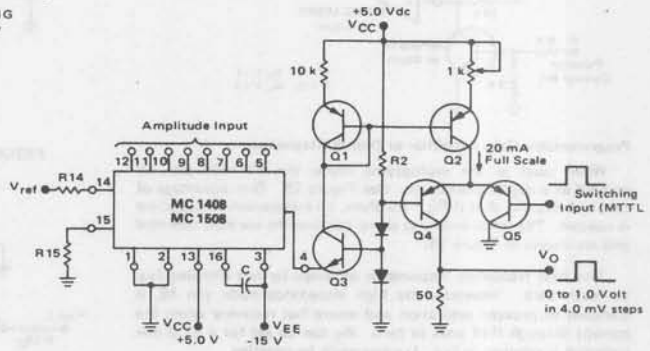
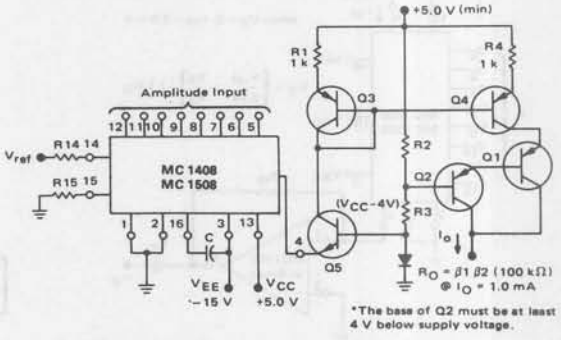


FIGURE 31 – PROGRAMMABLE PULSE GENERATION



Fast rise and fall times require the use of high-speed switching transistors for the differential pair, Q4 and Q5. Linear ramps and sine waves may be generated by the appropriate reference input.

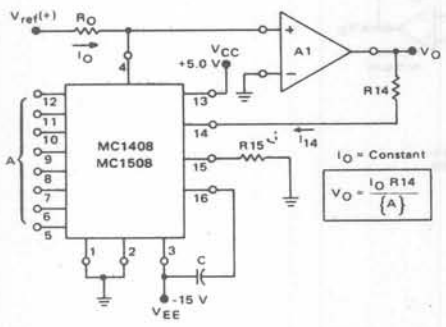
FIGURE 32 – PROGRAMMABLE CONSTANT CURRENT SOURCE



Current pulses, ramps, staircases, and sine waves may be generated by the appropriate digital and reference inputs. This circuit is especially useful in curve tracer applications.

APPLICATIONS INFORMATION (continued)

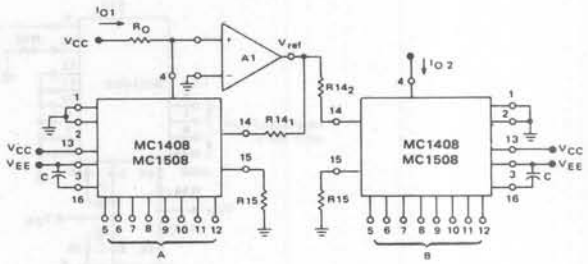
FIGURE 33 – ANALOG DIVISION BY DIGITAL WORD



This circuit yields the inverse of a digital word scaled by a constant. For minimum error over the range of operation, I_O can be set at 16 μA so that I_{14} will have a maximum value of 3.984 mA for a digital bit input configuration of 00000001.

Compensation is necessary for loop stability and depends on the type of operational amplifier used. If a standard 1.0 MHz operational amplifier is employed, it should be overcompensated when possible. If the MC1733, MC1520 or any other wideband amplifier are used, the reference amplifier should always be overcompensated.

FIGURE 34 – ANALOG QUOTIENT OF TWO DIGITAL WORDS



$$V_{ref} = \frac{I_{O1} R14_1}{\{A\}}$$

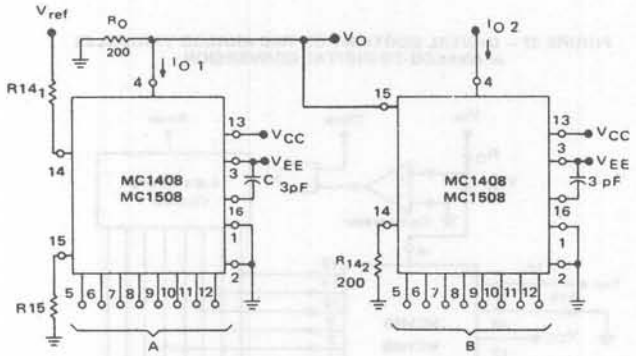
$$I_{O2} = \frac{V_{ref}}{R14_2} \{B\}$$

if $R14_1 = R14_2$

$$I_{O2} = I_{O1} \frac{\{B\}}{\{A\}}$$

2

FIGURE 35 – ANALOG PRODUCT OF TWO DIGITAL WORDS
(High-Speed Operation)



$$V_O = -I_{O1} R_O = \frac{V_{ref}}{R14_1} \{A\} R_O$$

$$I_{O2} = \frac{\{B\} |V_O|}{R14_2} = \frac{\{B\}}{R14_2} \left[R_O \left(\frac{V_{ref}}{R14_1} \right) \{A\} \right]$$

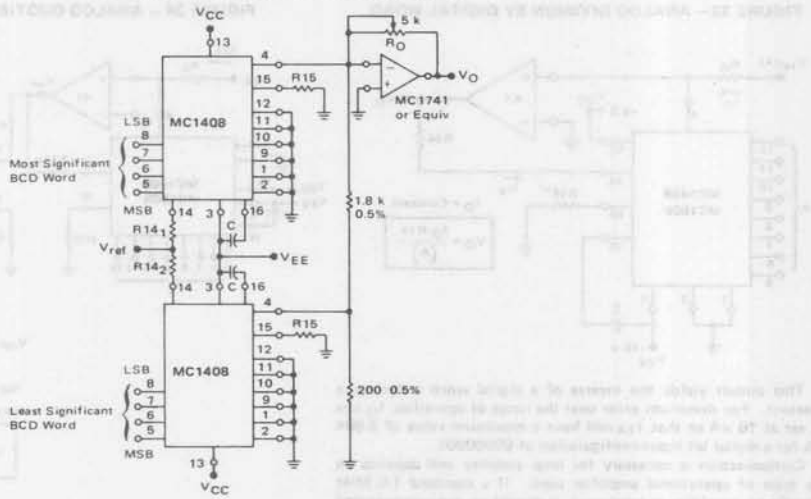
Since $R_O = R14_2$ and $K = \frac{V_{ref}}{R14_1}$

$$I_{O2} = K \{A\} \{B\}$$

K can be an analog variable.

APPLICATIONS INFORMATION (continued)

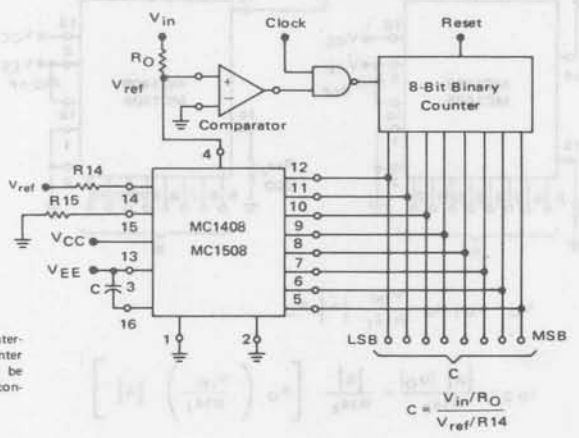
FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten.

2

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA

MC6108

Advance Information

8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

The MC6108 is a microprocessor compatible, 8-bit, high speed analog-to-digital converter. Included are a precision reference, DAC, comparator, SAR, matched scale resistors, 3-state output buffers, and control logic. Conversion can be completed in under 2.0 μs and input voltage ranges of 0 to +10 V, 0 to +5.0 V, and −5.0 to +5.0 V can be converted without additional external components. With appropriate external resistors, the converter can accommodate other input voltage ranges. 8-bit linearity and monotonic operation with no missing codes are guaranteed over temperature. Bus compatibility is provided for by the 3-state outputs (latches not required).

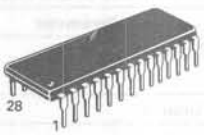
The MC6108 conversion time is short enough to allow most microprocessors to accept the data immediately after requesting a conversion. Applications include process control systems, servo control systems, waveform storage, signal processing, and others.

This device is functionally and pin compatible with the AM6108.

- 1.8 μs Conversion Time (Guaranteed)
- Microprocessor Compatible — Connect Directly to Data Bus
- Trimmed Internal Voltage Reference
- 0.1% Nonlinearity (Typ)
- Low Operating Voltage (+5.0 V, −5.2 V)
- Internal Matched Gain, Reference, and Offset Resistors
- Pin Programmable Natural Binary or Two's Complement
- Conversion Complete Available as Interrupt or on Data Bus
- Max Power Dissipation — 415 mW

8-BIT MPU BUS-COMPATIBLE HIGH SPEED A-TO-D CONVERTER

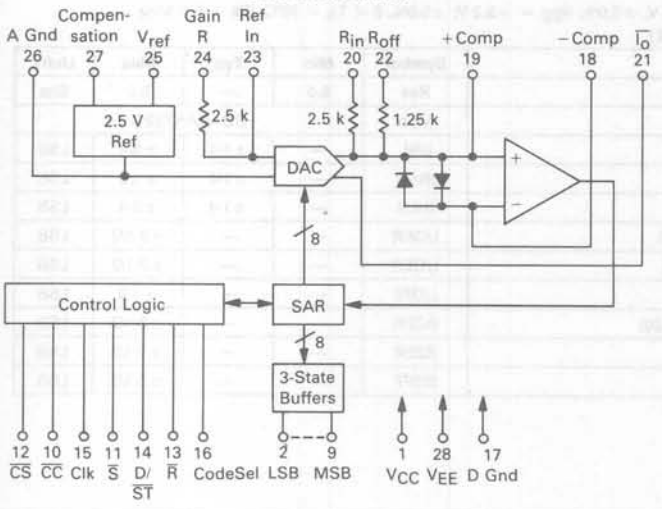
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

2

BLOCK DIAGRAM



PIN CONNECTIONS

ADI1328

ABSOLUTE MAXIMUM RATINGS

(Voltages referred to D. Gnd except where noted)

Parameter	Value	Units
V_{CC} (Pin 1)	−0.3, +7.0	V
V_{EE} (Pin 28)	+0.3, −7.0	V
Max Differential ($V_{CC} - V_{EE}$)	12	V
Digital Inputs (Pins 11–16)	−0.5, +6.0	V
A. Gnd (Pin 26)	±1.0	V
Input Current @ Ref In, Gain R	3.0	mA
Voltage @ Gain R	V_{CC}, V_{EE}	V
Voltage @ R_{in}, R_{off}	±12	V
Voltage @ +Comp, −Comp, $\overline{I_o}$	−2.5, +12	V
Voltage @ D0–D7 (in 3-state mode)	−0.5, +6.0	V
Junction Temperature	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

(Voltages referred to D. Gnd except where noted)

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{EE}	−5.46	−5.2	−4.94	V
Analog Ground	AGnd	−0.1	0	0.1	V
V_{ref} Current	I_{Vref}	0	—	5.0	mA
Voltage @ Gain R	—	1.25	2.5	5.0	V
Ref In Current	I_{ref}	0.5	1.0	2.0	mA
Voltage @ R_{in}	V_{in}	−8.0	—	10	V
Voltage @ R_{off}	V_{off}	−8.0	—	10	V
Clock Frequency	f_{clk}	0	—	5.0	MHz
Voltage @ −Comp	—	0	0	4.0	V
Voltage @ $\overline{I_o}$	—	−1.0	0	+5.0	V
Digital Input Voltage	—	0	—	5.25	V
Ambient Temperature	T_A	0	—	+70	°C

TRANSFER CHARACTERISTICS

(V_{CC} = +5.0 V, ±5.0%, V_{EE} = −5.2 V, ±5.0%, 0 < T_A < 70°C, Clk = 5.0 MHz, V_{ref} connected to Gain R, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units
Resolution	Res	8.0	—	8.0	Bits
Monotonicity	Mon	GUARANTEED			
Differential Non-Linearity	DNL	—	±1/4	±3/4	LSB
Integral Non-Linearity (Unipolar)	INLU	—	±1/4	±1/2	LSB
Integral Non-Linearity (Bipolar)	INLB	—	±1/4	±3/4	LSB
Unipolar Gain Error (V_{in} = 0 to +5.0 V @ Pin 22)	UGER	—	—	±2-1/2	LSB
Unipolar Gain Error (V_{in} = 0 to +10 V @ Pin 20)	UGER	—	—	±2-1/2	LSB
Unipolar Offset Error (D7–D0 = 00_H to 01_H)	UOFF	—	—	±1.0	LSB
Bipolar Gain Error (V_{in} = −5.0 to +5.0 V @ Pin 20)	BGER	—	—	±2-1/2	LSB
Bipolar Zero Error (D7–D0 = $7F_H$ to 80_H)	BZER	—	—	±1-1/2	LSB
Bipolar Offset Error (D7–D0 = 00_H to 01_H)	BOFF	—	—	±2-1/2	LSB

TRANSFER CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
I_o Full Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	I_{FS}	3.1	3.992	4.9	mA
$\overline{I_o}$ Zero Scale Current (D7–D0 = FF_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{ZS}}$	−5.0	—	+5.0	μA
I_o Zero Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	I_{ZS}	3.0	7.8	13	μA
$\overline{I_o}$ Full Scale Current (D7–D0 = 00_H, T_A = 25°C) (See Text "DAC")	$\overline{I_{FS}}$	3.1	3.984	4.9	mA
DAC Current Gain (See Text "DAC")	G_{DAC}	3.92	4.0	4.08	—
Gain Sensitivity to V_{CC} Variations ($4.75 < V_{CC} < 5.25$ V, $V_{EE} = -5.2$ V)	$PSSV_{CC}$	—	±0.01	±0.2	%FS
Gain Sensitivity to V_{EE} Variations ($-5.46 < V_{EE} < -4.94$ V, $V_{CC} = +5.0$ V)	$PSSV_{EE}$	—	±0.02	±0.2	%FS
INTERNAL REFERENCE SUPPLY					
Pin 25 Voltage ($I_{ref} = -1.0$ mA, $V_{CC} = +5.0$, $V_{EE} = -5.2$)	V_{ref}	2.475	2.5	2.525	V
Temperature Coefficient	T_C	—	±20	—	ppm/°C
Load Regulation (-1.0 mA $< I_{ref} < -5.0$ mA)	Reg_{load}	—	±0.05	±0.2	$\%V_{ref}$
Line Regulation ($4.75 < V_{CC} < 5.25$ V)	Reg_{line}	—	±0.02	±0.2	$\%V_{ref}$
Noise (f_n = 10 kHz to 1.0 MHz, T_A = 25°C)	—	—	20	—	μV_{rms}
Short Circuit Current (T_A = 25°C)	IRSC	−30	−20	−5	mA
POWER SUPPLIES					
V_{CC} Current (Outputs unloaded)	I_{CC}	5.0	20	27	mA
V_{EE} Current (Outputs unloaded)	I_{EE}	−50	−38	−5	mA
Power Dissipation (Outputs unloaded)	P_D	—	300	415	mW
ANALOG INPUTS (T_A = 25°C)					
Input Resistance @ Gain R (Pin 24)	R_{GR}	—	2.5	—	kΩ
Input Resistance @ R_{in} (Pin 20)	R_{RI}	1.75	2.5	3.25	kΩ
Input Resistance @ R_{off} (Pin 22)	R_{RO}	—	1.25	—	kΩ
Reference Input Offset Voltage (Pin 23–26)	Ref_{off}	−10	—	+10	mV
Comparator Input Clamp Voltage (4.0 mA through the back-to-back diodes)	V_{clamp}	±0.4	±0.8	±1.3	V
Input Capacitance @ +Comp (Pin 19)	C_C	—	20	—	pF
Input Capacitance @ $\overline{I_o}$ (Pin 21)	C_I	—	10	—	pF
Input Capacitance @ R_{in}, R_{off}, Ref In, Gain R, −Comp.	—	—	2.0	—	pF
DIGITAL INPUTS					
Input Voltage — High (Pins 11–16)	V_{IH}	2.0	—	5.25	V
Input Voltage — Low (Pins 11–16)	V_{IL}	0	—	0.8	V
Input Current @ 4.0 V (Pins 11–16)	I_{IH}	—	—	10	μA
Input Current @ 0 V (Pins 11–16)	I_{IL}	—	—	10	μA
DIGITAL OUTPUTS					
Output Voltage — High ($I_{OH} = -400$ μA, Pins 2–10)	V_{OH}	2.4	3.2	—	V
Output Voltage — Low (I_{OL} = 8.0 mA, Pins 2–10)	V_{OL}	—	0.15	0.4	V
Short Circuit Current* (Pins 2–10, T_A = 25°C)	I_{SC}	−50	−25	—	mA
Three-State Leakage (V_O = 2.4 V, Pins 2–9) (V_O = 0.4 V, Pins 2–9)	I_{HLK} I_{LLK}	−20 −20	— —	+20 +20	μA
Capacitance (3-State Mode, Pins 2–9)	C_O	—	7.0	—	pF

*Short circuits should be limited to 1.0 second max, 1 output at a time.
Note: Currents into a pin designated as +, currents out of a pin designated as −

2

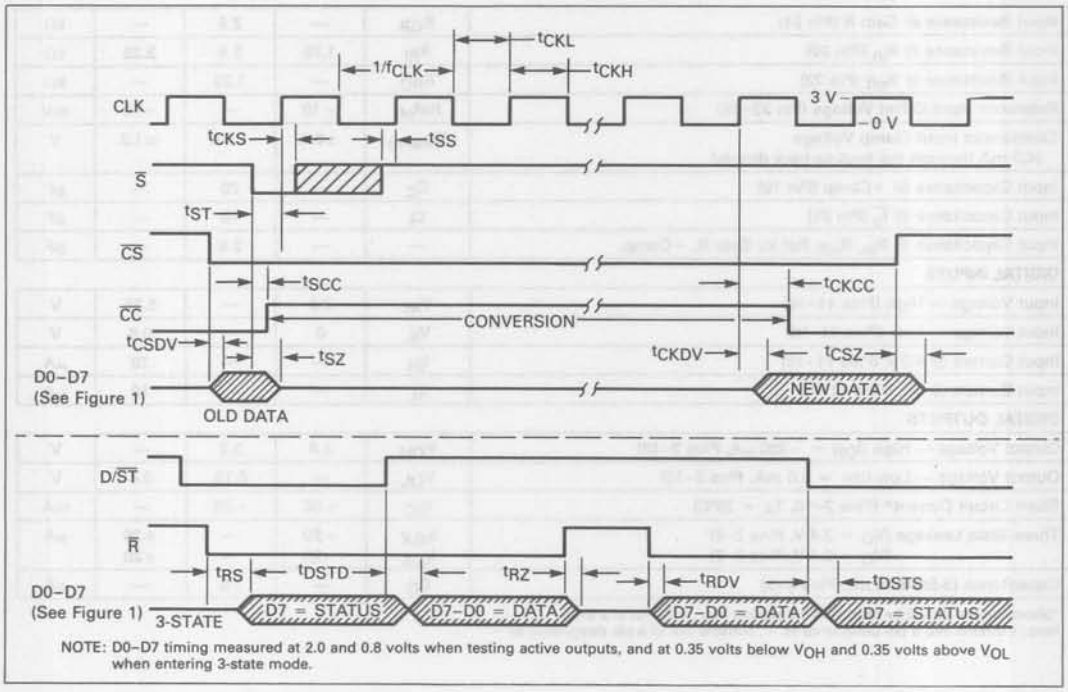
TIMING CHARACTERISTICS (T_A = 25°C, See System Timing Diagram)

Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
$\overline{S}$ High After CLK High*	t_{CKS}	0	—	—	ns
$\overline{S}$ High Before CLK High*	t_{SS}	25	—	—	ns
CLK Low Time	t_{CKL}	50	—	—	ns
CLK High Time	t_{CKH}	50	—	—	ns
CLK Rise, Fall Time	t_r, t_f	—	—	100	ns
$\overline{CS}$, CLK, $\overline{S}$ Concurrent Low Time*	t_{ST}	50	—	—	ns
Clock Frequency	f_{CLK}	—	—	5.0	MHz
*See text (Sequence of Operation)					
OUTPUTS					
$\overline{CC}$ High from $\overline{S}$, $\overline{CS}$, or CLK Low	t_{SCC}	—	25	55	ns
Data to 3-State from $\overline{S}$, and CLK Low**	t_{SZ}	—	25	55	ns
$\overline{CC}$ Low from CLK High	t_{CKCC}	—	15	40	ns
Data Valid from CLK High**	t_{CKDV}	—	25	50	ns
Data Valid from $\overline{CS}$ Low**	t_{CSDV}	—	25	40	ns
Data to 3-State from $\overline{CS}$ High**	t_{CSZ}	—	20	40	ns
Data Valid from $\overline{R}$ Low**	t_{RDV}	—	20	40	ns
Data to 3-State from $\overline{R}$ High**	t_{RZ}	—	20	40	ns
D7 to Status from D/$\overline{ST}$ Low**	t_{DSTS}	—	20	40	ns
D7 to Data from D/$\overline{ST}$ High**	t_{DSTD}	—	20	40	ns
D7 to Status from $\overline{R}$ Low**	t_{RS}	—	20	40	ns

**See Figure 1 for output conditions

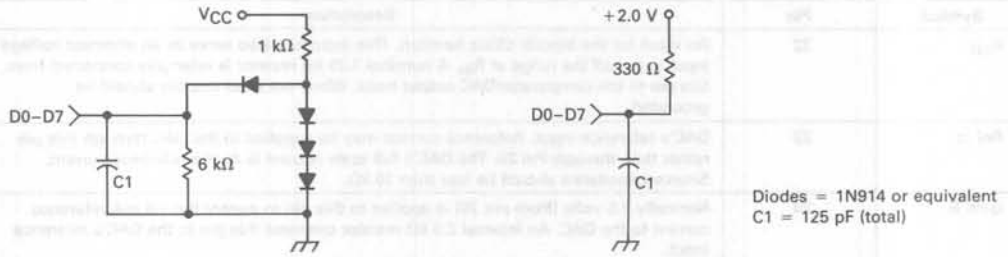
2

SYSTEM TIMING DIAGRAM



NOTE: D0–D7 timing measured at 2.0 and 0.8 volts when testing active outputs, and at 0.35 volts below V_{OH} and 0.35 volts above V_{OL} when entering 3-state mode.

FIGURE 1 — DATA OUTPUT LOAD TEST CIRCUIT



TEMPERATURE SPECIFICATIONS ($0° < T_A < 70°$ C)

Function	Pin	Typical Change	Units
V_{ref}	25	±20	ppm/°C
DAC Current Gain	—	±8.0	ppm/°C
$\overline{I_o}$ Dynamic Impedance	21	+1.1	%/°C
Reference Input Offset	23–26	±20	μV/°C
Resistance @ R_{in}, R_{off}, Gain R	20,22,24	+0.1	%/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
V_{CC}	1	To be connected to a 5.0 volts (±5.0%) supply.
D0–D7	2–9	TTL level data outputs capable of three-state mode. Pin 2 is the LSB, Pin 9 is the MSB. Pin 9 can also indicate conversion status.
$\overline{CC}$	10	Conversion Complete. TTL level output. High indicates conversion in progress, low indicates conversion complete and valid data at the outputs. This output does not have three-state capability.
$\overline{S}$	11	Start conversion — TTL Input. Taking $\overline{S}$ low (with Clock and Chip Select low) resets the SAR. Taking $\overline{S}$ high allows the conversion to start.
$\overline{CS}$	12	Chip Select — TTL Input. When low, a conversion may be initiated or data read at the outputs. When high, data outputs are in the three-state mode, and other digital inputs are ignored.
$\overline{R}$	13	Read — TTL Input. When low, data may be read at D0–D7. When high, D0–D7 are in three-state condition.
D/$\overline{ST}$	14	Data/$\overline{Status}$ — TTL Input. When high, D0–D7 provide normal data. When low, D7 indicates "Conversion Complete" status, while D0–D6 are in three-state mode.
CLK	15	Clock — TTL Input. 0–5.0 MHz.
CodeSel	16	Code Select — TTL Input. When low, output data is in 2's complement format. When high, output data is straight binary (offset binary when used in the bipolar mode).
D. Gnd	17	Digital Ground. Connect to ground associated with digital side of the circuitry.
−Comp	18	Negative input of the comparator. Normally grounded, a voltage on this pin will provide an offset of the input voltage range.
+Comp	19	Positive input of the comparator. Normally open, this pin may be used for input voltage ranges other than 0–10 volts, or ±5.0 volts.
R_{in}	20	The voltage to be converted to a digital equivalent is normally applied to this pin. A nominal 2.5 kΩ resistor is internally connected from this pin to the comparator/DAC output node.
$\overline{I_o}$	21	Current flows into this pin, complementary in value to the DAC's normal current output (I_o). Normally grounded, it may be connected to a resistor to ground or a positive voltage source in order to provide an analog output.

PIN DESCRIPTIONS — continued

Symbol	Pin	Description
R_{off}	22	An input for the bipolar offset function. This input can also serve as an alternate voltage input with half the range at R_{in}. A nominal 1.25 kΩ resistor is internally connected from this pin to the comparator/DAC output node. When not used this pin should be grounded.
Ref In	23	DAC's reference input. Reference current may be supplied to the DAC through this pin rather than through Pin 24. The DAC's full scale current is 4x the reference current. Source impedance should be less than 10 kΩ.
Gain R	24	Normally 2.5 volts (from pin 25) is applied to this pin to supply the 1.0 mA reference current to the DAC. An internal 2.5 kΩ resistor connects this pin to the DAC's reference input.
V_{ref}	25	Output of the internal precision 2.5 volt reference supply, it can supply up to 5.0 mA. Normally used to supply the DAC's reference current and the bipolar offset current.
A. Gnd	26	Analog Ground. Connect to ground associated with the analog side of the circuitry.
Compen	27	Compensation for the reference supply regulator. Typically, a 0.01 μF capacitor is connected from this pin to A. Gnd or to V_{EE}.
V_{EE}	28	To be connected to a −5.2 volts (±5.0%) supply.

DESIGN GUIDELINES

ANALOG SECTION

DAC (Refer to Figures 2 and 3)

The DAC generates an output current (I_o) which is proportional to both the reference current and the digital input presented to it by the Successive Approximation Register (SAR), according to the following formula:

$$I_o = \frac{I_{ref} \times 4 \times A}{256} + I_{zs} \qquad (1)$$

where A is the binary digital code (0–255), and I_{zs} is the zero scale current. I_o flows ***into*** the DAC, never out. The 4x (±2.0%) factor is a current gain built into the DAC. For a nominal I_{ref} of 1.0 mA, the maximum I_o (@A = 255) is 3.992 mA (which includes an I_{zs} of 7.8 μA). I_{zs} is built in so the first transition occurs when the signal voltage (V_{in}) is 1/2 LSB above its minimum value. In normal operation, I_o is supplied from the signal voltage that is being converted to a digital code. Therefore, the signal source must be capable of supplying up to 4.0 mA in the unipolar mode. I_{ref} is the reference current flowing in through either pin 23 or 24. See Figure 2 for the basic unipolar configuration.

In the bipolar mode, an offset current of 2.0 mA is supplied to the I_o node (normally through R_{off}) in order that V_{in} may be symmetrical about zero volts. The signal source must be capable of sinking 2.0 mA when at the negative extreme, and sourcing 2.0 mA when at the positive extreme. See Figure 3 for the basic bipolar configuration.

+Comp (Pin 19) is maintained close to a virtual ground after a conversion as long as −Comp (Pin 18) is at ground. The voltage at +Comp varies (nominally ±0.8 volts) during a conversion as the DAC forces different current values at I_o and will end up close to zero at the end of a conversion. Because of the varying voltage at +Comp, the current from the signal source and the offset source (if used) will vary with each step of the successive approximation sequence, necessitating that the signal source have a dynamic impedance less than

$$\frac{V_1 \times R_X}{1.6\ V} \qquad (2)$$

where V_1 = 1/2 LSB of the signal voltage, and
R_X = Resistance between the signal source and Pin 19
(2.5 kΩ if using R_{in}, 1.25 kΩ if using R_{off}).

Normally Pin 19 is left open, although it may be used as a path for the offset current, or the signal current (to be digitized), with appropriate external resistors. See the Applications Information for more details.

I_{ref} flows ***into*** the DAC, never out, and should be between 0.5 mA and 2.0 mA to preserve linearity and accuracy. Linearity specified in the Electrical Characteristics is tested @ I_{ref} of ≈1.0 mA. The reference input stage is depicted in Figure 4. Normally I_{ref} is supplied by the MC6108's internal 2.5 volt reference (Pin 25) through Gain R (Pin 24). If a separate voltage source is used for the reference current, it must be free of noise, spikes, and ripple since the accuracy of a conversion is directly related to the quality and stability of the reference.

SIGNAL VOLTAGE

The input signal voltage (to be digitized) is applied to either R_{in}, R_{off}, or through an appropriate external resistor to +Comp, such that current from the signal source flows into the DAC's I_o port. The preset ranges, with V_{ref} connected to Gain R are as follows:

Input Range	Connect R_{in} to	Connect R_{off} to
0 to +10 V	V_{in}	A. Gnd
0 to +5.0 V	A. Gnd	V_{in}
−5.0 to +5.0 V	V_{in}	V_{ref}

FIGURE 2 — BASIC UNIPOLAR CONFIGURATION

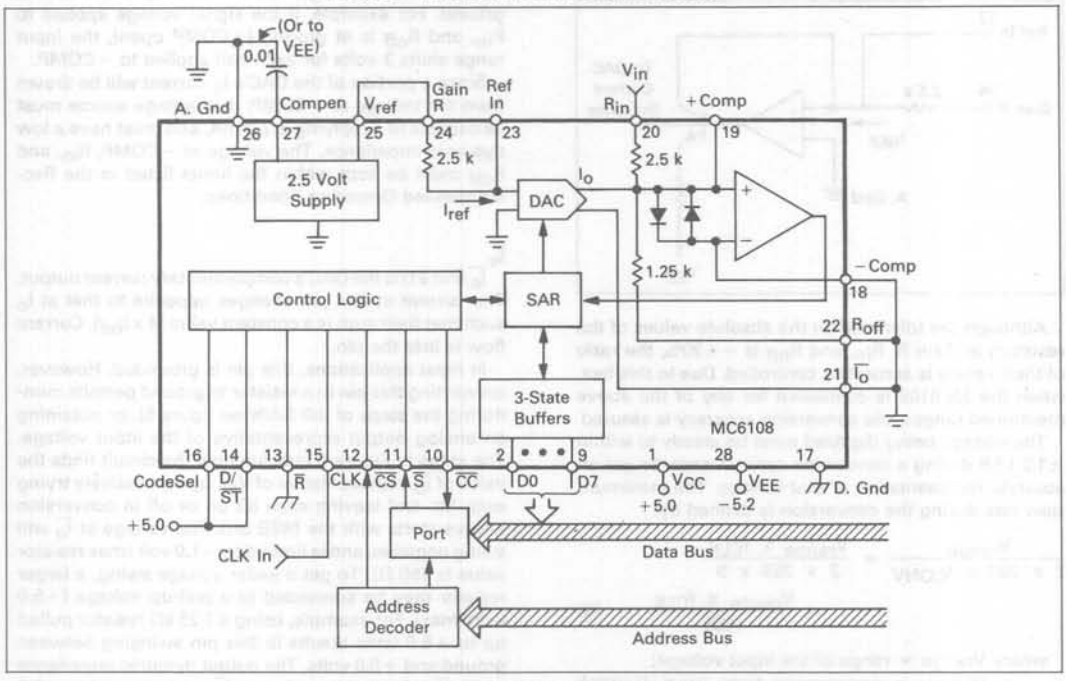


FIGURE 3 — BASIC BIPOLAR CONFIGURATION

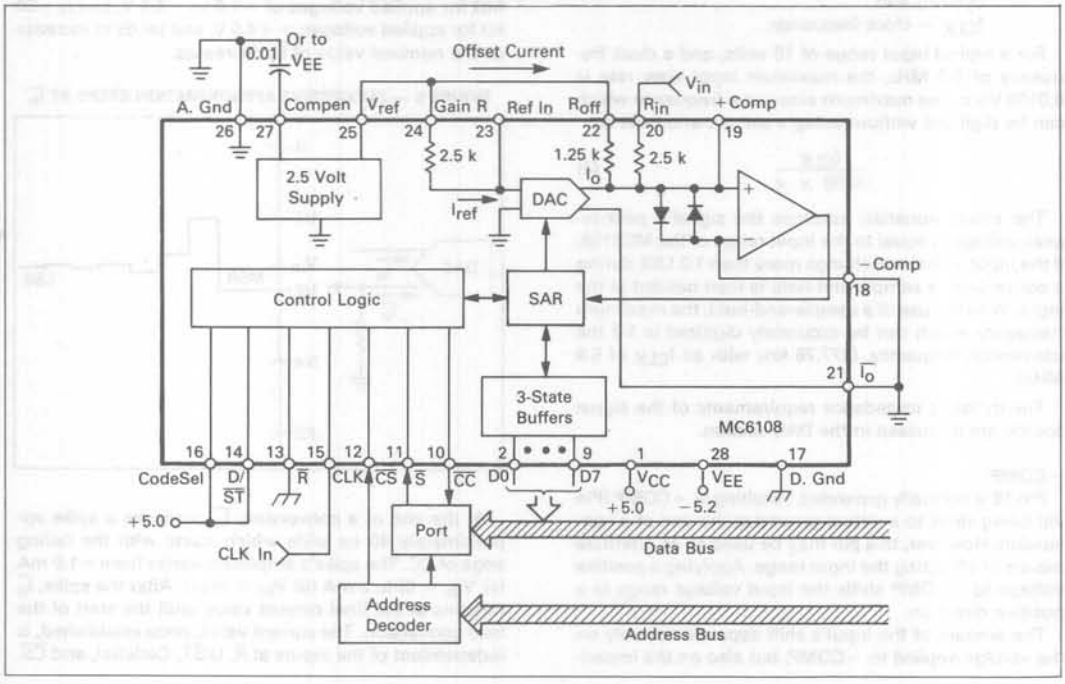


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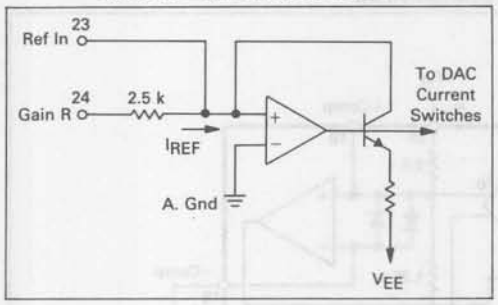
FIGURE 4 — REFERENCE AMPLIFIER



Although the tolerance on the absolute values of the resistors at Gain R, R_{in}, and R_{off} is $\approx \pm 30\%$, the ***ratio*** of their values is accurately controlled. Due to this fact, when the MC6108 is connected for any of the above mentioned ranges, the conversion accuracy is assured.

The voltage being digitized must be steady to within $\pm 1/2$ LSB during a conversion cycle in order to get an accurate representation of that voltage. The maximum slew rate during the conversion is defined by:

$$\frac{V_{range}}{2 \times 256 \times t_{CONV}} = \frac{V_{range} \times f_{CLK}}{2 \times 256 \times 9} = \frac{V_{range} \times f_{CLK}}{4608} \quad (3)$$

where Vrange = range of the input voltage;
t_{CONV} = conversion time (min. 9 clock cycles); and
f_{CLK} = clock frequency.

For a typical input range of 10 volts, and a clock frequency of 5.0 MHz, the maximum input slew rate is 0.0108 V/μs. The maximum sine-wave frequency which can be digitized without using a sample-and-hold is:

$$\frac{f_{CLK}}{4608 \times \pi} \quad (4)$$

The above equation assumes the signal's peak-to-peak voltage is equal to the input range of the MC6108. If the input signal will change more than 1/2 LSB during a conversion, a sample-and-hold is then needed at the input. With the use of a sample-and-hold, the maximum frequency which can be accurately digitized is 1/2 the conversion frequency, (277.78 kHz with an f_{CLK} of 5.0 MHz).

The dynamic impedance requirements of the signal source are discussed in the DAC section.

−COMP

Pin 18 is normally grounded, resulting in +COMP (Pin 19) being close to a virtual ground at the end of a conversion. However, this pin may be used as an alternate means of offsetting the input range. Applying a positive voltage to −COMP shifts the input voltage range in a positive direction.

The amount of the input's shift depends not only on the voltage applied to −COMP, but also on the impedances between the I_O node and the input source and ground. For example, if the signal voltage applied to R_{in}, and R_{off} is at ground (+COMP open), the input range shifts 3 volts for each volt applied to −COMP.

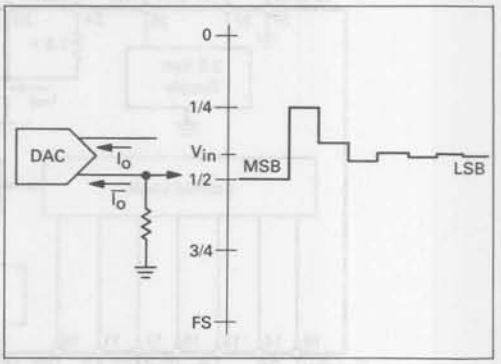
Since a portion of the DAC's I_O current will be drawn from the voltage at −COMP, that voltage source must be capable of supplying ± 2.0 mA, and must have a low dynamic impedance. The voltage at −COMP, R_{in}, and R_{off} must be kept within the limits listed in the Recommended Operating Conditions.

$\overline{I_O}$

$\overline{I_O}$ (Pin 21) is the DAC's complementary current output. The current at this pin changes opposite to that at I_O such that their sum is a constant value [4 x I_{ref}]. Current flow is ***into*** the pin.

In most applications, this pin is grounded. However, connecting this pin to a resistor to ground permits monitoring the steps of the SAR(see figure 5), or obtaining an analog output representative of the input voltage. The steps in Figure 5 indicate how the circuit finds the value of $\overline{I_O}$, representative of V_{in}, by successively trying each bit, and leaving each bit on or off (a conversion always starts with the MSB on). The voltage at $\overline{I_O}$ will swing negative, and is limited to −1.0 volt (max resistor value is 250 Ω). To get a wider voltage swing, a larger resistor may be connected to a pull-up voltage (+5.0 volts max). For example, using a 1.25 kΩ resistor pulled up to +5.0 volts results in this pin swinging between ground and +5.0 volts. The output dynamic impedance of the $\overline{I_O}$ current source (when $\overline{I_O}$ is maximum) is ≈ 2.0 MΩ for applied voltages of −1.0 to +4.0 V, and is ≈50 kΩ for applied voltages > +4.0 V, and tends to increase as the nominal value of $\overline{I_O}$ decreases.

FIGURE 5 — SUCCESSIVE APPROXIMATION STEPS AT $\overline{I_O}$



At the end of a conversion, $\overline{I_O}$ produces a spike approximately 40 ns wide which starts with the falling edge of $\overline{CC}$. The spike's amplitude varies from ≈1.0 mA (@ V_{in} = 0) to 0 mA (@ V_{in} = max). After the spike, $\overline{I_O}$ remains at the final current value until the start of the next conversion. The current value, once established, is independent of the inputs at $\overline{R}$, D/$\overline{ST}$, CodeSel, and $\overline{CS}$.

REFERENCE SUPPLY

The internal bandgap reference produces an output of +2.500 volts, ±25 mV (@ V_{ref}, pin 25), and is primarily intended to supply the reference current and the bipolar offset current. The output impedance is typically <0.5 Ω for load currents up to 5.0 mA, and increases rapidly at higher currents. Variations in V_{ref} are typically < 0.5 mV as V_{CC} is varied from +4.75 to +5.25 volts, and V_{ref} is independent of V_{EE} variations. The output is designed to source, not sink current.

A 0.001 μF capacitor from V_{ref} to A. Gnd is recommended to reduce noise on this output produced by the digital section. A 0.01 μF capacitor from the Compensation pin (Pin 27) to A. Gnd, or to V_{EE}, is necessary to stabilize the regulator.

POWER SUPPLIES

The power supplies are to be +5.0 volts, ±5.0% at V_{CC} (Pin 1), and −5.2 volts, ±5.0% at V_{EE} (Pin 28). For proper operation, bypassing is required for both supplies ***at the IC.*** 10 μF tantalum in parallel with 0.01 μF ceramic is recommended for each supply.

I_{CC} varies with the chip's different operating conditions, and is a maximum (typically 20 mA) during a conversion ($\overline{R}=0$, $D/\overline{ST}=1$, $\overline{CS}=0$) with the signal voltage at its minimum value. Minimum I_{CC} (typically 12 mA) occurs during a conversion with the signal voltage at its maximum value. I_{CC} is typically 16 mA when the MC6108 is deselected ($\overline{CS}=1$), and under all conditions, I_{CC} is independent of clock frequency.

I_{EE} is typically 38 mA, and varies <2.0 mA over different operating conditions. I_{EE} is independent of clock frequency.

DIGITAL SECTION

SEQUENCE OF OPERATION

A conversion is initiated when the $\overline{S}$ (Start), $\overline{CS}$ (Chip select), and CLK (Clock) inputs are simultaneously low for a minimum of 50 ns. The three inputs may be taken low in any sequence, including simultaneously. After all three have been brought low, $\overline{CC}$ (Conversion Complete) will change to a high state ≈25 ns later, indicating the SAR has been reset. A clock low-to-high transition must then occur before or with $\overline{S}$ switching high, and the conversion begins with the next CLK rising edge ($\overline{S}$ must precede that one by >25 ns). The conversion then requires seven complete clock cycles. At the end of the conversion, $\overline{CC}$ will switch low indicating the end of the conversion, and that valid data is available. See Figure 6 for the basic timing sequence.

If the $\overline{S}$, $\overline{CS}$, and CLK inputs appear simultaneously low ***during*** a conversion, the conversion sequence will be re-initiated at that point.

The following truth table describes the relationship of the six digital inputs (Pins 11–16):

Logic Inputs						Function
CLK	$\overline{CS}$	$\overline{S}$	$\overline{R}$	$D/\overline{ST}$	CodeSel	
X	1	X	X	X	X	Chip de-selected, D0–D7 @ Hi-Z
0	0	0	X	X	X	Reset SAR
↑ ↓	X	1	X	X	X	Conversion process (after SAR is reset)
X	0	X	1	X	X	D0–D7 @ Hi-Z
X	0	1	0	1	1	Read binary or offset binary data at D0–D7 after conversion
X	0	1	0	1	0	Read 2's complement data at D0–D7 after conversion
X	0	1	0	0	X	Read $\overline{CC}$ status at D7 (D0–D6 @ Hi-Z)

X = Don't care

Figure 7 depicts the input configurations in order to read the various output formats. Any digital input left open is equivalent to a Logic "0" — however, good design practice dictates that inputs should never be left open.

FIGURE 6 — CONVERSION TIMING DIAGRAM

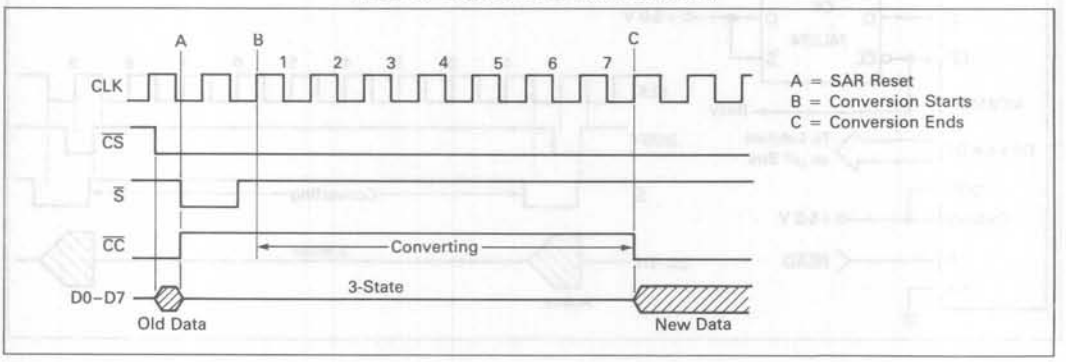
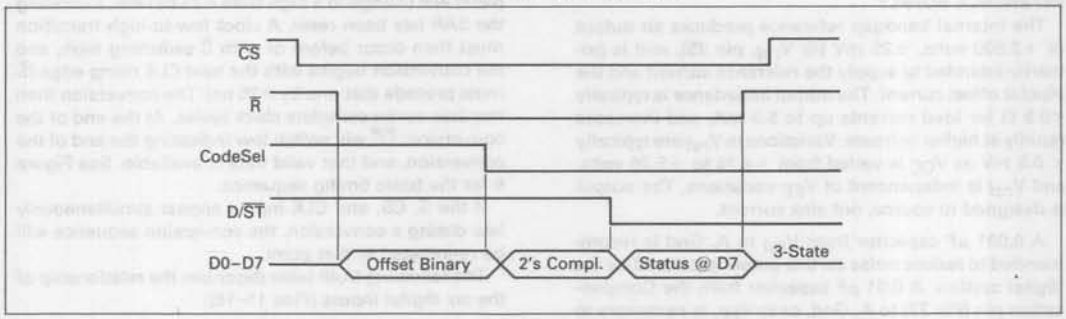


FIGURE 7 — OUTPUT DATA CONTROL



CLOCK

The clock input (Pin 15) is a TTL level input which steps the SAR through the successive approximation conversion process. There is no minimum required frequency, and the maximum operating frequency is listed in the timing characteristics. The clock duty cycle does not have to be 50%, but the minimum low and high times must be observed. The clock is needed only for the conversion, and may be removed or left applied to the MC6108 between conversions. The operation of $\overline{CS}$, D/$\overline{ST}$, $\overline{R}$, and CodeSel are not affected by the presence or absence of the clock.

CHIP SELECT

Chip Select (Pin 12) is a TTL level input which is normally used by a microprocessor's address decoding to select and de-select the device. A Logic "0" selects (enables) the MC6108, while a Logic "1" disables it. $\overline{CS}$ must be low for a conversion to start, and to read data at D0–D7 or status at D7 (see D/$\overline{ST}$ description). $\overline{CS}$ may be taken high during a conversion, as long as the minimum low time for $\overline{CS}$, $\overline{S}$, and CLK is adhered to, and then taken low in order to read the data after $\overline{CC}$ goes low. Alternately $\overline{CS}$ may be left low during the entire conversion.

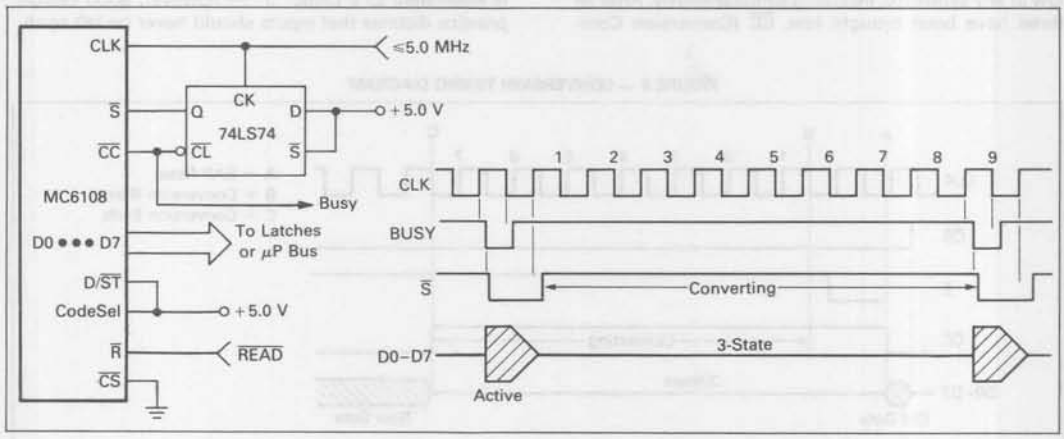
Whenever the MC6108 is de-selected, a conversion cannot be initiated, and D0–D7 are in the high-impedance condition, regardless of the other digital inputs.

START

$\overline{S}$ (Pin 11) is a TTL level input used to reset the SAR, and initiate a conversion. The SAR is reset when this pin is low simultaneous with the Clock and $\overline{CS}$ inputs for a minimum of 50 ns. $\overline{CC}$ output will then change to a high state. A clock rising edge must occur while $\overline{S}$ is low, or no later than coincident with its rising edge. There is no maximum time limit for $\overline{S}$ to stay low, but the conversion will not begin until the next rising edge of the Clock input ***after*** $\overline{S}$ goes high. Seven complete clock cycles are then needed to complete the conversion.

If the $\overline{S}$ input is connected to the $\overline{CC}$ output through a flip-flop (see Figure 8), the MC6108 will operate at the maximum possible conversion repetition rate, i.e. one conversion each 9 clock cycles.

FIGURE 8 — CONFIGURATION FOR MAXIMUM CONVERSION RATE



$\overline{\text{READ}}$

$\overline{\text{Read}}$ (Pin 13) is a TTL level input which controls the state of the outputs (D0–D7) between conversions as long as the MC6108 is enabled ($\overline{CS}$ = 0). A Logic "1" forces the 8 outputs to a high impedance condition regardless of the other digital inputs. A Logic "0" permits reading the data at D0–D7 after the conversion is complete, or the $\overline{CC}$ status at D7 (depending on the D/$\overline{ST}$ input). During a conversion, $\overline{R}$ is ineffective, except for controlling D7 if D/$\overline{ST}$ is low.

The $\overline{\text{Read}}$ input differs from the $\overline{CS}$ input in that taking $\overline{\text{Read}}$ high does not prevent a conversion from being initiated in response to the $\overline{CS}$, CLK, and $\overline{S}$ inputs (described elsewhere). If desired, the $\overline{\text{Read}}$ input may be kept low at all times in a simple application.

$\overline{\text{CONVERSION COMPLETE}}$

$\overline{CC}$ (Pin 10) is a TTL level output which indicates the status of the conversion. After $\overline{CS}$, CLK, and $\overline{S}$ are taken low to initiate a conversion, $\overline{CC}$ will go high ≈25 ns later. $\overline{CC}$ will stay high during the conversion, and then go low ≈15 ns after the rising edge of the clock corresponding to the end of the conversion. See Figure 6 and the System Timing Diagram.

The $\overline{CC}$ pin does not have a high impedance capability, and is therefore always active. The $\overline{CC}$ status is typically monitored through a port, or an interrupt pin.

DATA/$\overline{\text{STATUS}}$

D/$\overline{ST}$ (Pin 14) is a TTL level input which controls the information presented at D0–D7. When at a Logic "1", D0–D7 will provide the digital equivalent of the analog input at the end of the conversion (D0–D7 are in a high impedance mode during the conversion). When at a Logic "0", D0–D6 are maintained in a high impedance mode, while D7 provides the Conversion Complete status both during and after the conversion (D7 does not go into a high impedance mode). The rising and falling edges of D7, when providing status, follow those of $\overline{CC}$ (Pin 10) within ≈ 10 ns.

D/$\overline{ST}$ may be used by the microprocessor as a means of reading the Status ***and*** the Data on the bus rather than using a separate port for the $\overline{CC}$ output (Pin 10). However, since D7 is active during the conversion, the microprocessor cannot be busy with other functions during this time. If the microprocessor is to be busy during the conversion, the status may be checked by periodically switching the D/$\overline{ST}$ pin, or the $\overline{CS}$ pin, or by reading the $\overline{CC}$ pin (Pin 10) through a separate port or interrupt pin. $\overline{R}$ (Pin 13) must be low to read data or status.

CODE SELECT

CodeSel (Pin 16) is a TTL level input which controls the format of the binary data presented at D0–D7 at the end of a conversion. When at a Logic "1", the data is presented as natural binary or offset binary, depending on whether the analog input is unipolar or bipolar, respectively. When at a Logic "0", the output code is in 2's complement form (applicable to bipolar operation only). This pin has no effect on D7 when the D/$\overline{ST}$ input is low (see section on Data/$\overline{\text{Status}}$). The following tables illustrate examples of the different codes:

UNIPOLAR

Input	+10 V Range	+5.0 V Range	Natural Binary
FS — 1LSB	9.961 V	4.980 V	1111 1111
3/4 FS	7.500 V	3.750 V	1100 0000
1/2 FS	5.000 V	2.500 V	1000 0000
1/4 FS	2.500 V	1.250 V	0100 0000
0	0.000 V	0.000 V	0000 0000

BIPOLAR

Input	±5.0 V Range	Offset Binary	2's Complement
+FS — 1LSB	4.961 V	1111 1111	0111 1111
+1/2 FS	2.500 V	1100 0000	0100 0000
MidScale	0.000 V	1000 0000	0000 0000
−1/2 FS	−2.500 V	0100 0000	1100 0000
−FS + 1LSB	−4.961 V	0000 0001	1000 0001
−FS	−5.000 V	0000 0000	1000 0000

If an input voltage range other than those listed above is used, and CodeSel is at a Logic "1" (binary format), the code 0000 0000 will correspond to the most negative input voltage, while the code 1111 1111 corresponds to the most positive input voltage (−1 LSB). The 2's complement code is the same as the binary with the MSB (D7) inverted.

DATA OUTPUTS

The data outputs (Pins 2–9) are TTL level outputs with high impedance capability. Pin 2 is the LSB (D0), while Pin 9 is the MSB (D7). The 8 outputs are in the high impedance mode during a conversion ($\overline{CC}$ = high), or if $\overline{CS}$ or $\overline{R}$ are high. D0–D6 are in the high impedance mode, and D7 is active, anytime that D/$\overline{ST}$ is low ($\overline{CS}$ = $\overline{R}$ = 0).

During normal operation, the 8 outputs change from valid data to high impedance within 55 ns after the SAR has been reset ($\overline{CS}$ = CLK = $\overline{S}$ = 0) at the beginning of a conversion, and back to valid data within 50 ns after the rising edge of the CLK at the end of a conversion.

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The P.C. board layout, the quality of the power supplies and the ground system ***at the IC*** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC6108 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground ***at the IC*** (within 1" max) with a 10 μF tantalum and a 0.01 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors (<10 Ω, metal film) or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50 – 200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC6108.

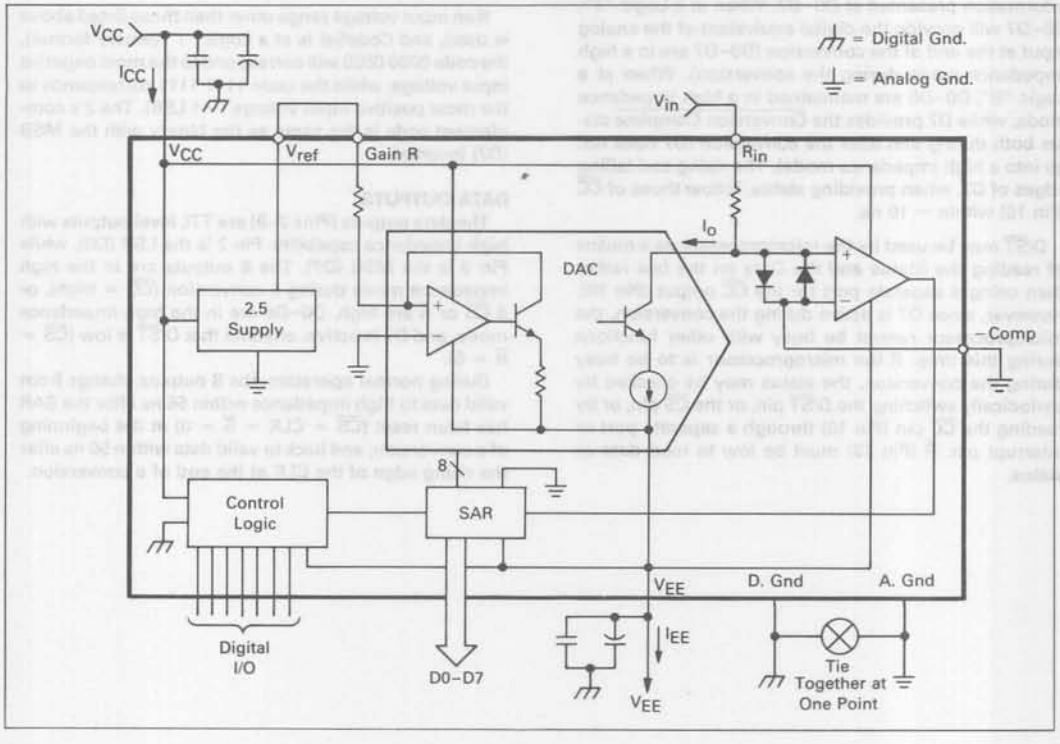
The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The P.C. board tracks supplying V_{CC} and V_{EE} to the MC6108 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC6108 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC6108.

The MC6108 has two ground pins — A. Gnd (Pin 26), and D. Gnd. (Pin 17). V_{CC} and V_{EE} should be referenced to D. Gnd. A. Gnd is mainly a signal ground, and is the return path for the internal 2.5 volt reference, and the DAC's reference amplifier. A. Gnd must be connected to D. Gnd, preferably at one point, and in a manner so as to not pick up noise. The dc voltage between A. Gnd and D. Gnd must be <100 mV. Long PC tracks between them should be avoided as the inductance (at 5.0 MHz) can create stability problems. See Figure 9 for a depiction of the major current paths.

2

FIGURE 9 — MAJOR CURRENT PATHS



FULL SCALE, ZERO ADJUSTMENTS

The unadjusted full scale accuracy (at max. V_{in}) of the MC6108, when the internal resistors are used (Figures 2 and 3), is guaranteed to be within 2-1/2 LSBs. The offset error (at min. V_{in}) is guaranteed to be less than 1LSB for the unipolar configuration, and 2-1/2 LSBs for the bipolar configuration. If the application requires greater accuracy at the end points, then adjustments are needed, as shown in Figures 10 and 11. The potentiometers should be 20-turn type, with low T.C. The 50 Ω resistor is added to the R_{in} pin to ensure that the potentiometers can provide adjustment over the full plus and minus error range.

FIGURE 10 — UNIPOLAR ADJUSTMENTS

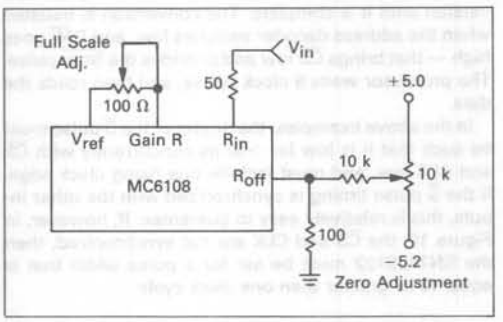
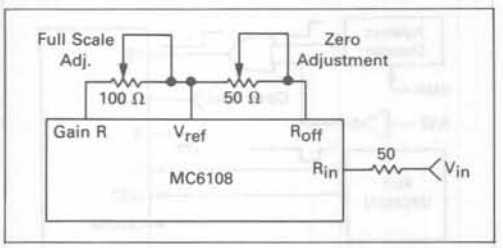


FIGURE 11 — BIPOLAR ADJUSTMENTS

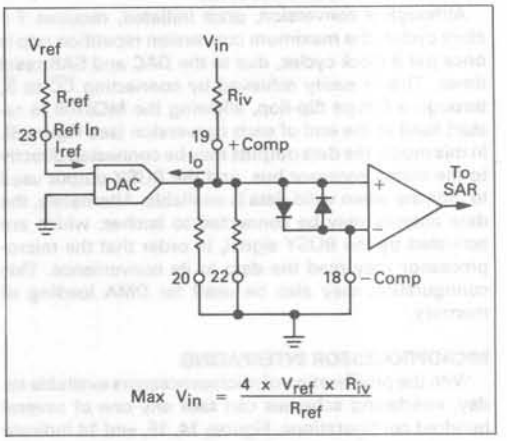


OTHER INPUT RANGES

The MC6108 has internal resistors providing preset input ranges of 0 to +10 volts, 0 to +5.0 volts, and −5.0 to +5.0 volts (see previous section entitled "Signal Voltage"). The input range, and the offset, are determined by the value of the resistors at Pins 20, 22, and 24. Where input ranges other than those listed above are to be digitized, then external resistors of comparable tolerance and temperature coefficient should be used for the reference (at Pin 23), ***and*** for the input signal (at Pin 19), ***and*** for the bipolar offset function (also at Pin 19). See Figures 12 and 13. R_{in} and R_{off} should be connected to A. Gnd when not used. Due to the tolerances of the absolute value of the internal resistors, they should not be used in conjunction with external resistors.

Figure 13 shows the reference current and the offset current supplied from the same reference source, which may be the internal reference (Pin 25). However, separate sources may be used for the two currents if desired.

FIGURE 12 — UNIPOLAR CONVERSION USING EXTERNAL REFERENCE AND RESISTORS



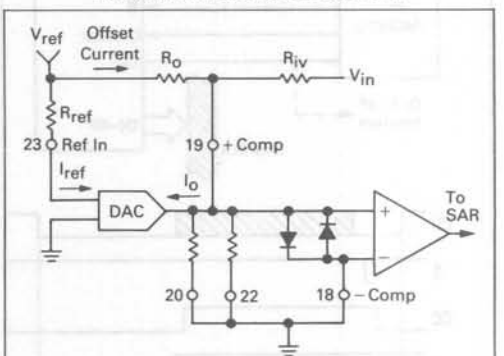
$$\text{Max } V_{in} = \frac{4 \times V_{ref} \times R_{iv}}{R_{ref}}$$

A modulation of the input signal (for waveform manipulation or signal processing) may be done by applying the modulating signal to the reference current. Rewriting equation 1 to determine the output code results in:

$$A = \frac{I_o \times 256}{4 \times I_{ref}} = \frac{V_{in} \times 256}{R_{in} \times 4 \times I_{ref}} \qquad (5)$$

(The offset term has been omitted to simplify the equation.) As can be seen, the output code varies inversely with the reference. When varying the reference current, its value must be maintained between 0.5 and 2.0 mA, and the current flow ***must*** always be ***into*** Pin 23 or 24.

FIGURE 13 — BIPOLAR CONVERSION USING EXTERNAL REFERENCE & RESISTORS



$$\text{Max } V_{in} = V_{ref} \times R_{iv} \left[\frac{4}{R_{ref}} - \frac{1}{R_o}\right]$$

$$\text{Min } V_{in} = -\frac{V_{ref} \times R_{iv}}{R_o}$$

MAXIMUM CONVERSION RATE

Although a conversion, once initiated, requires 7+ clock cycles, the maximum conversion repetition rate is once per 9 clock cycles, due to the DAC and SAR reset times. This is easily achieved by connecting $\overline{CC}$ to $\overline{S}$, through a D-type flip-flop, allowing the MC6108 to restart itself at the end of each conversion (see Figure 8). In this mode, the data outputs may be connected directly to the microprocessor bus, and the BUSY output used to indicate when valid data is available. Alternately, the data outputs may be connected to latches, which are activated by the BUSY signal, in order that the microprocessor may read the data at its convenience. This configuration may also be used for DMA loading of memory.

MICROPROCESSOR INTERFACING

With the proliferation of microprocessors available today, interfacing schemes can take any one of several hundred configurations. Figures 14, 15, and 16 indicate some generic interfacing schemes which can be adapted to most any microprocessor. Some of the terminology in the Figures is based on the MC6800 series of processors — other processors have similar functions by different names.

Figure 14 depicts a simple basic interface using a port (such as an MC6821) and/or an interrupt. A conversion is initiated when the active low address decoder switches low, R/$\overline{W}$ is high, and the port outputs one active low pulse to $\overline{S}$. At the end of the conversion, $\overline{CC}$ goes low, alerting the processor through the port or through an interrupt. The processor can then read the data at its convenience by switching $\overline{R}$ and $\overline{CS}$ low.

Figure 15 eliminates the need for an interrupt, and instead periodically checks the conversion status at D7 (D/$\overline{ST}$ = low) by reading the data bus. When D7 is low, the conversion is complete, and the D/$\overline{ST}$ input is then taken high so as to read the data at D0–D7.

Figure 16 eliminates the need for an interrupt or a port, but requires the processor to wait during the conversion until it is complete. The conversion is initiated when the address decoder switches low, and R/$\overline{W}$ goes high — that brings $\overline{CS}$ low ***and*** provides the $\overline{Start}$ pulse. The processor waits 9 clock cycles, and then reads the data.

In the above examples, the timing of the $\overline{S}$ pulse must be such that it is low for >50 ns concurrently with $\overline{CS}$ and CLK low, and must include one rising clock edge. If the $\overline{S}$ pulse timing is synchronized with the other inputs, this is relatively easy to guarantee. If, however, in Figure 16, the $\overline{CS}$ and CLK are not synchronized, then the SN74LS122 must be set for a pulse width that is equal to or greater than one clock cycle.

2

FIGURE 14 — BASIC MICROPROCESSOR INTERFACE

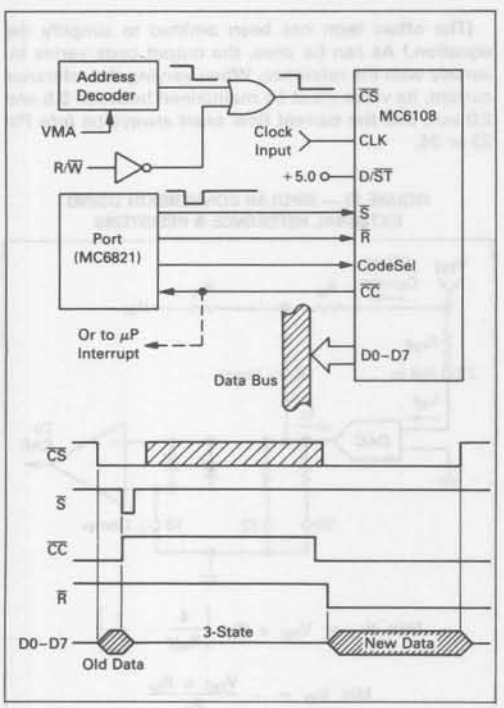


FIGURE 15 — MICROPROCESSOR INTERFACE WITHOUT AN INTERRUPT

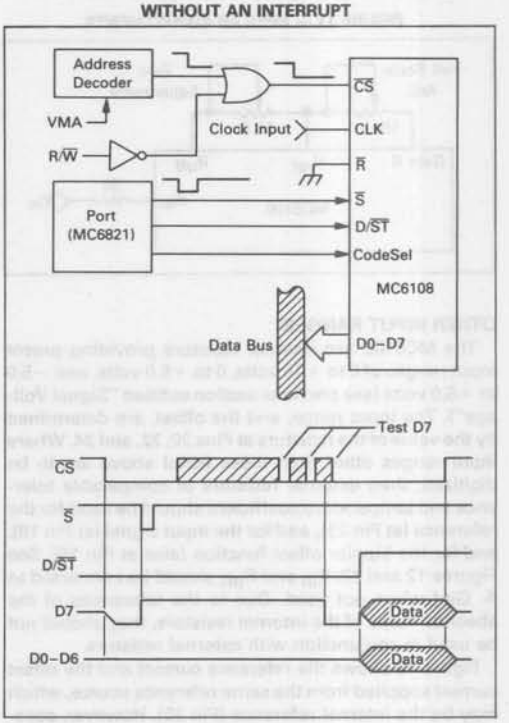
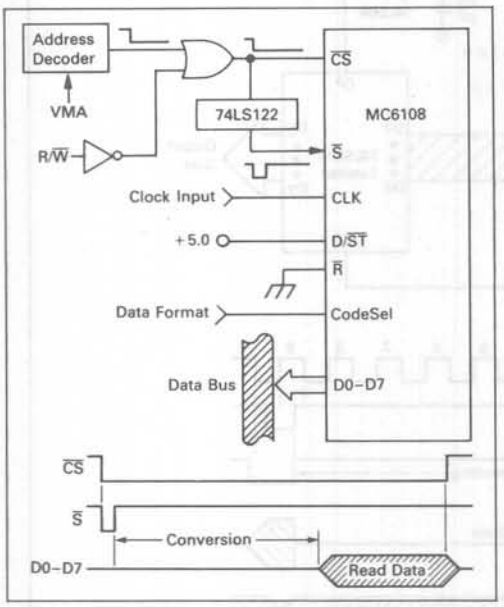


FIGURE 16 — MICROPROCESSOR INTERFACE WITHOUT USING A PORT OR INTERRUPT



STAND-ALONE USE

Although the MC6108 was designed for use with microprocessors, it can be used in a stand-alone mode. The digital inputs may be controlled by other digital circuitry, or hard-wired in a simple application. Figure 17 shows a simple configuration whereby the MC6108 is permanently enabled, and each $\overline{S}$ input pulse provides new data at the outputs. Figure 18 shows a circuit whereby the MC6108 is continually self-updating the information into latches. The latches are necessary since in this mode of operation, the MC6108 data outputs are in the 3-state mode the majority of the time. The 430 Ω resistor and 68 pF capacitor provide a ≈60 ns delay from $\overline{CC}$'s falling edge to allow D0–D7 to stabilize, and to allow the setup time required by the SN74LS374 latches. The clock high time in this circuit must be ≥100 ns.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −5.2 volts, nor a higher negative voltage from which to derive the −5.2 volts — the circuit of Figure 19 can be used to generate the −5.2 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC6108. The MC34063 is a switching regulator, and in Figure 19 is configured in an inverting mode of operation. The regulator operating specifications are given in the Figure.

2

FIGURE 17 — STAND-ALONE OPERATION (CONTINUOUSLY ENABLED)

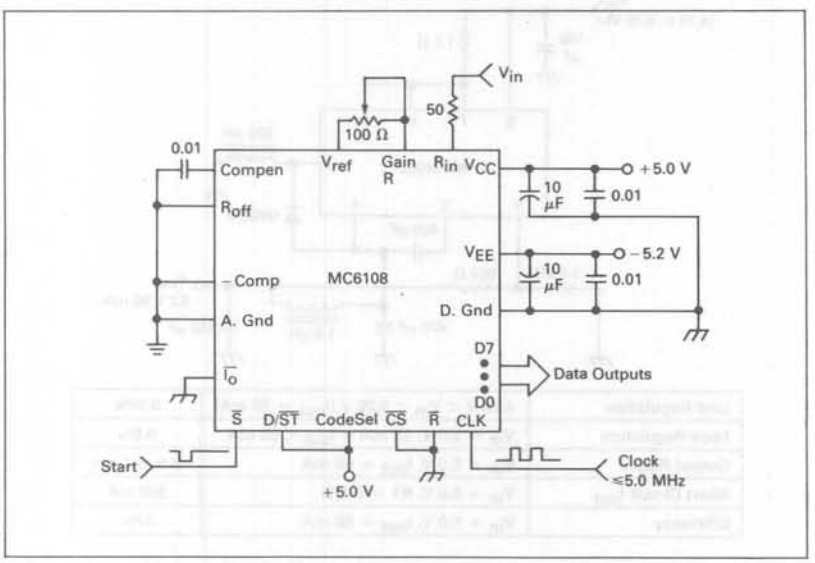


FIGURE 18 — STAND-ALONE OPERATION AT MAXIMUM UPDATE RATE

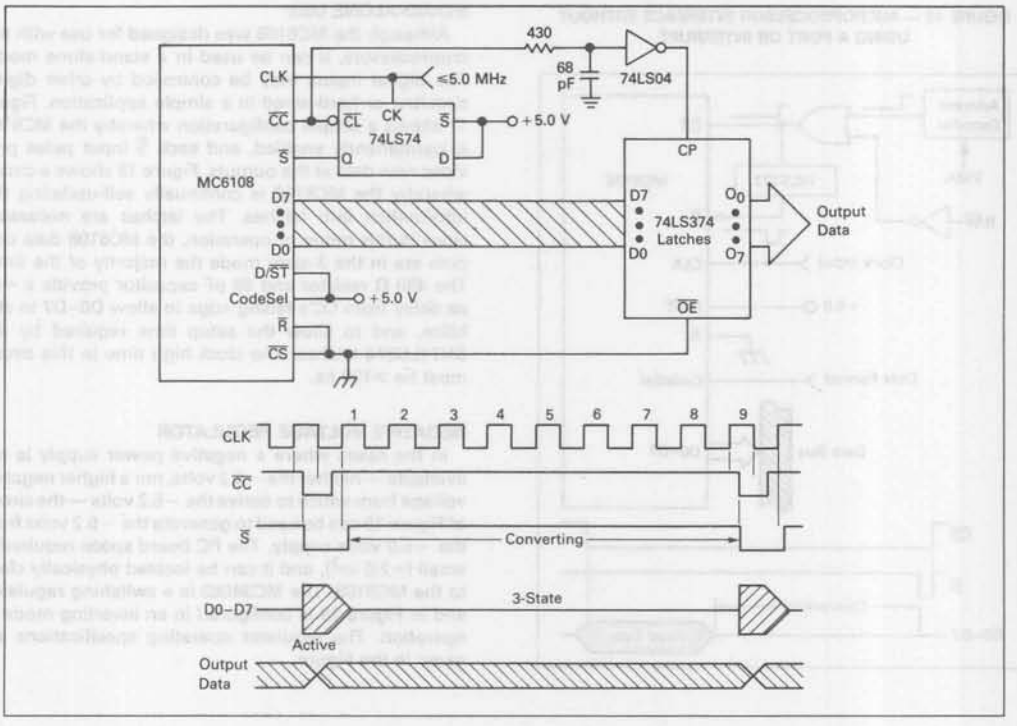
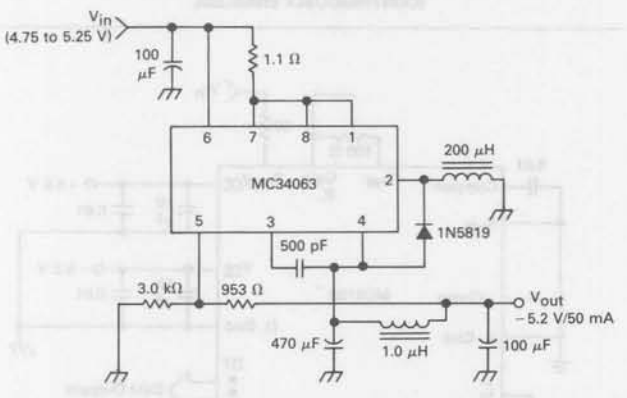


FIGURE 19 — −5.2 VOLTAGE REGULATOR



Line Regulation	$4.75\ V < V_{in} < 5.25\ V$ (I_{out} = 20 mA)	0.04%
Load Regulation	V_{in} = 5.0 V, 20 mA < I_{out} < 50 mA	0.8%
Output Ripple	V_{in} = 5.0 V, I_{out} = 50 mA	3.0 mV p-p
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	300 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	57%

2

GLOSSARY

BANDGAP REFERENCE — A voltage reference circuit based on the predictable base-emitter voltage of a transistor. The silicon bandgap voltage of ≈1.2 volts is the basis for generating other voltages which are stable with time and temperature.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −5 to +5 V, −2 to +8 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the $7F_H$ to 80_H transition. The ideal location is 1/2 LSB below zero volts in the case of an A-D set up for a symmetrical bipolar input (e.g., −5 to +5 V).

DAC CURRENT GAIN — The internal gain the DAC applies to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

DIFFERENTIAL NON-LINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n.(n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE CURRENT or RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), or output (of a DAC), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point) of a data converter, with respect to the device's internal reference. The gain error is usually expressed in LSBs.

INTEGRAL NON-LINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code whose normalized decimal value is defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A-D, and all ones corresponds to the most positive input voltage.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A-D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

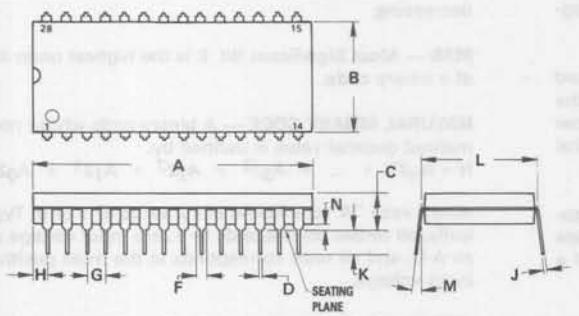
SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

TWO'S COMPLEMENT CODE — A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeroes, plus a carry. It is the same as Offset Binary Code, with the MSB inverted.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +10 V, 0 to −5 V, +2 to +8 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

OUTLINE DIMENSIONS



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

2

MOTOROLA

MC10318

Specifications and Applications Information

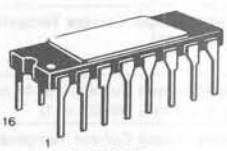
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

The MC10318 is a high-speed D/A converter capable of data conversion rates in excess of 25 MHz. The digital inputs are compatible with MECL 10,000 Series Logic. Complementary current outputs provide up to 56 mA full scale capability. The MC10318 meets the requirements of many applications, including: high-speed instrumentation and test equipment, storage oscilliscopes, display processing, radar systems, and digital video systems (broadcast and receiver applications).

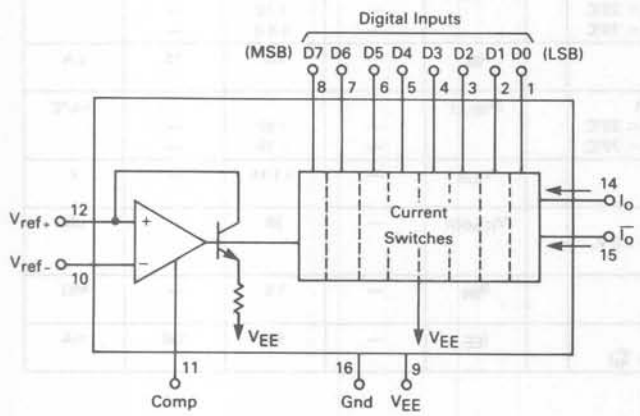
- FAST Settling Time — 10 ns (Typ to ±0.19%)
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: −1.3 V to +2.5 V
- Single MECL Supply: −5.2 V
- Standard 16-Pin Dual-in-Line Package



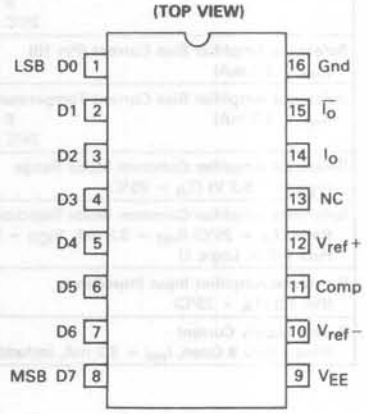
L SUFFIX
CERAMIC PACKAGE
CASE 690

2

BLOCK DIAGRAM



PIN CONNECTIONS
(TOP VIEW)



DS9580
(Replaces AD1-510 R1)

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{EE}	−6.0 to +0.5	Vdc
Digital Input Voltage		V_I	0 to V_{EE}	Vdc
Applied Output Voltage		V_O	+5.0 to V_{EE}	Vdc
Reference Current		$I_{ref}(12)$	5.0	mA
Output Current		I_{FS}	−75	mA
Reference Amplifier Input Range		V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs		$V_{ref}(D)$	±5.0	Vdc
Operating Temperature Range		T_A	0 to +70	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Junction Temperature	Ceramic Package	T_J	+175	°C
Thermal Resistance, Junction to Ambient	Still Air With 500 LFPM	$R\theta_{JA}$	80 50	°C/W

DC CHARACTERISTICS (V_{EE} = −5.2 V, ±5% T_A = 0°C to +70°C after thermal equilibrium is reached.)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Nonlinearity (Integral) (Pin 14 or 15) MC10318L (@ I_{FS} = 51 mA, 25.5 mA)		—	—	—	±0.19	%FS
Zero Scale Output Current (Pin 14 or 15) (T_A = 25°C)	10	I_{ZS}	—	5.0	50	μA
Zero Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$I_{ZS}/\Delta T$	— —	±17 ±2.0	— —	nA/°C
Full Scale Output Current (Pin 14 or 15) (I_{ref} = 3.2 mA, D0–D7 = 1)	10	I_{FS}	−46.00	−51.00	−56.00	mA
Full Scale Output Current Temperature Drift (Pin 14 or 15) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{FS}/°C$	— —	±50 ±10	— —	ppm/°C
Full Scale Output Sensitivity to Power Supply Variations (Pin 14 or 15) MC10318L (−4.94 V < V_{EE} < −5.46 V)		I_{FSPSS}	—	±0.005	±0.02	%/%
Full Scale Symmetry (I_{FS} — $\overline{I_{FS}}$)	10	I_{FSS}	—	±21	±100	μA
Output Voltage Compliance (Pin 14 or 15) Full Scale Current Change ≤ ½ LSB (Specified Nonlinearity) (T_A = 25°C)		V_{OC}	−1.3	—	+2.5	V
Output Resistance (Pin 14 or 15) (T_A = 25°C)	12	R_O	—	69	—	kΩ
Reference Amplifier Offset Voltage (T_A = 25°C)		V_{IO}	—	±3.2	—	mV
Reference Amplifier Offset Voltage Temperature Drift 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta V_{IO}/\Delta T$	— —	±10 ±4.0	— —	μV/°C
Reference Amplifier Bias Current (Pin 10) (I_{ref} = 3.2 mA)		I_{IB}	—	4.0	15	μA
Reference Amplifier Bias Current Temperature Drift (I_{ref} = 3.2 mA) 0 < T_A < 25°C 25°C < T_A < 70°C		$\Delta I_{IB}/\Delta T$	— —	−40 −10	— —	nA/°C
Reference Amplifier Common Mode Range (V_{EE} = −5.2 V) (T_A = 25°C)		V_{ICR}	—	±1.15	—	V
Reference Amplifier Common Mode Rejection Ratio (T_A = 25°C) (I_{ref} = 3.2 mA, V_{ICR} = 0 to −2.0 V, Pins 1–8 = Logic 1)		V_{ICMRR}	—	58	—	dB
Reference Amplifier Input Impedance (Pin 10) (T_A = 25°C)		R_{IN}	—	1.0	—	MΩ
Power Supply Current (Pins 1 thru 8 Open, I_{ref} = 3.2 mA, Includes I_O + $\overline{I_O}$)		I_{EE}	—	90	130	mA

AC CHARACTERISTICS (T_A = 25°C, V_{EE} = −5.2 V, ±5%)

Characteristics	Fig.	Symbol	Min	Typ	Max	Unit
Feedthrough Current — All Bits Off	9	I_{FC}				μA p-p
f = 10 kHz			—	2.0	—	
f = 100 kHz			—	18	—	
Distortion — (@ I_O) (Sinewave applied to reference amplifier Input, D0–D7 = Logic 1)						%
C = 0.01 μF, f = 20 kHz		THD	—	1.0	—	
C = 0.01 μF, f = 65 kHz		THD	—	5.0	—	
C = 0.001 μF, f = 340 kHz		THD	—	1.0	—	
C = 0.001 μF, f = 600 kHz		THD	—	2.0	—	
C = 240 pF, f = 600 kHz		THD	—	0.8	—	
Reference Amplifier Slew Rate (Step change at Pin 10, all bits on)	13					mA/μs
C = 0.01 μF			—	0.5	—	
C = 0.001 μF			—	5.0	—	
C = 240 pF			—	20	—	
Settling Time (to ±0.19% of Full Scale)	1,22	t_s				ns
1 LSB Change			—	7.0	—	
All Bits Switched			—	10	—	
Propagation Delay	2	t_p	—	5.0	—	ns
Output Glitch Energy (with De-Skewing Capacitors) (Input Change: 01111111 ⟷ 10000000)			—	50	—	LSB·ns
Glitch Duration			—	5.0	—	ns

DIGITAL INPUT VOLTAGE LEVELS				
Volts (See Note)				
T_A	V_{IH}max	V_{IHA}min	V_{ILA}max	V_{IL}min
0°C	−0.845	−1.151	−1.516	−1.868
25°C	−0.810	−1.105	−1.505	−1.850
70°C	−0.727	−1 052	−1.480	−1.830

FUNCTIONAL PIN DESCRIPTION

D0–D7 (Pins 1-8) The eight ECL digital inputs compatible with MECL 10,000 series devices. Logic "0" is nominally −1.8 V, and Logic "1" is nominally −0.9 V.

V_{ref-} (Pin 10) The high impendance input of the reference amplifier. This input is normally grounded, but may be used for ac applications involving modulation, digitally controlled gain, etc. Normal operating range is from ground to V_{EE} + 2.9 V (nominally −2.3 V).

V_{ref+} (Pin 12) The noninverting input of the reference amplifier. The inverted output of the reference amplifier is internally fed back to this input, thus causing it to track Pin 10. A nominal 3.2 mA is to be supplied to this pin from an external (stable and noise free) voltage source and current setting resistor.

Comp. (Pin 11) A nominal 0.01 μF capacitor is connected to this pin and to ground to stabilize the reference amplifier. Lower values of capacitor may be used if a good PC board layout is used, where frequencies higher than 10 kHz are applied to the reference amplifier.

I_o, $\overline{I_o}$ (Pins 14,15) The complementary current outputs. Current flow is into the DAC and varies linearily with I_{ref} and the digital input code. I_{out} increases as the digital input increases. Output compliance range is −1.3 V to +2.5 V.

V_{EE} (Pin 9) The power supply pin. V_{EE} is nominal −5.2 V, ±5%.

Gnd (Pin 16) The ground pin. This line should be as noise-free as possible in order to obtain a noise-free output.

NOTE: V_{EE} = −5.2 V, ±5% Inputs are MECL 10,000 compatible within the temperature and power supply ranges listed. See MECL System Design Handbook for further details. See Fig. 19 in this data sheet.

FIGURE 1 — SETTLING TIME

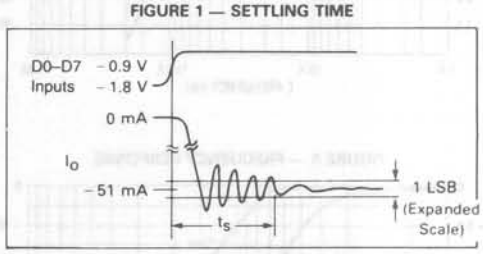
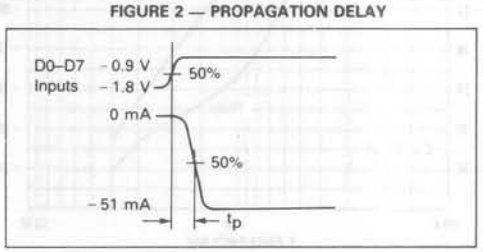


FIGURE 2 — PROPAGATION DELAY



REFERENCE AMPLIFIER RESPONSE

Inverting Input (V_{ref-})
Test Circuit of Fig. 14

Noninverting Input (V_{ref+})
Test Circuit of Fig. 11

FIGURE 3 — FREQUENCY RESPONSE

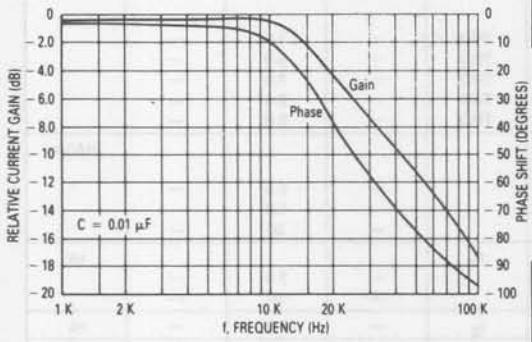


FIGURE 4 — FREQUENCY RESPONSE

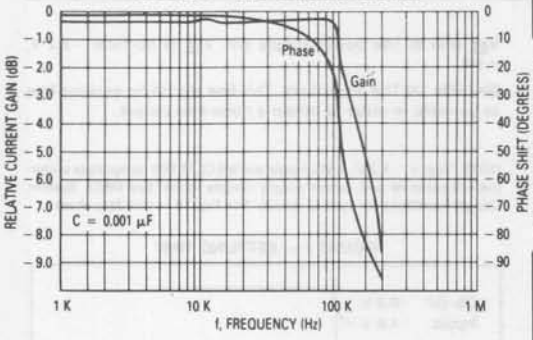


FIGURE 5 — FREQUENCY RESPONSE

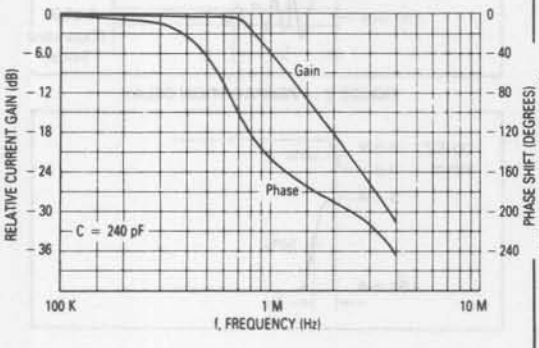


FIGURE 6 — FREQUENCY RESPONSE

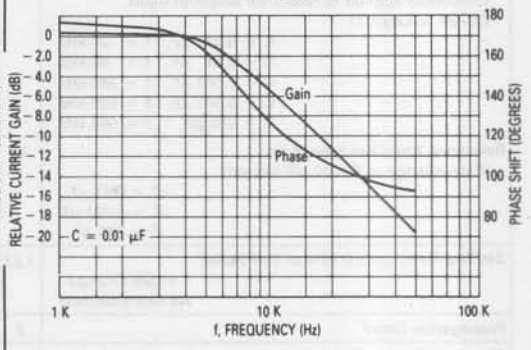


FIGURE 7 — FREQUENCY RESPONSE

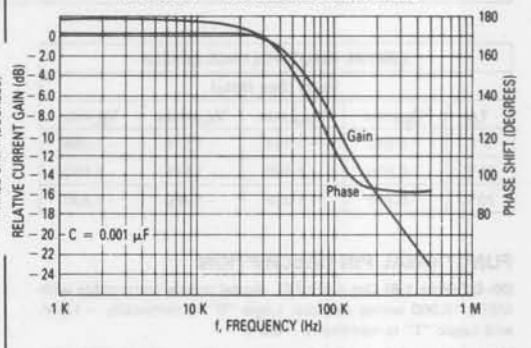
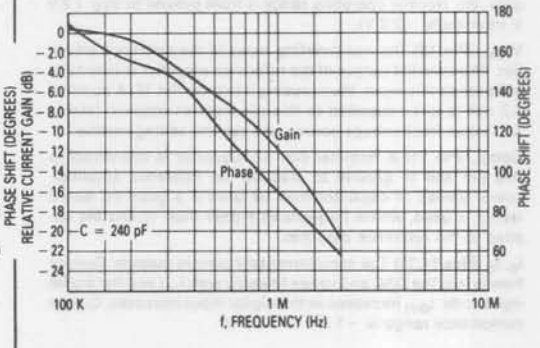


FIGURE 8 — FREQUENCY RESPONSE



2

TEST CIRCUITS

FIGURE 9 — FEEDTHROUGH MEASUREMENT

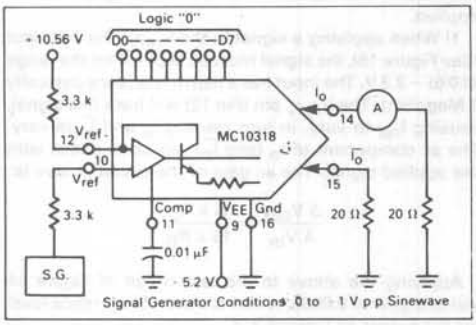


FIGURE 10 — ZERO/FULL SCALE CURRENT

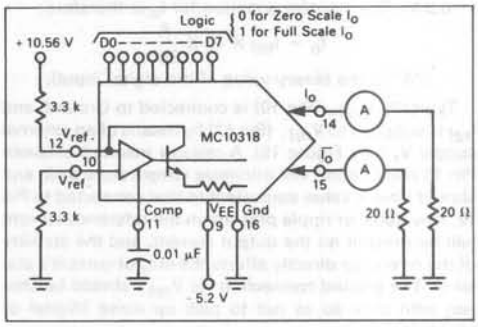
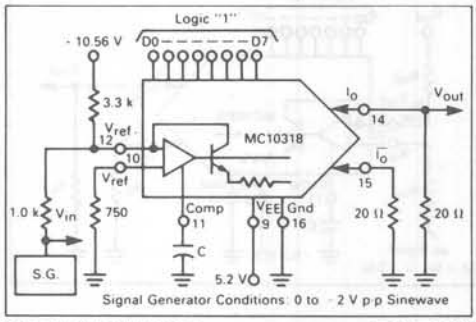


FIGURE 11 — GAIN/PHASE MEASUREMENT



Reference dB Level: See Text

See Figures 6-8

FIGURE 12 — OUTPUT RESISTANCE

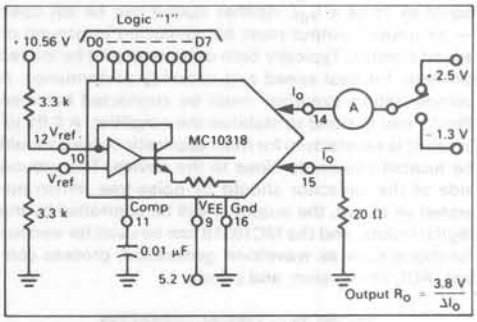


FIGURE 13 — REFERENCE AMPLIFIER SLEW RATE

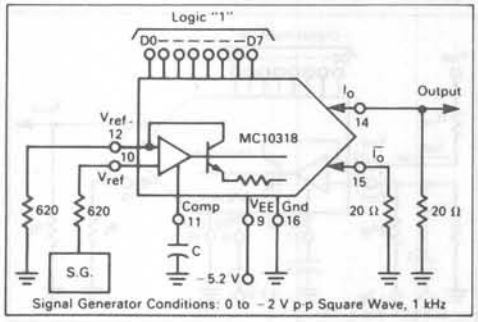
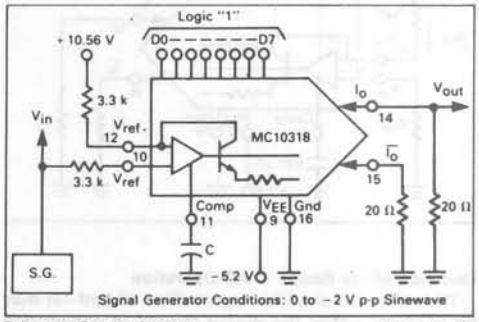


FIGURE 14 — GAIN/PHASE MEASUREMENT



Reference dB Level: See Text.

See Figures 3-5

2

OPERATIONAL INFORMATION

Typical DAC Operation

The MC10318 is designed to be operated with an I_{ref} (Pin 12) of 3.2 mA, resulting in a full scale output current (I_O) of 51 mA when D0 through D7 are at a Logical "1" (−0.9 V). The transfer equation for I_O is therefore:

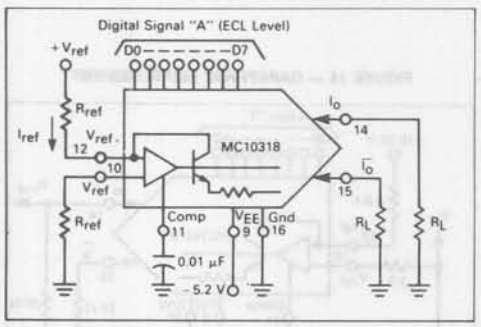
$$I_O = I_{ref} \times 16 \times \frac{A}{256}$$

("A" is the binary value of the digital input).

Typically V_{ref-} (Pin 10) is connected to Ground, and I_{ref} is supplied to V_{ref+} (Pin 12) by means of an external supply V_r (see Figure 15). A resistor inserted between Pin 10 and Ground will minimize temperature drift, and should have a value equivalent to that connected to Pin 12. Any noise or ripple present on the reference current will be present on the output current, and the stability of the reference directly affects the output current's stability. The ground connection for V_{ref-} should be chosen with care so as not to pick up noise (digital or otherwise).

The complementary outputs (I_O and $\overline{I_O}$) are high impedance current sources having a compliance range of 3.8 V (−1.3 to +2.5 V). I_O increases with increasing digital input, while $\overline{I_O}$ decreases. Their sum is a constant equal to 15.94 x I_{ref}. Neither output can be left open — an unused output must be connected to ground or a load resistor. Typically both outputs should be loaded similarly for best speed and accuracy performance. A compensation capacitor must be connected between Pin 11 and Ground to stabilize the amplifier. A 0.01 μF ceramic is satisfactory for most applications, and should be located physically close to the device. The ground side of the capacitor should be noise-free. When operated as above, the output(s) will be controlled by the digital inputs, and the MC10318 can be used for various functions such as waveform generation, process control, ADC conversion, and others.

FIGURE 15 — TYPICAL OPERATION



Common Mode Range — AC Operation

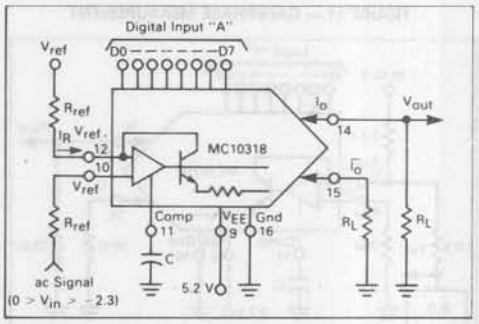
The reference amplifier inputs (Pins 10 and 12) may be used to control the output current in conjunction with the digital inputs for applications such as digitally controlled gain of an ac signal, digitally controlled amplitude modulation, and others. Either the positive or negative input of the reference amplifier may be used, depending on the application. There are, however, differences in the manner in which an ac signal is to be applied.

1) When applying a signal to the V_{ref-} (Pin 10) input (See Figure 16), the signal must be kept within the range of 0 to −2.3 V. The input has a high impedance (typically 1 Megohm). The V_{ref+} pin (Pin 12) will track this signal, causing I_{ref} to vary, in turn causing I_O and $\overline{I_O}$ to vary. The ac component of I_O (and $\overline{I_O}$) will be in phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{A \times R_L}{16 \times R_R}$$

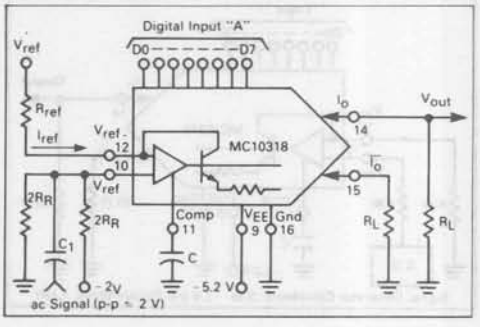
Applying the above to the test circuit of Figure 14 yields a gain of 0.0966, which is the 0 dB reference level for the curves of Figures 3–5.

FIGURE 16 — AC OPERATION, NONINVERTING



If the peak values of the applied ac signal cannot be kept within the above mentioned voltage range, an alternate circuit is shown in Figure 17.

FIGURE 17 — AC OPERATION, NONINVERTING (ALTERNATE)



The compensation capacitor (Pin 11) of Figures 16 and 17 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 10 kHz are to be applied to the reference input, a smaller value capacitor will be necessary as indicated by Figures 3–5. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

2) When applying a signal to the V_{ref_+} (Pin 12) input (see Figure 18), the effect is a direct modulation of the reference current supplied by V_{ref}. Pin 12 is a virtual ground, and therefore the current I_{ref} is equal to:

$$I_{ref} = \frac{V_{ref}}{R_{ref}} + \frac{V_i}{R_i}$$

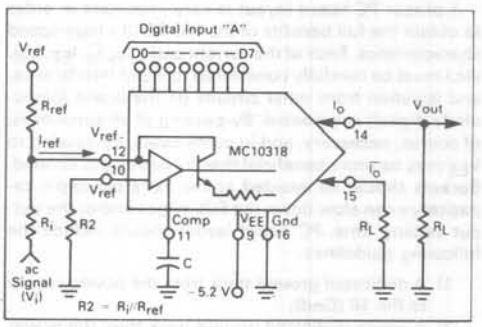
I_O and $\overline{I_O}$ will vary with the reference current, but the ac component will be 180° out of phase with the applied signal. The ac gain of the circuit shown is:

$$\frac{\Delta V_{out}}{\Delta V_i} = \frac{-A \times R_L}{16 \times R_i}$$

Applying the above to the test circuit of Figure 11 yields a gain of −0.3188, which is the 0 dB reference level for the curves of Figures 6–8.

The reference current I_{ref} must always flow **into** Pin 12, requiring that the values of V_{ref}, R_{ref}, R_i, and V_i be chosen so as to guarantee this.

FIGURE 18 — AC OPERATION, INVERTING

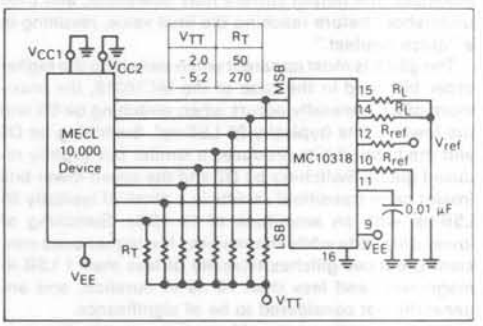


The compensation capacitor (Pin 11) of Figure 18 is to be nominally 0.01 μF for best overall stability. If frequencies higher than 4 kHz are to be applied, a smaller value capacitor will be necessary as indicated by Figures 6–8. However, greater care will be necessary in the breadboarding and PC layout to prevent instabilities caused by unintended feedback paths.

DIGITAL INTERFACE

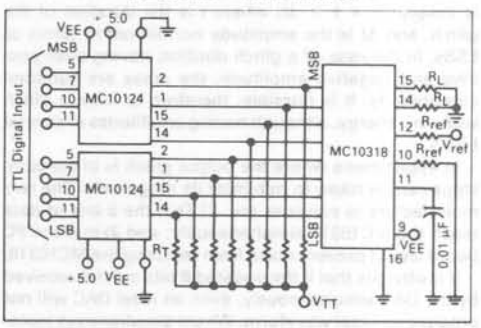
The digital inputs (Pins 1–8) are compatible with MECL 10,000 series devices over the temperature and V_{EE} range listed on page 3. Standard MECL 10,000 design guidelines apply, and should be implemented. Maximum speed response requires careful PC board layout and choice of components. See Motorola's MECL System Design Handbook for a complete explanation of specifications and characteristics. Figure 19 shows a typical ECL interconnection with recommended values for optimum speed performance. Other values of R_T and V_{TT} may be used, but at a slight increase in overall propagation delay. Unused inputs should not be left open, but should be connected to a Logic 0 (−1.8 V), or a Logic 1 (−0.9 V). Resistors R_T should be connected at the receiving end of the interconnection, i.e. physically located adjacent to the MC10318 inputs, for best speed performance.

FIGURE 19 — STANDARD MECL INTERFACE



Interfacing a TTL system to the MC10318 is easily accomplished by the use of two MC10124 devices (Figure 20).

FIGURE 20 — TTL INTERFACE



OUTPUT CHARACTERISTICS

The MC10318 DAC has been designed specifically for high-speed operation by incorporating ECL structured inputs, bit switching circuits which are small in size and

simple in operation, and high-current complementary outputs (which permits current steering rather than on-off switching). In this manner, very short propagation delays and settling times are possible.

Output Glitch

All DAC's will produce a glitch at the output when various bits are switched in opposite directions, due to differences in transition times of the switching transistors. During the switching period, typically the output current will momentarily seek a value other than the desired final value, and then return to and settle at the final value. This glitch can be several LSBs in magnitude, but of a very short duration (5–6 ns). In some instances, the output current may overshoot, and then undershoot before reaching the final value, resulting in a "glitch doublet."

The glitch is most apparent when switching the higher order bits, and in the case of the MC10318, the maximum glitch generally occurs when switching bit D5 and the lower 5 bits (typically 85 LSB·ns). Switching bit D6 and the lower 6 bits produces a similar but slightly reduced glitch. Switching bit D7 and the seven lower bits (major carry transition) results in a glitch of typically 50 LSB·ns, with an amplitude of 17 LSBs. Switching of lower order bits while maintaining the higher ones constant produces glitches typically of less than 1 LSB in magnitude, and less than 10 ns in duration, and are generally not considered to be of significance.

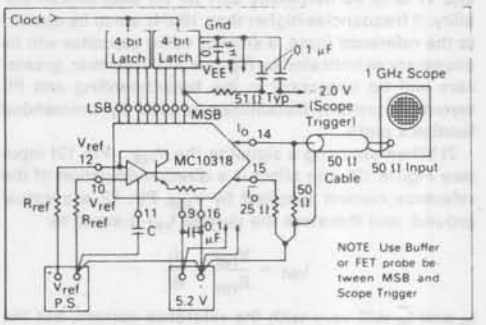
Glitches can be removed from the output by filtering, or by using a sample-and-hold circuit on the output, or by using de-skewing capacitors on the higher order bits. See Fig. 31.

Output glitch is generally specified in terms of glitch energy, which is the area under the curve of the waveform. Most glitches appear as a triangle, and so the area is simply $\frac{1}{2} \times t \times \Delta I$, where t is the duration of the glitch, and ΔI is the amplitude normalized in terms of LSBs. In the case of a glitch doublet, having both positive and negative amplitude, the areas are summed algebraically. It is possible, therefore to have a glitch with zero energy, although having amplitudes of several LSB's.

In applications where the output glitch is of concern, steps can be taken to minimize its magnitude. The two main factors to consider are: 1) That the 8 bits of data reach the MC10318 simultaneously; and 2) that the PC board layout prevent noise from reaching the MC10318.

It is obvious that if the updated 8 bits are not received by the DAC simultaneously, even an ideal DAC will not produce an ideal waveform. Where simultaneous transmission by the sending device(s) cannot be guaranteed (such as two cascaded counters), latches should be used ahead of the MC10318. The latches should then be clocked after their inputs have settled. Suggested latches are the MC10133/MC10153/MC10168 at the ECL level, and the SN74LS273 at the TTL level.

FIGURE 21 — PRECISION HIGH-SPEED MEASUREMENTS



Nonlinearity

Integral nonlinearity has been specified, rather than differential nonlinearity, as this is a better indicator of the maximum error to be expected. Integral nonlinearity is measured by comparing the **actual** output (at each digital value) with the expected ideal value. The expected values lie along a straight line between zero and the full scale output current. The MC10318 will not differ from the **ideal** value by more than the specified nonlinearity.

PC Board Layout

A proper PC board layout is very important in order to obtain the full benefits of the MC10318's high-speed characteristics. Each of the current paths (I_O, $\overline{I_O}$, I_{EE}, I_{ref}, etc.) must be carefully considered to avoid interference, and isolation from other circuits on the board (particularly digital) is essential. By-passing of all supplies is, of course, necessary, and in some cases, by-passing to V_{EE} may be more beneficial than by-passing to Ground. Sockets should be avoided as the extra pin-to-pin capacitance can slow down the ECL edges and/or the output settling time. PC board layout should include the following guidelines:

1) A dedicated ground track from the power supply to Pin 16 (Gnd);
2) A single dedicated ground track from the power supply to the **two** load resistors associated with I_O and $\overline{I_O}$ — this results in a constant dc current in this track;
3) A separate ground for the circuitry associated with V_{ref+}, V_{ref-}, and Comp (Pins 10–12). Any noise on this ground will feed through the reference amplifier and show up on the output;
4) The compensation capacitor must be physically adjacent to Pin 11;
5) Bypass V_{EE} (Pin 9) with a 0.1 μF to the ground line feeding the load resistors;
6) Provide proper terminations at the inputs — the suggested values for R_T and V_{TT} will provide best speed response;

7) Bypass V_{TT} to V_{EE} **and** to Ground with 0.1 μF capacitors;
8) If the power supplies are not on the same PC board with the MC10318, bypass V_{EE} and V_{TT} to Ground with (minimum) 10 μF and 0.1 μF where the supply voltages enter the PC board;
9) Use of a ground plane is mandatory in all high speed applications;
10) Keep all TTL circuitry tracks separate from the MC10318 by means of ground tracks and/or ground planes.

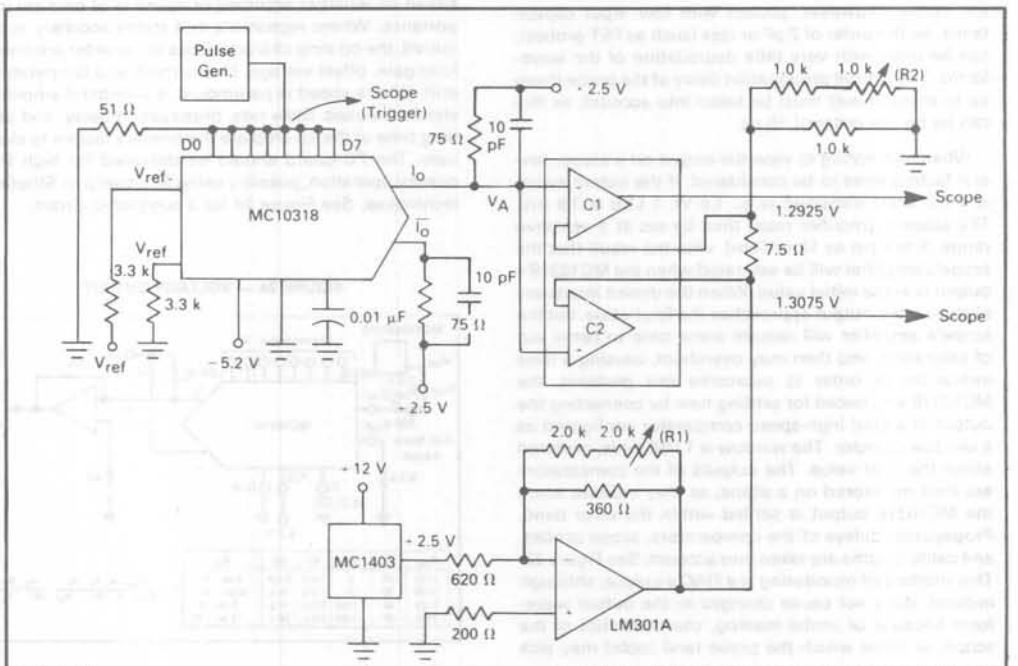
Many of the above points have to do with isolating the device from all other circuitry, since most applications involve using the MC10318 (which is 50% analog) in a (noisy) digital circuit. If the output voltage swing is typically 1 volt, then 1 LSB is approximately 4 mV. Since TTL circuitry can easily generate 50 mV noise on the ground line, the need for isolation is apparent.

The above points are not the only ones to be considered by the designer, as each application will have its own individual additional requirements.

Propagation Delay

The propagation delay is measured from the 50% point of the input transition to the 50% point of the output transition. Since the typical propagation delay is on the order of 5 ns, see Figure 21 and the information in Settling Time if this parameter is to be measured. Switching 1 LSB or all of the bits simultaneously produces no significant difference in propagation delay.

FIGURE 22 — SETTLING TIME MEASUREMENT



NOTES:
1) Pulse generator outputs − 0.9 V to − 1.8 V, t_r and t_f ≈ 2 ns.
2) Adjust v_{ref} for full scale output at V_A = − 1.3000 V.
3) Adjust R1 for − 1.3075 V at input of lower comparator.
4) Adjust R2 for − 1.2925 V at input of upper comparator.
5) R1, R2 are 20 turn trimpots.
6) Keep all wiring as short, tidy as possible — isolate all digital and analog supplies, grounds, signal lines, etc.
7) Heavily bypass all supplies at each device, and reference (−) inputs to the comparators.
8) Comparators are high-speed devices, such as AM687ADL.
9) Account for comparator offset when setting reference values.

Settling Time

The settling time is defined as the time from the 50% point of the input transition to the point at which the output enters into **and** stays within ± ½LSB (the error band) of the final value. Minimum settling time occurs when the output enters the error band at the maximum slew rate, and then settles out within the band. In actuality, however, the output's slew rate will lessen prior to entering the error band, and then may exit and enter the band once or twice as it settles to its final value. The settling time is determined by the last time the output enters the error band. See Figure 1.

When testing for settling time, the measurement technique used will have an effect on the result. Simply connecting scope probes to an input and output is generally not satisfactory due to the capacitive loading (typically 10–20 pF) of the probes. The rise (fall) time of an ECL input can be significantly increased by such a probe, with the result that the inputs of the MC10318 may be skewed from each other, which, in turn, affects the output. However, probes with low input capacitance, on the order of 2 pF or less (such as FET probes), can be used with very little degradation of the waveforms. The overall propagation delay of the probe (from tip to scope input) must be taken into account, as this can be on the order of 10 ns.

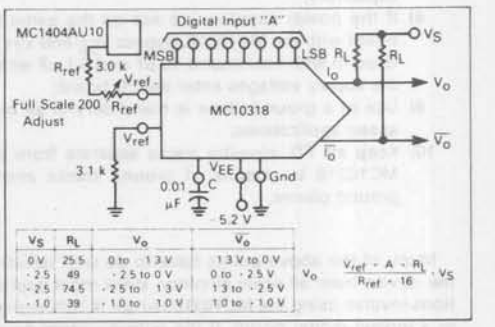
When attempting to view the output on a scope, several factors need to be considered. If the output swing is a full scale transition (e.g., 1.0 V), 1 LSB is 3.9 mV. The scope's amplifier must then be set at a sensitive range (5 mV/cm or 10 mV/cm), with the result that the scope's amplifier will be saturated when the MC10318's output is at the initial value. When the device inputs are switched, the output approaches the final value, but the scope's amplifier will require some time to come out of saturation, and then may overshoot, causing a false indication. In order to overcome this problem, the MC10318 was tested for settling time by connecting the output to a dual high-speed comparator configured as a window detector. The window is 1 LSB wide, centered about the final value. The outputs of the comparators are then monitored on a scope, as they indicate when the MC10318 output is settled within the error band. Propagation delays of the comparators, scope probes, and cable lengths are taken into account. See Figure 22. This method of monitoring the DAC's output, although indirect, does not cause changes to the output waveform because of probe loading, characteristics of the scope, or noise which the probe (and cable) may pick up.

APPLICATIONS

Voltage Output

There are two methods of converting the current output of the MC10318 to voltage outputs, depending on the voltage swing desired. For a limited range (<3.8 V p-p) the circuit of Figure 23 can be used.

FIGURE 23 — VOLTAGE OUTPUT

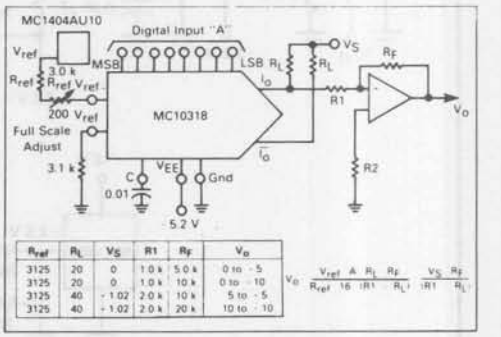


V_S	R_L	V_o	$\overline{V_o}$
0 V	25 5	0 to - 1 3 V	1 3 V to 0 V
- 2 5	49	- 2 5 to 0 V	0 to - 2 5 V
- 2 5	74 5	- 2 5 to - 1 3 V	1 3 to - 2 5 V
- 1 0	39	- 1 0 to - 1 0 V	1 0 to - 1 0 V

$V_o = \frac{V_{ref} - A - R_L}{R_{ref} - 16} \cdot V_S$

Where a larger voltage swing is required, an op amp is required at the output. The choice of op amp will be based on whether accuracy or speed is of primary importance. Where repeatable and stable accuracy is required, the op amp characteristics to consider are open-loop gain, offset voltage, bias current, and temperature drift. Where speed is paramount, a wideband amplifier should be used. Slew rate, propagation delay, and settling time of the op amp are the primary factors to evaluate. The PC board should be designed for high frequency operation, possibly using Microstrip or Stripline techniques. See Figure 24 for a suggested circuit.

FIGURE 24 — VOLTAGE OUTPUT



R_{ref}	R_L	V_S	R1	R_F	V_o
3125	20	0	1 0 k	5 0 k	0 to - 5
3125	20	0	1 0 k	10 k	0 to - 10
3125	40	- 1 02	2 0 k	10 k	5 to - 5
3125	40	- 1 02	2 0 k	20 k	10 to - 10

$V_o = \frac{V_{ref} \cdot A \cdot R_L}{R_{ref} \cdot 16} \cdot \frac{R_F}{R1} - \frac{V_S}{R1} \cdot \frac{R_F}{R_L}$

Connecting I_o and $\overline{I_o}$ as shown in the above figures places a constant dc load (51 mA) on the V_S supply, thus facilitating its design. The Gain Adjust resistor should be a 20 turn trimpot, as this will result in one turn equaling approximately 1 LSB of adjustment (for the recommended values in the figure). All of the resistors should have similar temperature coefficients for best temperature stability.

WAVEFORM GENERATION

FIGURE 25 — SAWTOOTH GENERATOR

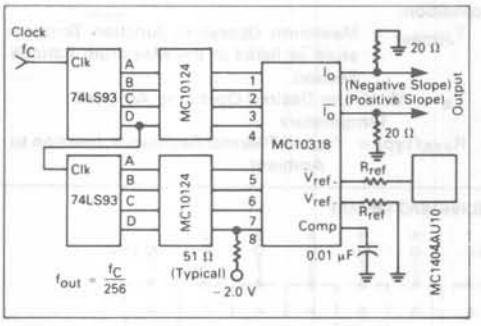


FIGURE 26 — TRIANGLE GENERATOR

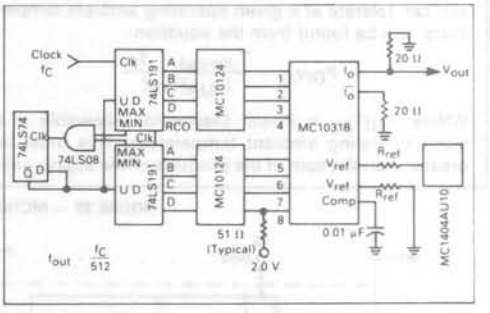


FIGURE 27 — SINEWAVE GENERATOR

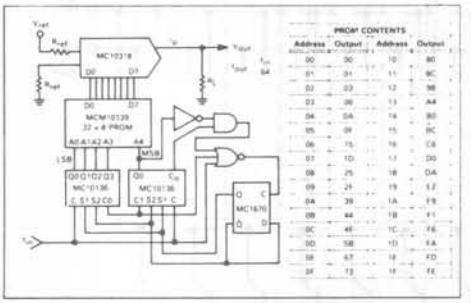


FIGURE 28 — OUTPUT CONNECTED TO 75 Ω LINE

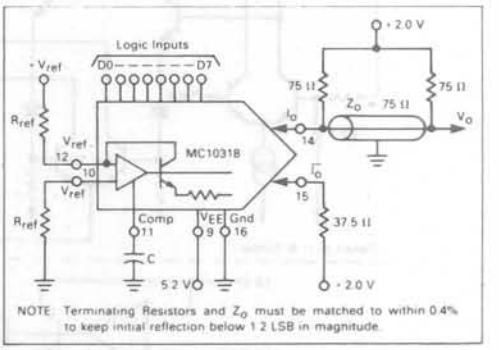


FIGURE 29 — OUTPUT CONNECTED TO 50 Ω LINE

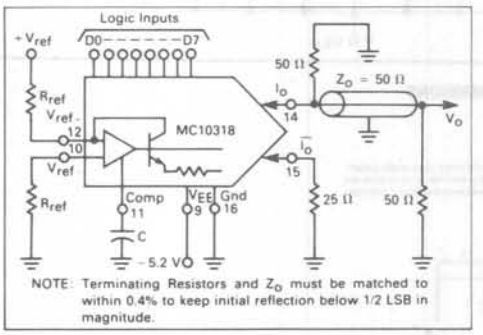
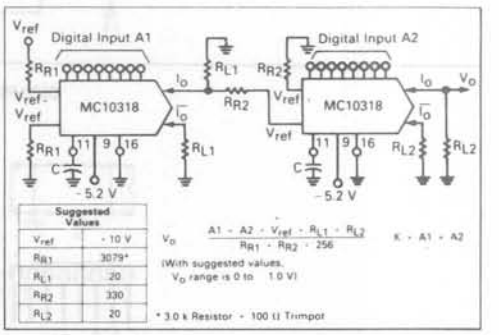


FIGURE 30 — DIGITAL MULTIPLICATION



NOTES:

1) When generating waveforms at low frequencies, filtering the output is recommended to smooth out the steps.

2) In many applications, bipolar voltage output may be obtained by monitoring the differential voltage at Pins 14 and 15 (with equal load resistors).

3) When connecting the outputs to transmission lines (See Figures 28 and 29), proper transmission line theory and techniques must be used for optimum performance.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

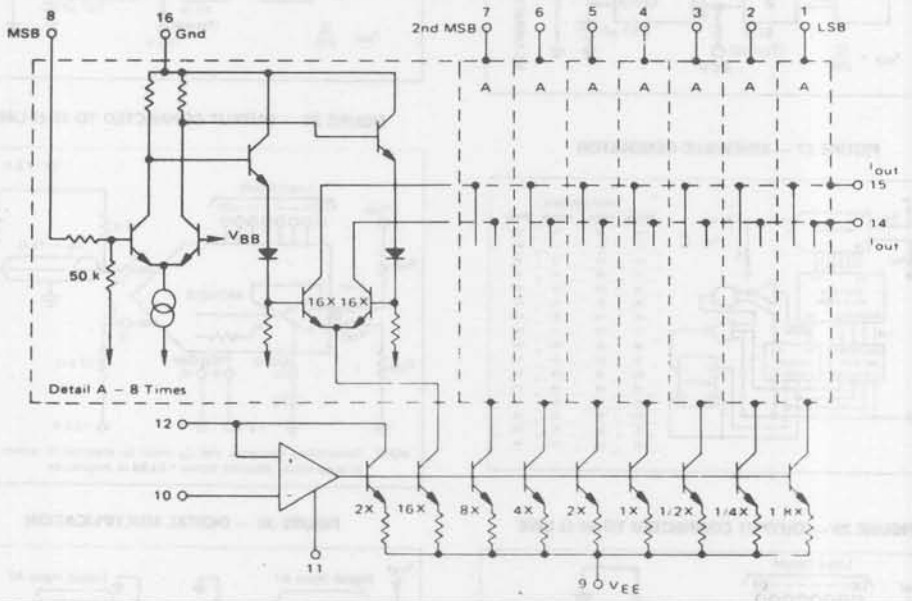
Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

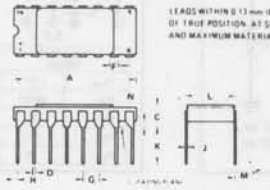
$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 35 — MC10318 EQUIVALENT CIRCUIT



2

OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.62	0.280	0.300
C	2.67	3.94	0.105	0.155
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M		10°		10°
N	0.38	1.40	0.015	0.055

CASE 690-13

MOTOROLA

MC10319

Specifications and Applications Information

HIGH SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTER

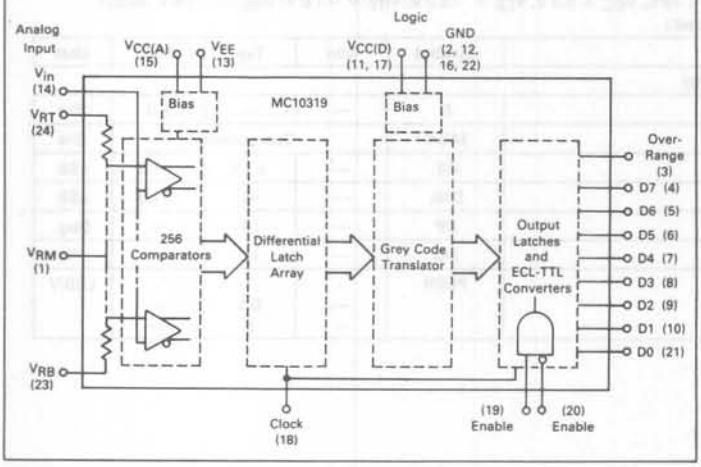
The MC10319 is an 8-bit high speed parallel flash A/D converter. The device employs an internal Grey code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 V supply and a wide tolerance negative supply of −3.0 to −6.0 V. Three-state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8-bit data byte plus an overrange bit. The data is latched and converted to 3-state LS-TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9-bit A/D converter.

Applications include Video Display and Radar processing, high speed instrumentation and TV Broadcast encoding.

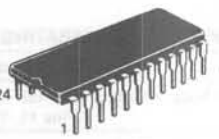
- Internal Grey Code for Speed and Accuracy, Binary Outputs
- 8-Bit Resolution/9-Bit Typical Accuracy
- Easily Interconnected for 9-Bit Conversion
- 3-State LS-TTL Outputs with True and Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0–2.0 V_{p-p} Between ±2.0 V
- Low Input Capacitance: 50 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

BLOCK DIAGRAM



HIGH SPEED 8-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 623-05

PIN DIAGRAM

ORDERING INFORMATION

Device	Temperature Range	Package
MC10319L	0° to +70°C	Ceramic

DS9680
(Replacing NP180)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3 to +0.3	Vdc
Digital Input Voltage (Pins 18–20)	$V_{I(D)}$	−0.5 to +7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	−2.5 to +2.5	Vdc
Reference Voltage Span (Pin 24–Pin 23)	—	2.3	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	—	−0.3 to +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+4.5	+5.0	+5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	−0.1	0	+0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 18–20)	$V_{I(D)}$	0	—	+5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	−1.0	—	+2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	−2.1	—	+1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+1.0	—	+2.1	Vdc
$V_{RB} - V_{EE}$	—	1.3	—	—	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	V_o	0	—	5.5	Vdc
Clock Pulse Width — High Low	t_{CKH} t_{CKL}	5.0 15	20 20	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	8.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity	INL	—	±1/4	±1.0	LSB
Differential Nonlinearity	DNL	—	—	±1.0	LSB
Differential Phase (See Figure 16)	DP	—	1.0	—	Deg.
Differential Gain (See Figure 16)	DG	—	1.0	—	%
Power Supply Rejection Ratio ($4.5\ V < V_{CC} < 5.5\ V$, V_{EE} = −5.2 V) ($-6.0\ V < V_{EE} < -3.0\ V$, V_{CC} = +5.0 V)	PSRR	— —	0.1 0	— —	LSB/V

ELECTRICAL CHARACTERISTICS — continued ($0° < T_A$ 70 C, V_{CC} 5.0 V, V_{EE} 5.2 V, V_{RT} +1.0 V, V_{RB} = 1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
ANALOG INPUT (PIN 14)					
Input Current @ $V_{in} = V_{RB}$ (See Figure 5)	I_{INL}	−100	0	—	μA
Input Current @ $V_{in} = V_{RT}$ (See Figure 5)	I_{INH}	—	60	150	μA
Input Capacitance ($V_{RT} - V_{RB}$ = 2.0 V, See Figure 4)	C_{in}	—	36	—	pF
Input Capacitance ($V_{RT} - V_{RB}$ = 1.0 V, See Figure 4)	C_{in}	—	55	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 open)	C_{ref}	—	25	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V) (See Figure 6)					
Input Voltage — High (Pins 19–20)	V_{IHE}	2.0	—	—	V
Input Voltage — Low (Pins 19–20)	V_{ILE}	—	—	0.8	V
Input Current @ 2.7 V	I_{IHE}	—	0	20	μA
Input Current @ 0.4 V @ $\overline{EN}$ (0 < EN < 5.0 V)	I_{IL1}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 0 V)	I_{IL2}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 2.0 V)	I_{IL3}	−20	−2.0	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage High	V_{IHC}	2.0	—	—	Vdc
Input Voltage Low	V_{ILC}	—	—	0.8	Vdc
Input Current @ 0.4 V (See Figure 7)	I_{ILC}	−400	−80	—	μA
Input Current @ 2.7 V (See Figure 7)	I_{IHC}	−100	−20	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA, V_{CC} = 4.5 V, See Figure 8)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA, See Figure 9)	V_{OL}	—	0.35	0.4	V
Output Short Circuit Current* (V_{CC} = 5.5 V)	I_{SC}	—	35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D7 in 3-State Mode)	I_{LK}	−50	—	+50	μA
Output Capacitance (D0–D7 in 3-State Mode)	C_{out}	—	9.0	—	pF
POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	I_{EE}	−14	−10	−6.0	mA
Power Dissipation ($V_{RT} - V_{RB}$ = 2.0 V) (Outputs unloaded)	P_D	—	618	995	mW

*Only one output is to be shorted at a time, not to exceed 1 second.

2

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}HZ}$	—	32	—	ns
Data Low to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}LZ}$	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	—	15	—	ns
Valid Data from $\overline{\text{Enable}}$ Low (Pin 19 = 5.0 V)*	$t_{\overline{E}DV}$	—	16	—	ns
Output Transition Time* (10%–90%)	t_{tr}	—	8.0	—	ns

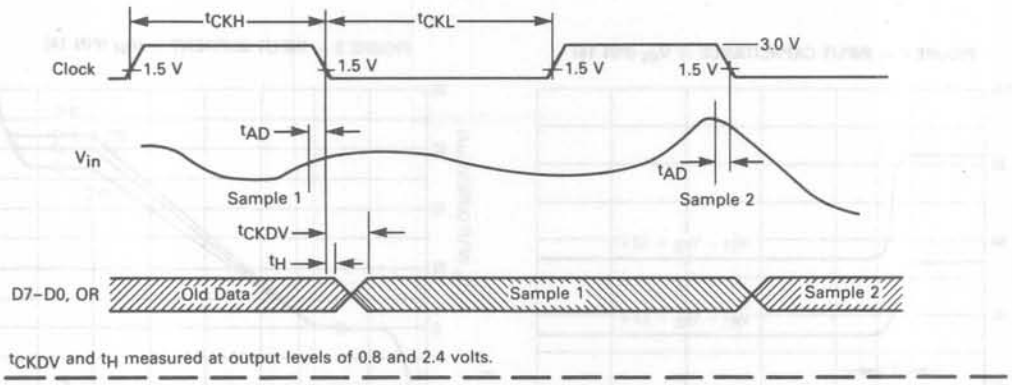
*See Figure 2 for output loading.

2

PIN DESCRIPTIONS

Symbol	Pin	Description
V_{RM}	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2,12 16,22	Power supply and signal ground. The four pins should be connected directly together, and through a low impedance to the power supply.
OVR	3	Overrange output. Indicates V_{in} is more positive than V_{RT}-1/2 LSB. This output does not have 3-state capability.
D7–D0	4–10, 21	Digital Outputs. D7 (Pin 4) is the MSB, D0 (Pin 21) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	11,17	Power supply for the digital section. +5.0 V, ±10% required.
V_{EE}	13	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by > 1.3 V.
V_{in}	14	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 kΩ in parallel with 36 pF.
$V_{CC(A)}$	15	Power supply for the analog section. +5.0 V, ±10% required.
CLK	18	Clock input. TTL compatible.
EN	19	Enable input. TTL compatible, a Logic "1" (and Pin 20 a Logic "0") enables the data outputs. A Logic "0" puts the outputs in a 3-state mode.
$\overline{\text{EN}}$	20	$\overline{\text{Enable}}$ input. TTL compatible, a Logic "0" (and Pin 19 a Logic "1") enables the data outputs. A Logic "1" puts the outputs in a 3-state mode.
V_{RB}	23	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	The top (most positive point) of the internal reference resistor ladder.

FIGURE 1 — SYSTEM TIMING DIAGRAM



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 volts.

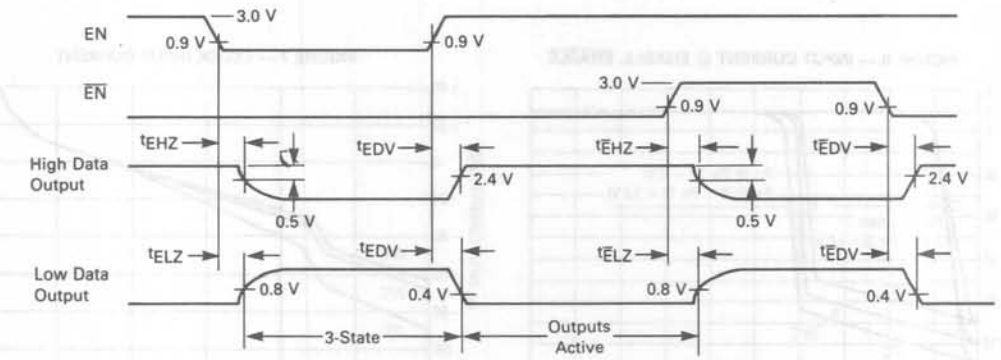
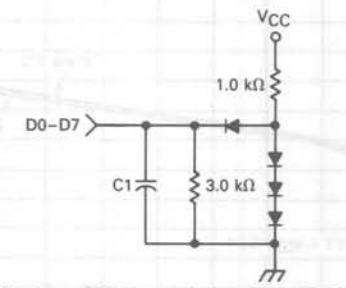


FIGURE 2 — DATA OUTPUT TEST CIRCUIT



Diodes = 1N914 or equivalent, C1 ≈ 15 pF

FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

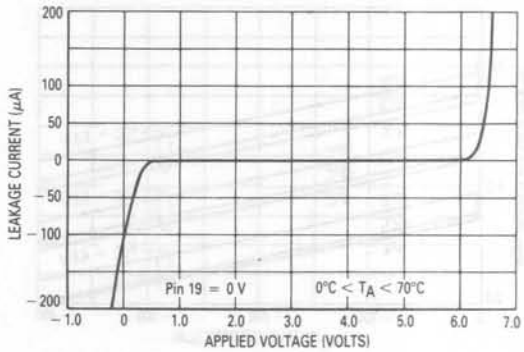


FIGURE 4 — INPUT CAPACITANCE @ V_{IN} (PIN 14)

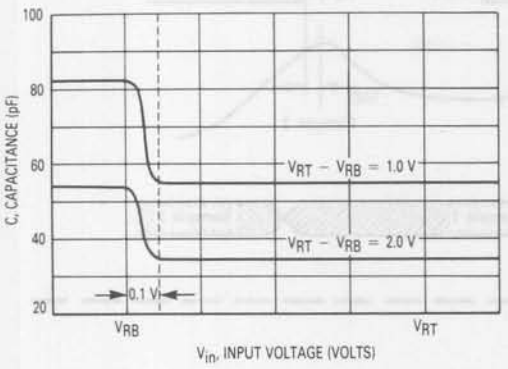


FIGURE 5 — INPUT CURRENT @ V_{IN} (PIN 14)

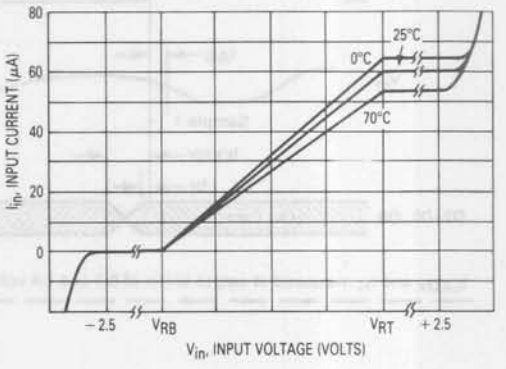


FIGURE 6 — INPUT CURRENT @ ENABLE, $\overline{\text{ENABLE}}$

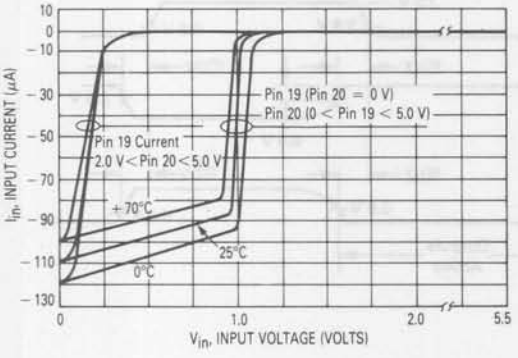


FIGURE 7 — CLOCK INPUT CURRENT

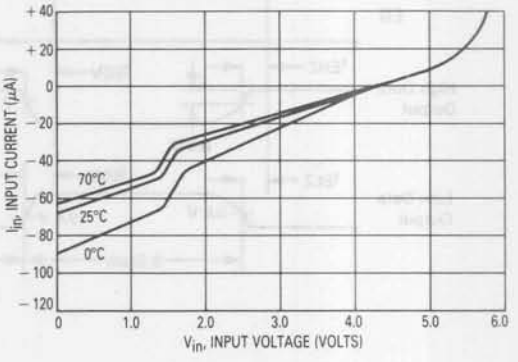


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

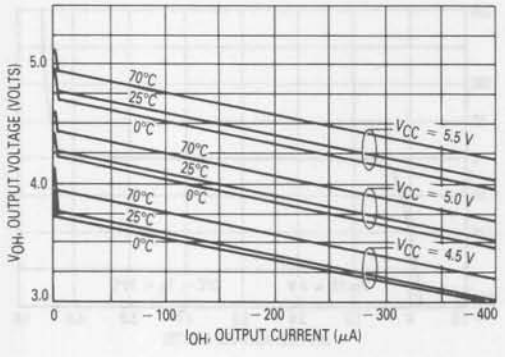


FIGURE 9 — OUTPUT VOLTAGE versus OUTPUT CURRENT

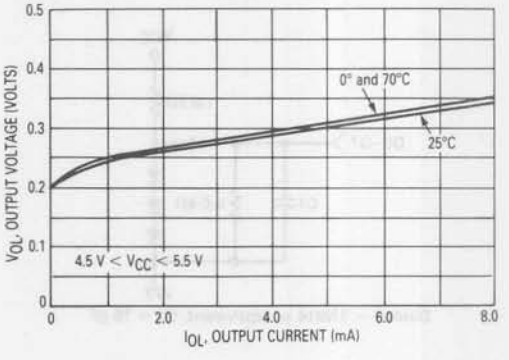


FIGURE 10 — SUPPLY CURRENT versus TEMPERATURE

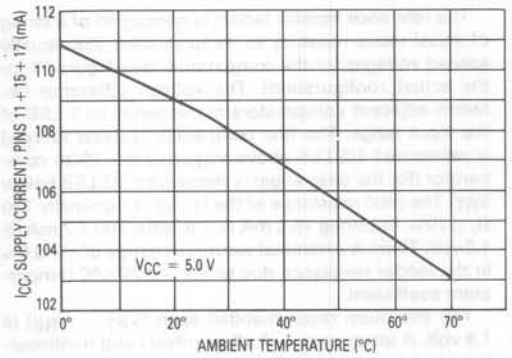


FIGURE 11 — SUPPLY CURRENT versus TEMPERATURE

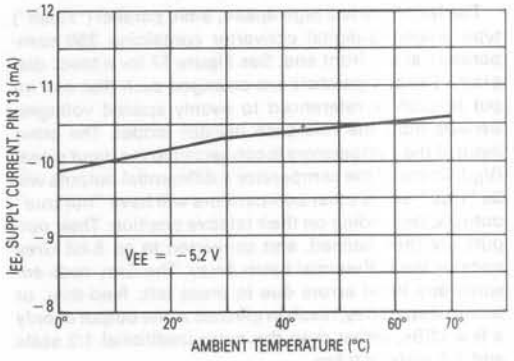


FIGURE 12 — DIFFERENTIAL LINEARITY ERROR

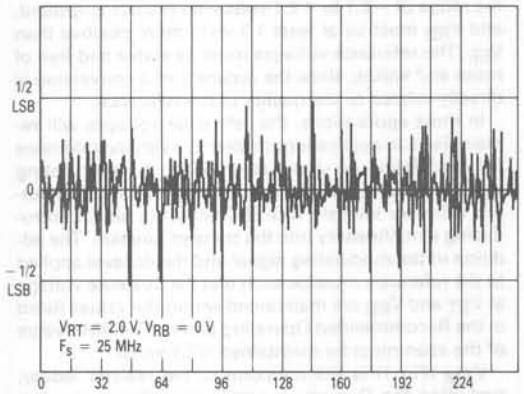


FIGURE 13 — INTEGRAL LINEARITY ERROR

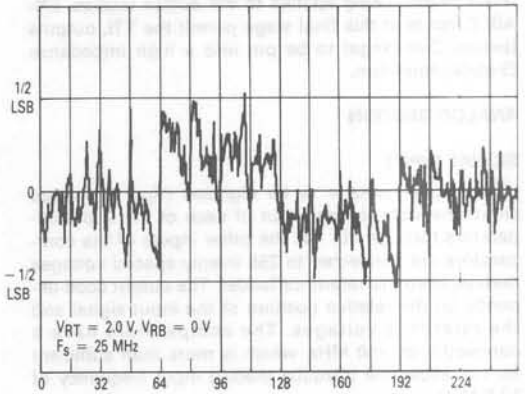


FIGURE 14 — DIFFERENTIAL LINEARITY ERROR

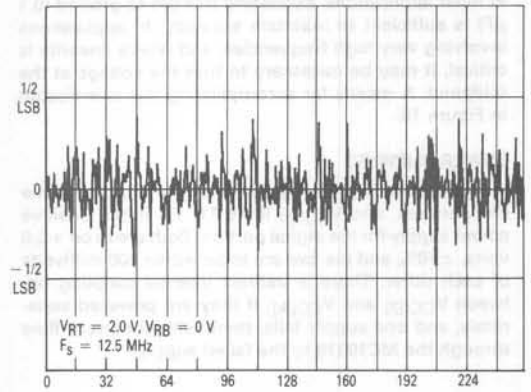
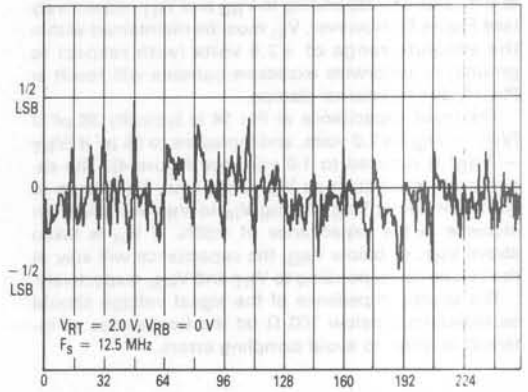


FIGURE 15 — INTEGRAL LINEARITY ERROR



2

DESIGN GUIDELINES

INTRODUCTION

The MC10319 is a high-speed, 8-bit, parallel ("Flash") type analog-to-digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to an 8-bit Grey code by the Differential Latch Array. The Grey code ensures any input errors due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

2

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if [$V_{RT} - V_{RB}$] is 2.0 volts, and increases to 55 pF if [$V_{RT} - V_{RB}$] is reduced to 1.0 volt (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈0.1 volt above V_{RB}. Taking V_{in} to V_{RB} will show an increase in the capacitance of ≈50%. If V_{in} is taken above V_{RT}, or below V_{RB}, the capacitance will stay at the values corresponding to V_{RT} and V_{RB}, respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 130 Ω, ±20%, requiring 15.4 mA @ 2.0 volts, and 7.7 mA @ 1.0 volt. There is a nominal warm-up change of ≈ +9.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversly with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 μF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

POWER SUPPLIES

$V_{CC(A)}$ (Pin 15) is the positive power supply for the comparators, and $V_{CC(D)}$ (Pins 11, 17) is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

$I_{CC(A)}$ is nominally 17 mA, and does not vary with clock frequency or with V_{in}. It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6–7 mA as V_{in} is changed, with the lowest current occuring when $V_{in} = V_{RT}$. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −10 mA, and is independent of clock frequency, V_{in}, and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC.** A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 18) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 19, 20) are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3-state. This capability allows cascading two MC10319s into a 9-bit configuration, flip-flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic "1," and Pin 20 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input — output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 3) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 4–10, 21) are TTL level outputs with high impedance capability. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overrange output (Pin 3) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9-bit A/D converter (see Figure 27).

Input	V_{RT}, V_{RB} (volts)			Output Code	Overrange
	2.048 V, 0 V	+1.0 V, −1.0 V	+1.0 V, 0 V		
>V_{RT} − 1/2 LSB	>2.044 V	>0.9961 V	>0.9980 V	FF_H	1
V_{RT} − 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FF_H	0 ↔ 1
V_{RT} − 1 LSB	2.040 V	0.992 V	0.9961 V	FF_H	0
V_{RT} − 1-1/2 LSB	2.036 V	0.988 V	0.9941 V	$FE_H \leftrightarrow FF_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	80_H	0
V_{RB} + 1/2 LSB	4.0 mV	−0.9961 V	1.95 mV	$00_H \leftrightarrow 01_H$	0
<V_{RB}	<0 V	< −1.0 V	<0 V	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, 22) must be connected directly together. Any long path beween them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2 volts, then 1/2 LSB is only 3.9 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of 0 to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (50–400 mV) present on the supplies and on their ground lines. Generally $\pm$15 volts, or $\pm$12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @2.0 volts). The MC1400 and MC1403 series of reference sources have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. Although the MC1400G2 is meant to provide a positive voltage, it can be configured to provide a negative regulated voltage by grounding the input and output, and deriving the regulated voltage at the ground pin (Pin 4). The MC1403 series of regulators cannot be used in this manner. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9-BIT A/D CONVERTER

Figure 27 shows how two MC10319s can be connected to form a 9-bit converter. In this configuration, the outputs (D7–D0) of the two 8-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non-equal voltage division would occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application.

50 MHz, 8-BIT A/D CONVERTER

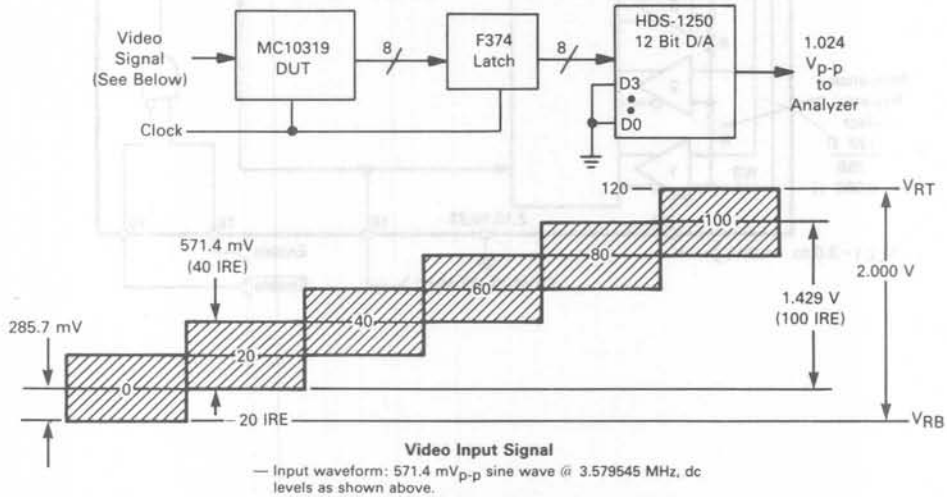
Figure 28 shows how two MC10319s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the ENABLES so as to alternately enable and disable the outputs. The Overranges do not have 3-state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high-to-low transition of the 50 MHz clock.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 29 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10319. The MC34063 is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are given in the Figure.

2

FIGURE 16 — DIFFERENTIAL PHASE AND GAIN TEST



Video Input Signal

— Input waveform: 571.4 mV_{p-p} sine wave @ 3.579545 MHz, dc levels as shown above.
— MC10319 clock at 14.31818 MHz (4x) asynchronous to input.
— Differential gain: p-p output @ each IRE level compared to that at 0 IRE.
— Differential phase: Phase @ each IRE level compared to that @ 0 IRE.

FIGURE 17 — MC10319

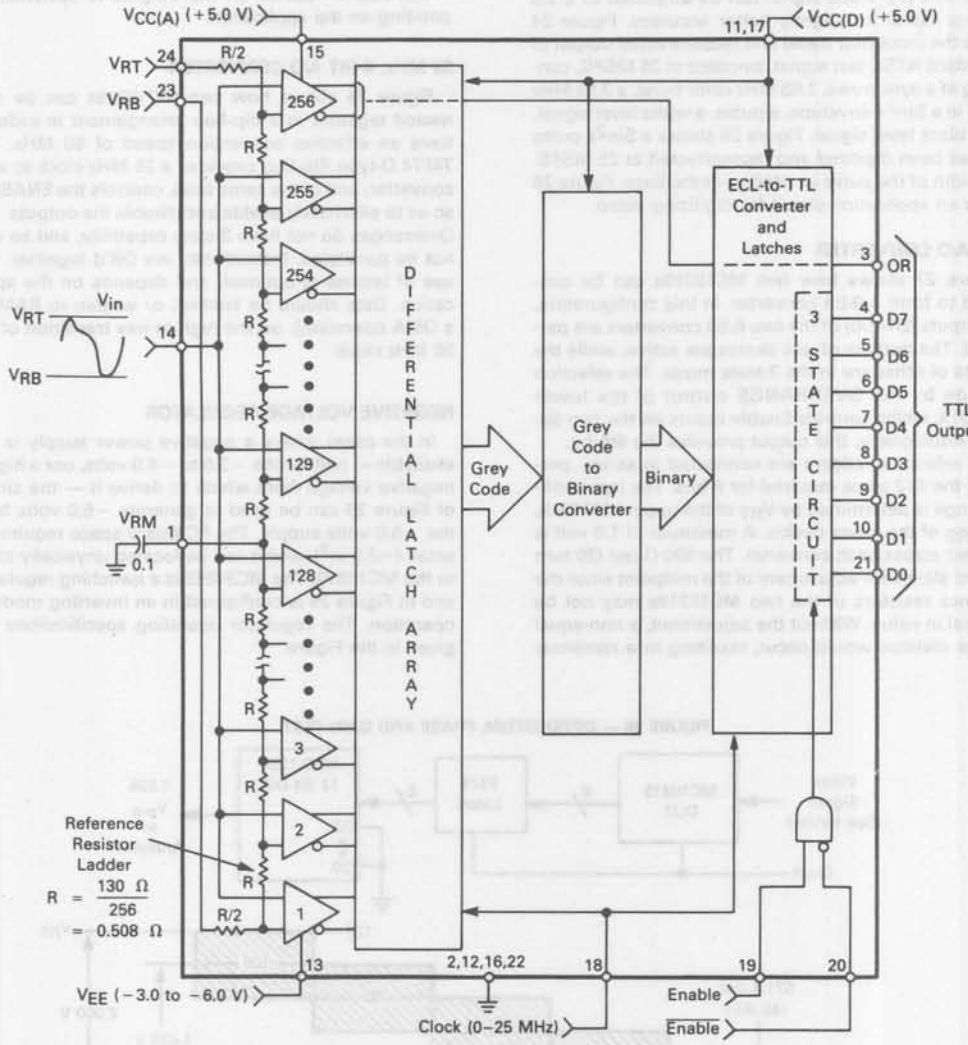


FIGURE 18 — ADJUSTING V_{RM} FOR IMPROVED LINEARITY

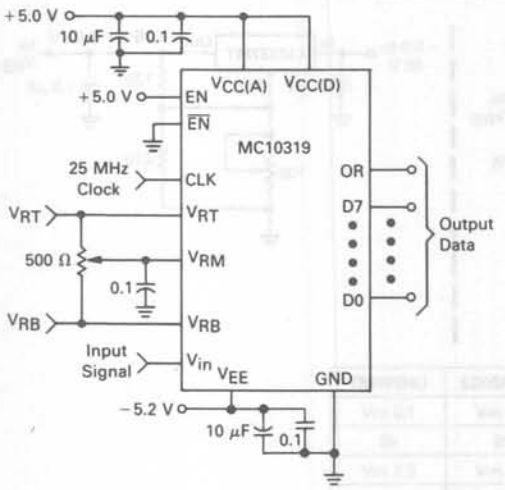


FIGURE 19 — CONVERSION SEQUENCE

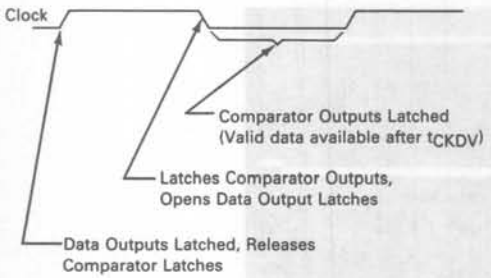
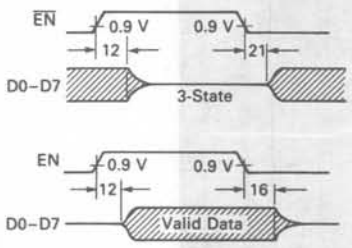
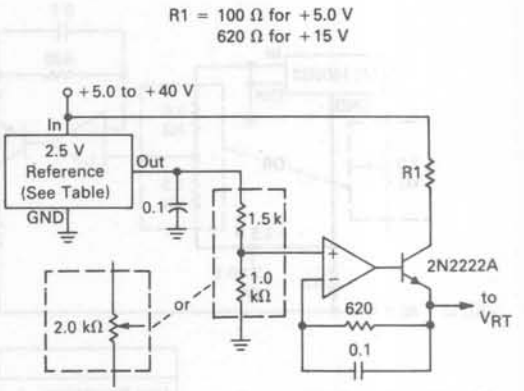


FIGURE 20 — ENABLE TO OUTPUT CRITICAL TIMING



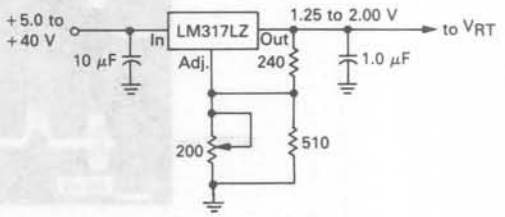
Timing @ D7–D0 measured where waveform starts to change.
Indicated time values are typical @ 25°C, and are in ns.

FIGURE 21 — PRECISION V_{RT} VOLTAGE SOURCE



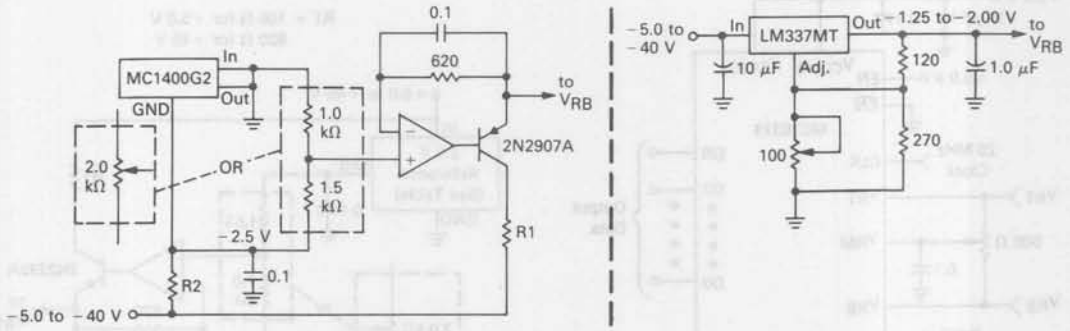
2.5 V References	MC1400G2	MC1403U	MC1403AU
Line Regulation	1.0 mV	0.5 mV	0.5 mV
T_C (ppm/°C) max	25	40	25
ΔV_{out} for 0–70°C	4.4 mV	7.0 mV	4.4 mV
Initial Accuracy	±0.2%	±1%	±1%

FIGURE 22 — V_{RT}, VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
T_C (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4%

FIGURE 23 — V_{RB} VOLTAGE SOURCES



R1 = 100 Ω for −5.0 V
620 Ω for −15 V
R2 = 620 Ω for −5.0 V
3.0 kΩ for −15 V

	MC1400G2	LM337MT
Line Regulation	1.0 mV	1.0 mV
T_C (ppm/°C) max	25	48
ΔV_{out} for 0–70°C	4.4 mV	6.7 mV
Initial Accuracy	±0.2%	±4%

FIGURE 24 — COMPOSITE VIDEO WAVEFORM

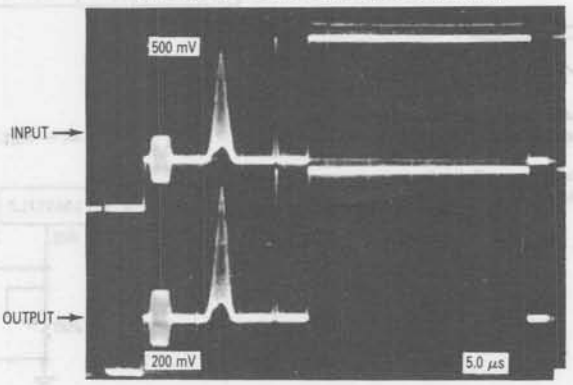


FIGURE 25 — SIN^2 X WAVEFORM

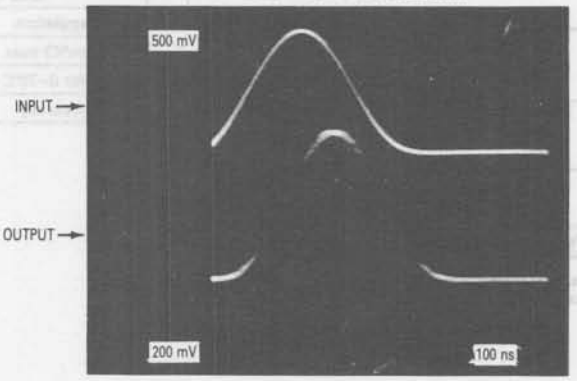
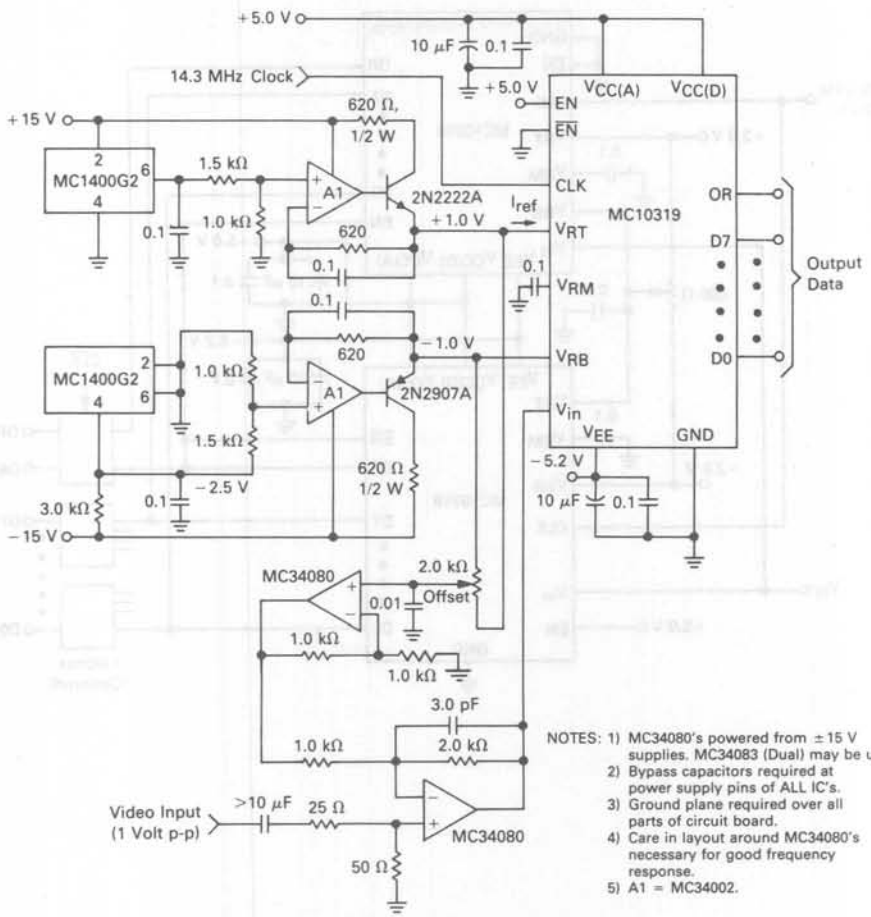


FIGURE 26 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) MC34080's powered from ±15 V supplies. MC34083 (Dual) may be used.
2) Bypass capacitors required at power supply pins of ALL IC's.
3) Ground plane required over all parts of circuit board.
4) Care in layout around MC34080's necessary for good frequency response.
5) A1 = MC34002.

2

FIGURE 27 — 9-BIT A/D CONVERTER

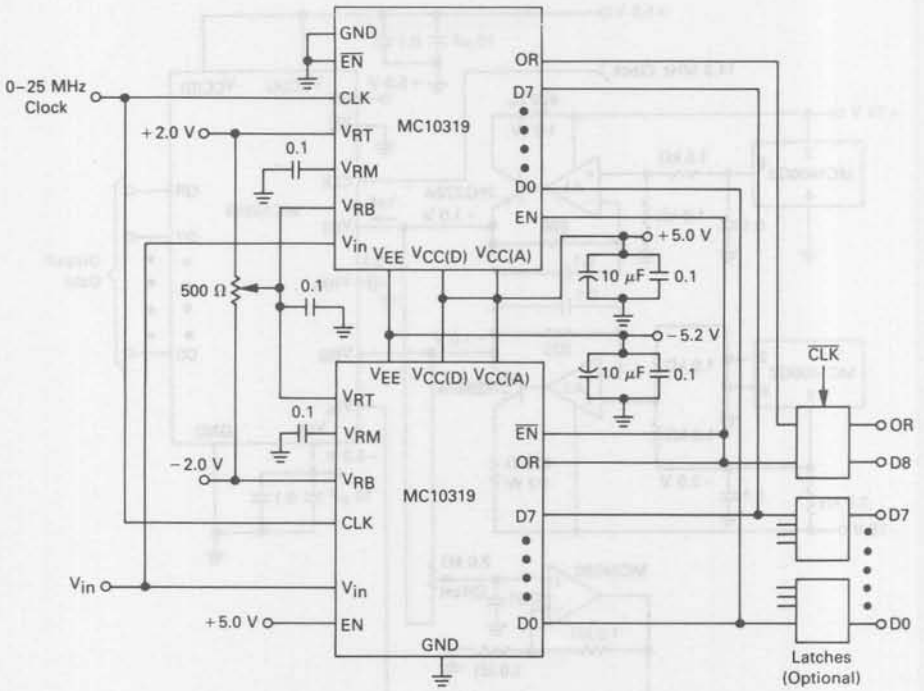


FIGURE 28 — 50 MHz 8-BIT A/D CONVERTER

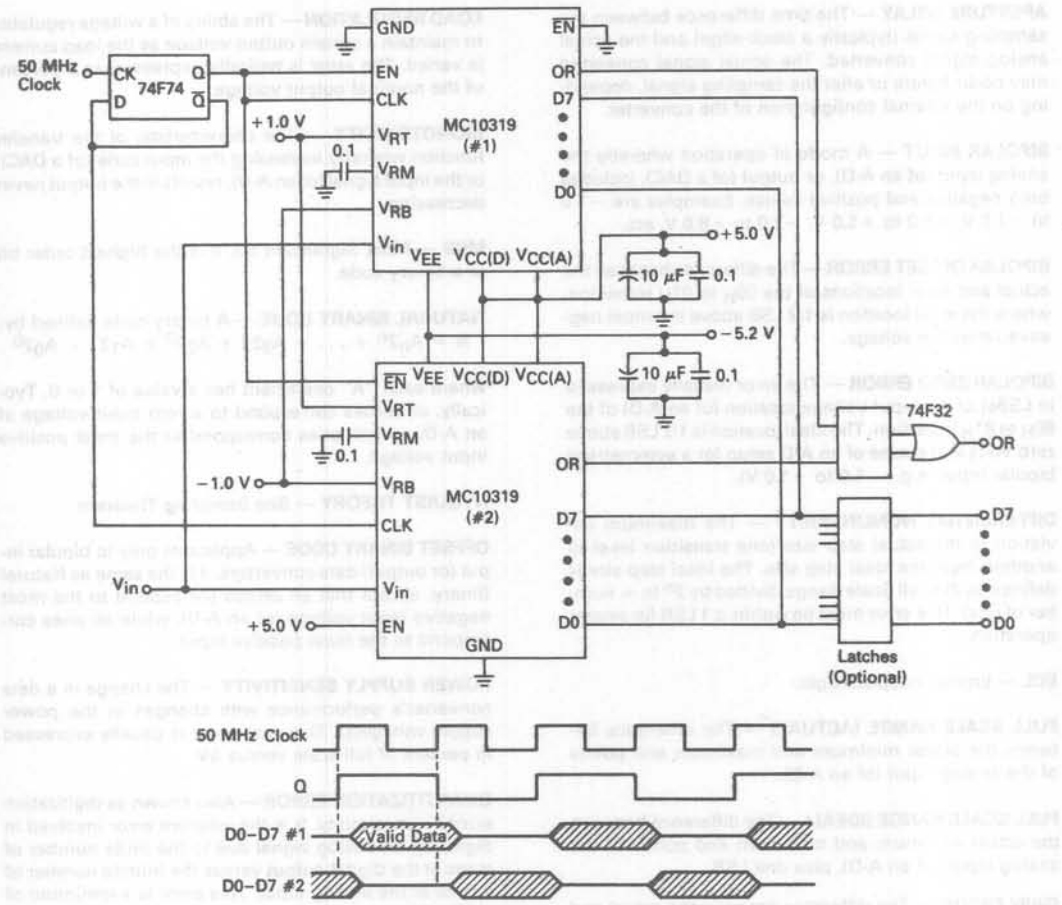
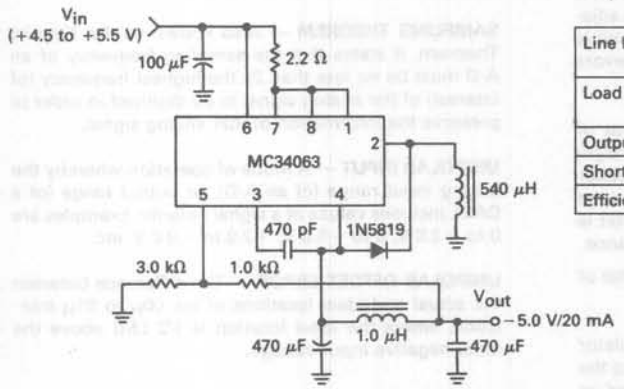


FIGURE 29 — −5.0 VOLT REGULATOR



Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA < I_{out} < 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2 mV_{p-p}
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

2

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the 80_H to 81_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A-D setup for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

ECL — Emitter coupled logic.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as *reflected binary code*, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent o

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A-D, and all ones correspond to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes correspond to the most negative input voltage (of an A-D), while all ones correspond to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

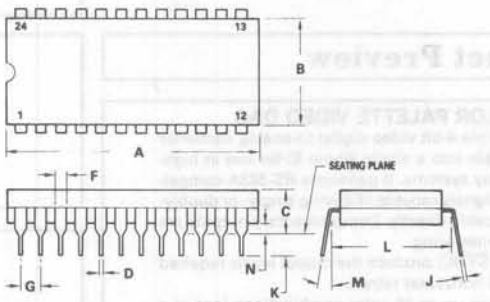
RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

OUTLINE DIMENSIONS



NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

L SUFFIX
CERAMIC PACKAGE
CASE 623-05

2

MOTOROLA

MC10320

Product Preview

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

The MC10320 integrates a triple 4-bit video digital-to-analog converter and a 16 x 12 color look-up table into a single 28-pin IC for use in high-resolution color graphics display systems. It generates RS-343A compatible red, green and blue video signals capable of driving singly- or doubly-terminated 50 ohm or 75 ohm cable directly. Complementary outputs are provided for custom monitor interfacing.

Control signals ($\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$) produce the output levels required by the monitor for vertical and horizontal retrace.

The color look-up table allows up to 16 color combinations (out of a palette of 4096) on the screen at any one time. The table can be updated as often as desired during vertical retrace.

The lower speed digital inputs ($\overline{\text{Write}}$, Data and $\overline{\text{SYNC}}$) are TTL compatible, whereas the high-speed signals (Address, PIXEL CLOCK and $\overline{\text{BLANK}}$) can be user programmed to either ECL or TTL compatibility. The address and blank signals are latched into input registers, providing great input timing flexibility. Additional registers frame the data as it is presented to the three DACs, ensuring low glitch area and matched responses.

Innovative level translators allow for both single- and dual-supply operation for tremendous flexibility to meet the demands of any system design.

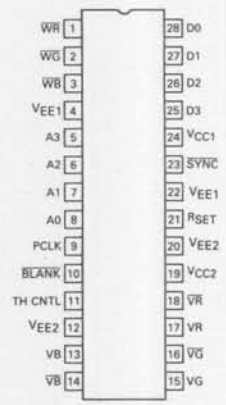
The MC10320 is fabricated with Motorola's MOSAIC process to obtain high speed and low power dissipation.

- Triple 4-Bit Video DAC with 16 x 12 Color Look-Up Table
- Monolithic Construction
- 125 MHz Pixel Rate (MC10320L) or 90 MHz Pixel Rate (MC10320L1)
- User Selectable TTL or ECL Compatibility on High-Speed Inputs
- Single- or Dual-Supply Operation
- RS-343A Compatible Outputs
- Low Glitch Area — 20 pV-S Typical
- Low Power Dissipation — 750 mW Typical
- Internal Bandgap Reference
- Excellent Supply Rejection
- Differential Current Outputs
- Sync and Blank Video Control Signals

TRIPLE 4-BIT COLOR PALETTE VIDEO DAC

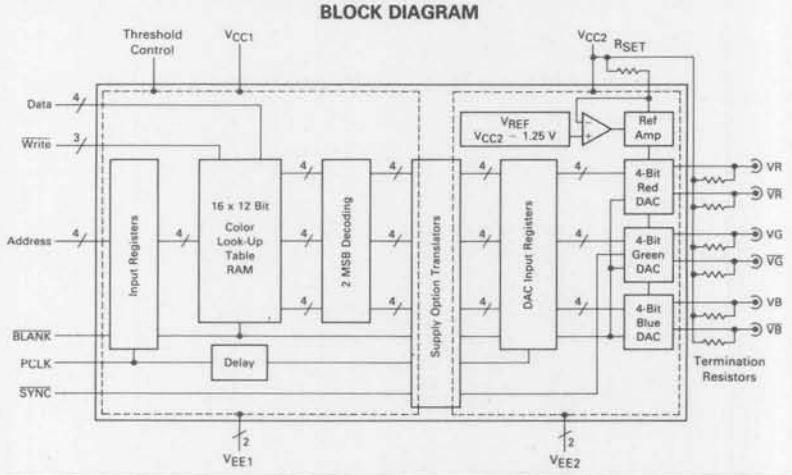
SILICON MONOLITHIC INTEGRATED CIRCUIT

L or L1 SUFFIX CERAMIC PACKAGE CASE 733-03



2

BLOCK DIAGRAM



NP193

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Supply Voltages V_{CC1} (measured to V_{EE1}) V_{CC2} (measured to V_{EE2}) V_{EE2} (measured to V_{EE1})	 −0.5 to +7.0 −0.5 to +7.0 −7.0 to +0.5	Vdc
Input Voltages (Address, Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$, $\overline{BLANK}$, PCLK) Threshold Control (measured to V_{EE1}) R_{SET} Pin (measured to V_{EE2})	 −0.5 to V_{CC1} +0.5 −0.5 to V_{CC1} +0.5 −0.5 to V_{CC2}	Vdc
Output Voltages (VR, $\overline{VR}$, VG, $\overline{VG}$, VB, $\overline{VB}$, measured to V_{EE2})	+2.5 to +8.0	Vdc
Junction Temperature	−55 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Single Supply — V_{CC1} V_{EE1} V_{CC2} V_{EE2}	4.5 — 4.5 —	5.0 0 5.0 0	5.5 — 5.5 —	Vdc
Dual Supply — V_{CC1} V_{EE1} V_{CC2} V_{EE2}	4.5 — — −4.5	5.0 0 0 −5.0	5.5 — — −5.5	Vdc
R_{SET} R_L	500 0	1.0K 37.5	2.0K 75	Ω
Input Voltages — TTL High TTL Low ECL High ECL Low	V_{EE1} + 2.0 V_{EE1} V_{CC1} − 1.13 V_{EE1}	— — — —	V_{CC1} V_{EE1} + 0.8 V_{CC1} V_{CC1} − 1.48	Vdc
Output Compliance (measured to V_{CC2})	−2.0	0	+2.0	Vdc
Ambient Temperature	0	—	+70	°C

ELECTRICAL CHARACTERISTICS (R_{SET} = 1 kΩ, R_L = 37.5 Ω, T_A = +25°C)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (Each DAC)	Res	4.0	4.0	4.0	Bits
Palette Colors (Active) (Possible Range)	— —	— —	— —	16 4096	Colors
Voltage Output (Each DAC, VR, VG, VB, relative to V_{CC2}) Ref White (DAC Input = 1111) Ref Black (DAC Input = 0000) Blank ($\overline{BLANK}$ = 0) Sync ($\overline{SYNC}$ = 0, $\overline{BLANK}$ = 0, Green Only)	 V_{RW} V_{RB} V_B V_{SY}	 −15 −672 −724 −1029	 −2.0 −640 −690 −980	 0 −608 −655 −931	mV
Output Impedance	Z_o	—	100	—	kΩ
Gain Error (Each DAC, Ref White to Ref Black)	G_{ER}	−5.0	0	+5.0	%
Gain Tracking Error (Any Two DACs @ Ref Black)	G_{TR}	−3.0	0	+3.0	%
Integral Nonlinearity	INL	−1/4	0	+1/4	LSB
Differential Nonlinearity	DNL	−1/4	0	+1/4	LSB
Monotonicity	—	Guaranteed			
Offset (@ Ref White)	I_{OS}	—	50	—	μA
Input Voltage High (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{IHA}	V_{EE1} + 2.0	—	—	Vdc
Input Voltage Low (Data, $\overline{WR}$, $\overline{WG}$, $\overline{WB}$, $\overline{SYNC}$)	V_{ILA}	—	—	V_{EE1} + 0.8	Vdc
Input Voltage High (Address, PCLK, $\overline{BLANK}$) (Threshold Cont. @ V_{EE1} [TTL Mode]) (Threshold Cont. @ V_{CC1} [ECL Mode])	 V_{IHB} V_{IHC}	 V_{EE1} + 2.0 V_{CC1} − 1.13	 — —	 — —	Vdc

(continued)

ELECTRICAL CHARACTERISTICS — continued

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Low (Address, PCLK, $\overline{BLANK}$)					Vdc
(Threshold Cont. @ V_{EE1} [TTL Mode])	V_{ILB}	—	—	V_{EE1} + 0.8	
(Threshold Cont. @ V_{CC1} [ECL Mode])	V_{ILC}	—	—	V_{CC1} − 1.48	
Input Current @ 2.4 V (TTL Mode) (All Digital Inputs	I_{IHA}	—	50	—	μA
@ 0.4 V (TTL Mode) except Pin 11)	I_{ILA}	—	10	—	
@ V_{CC1} − 0.8 V (ECL Mode)	I_{IHB}	—	100	—	
@ V_{CC1} − 1.8 V (ECL Mode)	I_{ILB}	—	60	—	
Power Supply Rejection Ratio (All DACs @ Ref Black)	PSRR				dB
V_{CC1} @ 1.0 kHz		—	60	—	
V_{CC1} @ 1.0 MHz		—	45	—	
V_{CC1} @ 50 MHz		—	30	—	
V_{EE} @ 1.0 kHz		—	50	—	
V_{EE} @ 1.0 MHz		—	33	—	
V_{EE} @ 50 MHz		—	12	—	
Signal Feedthrough due to	SRR				dB
Pixel Clock @ 125 MHz		—	−50	—	
$\overline{BLANK}$ @ 125 MHz		—	−50	—	
Data @ 125 MHz		—	−60	—	
Power Supply Requirements					mA
V_{CC1} Current	I_{CC1}	—	50	—	
V_{EE1} Current	I_{EE1}	—	50	—	
V_{CC2} Current	I_{CC2}	—	28	—	
V_{EE2} Current (Includes Output Current)	I_{EE2}	—	−95	—	
Power Dissipation	PW	—	750	—	mW

TIMING CHARACTERISTICS (T_A = +25°C)

Parameter	Symbol	Min	Typ	Max	Units
Max Pixel Clock Rate	fCLK				MHz
MC10320L		125			
MC10320L1		90			
READ Cycle (Display Mode)					ns
Address, $\overline{BLANK}$, Setup Time	t_{RSA}	—	1.5	—	
Address, $\overline{BLANK}$, Hold Time	t_{RHA}	—	1.5	—	
Min Clock Pulse Width — High	t_{PWH}	—	3.0	—	
Min Clock Pulse Width — Low	t_{PWL}	—	3.0	—	
Pipeline Delay	t_{PIPE}	1.0	1.0	1.0	Clock Cycle
DAC Prop Delay (to 50% Point)	t_{DPD}	—	9.0	—	ns
DAC Prop Delay Difference (DAC to DAC)	$t_{DPD\Delta}$	—	0.5	—	
$\overline{SYNC}$ Prop Delay	t_{SPD}	—	6.0	—	
Output Settling Time (±1/2 LSB to ±1/2 LSB)	t_{DS}	—	3.0	—	
Output Slew Rate	SR	—	300	—	V/μs
Glitch Area	A_G	—	20	—	pV−S
WRITE Cycle (RAM Update Mode)					ns
Address Setup Time	t_{WSA}	—	1.5	—	
Clock Setup Time	t_{WSC}	—	5.0	—	
Data Setup Time	t_{WSD}	—	60	—	
Write Pulse Width	t_{WPW}	—	60	—	
Address Hold Time	t_{WHA}	—	1.5	—	
Clock Hold Time	t_{WHC}	—	10	—	
Data Hold Time	t_{WHD}	—	10	—	

TEMPERATURE CHARACTERISTICS (0°C < T_A < +70°C)

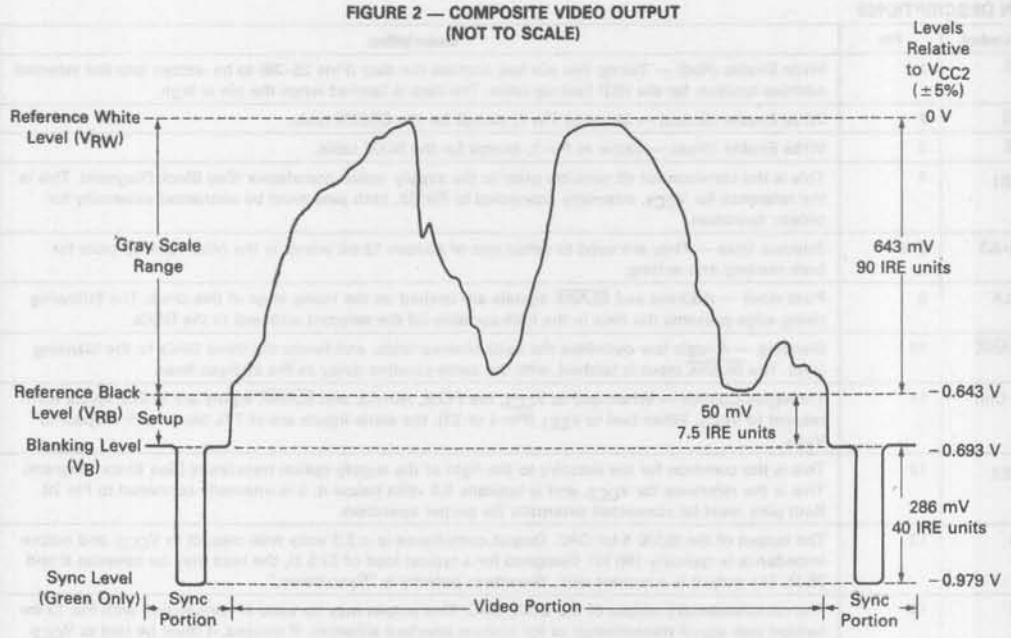
Parameter	Typical Change	Units
Offset (at Ref White)	±20	ppm GS/°C
DAC Gain	±100	
Gain Tracking (any 2 DACs @ Ref Black)	±50	
Linearity	±100	

Note: ppm GS/°C = Parts Per Million of Gray Scale/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
$\overline{WR}$	1	Write Enable (Red) — Taking this pin low enables the data (Pins 25–28) to be written into the selected address location for the RED look-up table. The data is latched when the pin is high.
$\overline{WG}$	2	Write Enable (Green) — Same as Pin 1, except for the GREEN table.
$\overline{WB}$	3	Write Enable (Blue) — Same as Pin 1, except for the BLUE table.
V_{EE1}	4	This is the common for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}. Internally connected to Pin 22, both pins *must* be connected externally for proper operation.
A0–A3	5–8	Address lines — They are used to select one of sixteen 12-bit words in the color look-up table for both reading and writing.
PCLK	9	Pixel clock — Address and $\overline{BLANK}$ signals are latched on the rising edge of this clock. The following rising edge presents the data in the look-up table (of the selected address) to the DACs.
$\overline{BLANK}$	10	Blanking — A logic low overrides the color look-up table, and forces the three DACs to the blanking level. The $\overline{BLANK}$ input is latched, with the same pipeline delay as the address lines.
Th Cntl	11	Threshold Control — When tied to V_{CC1}, the PCLK, A0–A3, and $\overline{BLANK}$ inputs are at ECL levels with respect to V_{CC1}. When tied to V_{EE1} (Pin 4 or 22), the same inputs are at TTL levels with respect to V_{EE1}.
V_{EE2}	12	This is the common for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally conneced to Pin 20. Both pins must be connected externally for proper operation.
VB	13	The output of the BLUE 4-bit DAC. Output compliance is ±2.0 volts with respect to V_{CC2}, and output impedance is typically 100 kΩ. Designed for a typical load of 37.5 Ω, the load may be between 0 and 75 Ω. The output is a current sink. Waveform polarity is "Sync down."
$\overline{VB}$	14	The complementary output of the BLUE DAC. This output may be used in conjunction with Pin 13 for twisted pair signal transmission or for custom interface schemes. If unused, it must be tied to V_{CC2}.
VG	15	Same as Pin 13, except for the GREEN DAC.
$\overline{VG}$	16	Same as Pin 14, except for the GREEN DAC.
VR	17	Same as Pin 13, except for the RED DAC.
$\overline{VR}$	18	Same as Pin 14, except for the RED DAC.
V_{CC2}	19	Power supply pin for the circuitry to the right of the supply option translators (See Block Diagram). Its reference is V_{EE2}, and nominally 5.0 volts more positive than V_{EE2}.
V_{EE2}	20	This is the common for the circuitry to the right of the supply option translators (See Block Diagram). This is the reference for V_{CC2}, and is typically 5.0 volts below it. It is internally connected to Pin 12. Both pins must be connected externally for proper operation.
R_{SET}	21	Current setting resistor — A user supplied low inductance resistor is to be connected between V_{CC2} and this pin to set the DAC's full scale current. An R_{SET} of 1.0 kΩ, combined with load resistors of 37.5 Ω (at Pins 13, 15, 17) provides output signals consistent with RS-343A. The R_{SET} resistor is to be between 500 Ω and 2.0 kΩ.
V_{EE1}	22	This is the common for all circuitry prior to the supply option translators (See Block Diagram). This is the reference for V_{CC1}. Internally connected to Pin 4, both pins *must* be connected externally for proper operation.
$\overline{SYNC}$	23	A logic low on this input forces the GREEN DAC to increase its output current by 7.6 mA (R_{SET} = 1.0 kΩ), providing the sync level of 286 mV (R_L = 37.5 Ω) below blanking. The $\overline{BLANK}$ input must have been asserted previously.
V_{CC1}	24	Power supply pin for the circuitry to the left of the supply option translators (See Block Diagram).
D0–D3	25–28	Data inputs — Data on these pins is written into the color look-up table, at the locations specified by the address lines, by taking the appropriate WRITE pin low.

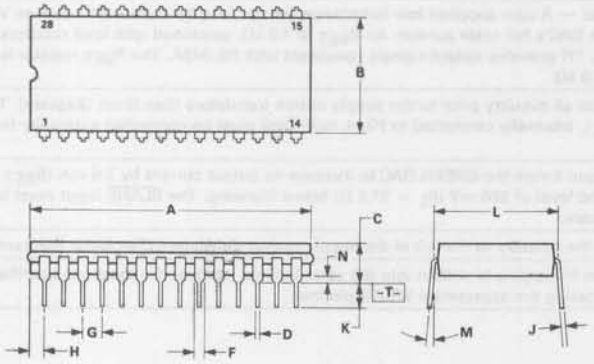
FIGURE 2 — COMPOSITE VIDEO OUTPUT
(NOT TO SCALE)



R_{SET} = 1.0 kΩ, R_L = 37.5 Ω

2

OUTLINE DIMENSIONS



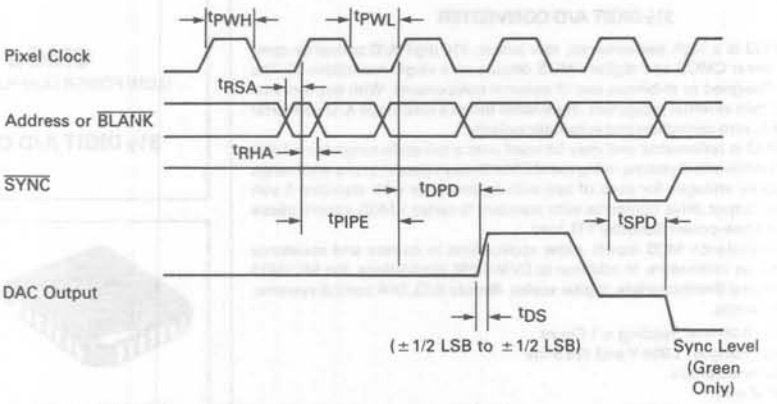
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌀ 0.25 (0.010) M T A M
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

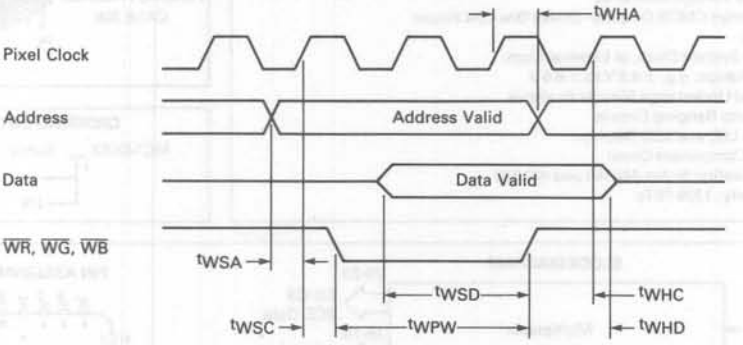
L SUFFIX
CERAMIC PACKAGE
CASE 733-03

FIGURE 1 — TIMING DIAGRAM

READ CYCLE (PIXEL DISPLAY MODE)



WRITE CYCLE (COLOR LOOK-UP TABLE UPDATE MODE)



2

MOTOROLA

MC14433

3½ DIGIT A/D CONVERTER

The MC14433 is a high performance, low power, 3½ digit A/D converter combining both linear CMOS and digital CMOS circuits on a single monolithic IC. The MC14433 is designed to minimize use of external components. With two external resistors and two external capacitors, the system forms a dual slope A/D converter with automatic zero correction and automatic polarity.

The MC14433 is ratiometric and may be used over a full-scale range from 1.999 volts to 199.9 millivolts. Systems using the MC14433 may operate over a wide range of power supply voltages for ease of use with batteries, or with standard 5 volt supplies. The output drive conforms with standard B-series CMOS specifications and can drive a low-power Schottky TTL load.

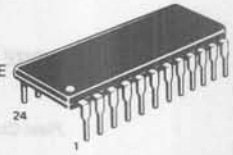
The high impedance MOS inputs allow applications in current and resistance meters as well as voltmeters. In addition to DVM/DPM applications, the MC14433 finds use in digital thermometers, digital scales, remote A/D, D/A control systems, and in MPU systems.

- Accuracy: ± 0.05% of Reading ± 1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions/s
- Z_{in} > 1000 M ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs - Drives One Low Power Schottky Load
- Uses On-Chip System Clock, or External Clock
- Wide Supply Range: e.g. ± 4.5 V to ± 8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates with LED and LCD Displays
- Low External Component Count
- See also Application Notes AN-769 and AN-770
- Chip Complexity: 1326 FETs

CMOS LSI
(LOW POWER COMPLEMENTARY MOS)

3½ DIGIT A/D CONVERTER

FN SUFFIX
PLCC PACKAGE
CASE 776-01

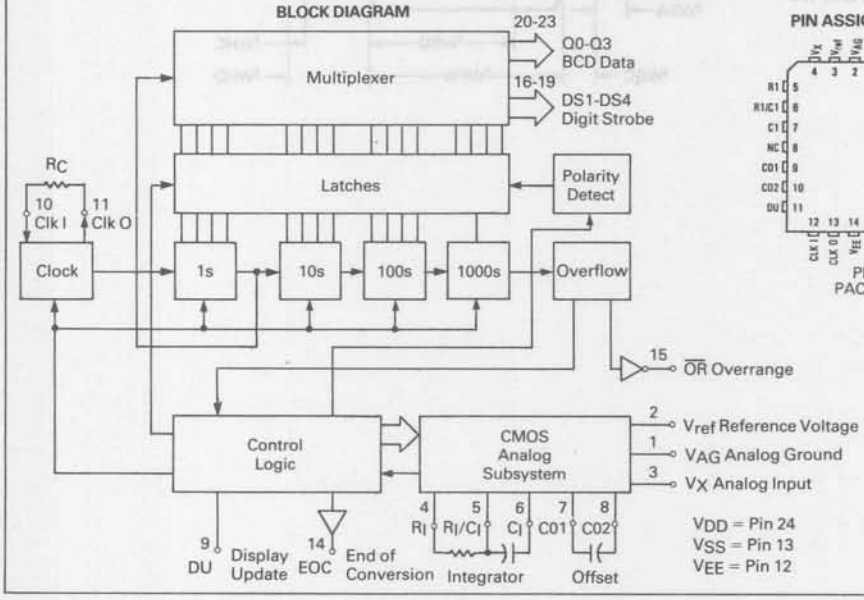


P SUFFIX
PLASTIC PACKAGE
CASE 709

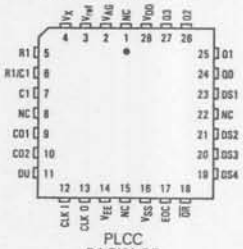
ORDERING INFORMATION

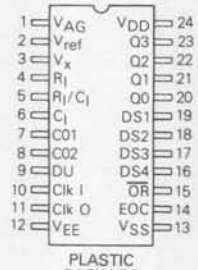
MC14XXX	Suffix	Denotes
	P	Plastic Package
	FN	PLCC Package

BLOCK DIAGRAM



PIN ASSIGNMENTS





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD} to V_{EE}	−0.5 to +18	V
Voltage, any pin, referenced to V_{EE}	V	−0.5 to V_{DD} +0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{EE} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 or V_{EE})

Parameter	Symbol	Value	Unit
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	−2.8 to −8.0	
Clock Frequency	f_{Clk}	32 to 400	kHz
Zero Offset Correction Capacitor	C_o	0.1 ± 20%	μF

ELECTRICAL CHARACTERISTICS (C_I = 0.1 μF mylar, R_I = 470 kΩ@V_{ref} = 2.000 V, R_I = 27 kΩ@V_{ref} = 200.0 mV, C_o = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1, unless otherwise indicated)

Characteristic	Symbol	V_{DD} Vdc	V_{EE} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Linearity-Output Reading (Note 1)	–										%rdg
(V_{ref} = 2.000 V)		5.0	−5.0	–	–	−0.05 − Count	±0.05	+0.05 + Count	–	–	
(V_{ref} = 200.0 mV)		5.0	−5.0	–	–	–	±0.05	–	–	–	
Stability — Output Reading (V_X = 199.0 mV, V_{ref} = 200.0 mV)	–	5.0	−5.0					3			LSD
Symmetry — Output Reading (Note 2) (V_{ref} = 2000 mV)	–	5.0	−5.0					4			LSD
Zero-Output Reading (V_X = 0 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0	0	–	–	LSD
Bias Current — Analog Input	–	5.0	−5.0	–	–	–	±20	±100	–	–	pA
Reference Input		5.0	−5.0	–	–	–	±20	±100	–	–	
Analog Ground		5.0	−5.0	–	–	–	±20	±500	–	–	
Common Mode Rejection (f_{clk} = 32 kHz, V_X = 1.4 V, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	65	–	–	–	dB
Input Voltage* Pins 9, 10 "0" Level	V_{IL}										V
(V_O = 4.5 or 0.5 V)		5.0	–	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}										V
(V_O = 0.5 or 4.5 V)		5.0	–	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	–	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	–	11.0	–	11.0	8.25	–	11.0	–	
Output Voltage — Pins 14 to 23											V
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	−5.0	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	−5.0	–	4.95	–	
(V_{SS} = −5.0 V) "0" Level	V_{OL}	5.0	−5.0	–	4.95	–	−5.0	−4.95	–	−4.95	
"1" Level	V_{OH}	5.0	−5.0	4.95	–	4.95	5.0	–	4.95	–	
Output Current — Pins 14 to 23											mA
(V_{SS} = 0 V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	−5.0	−0.25	–	−0.2	−0.36	–	−0.14	–	
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	−5.0	0.64	–	0.51	0.88	–	0.36	–	
(V_{SS} = −5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	−5.0	−0.62	–	−0.5	−0.9	–	−0.35	–	
(V_{OL} = −4.5 V) Sink	I_{OL}	5.0	−5.0	1.6	–	1.3	2.25	–	0.9	–	
Input Current — DU, Pin 9	I_{DU}	5.0	−5.0	–	±0.3	–	±0.00001	±0.3	–	±1.0	μA
Quiescent Current	I_Q	5.0	−5.0	–	3.7	–	0.9	2.0	–	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	−8.0	–	7.4	–	1.8	4.0	–	3.2	
DC Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{ref} = 2.000 V)	–	5.0	−5.0	–	–	–	0.5	–	–	–	mV/V

Notes: 1. Accuracy — The accuracy of the meter at full scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full scale and zero is defined as the linearity specification.

2. Symmetry — Defined as the difference between a negative and positive reading of the same voltage at or near full scale.

*Referenced to V_{SS} for Pin 9. Referenced to V_{EE} for Pin 10.

TYPICAL CHARACTERISTICS

FIGURE 1 – TYPICAL ROLLOVER ERROR versus POWER SUPPLY SKEW

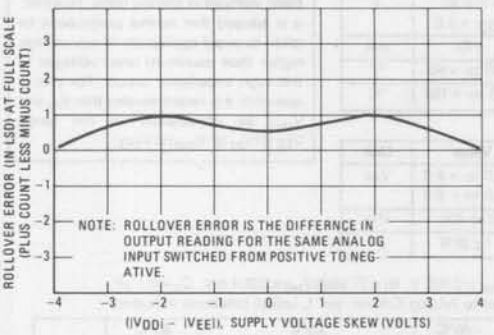


FIGURE 2 – TYPICAL QUIESCENT POWER SUPPLY CURRENT versus TEMPERATURE

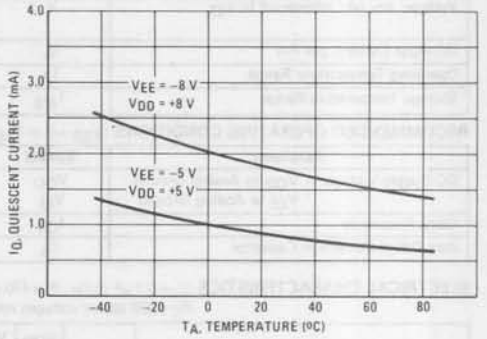


FIGURE 3 – TYPICAL N-CHANNEL SINK CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

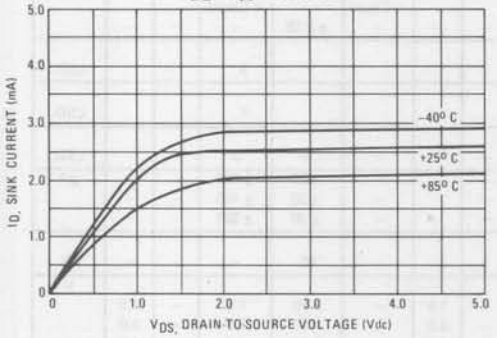


FIGURE 4 – TYPICAL P-CHANNEL SOURCE CURRENT AT $V_{DD}-V_{SS}$ = 5 VOLTS

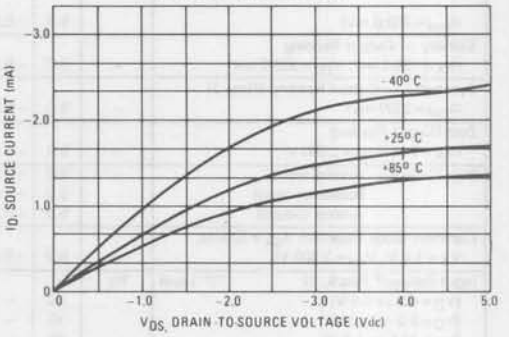


FIGURE 5 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)

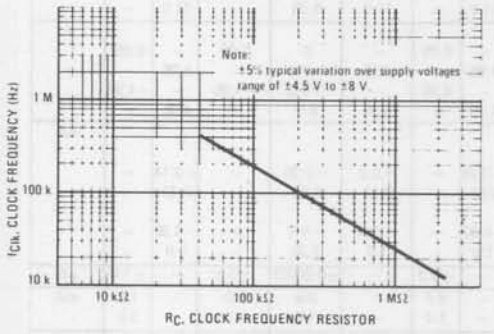
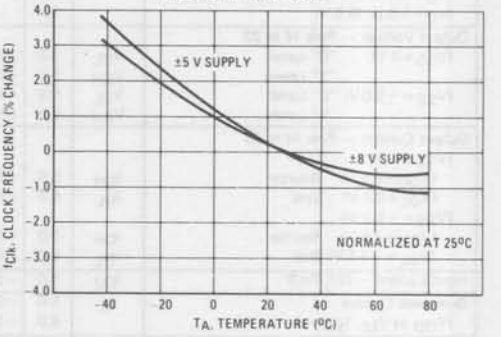


FIGURE 6 – TYPICAL % CHANGE OF CLOCK FREQUENCY versus TEMPERATURE



CONVERSION RATE = $\frac{\text{CLOCK FREQUENCY}}{16{,}400} \pm 1.5\%$
MULTIPLEX RATE = $\frac{\text{CLOCK FREQUENCY}}{80}$

PIN DESCRIPTIONS

ANALOG GROUND (V_{AG}, Pin 1)

Analog ground at this pin is the input reference level for the unknown input voltage (V_X) and reference voltage (V_{ref}). This pin is a high impedance input. The allowable operating range for V_{AG} is from V_{EE} +2.8 V to V_{DD} −4.5 V.

REFERENCE VOLTAGE (V_{ref}, Pin 2) UNKNOWN INPUT VOLTAGE (V_X, Pin 3)

This A/D system performs a ratiometric A/D conversion; that is, the unknown input voltage, V_X, is measured as a ratio of the reference voltage, V_{ref}. The full scale voltage is equal to that voltage applied to V_{ref}. Therefore, a full scale voltage of 1.999 V requires a reference voltage of 2.000 V while full scale voltage of 199.9 mV requires a reference voltage of 200 mV. Both V_X and V_{ref} are high impedance inputs. In addition to being a reference input, Pin 2 functions as a reset for the A/D converter. When Pin 2 is switched low (referenced to V_{EE}) for at least 5 clock cycles, the system is reset to the beginning of a conversion cycle.

EXTERNAL COMPONENTS (R_I, R_I/C_I, C_I; Pins 4, 5, 6)

These pins are for external components for the integration used in the dual ramp A/D conversion. A typical value for the capacitor is 0.1 μF (polystyrene or mylar) while the resistor should be 470 kΩ for 2.0 V full scale operation and 27 kΩ for 200 mV full scale operation. These values are for a 66 kHz clock frequency which will produce a conversion time of approximately 250 ms. The equations governing the calculation for the values for integrator components are as follows:

$$R_I = \frac{V_X(max)}{C_I} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X(max) - 0.5\ V$$

$$T = 4000 \times \frac{1}{f_{Clk}}$$

where:
R_I is in kΩ
V_{DD} is the voltage at Pin 24 referenced to V_{AG}
V_X is the voltage at Pin 3 referenced to V_{AG}, in V
f_{Clk} is the clock frequency at Pin 10 in kHz
C_I is in μF, ΔV is in Volts
T is the conversion time, in seconds

Example:
$C_I = 0.1\ \mu F$
$V_{DD} = 5.0$ volts
$f_{Clk} = 66$ kHz
For $V_X(max) = 2.0$ volts
$R_I = 480$ kΩ (use 470 kΩ ± 5%)
For $V_X(max) = 200$ mV
$R_I = 28$ kΩ (use 27 kΩ ± 5%)

Note that for worst case conditions, the minimum allowable value for R_I is a function of C_I min, V_{DD} min, and f_{Clk} max. The worst-case condition does not allow $\Delta V + V_X$ to exceed V_{DD}. The 0.5 V factor in the above equation for ΔV is for safety margin.

OFFSET CAPACITOR (C01, C02; Pins 7, 8)

These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF (polystyrene or mylar).

DISPLAY UPDATE INPUT (DU, Pin 9)

If a positive edge is received on this input prior to the ramp-down cycle, new data will be strobed into the output latches during that conversion cycle. When this pin is wired directly to the EOC output (Pin 14), every conversion will be displayed. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.

CLOCK (Clk I, Clk O, Pins 10, 11)

The MC14433 device contains its own oscillator system clock. A single resistor connected between pins 10 and 11 sets the clock frequency. If increased stability is desired, these pins will support a crystal or LC circuit. The clock input, Pin 10, may also be driven from an external clock source which need have only standard CMOS output drive. For external clock inputs this pin is referenced to V_{EE}. A 300 kΩ resistor results in clock frequency of about 66 kHz. (See the typical characteristic curves.) For alternate circuits see Figure 7.

NEGATIVE POWER SUPPLY (V_{EE}, Pin 12)

This is the connection for the most negative power supply voltage. The typical current is 0.8 mA. Note the current for the output drive circuit is not returned through this pin, but through Pin 13. V_X-V_{EE} should be greater than 0.8 V.

NEGATIVE POWER SUPPLY FOR OUTPUT CIRCUITRY AND INPUT DU (V_{SS}, Pin 13)

This is the low voltage level for the output pins of the MC14433 (BCD, Digit Selects, EOC, $\overline{OR}$) and the DU input. When this pin is connected to analog ground, the output voltage is from analog ground to V_{DD}. When connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The allowable operating range for V_{SS} is between V_{DD} −3.0 volts and V_{EE}.

END OF CONVERSION (EOC, Pin 14)

The EOC output produces a positive pulse at the end of each conversion cycle. This pulse width is equivalent to one half the period of the system clock (Pin 11).

OVERRANGE ($\overline{OR}$, Pin 15)

The $\overline{OR}$ pin is low when V_X exceeds V_{ref}. Normally it is high.

DIGIT SELECT (DS4, DS3, DS2, DS1; Pins 16, 17, 18, 19)

The digit select output is high when the respective digit is selected. The most significant digit (½ digit) turns on immediately after an EOC pulse followed by the remaining digits, sequencing from MSD to LSD. An interdigit blanking time of two clock periods is included to ensure that the BCD data has settled. The multiplex rate is equal to the clock frequency divided by 80. Thus with a system clock rate of 66 kHz, the multiplex rate would be 0.8 kHz. Relative timing among digital select outputs and the EOC signal is shown in the Digit Select Timing Diagram, Figure 8.

BCD DATA OUTPUTS (Q0, Q1, Q2, Q3, Pins 20, 21, 22, 23)

Multiplexed BCD outputs contain 3 full digits of information during DS2, 3, 4, while during DS1, the ½ digit, overrange, underrange and polarity are available. The adjacent truth table shows the formats of the information during DS1.

POSITIVE POWER SUPPLY (V_{DD}, Pin 24)

The most positive supply voltage pin. $V_{DD} - V_X$ should be greater than 2.5 V. $V_{DD} - V_{EE}$ should be greater than 7.8 V. V_{DD} determines V_{OH} for the digital outputs, and V_{IH} for the digital inputs.

TRUTH TABLE (DS1 = 1)

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table:

Q3 – ½ digit, low for "1", high for "0"

Q2 – Polarity: "1" = positive, "0" = negative

Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

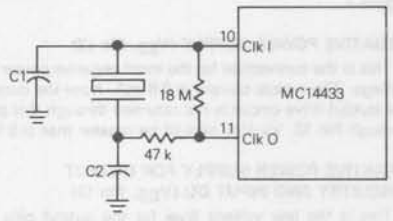
When only segment b and c of the decoder are connected to the ½ digit of the display 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

Caution: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

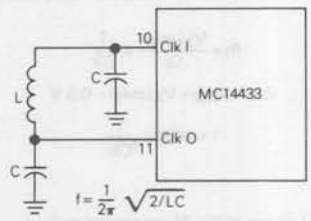
FIGURE 7 – ALTERNATE OSCILLATOR CIRCUITS

(a) Crystal Oscillator Circuit



10 pF < C1 and C2 < 200 pF

(b) LC Oscillator Circuit



For L = 5 mH and C = 0.01 μF, f ≅ 32 kHz

FIGURE 8 – DIGIT SELECT TIMING DIAGRAM

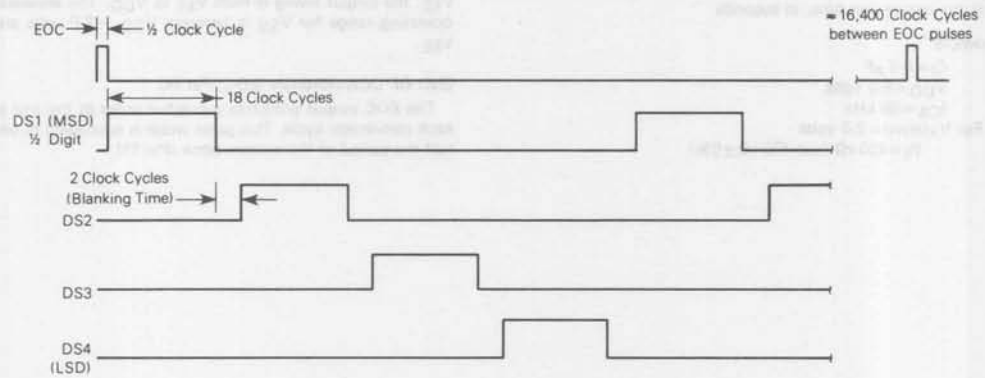


FIGURE 9 — INTEGRATOR WAVEFORMS AT PIN 6

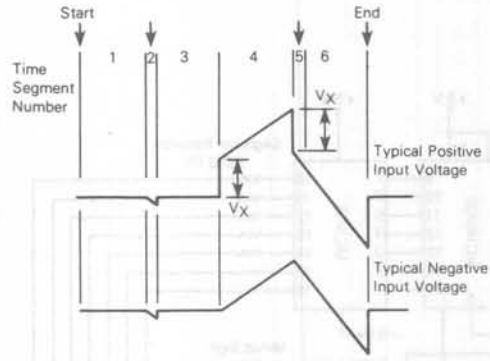
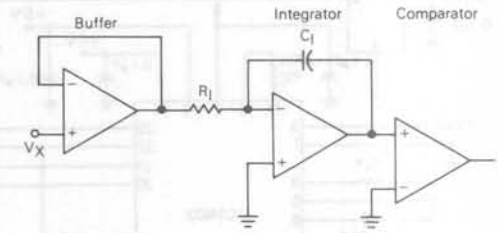


FIGURE 10 — EQUIVALENT CIRCUIT DIAGRAMS OF THE ANALOG SECTION DURING SEGMENT 4 OF THE TIMING CYCLE



CIRCUIT OPERATION

The MC14433 CMOS integrated circuit, together with a minimum number of external components, forms a modified dual ramp A/D converter. The device contains the customary CMOS digital logic providing counters, latches, and multiplexing circuitry as well as the CMOS analog circuitry providing operational amplifiers and comparators required to implement a complete single chip A/D. Autozero, high input impedances, and autopolarity are features of this system. Using CMOS technology, an A/D with a wide range of power supply voltage and low power consumption is now available with the MC14433.

During each conversion, the offset voltages of the internal amplifiers and comparators are compensated for by the system's autozero operation. Also each conversion 'ratiometrically' measures the unknown input voltage. In other words, the output reading is the ratio of the unknown voltage to the reference voltage with a ratio of 1 equal to the maximum count 1999. The entire conversion cycle requires slightly more than 16000 clock periods and may be divided into six different segments. The waveforms showing the conversion cycle with a positive input and a negative input are shown in Figure 9. The six segments of these waveforms are described below.

Segment 1 — The offset capacitor (C_O), which compensates for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. Also, the integrator capacitor is shorted. This segment requires 4000 clock periods.

Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the autozero process. The time for this segment is variable, and less than 800 clock periods.

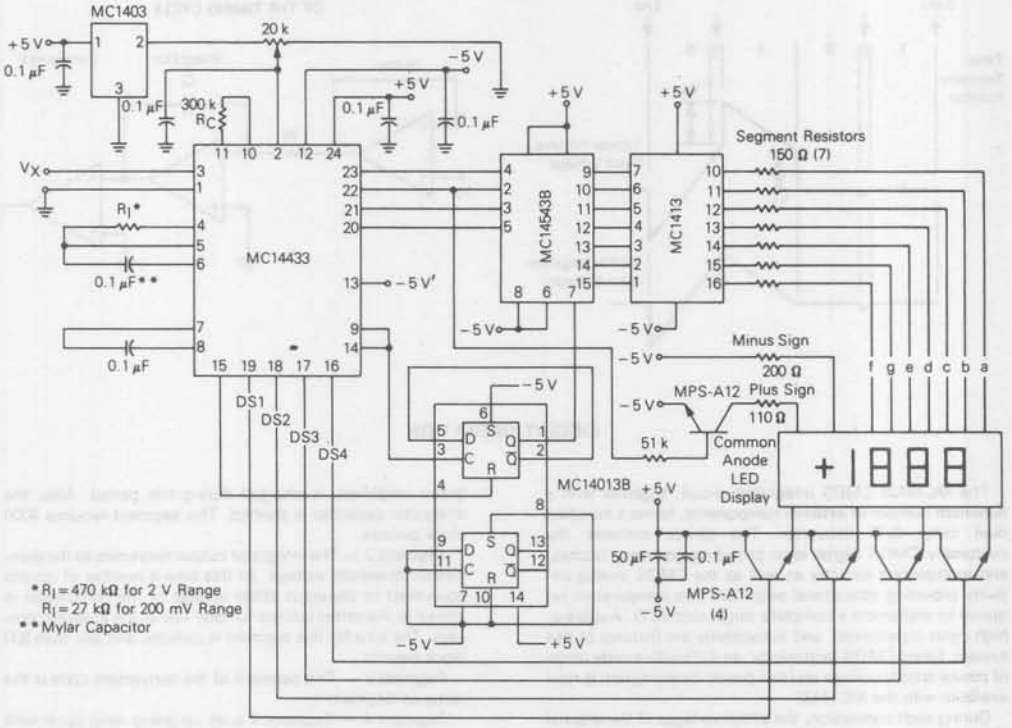
Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 4 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 10 shows the equivalent configuration of the analog section of the MC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — This segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

FIGURE 11 — 3½ DIGIT VOLTMETER—COMMON ANODE DISPLAYS, FLASHING OVERRANGE



APPLICATIONS INFORMATION

3½ DIGIT VOLTMETER — COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3½ digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 11. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

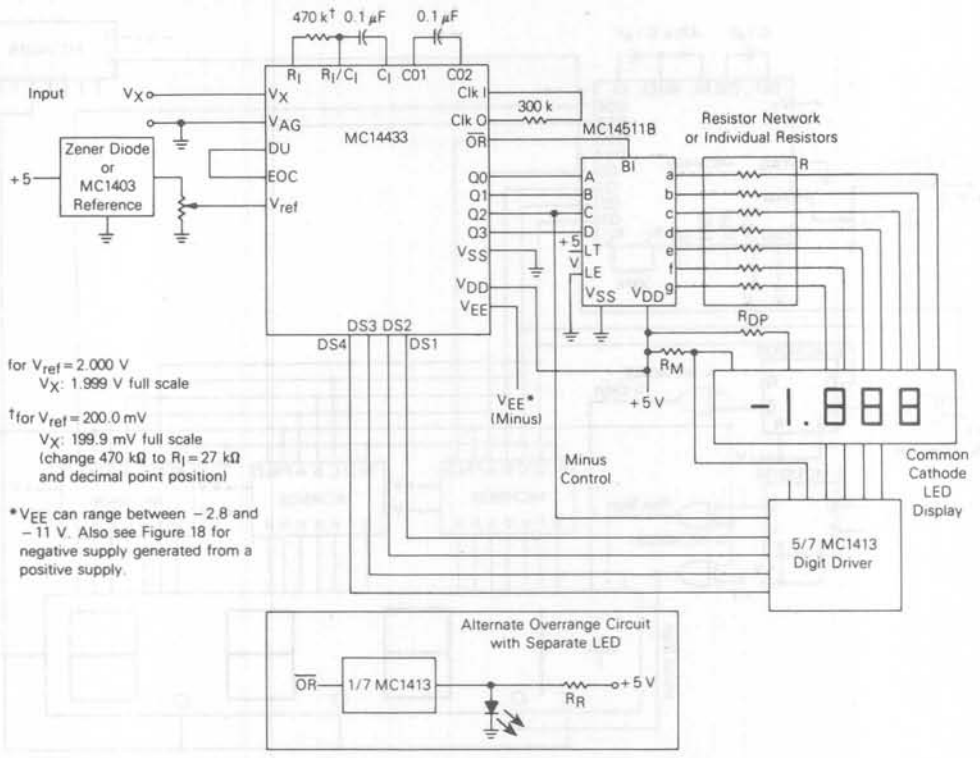
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with ½ MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in the above figure.

The power supply for the system is shown as a dual ±5 V supply. However, the MC14433 will operate over a wide range of voltages, and balance between the +5 and −5 V supplies is *not* required. See the recommended operating conditions and Figure 1.

FIGURE 12 – 3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT



3½ DIGIT VOLTMETER WITH LOW COMPONENT COUNT USING COMMON CATHODE DISPLAYS

The 3½ digit voltmeter of Figure 12 is an example of the use of the MC14433 in a system with a minimum of components. This circuit uses only 11 components in addition to the MC14433 to operate the MC14433 and drive the LED displays.

In this circuit the MC14511B provides the segment drive for the 3½ digits. The MC1413 provides sink for digit current. (The MC1413 is a device with 7 Darlingtons with common emitters.) The worst case digit current is 7 times the segment current at ¼ duty cycle. The peak segment current is limited by the value of R. The current for the display flows from V_{DD} (+5 V) to ground and does not flow through the V_{EE} (negative) supply. The minus sign is controlled by one section of the MC1413 and is turned off by shunting the current through R_M to ground, bypassing the minus sign LED. The minus sign is derived from the Q2 output. The decimal point brightness is controlled by resistor R_{DP}. Since the brightness and the type and size of LED display are the choice of the designer, the values of resistors R, R_M, R_{DP}, and R_R that govern brightness are not given.

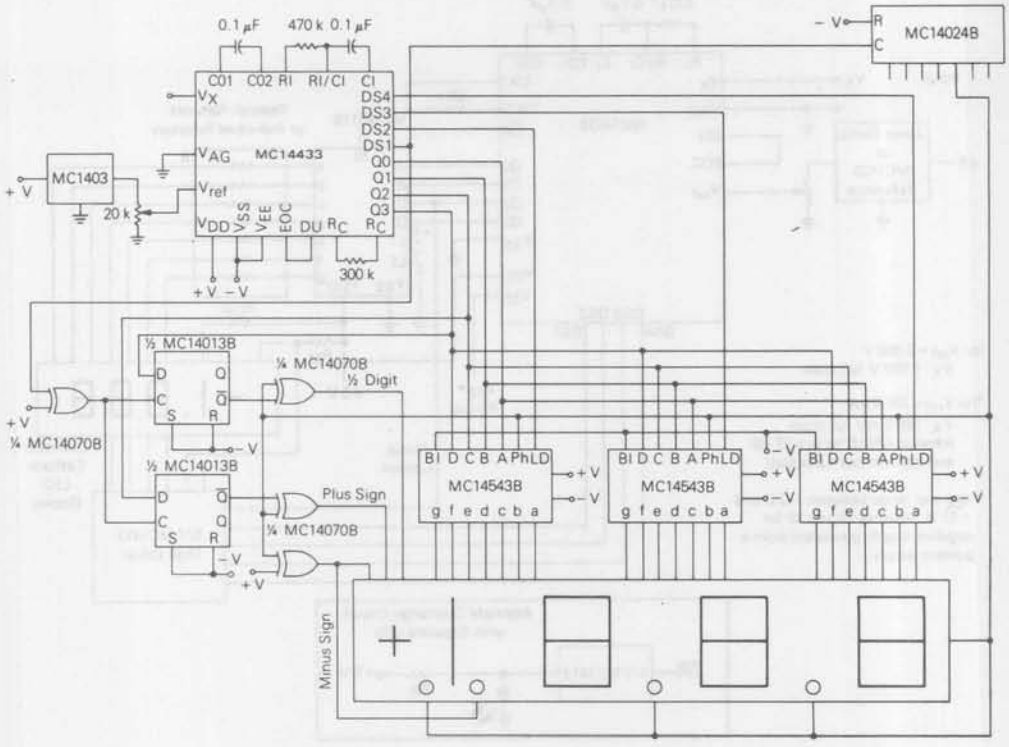
During an overrange condition the 3½ digit display is blanked at the BI pin on the MC14511B. The decimal point and minus sign will remain on during a negative overrange condition. In addition, an alternate overrange circuit with separate LED is shown.

3½ DIGIT VOLTMETER WITH LCD DISPLAY

A circuit for a 3½ digit voltmeter with a liquid crystal display is shown in Figure 13. Three MC14543B LCD latch/decoder/display drivers are used to demultiplex, decode the three digits, and drive the LCD. The half digit and polarity are demultiplexed with the MC14013B dual D flip-flop.

Since the LCD is best driven by an ac signal across the LCD, the low-frequency square wave drive for the LCD is derived from the MC14024B binary counter which divides the digit select output from the A/D. This low frequency square wave is connected to the backplane of the LCD and to the individual segments through the combination of the output cir-

FIGURE 13 – 3½ DIGIT VOLTMETER WITH LCD DISPLAY



cuitry of the MC14543B and the exclusive OR gates at the outputs of the MC14013B. Alternatively the square wave can be derived from a 50/60 Hz input signal when available.

The minus sign and the decimal point to the right of the half digit are connected to the inverted low frequency square wave signal. Unused decimal points are tied directly to the low frequency square wave.

The system shown operates from two power supplies (plus and minus). Alternatively one supply can be used when V_{SS} is connected to V_{EE}. In this case a level must be set for analog ground, V_{AG}, which must be at least 2.8 V above V_{EE}. This circuit may be implemented with a resistor network, resistor/forward-biased diode network or resistor-zener diode network. For example, a 9 V supply can be used with 3 V between V_{AG} and V_{EE}, leaving 6 V for V_{DD} to V_{AG}. This system leaves a comfortable margin for battery degeneration (end of life). Two versions of this circuit for single supply operation is shown in Figure 14.

For panel meter operation from a single 5 V supply, a negative supply can be generated as shown in Figure 18.

FIGURE 14 – TWO CIRCUITS FOR GENERATION OF V_{ref} AND V_{AG} FROM A SINGLE SUPPLY

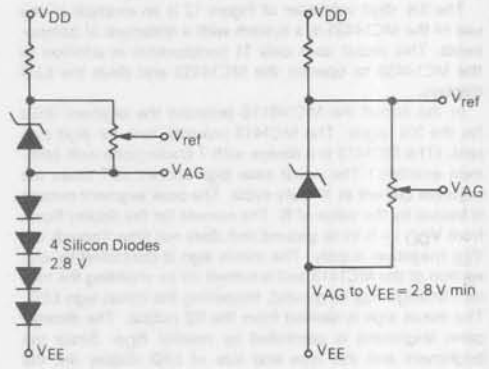
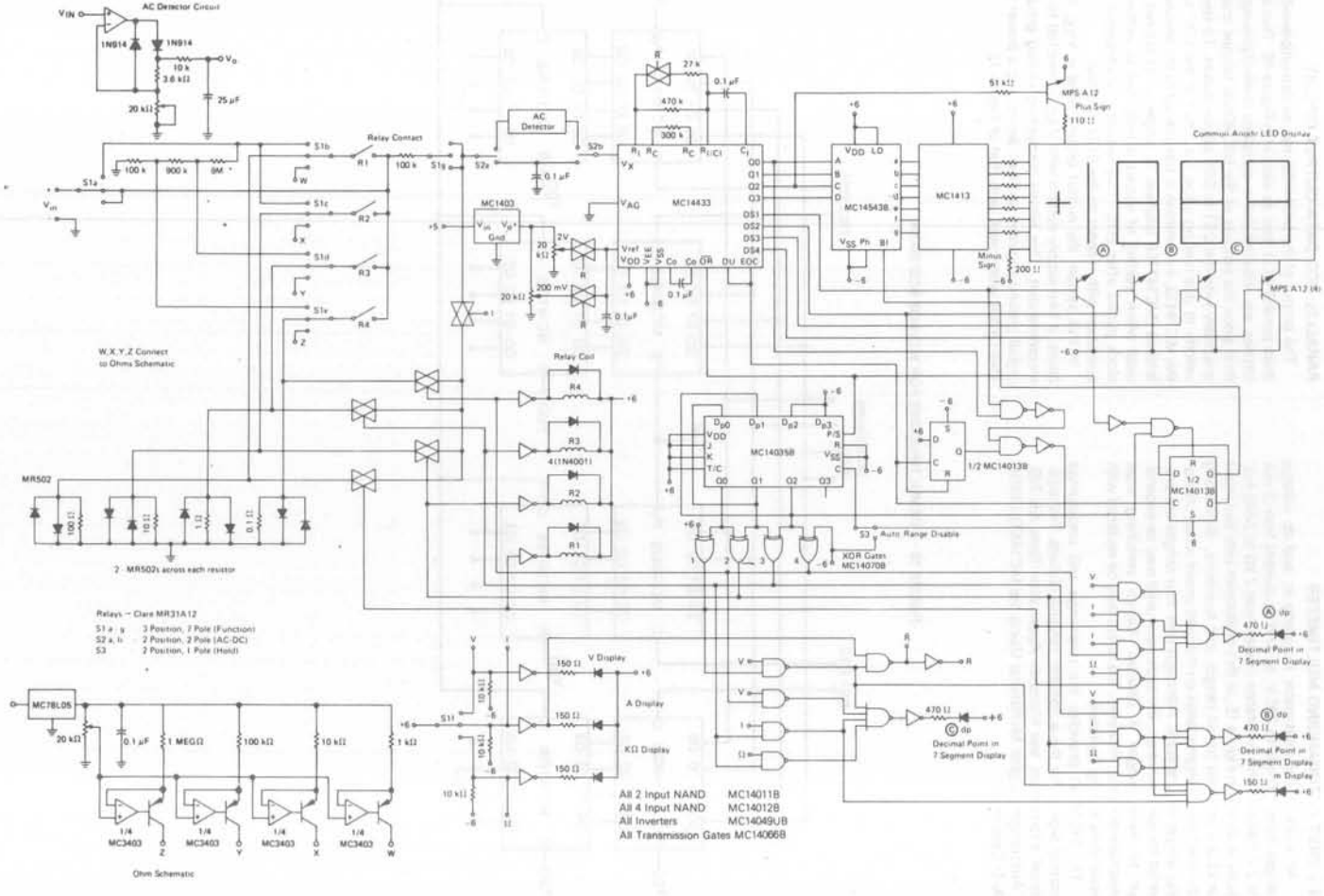


FIGURE 15 – 3½ DIGIT AUTORANGING MULTIMETER



3½ DIGIT AUTORANGING MULTIMETER

An autoranging multimeter including ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A fullscale and resistance ranges from 2 kΩ to 2 MΩ fullscale is shown in Figure 15. In this multimeter only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired. Range switching uses mechanical relays. However, the relays may be replaced with solid state analog switches.

The MC14433 provides the overrange and underrange control signals for the automatic ranging circuits. For additional information, see Motorola Application Note AN-769, "Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter."

PARALLEL BCD DATA OUTPUT CIRCUIT

The output of the MC14433 may be demultiplexed to produce parallel BCD data as shown in Figure 16. Two levels of latches are required for a complete demultiplexing of the data since the outputs of the MC14042B latches change sequentially with the DS1 to DS4 strobe pulses. To key output validity to one leading edge, i.e., that of the EOC signal of the MC14433, information is transferred to the second set of latches (MC14175B latches). A single set of latches can be used when reading of output is restricted to within 12,000 clock pulses after EOC. This requires synchronous system operation with respect to the BCD data bus.

In this system the output ground level is V_{SS}. In most cases, a two supply system with V_{SS} connected to V_{AG} is recommended. This allows connecting analog ground and digital ground together without destroying a power supply. This circuit works well with that of Figure 12.

FIGURE 16 — DEMULTIPLEXING FOR MC14433 BCD DATA

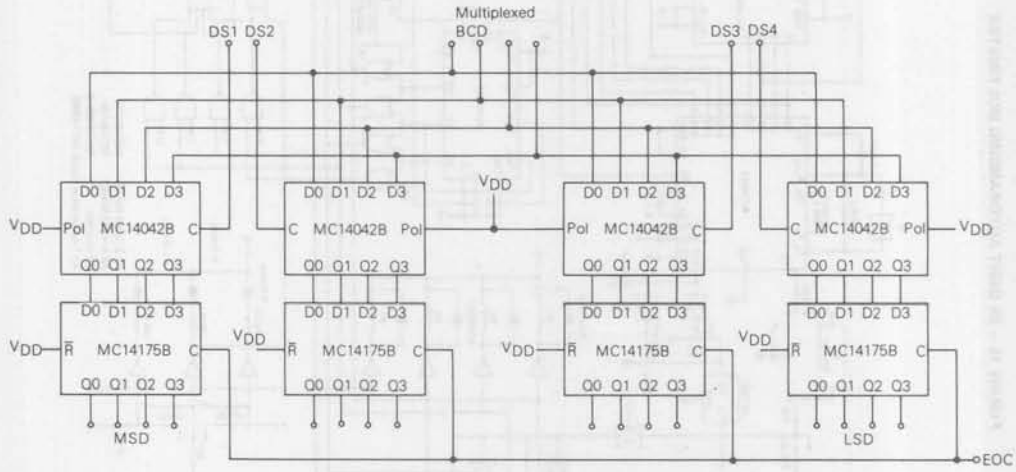
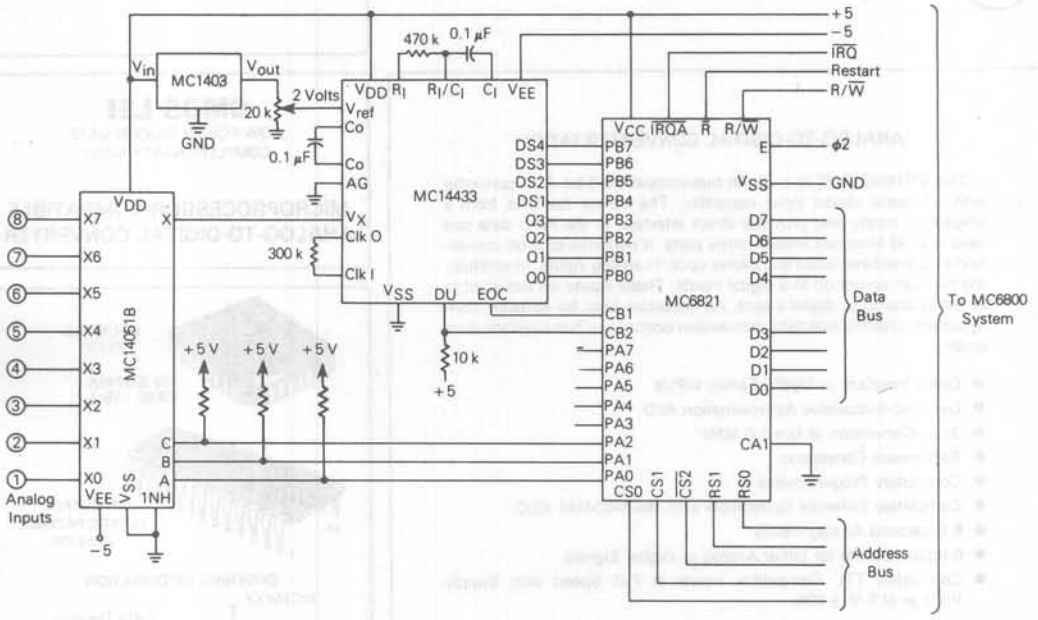


FIGURE 17 — CHANNEL DATA ACQUISITION HARDWARE

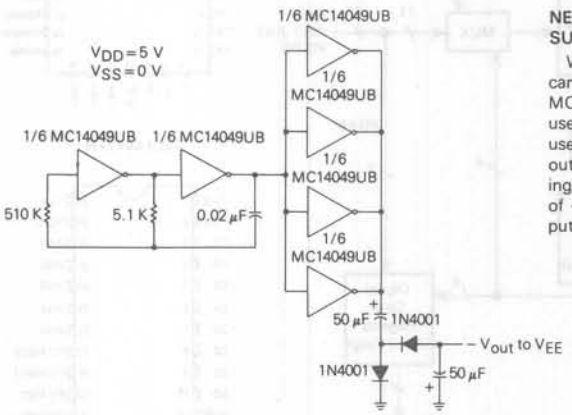


8 CHANNEL DATA ACQUISITION NETWORK

Figure 17 shows an 8-channel data acquisition network using the MC14433 and an MC6800 microprocessor system. The interface between the microprocessor data bus and the A/D system is done with an MC6821 PIA. One half of the PIA is used with the BCD and digit select outputs of the MC14433, while the second half of the PIA selects the channel to be measured via the MC14051B analog multiplexer. Control lines CB1 and CB2 are used for data flow control and are connected to DU and EOC of the MC14433.

A more detailed explanation of this system including the actual software required for the M6800 microprocessor may be found in Motorola Application Note AN-770, "Data Acquisition Networks With NMOS and CMOS."

FIGURE 18 — NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY



NEGATIVE SUPPLY GENERATED FROM POSITIVE SUPPLY

When only +5 V is available, a negative supply voltage can be generated with the circuit of Figure 18 using one MC14049UB. Two inverters from CMOS hex inverter are used as an oscillator (≈3 kHz) with the remaining inverters used as buffers for higher current output. The square wave output from the oscillator is level-translated to a negative going signal. This signal is rectified and filtered. A V_{DD} voltage of +5 V for the hex buffer will result in a −4.3 V no load output voltage while the output with a 2 mA load is ≈3.4 V.

MOTOROLA

MC14442

CMOS LSI

(LOW-POWER SILICON GATE COMPLEMENTARY MOS)

MICROPROCESSOR-COMPATIBLE ANALOG-TO-DIGITAL CONVERTER

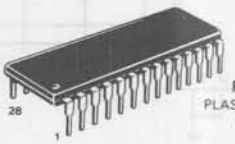
ANALOG-TO-DIGITAL CONVERTER (ADC)

The MC14442 ADC is a 28-pin bus-compatible 8-bit A/D converter with additional digital input capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles and allows up to 11 analog inputs. In addition, the part can accept up to 6 digital inputs. These inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control and bus interface is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Completely Software Compatible with the MC14444 ADC
- 5 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Speed with Supply Voltage of 5 V ± 10%

PACKAGE
PLCC

FN SUFFIX
CASE 776-1



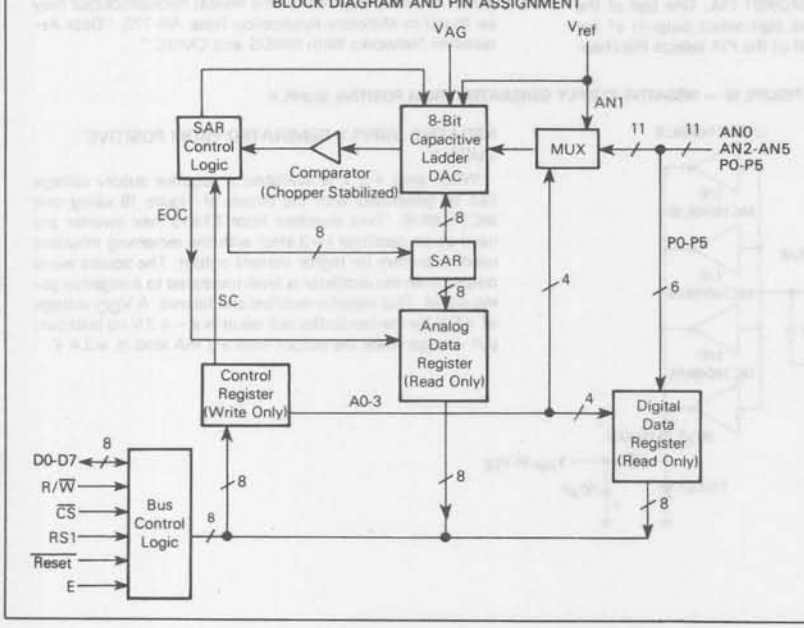
P SUFFIX
PLASTIC PACKAGE
CASE 710

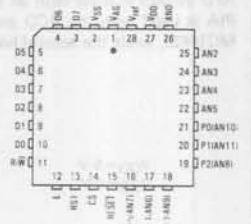
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- FN — PLCC Package
- P — Plastic Package

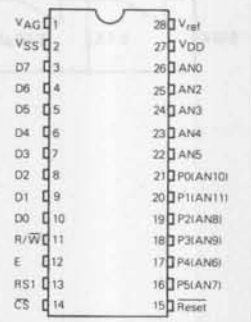
2

BLOCK DIAGRAM AND PIN ASSIGNMENT





MC14442FN



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +6.5	V
V_{in}	DC Input Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
V_{out}	DC Output Voltage (Referenced to V_{SS})	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±20	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

†Power Dissipation Temperature Derating:
Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: no derating

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5.0 V ±10%, V_{SS}=0 V, T_A=−40°C to 85°C unless otherwise noted)

Characteristic	Symbol	Conditions	Min	Max	Unit
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS1, $\overline{CS}$)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{in}=0 to 5.5 V	–	±1	μA
Data Bus (D0-D7)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Three-State (Off State) Input Leakage Current	I_{TSI}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±10	μA
Output High Voltage	V_{OH}	I_{OH}=−1.6 mA	2.4	–	V
Output Low Voltage	V_{OL}	I_{OL}=1.6 mA	–	0.4	V
Peripheral Inputs (P0-P5)					
Input High Voltage	V_{IH}		2.0	–	V
Input Low Voltage	V_{IL}		–	0.8	V
Input Leakage Current	I_{in}	V_{DD}=5.5 V, $V_{SS} \le V_{in} \le V_{DD}$	–	±1.0	μA
Current Requirements					
Supply Current	I_{DD}	V_{DD}=5.5 V	–	10	mA
Input Current, V_{ref}	I_{ref}	V_{ref}=4.5 to 5.5 V	–	800	μA

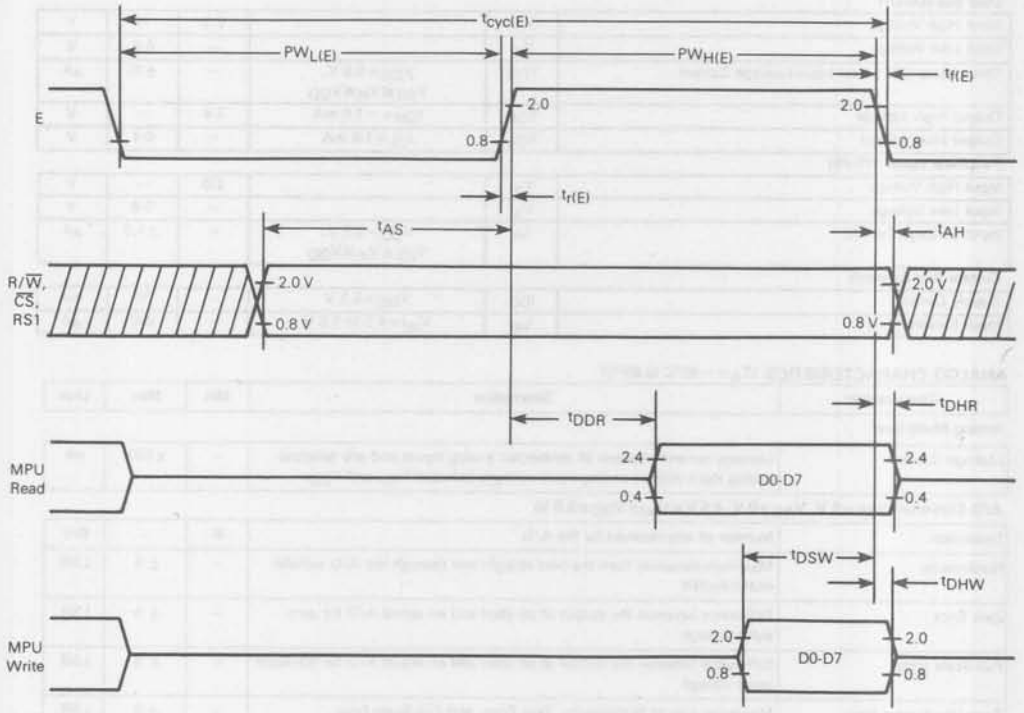
ANALOG CHARACTERISTICS (T_A=−40°C to 85°C)

Characteristic	Description	Min	Max	Unit
Analog Multiplexer				
Leakage Current	Leakage current between all deselected analog inputs and any selected analog input with all analog input voltages between V_{SS} and V_{DD}	–	±500	nA
A/D Converter (V_{SS}=0 V, V_{AG}=0 V, 4.5 V ≤ V_{ref} ≤ V_{DD} ≤ 5.5 V)				
Resolution	Number of bits resolved by the A/D	8	–	Bits
Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	–	± ½	LSB
Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	–	± ½	LSB
Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	–	± ½	LSB
Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	–	± ½	LSB
Quantization Error	Uncertainty due to converter resolution	–	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	–	±1.0	LSB
Conversion Time	Total time to perform a single analog-to-digital conversion	–	32	E cycles
Sample Acquisition Time	Time required to sample the analog input	–	12	E cycles

AC CHARACTERISTICS (T_A = −40° to 85°C) (See Figure 1)

Characteristic	Signal	Symbol	Min	Max	Unit
Enable Clock Cycle Time ($1/f_E$)	E	$t_{cyc(E)}$	943	–	ns
Enable Clock Pulse Width, High	E	$PW_{H(E)}$	440	–	ns
Enable Clock Pulse Width, Low	E	$PW_{L(E)}$	410	–	ns
Clock Rise Time	E	$t_{r(E)}$	–	25	ns
Clock Fall Time	E	$t_{f(E)}$	–	30	ns
Address Setup Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AS}	145	–	ns
Data Delay (Read)	D0-D7	t_{DDR}	–	335	ns
Data Setup (Write)	D0-D7	t_{DSW}	185	–	ns
Address Hold Time	RS1, R/$\overline{W}$, $\overline{CS}$	t_{AH}	10	–	ns
Input Data Hold Time	D0-D7	t_{DHW}	10	–	ns
Output Data Hold Time	D0-D7	t_{DHR}	10	–	ns
Input Capacitance	P0-P5, AN0-AN10,	C_{in}	–	55	pF
	R/$\overline{W}$, E, RS1, $\overline{CS}$, $\overline{RESET}$		–	15	
Three-State Output Capacitance	D0-D7	C_{out}	–	15	pF

FIGURE 1 – BUS TIMING



PIN FUNCTIONS

Pin No.	Pin Name	Function	Type
1	V_{AG}	A/D Converter Analog Ground	Supply
2	V_{SS}	Digital Ground	Supply
3	D7	Data Bus Bit 7 (MSB)	Input/Output
4	D6	Data Bus Bit 6	Input/Output
5	D5	Data Bus Bit 5	Input/Output
6	D4	Data Bus Bit 4	Input/Output
7	D3	Data Bus Bit 3	Input/Output
8	D2	Data Bus Bit 2	Input/Output
9	D1	Data Bus Bit 1	Input/Output
10	D0	Data Bus Bit 0 (LSB)	Input/Output
11	R/$\overline{W}$	Read/Write	Input
12	E	Enable Clock (ϕ2)	Input
13	RS1	Register Select	Input
14	$\overline{CS}$	Chip Select	Input
15	$\overline{Reset}$	Reset	Input
16	P5(AN7)	Digital Port or Analog Channel 7	Input
17	P4(AN6)	Digital Port or Analog Channel 6	Input
18	P3(AN9)	Digital Port or Analog Channel 9	Input
19	P2(AN8)	Digital Port or Analog Channel 8	Input
20	P1(AN11)	Digital Port or Analog Channel 11	Input
21	P0(AN10)	Digital Port or Analog Channel 10	Input
22	AN5	Analog Channel 5	Input
23	AN4	Analog Channel 4	Input
24	AN3	Analog Channel 3	Input
25	AN2	Analog Channel 2	Input
26	AN0	Analog Channel 0	Input
27	V_{DD}	Supply Voltage	Supply
28	V_{ref}	A/D Converter Positive Reference Voltage	Input

MC14442 MPU INTERFACE SIGNALS

Bidirectional Data Bus (D0-D7) – The bidirectional data lines D0-D7 comprise the bus over which data is transferred in parallel to and from the MPU. The data bus output drivers are three-state devices that remain in the high-impedence state except during an MPU read of an ADC data register.

Enable Clock (E) – The enable clock provides two functions for the MC14442. First, it serves to synchronize data transfers into and out of the ADC. The timing of all other external signals is referenced to the leading or trailing edge of the enable clock. Secondly, the enable clock is used internally to derive the necessary SAR A/D conversion clocks. Because this conversion is a dynamic process, enable clock must be a continuous signal into the ADC during an A/D conversion.

Read/Write (R/$\overline{W}$) – The R/$\overline{W}$ signal is provided to the MC14442 to control the direction of data transfers to and from the MPU. A low state on this line is required to transfer data from the MPU to the ADC control register. A high state is required on R/$\overline{W}$ to transfer data out of either of the ADC data registers.

Reset ($\overline{Reset}$) – The reset line supplies the means of externally forcing the MC14442 into a known state. When a low is applied to the $\overline{Reset}$ pin, the start conversion bit of the control register is cleared. Analog channel 0 is automatically selected by the analog multiplexer. The A/D status bit is also cleared. Any A/D results present in the Analog Data register are not affected by a reset. Reset forces the data bus output drivers to the high-impedance state. The internal byte pointer (discussed in the following pages) is set to point to the most significant byte of any subsequently selected internal register. In order to attain an internally stable reset state, the $\overline{Reset}$ pin must be low for at least one complete enable clock cycle.

Chip Select ($\overline{CS}$) – Chip select is an active-low input used by the MPU system to enable the ADC for data transfers. No data may be passed to or from the ADC through the data bus pins unless $\overline{CS}$ is in a low state. A selection of MPU address lines and the M6800 VMA signal or its equivalent should be utilized to provide chip select to the MC14442.

MC14442 ANALOG INPUTS AND DIGITAL INPUTS

(Refer to the ADC Block Diagram)

Dedicated Analog Channels (AN0, AN2-AN5) – These input pins serve as dedicated analog channels subject to A/D conversions. These channels are fed directly into the internal 12-to-1 analog multiplexer which feeds a single analog voltage to the A/D converter.

Shared Analog Channels (AN6-AN11) – These input pins are also connected to the analog multiplexer and may be used as analog channels for A/D conversion. However, these pins may also serve as digital input pins as described next.

Shared Digital Inputs (P0-P5) – P0-P5 comprise a 6-bit digital input port whose bits may also serve as analog channels. The state of these inputs may be read at any time from the ADC digital data register. The function of these pins is not programmed, but instead is simply assigned by the system designer on a pin-by-pin basis.

CAUTION: Digital values read from the P0-P5 bit locations do not guarantee the presence of true digital input levels on these pins. P0-P5 pass through a TTL-compatible input buffer and into the digital data register. These buffers are designed with enough hysteresis to prevent internal oscillations if an analog voltage between 0.8 and 2 V is present on one or more of these six pins.

MC14442 SUPPLY VOLTAGE PINS

Positive Supply Voltage (V_{DD}) – V_{DD} is used internally to supply power to all digital logic and to the chopper stabilized comparator. Because the output buffers connected to this supply must drive capacitive loads, ac noise on this supply line is unavoidable internally. Analog circuits using this supply within the MC14442 were designed with high V_{DD} supply rejection; however, it is recommended that a filtering capacitance be used externally between V_{DD} and V_{SS} to filter noise caused by transient current spikes.

Ground Supply Voltage (V_{SS}) – V_{SS} should be tied to system digital ground or the negative terminal of the V_{DD} power source. Again, the output buffers cause internal noise on this supply, so analog circuits were designed with high V_{SS} rejection.

Positive A/D Reference Voltage (V_{ref}) – This is the voltage used internally to provide references to the analog comparator and the digital-to-analog converter used by the SAR A/D. The analog-to-digital conversion result will be ratiometric to $V_{ref} - V_{AG}$ (full scale). Hence V_{ref} should be a very noise-free supply. Ideally V_{ref} should be single-point connected to the voltage supply driving the system's transducers. V_{ref} may be connected to V_{DD}, but degradation of absolute A/D accuracy may result due to switching noise on V_{DD}.

A/D Ground Reference Voltage (V_{AG}) – This supply is the ground reference for the internal DAC and several reference voltages supplied to the comparator. It should also be noise-free to guarantee A/D accuracy. Absolute accuracy may be degraded if V_{AG} is wired to V_{SS} at the ADC package unless V_{SS} has been sufficiently filtered to remove switching noise. Ideally V_{AG} should be single-point grounded to the system analog ground supply.

MC14442 INTERNAL REGISTERS

The MC14442 ADC has three 16-bit internal registers. Each register is divided into two 8-bit bytes: a most significant (MS) byte (bits 8-15) and a least significant (LS) byte (bits 0-7). Each of these bytes may not be addressed externally, but instead are normally addressed by a single 16-bit instruction such as the M6800 LDX instruction. An internal byte pointer selects the appropriate register byte during the two E cycles of a normal 16-bit access. In keeping with the M6800 X register format, the pointer points first to the MS byte of any selected register. After the E cycle in which the MS byte is accessed, the pointer will switch to the LS byte and remain there for as long as chip select is low. The pointer moves back to the MS byte on the falling edge of E after the first complete E cycle in which the ADC is not selected. (See Figure 2a for more detail.) The MS byte of any register may also be accessed by a simple 8-bit instruction as shown in Figure 2b. However, the LS byte of all registers may be accessed only by 16-bit instructions as described above. By connecting the ADC register select (RS1) to the MPU address line A1, the three registers may be accessed sequentially by 16-bit operations.

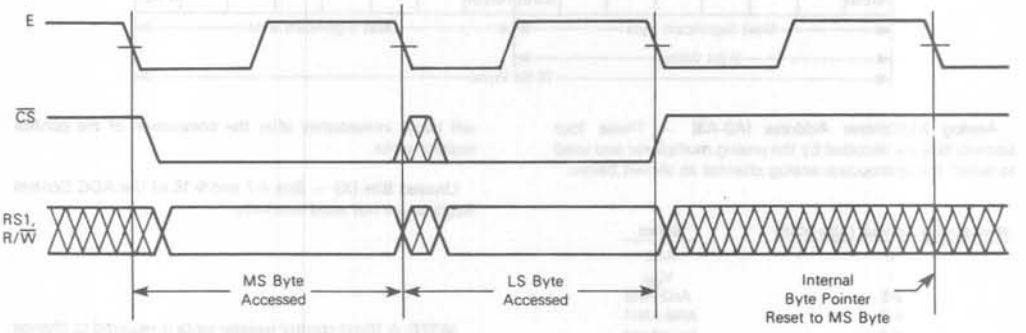
CAUTION: RS1 should **not** be connected to address line A0 and the addressing of the ADC should be such that RS1 does not change states during a 16-bit access.

INTERNAL REGISTER ADDRESSING

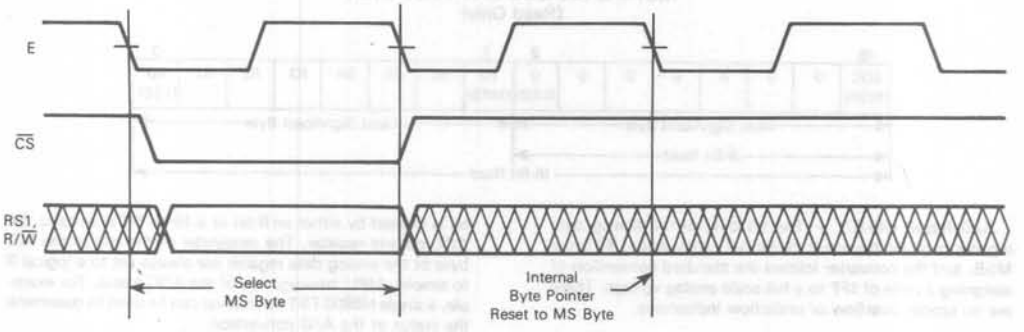
Addressing Signals				
$\overline{Reset}$	$\overline{CS}$	R/$\overline{W}$	RS1	ADC Response
0	X	X	X	Reset
1	0	0	0	No Response
1	0	0	1	MPU Write to Control Register
1	0	1	0	MPU Read from Analog Data Register
1	0	1	1	MPU Read from Digital Data Register
1	1	X	X	Chip Deselected (No Response)

FIGURE 2 — ADC ACCESS TIMING

a — Typical 16-Bit ADC Access

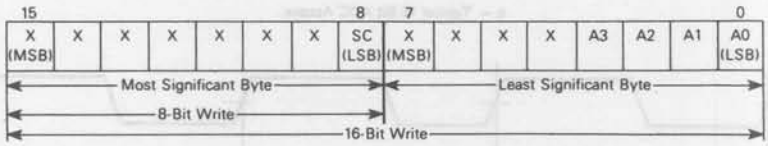


b — Typical 8-Bit ADC Access



2

MC14442 CONTROL REGISTER
(Write Only)



Analog Multiplexer Address (A0-A3) – These four address bits are decoded by the analog multiplexer and used to select the appropriate analog channel as shown below.

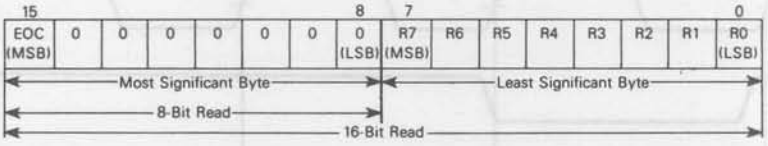
Hexadecimal Address (A3 = MSB)	Select
0	AN0
1	V_{ref}
2-5	AN2-AN5
6-B	AN6-AN11
C-F	Undefined

Start A/D Conversion (SC) – When the SC bit is set to a logical 1, an A/D conversion on the specified analog channel will begin immediately after the completion of the control register write.

Unused Bits (X) – Bits 4-7 and 9-15 of the ADC Control Register are not used internally.

NOTE: A 16-bit control register write is required to change the analog multiplexer address. However, 8-bit writes to the MC14442 can be used to initiate an A/D conversion if the analog MUX is already selecting the desired channel. This is useful when repeated conversions on a particular analog channel are necessary.

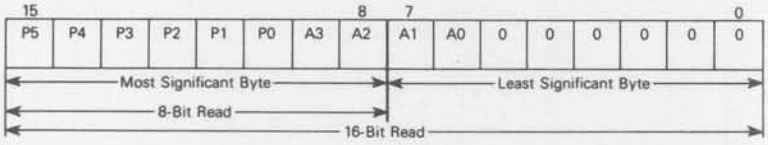
MC14442 ANALOG DATA REGISTER
(Read Only)



A/D Result (R0-R7) – The LS byte of the analog data register contains the result of the A/D conversion. R7 is the MSB, and the converter follows the standard convention of assigning a code of $FF to a full-scale analog voltage. There are no special overflow or underflow indications.

A/D Status (EOC) – The A/D status bit is set whenever a conversion is successfully completed by the ADC. The status bit is cleared by either an 8-bit or a 16-bit MPU write to the ADC control register. The remainder of the bits in the MS byte of the analog data register are always set to a logical 0 to simplify MPU interrogation of the ADC status. For example, a single M6800 TST instruction can be used to determine the status of the A/D conversion.

MC14442 DIGITAL DATA REGISTER
(Read Only)



Logical Zero (0) – These bits are always read as logical zero.

Analog Multiplexer Address (A0-A3) – The number of the analog channel presently addressed is given by these bits.

Shared Digital Port (P0-P5) – The voltage present on these pins is interpreted as a digital signal and the corresponding states are read from these bits.

WARNING: A digital value will be given for each pin even if some or all of the pins are being used as analog inputs.

ANALOG SUBSYSTEM
(See Block Diagram)

General Description

The analog subsystem of the MC14442 is composed of a 12-channel analog multiplexer, an 8-bit capacitive DAC (digital-to-analog converter), a chopper-stabilized comparator, a successive approximation register, and the necessary control logic to generate a successive approximation routine.

The analog multiplexer selects one of twelve channels and directs it to the input of the capacitive DAC. A fully-capacitive DAC is utilized because of the excellent matching characteristics of thin-oxide capacitors in the silicon-gate CMOS process. The DAC actually serves several functions. During the sample phase, the analog input voltage is applied to the DAC which acts as a sample-and-hold circuit. During the conversion phase, the capacitor array serves as a digital-to-analog converter. The comparator is the heart of the ADC; it compares the unknown analog input to the output of the DAC, which is driven by a conventional successive-approximation register. The chopper-stabilized comparator was designed for low offset voltage characteristics as well as V_{DD} and V_{SS} power supply rejection.

Device Operation

An A/D conversion is initiated by writing a logical 1 into the SC bit of the ADC control register. The MC14442 allows 2 enable clock cycles for the write into the control register even if only one byte is written. In this case, the second E cycle does not affect any internal registers. During the next 12½ enable cycles following a write command, the analog multiplexer channel is selected and the analog input voltage is stored on the sample and hold DAC. It is recommended that an input source impedance of 10 KΩ or less be used to allow complete charging of the capacitive DAC.

During cycle 13 the A/D is disconnected from the multiplexer output and the successive approximation A/D routine begins. Since the analog input voltage is being held on an internal capacitor for the entire conversion period, it is required that the enable clock run continuously until the A/D conversion is completed. The new 8-bit result is latched into the analog data register on the rising edge of cycle 32. At this point the end of conversion bit (EOC) is set in the analog data register MS byte. (See Figure 3, A/D Timing Sequence.)

NOTE: The digital data register or the analog data register may be read even if an A/D conversion is in progress. If the analog data register is read during an A/D conversion, valid results from the previous conversion are obtained. However, the EOC bit will be clear (logic 0) if an A/D conversion is in progress.

2

FIGURE 3 – A/D TIMING SEQUENCE

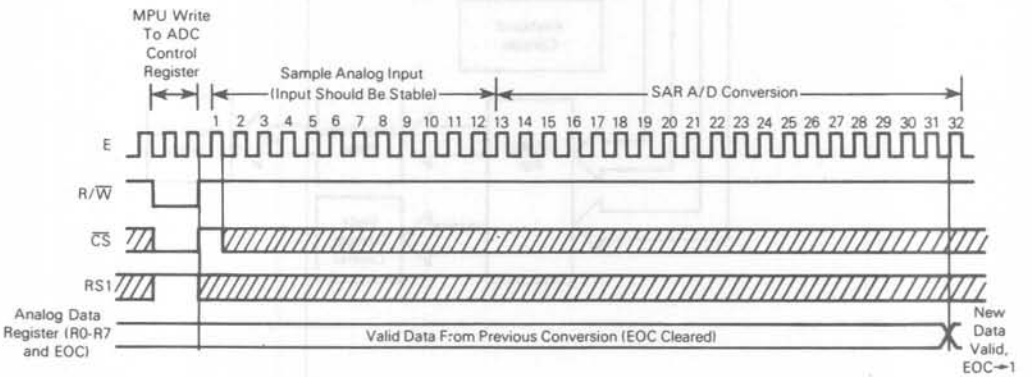
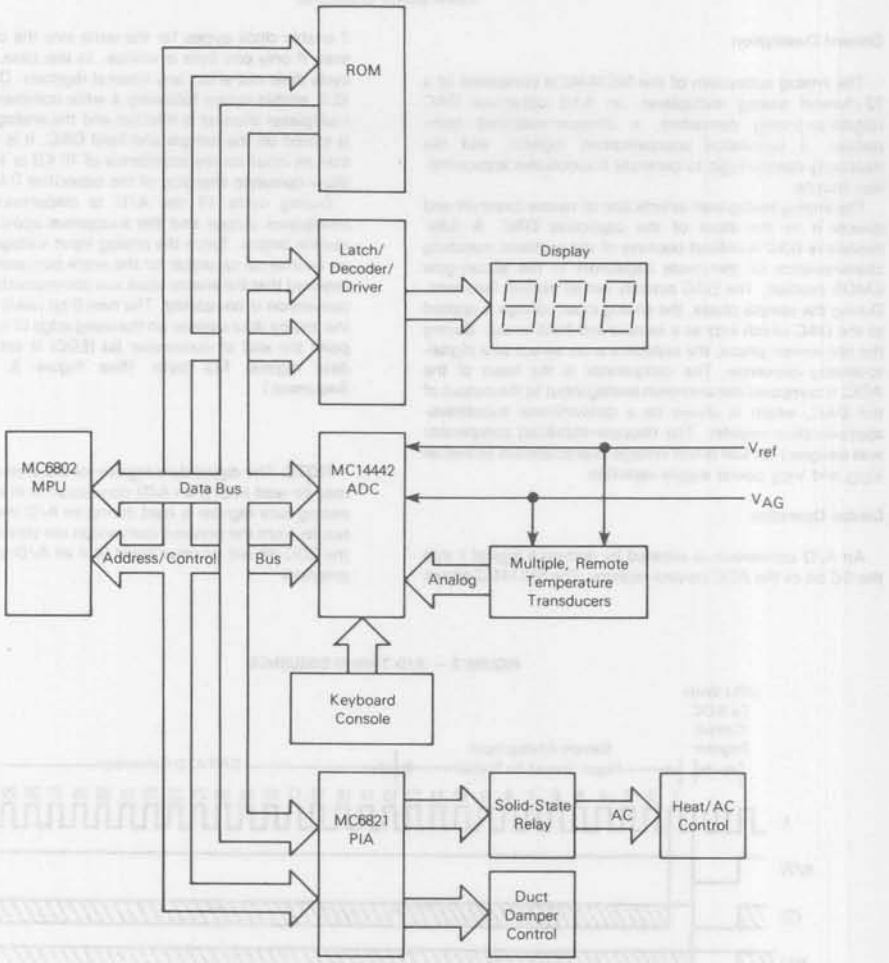


FIGURE 4 – TYPICAL MC14442 APPLICATION IN A CLIMATE CONTROLLER



MOTOROLA

MC14443
MC14447

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

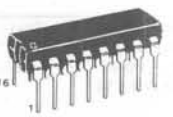
MICROPROCESSOR-BASED ANALOG-TO-DIGITAL CONVERTER

ANALOG-TO-DIGITAL CONVERTER LINEAR SUBSYSTEM

The MC14443 and the MC14447 are 6-channel, single-slope, 8-10 bit analog-to-digital converter linear subsystems for microprocessor-based data and control systems. Contained in both devices are a one-of-8 decoder, an 8-channel analog multiplexer, a buffer amplifier, a precision voltage-to-current converter, a ramp start circuit, and a comparator. The output driver of the MC14443's comparator is an open-drain N-channel which provides a sinking current. The output driver of the MC14447's comparator is a standard B-Series P-Channel, N-Channel pair.

A processor system (such as the MC141000 or MC146805) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog-to-digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at $V_{DD} = 5$ V
- Single Supply Operation +4.5 to +18 Volts
- Direct Interface to CMOS MPUs
- Typical Resolution — 8 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error
- Analog Input Voltage Range: V_{SS} to V_{DD} — 2 V
- Chip Complexity: MC14443 — 150 FETs
  MC14447 — 151 FETs

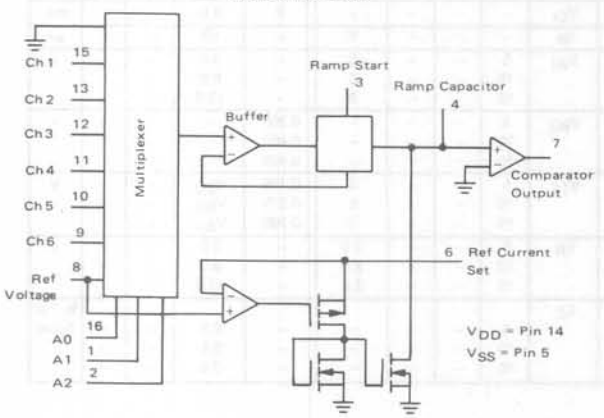


P SUFFIX
PLASTIC PACKAGE
CASE 648

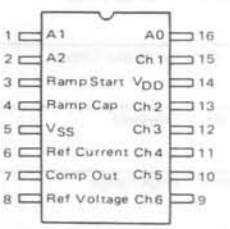
ORDERING INFORMATION

MC14XXX — Suffix Denotes
P Plastic Package

BLOCK DIAGRAM



PIN ASSIGNMENT



2

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +18	V
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD}+0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS (Voltage Referenced to V_{SS})

Characteristic	Symbol	V_{DD} V	−40°C Min	−40°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Max	Unit
Output Voltage—Comparator "0" Level	V_{OL}	5.0	–	0.05	–	0.01	0.05	–	0.05	V
V_{in} @ Pin 4 = 0 V		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 1.0 V "1" Level	V_{OH}	5.0	4.95	–	4.95	4.99	–	4.95	–	V
(R_{puliup} = 10 kΩ, MC14443 only)		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0" Level	V_{IL}									V
(V_O = 4.5 or 0.5 V)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 V)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 V)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									V
(V_O = 0.5 or 4.5 V)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 V)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 V)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current—Comparator	I_{OH}									mA
V_{in} @ Pin 4 = 1.0 V (MC14447 only)										
(V_{OH} = 2.5 V)		5.0	−2.5	–	−2.1	−4.2	–	−1.7	–	
(V_{OH} = 4.6 V)		5.0	−0.52	–	−0.44	−0.88	–	−0.36	–	
(V_{OH} = 9.5 V)		10	−1.3	–	−1.1	−2.25	–	−0.9	–	
(V_{OH} = 13.5 V)		15	−3.6	–	−3.0	−8.8	–	−2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mA
(V_{OL} = 0.4 V)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 V)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 V)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current—Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μA
Input Current—Analog Inputs	I_{in}	15	–	–	–	±0.1	±50	–	–	nA
Input Capacitance—Address, Ramp Start	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
V_{in} = 0 V										
Quiescent Current	I_{DD}	5	–	–	–	0.8	1.5	–	–	mA
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	3.0	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mV
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μA
Channel Input Voltage Range	V_{AI}	5	–	–	0	–	3.0	–	–	V
		10	–	–	0	–	8.0	–	–	
		15	–	–	0	–	13.0	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	V
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	0	0.195	V_{BO}	–	–	V
		10	–	–	0	0.275	V_{BO}	–	–	
		15	–	–	0	0.290	V_{BO}	–	–	
Reference Voltage Range	V_R	5	–	–	2.0	–	3.0	–	–	V
		10	–	–	2.0	–	8.0	–	–	
		15	–	–	2.0	–	13.0	–	–	
Conversion Linearity	L_C									% Full
C > 100 pF, V_{AI} = 0 to 2.5 V, V_{ref} = 2.5 V		5	–	–	–	–	0.5	–	–	Scale
V_{AI} = 0 to 7.0 V, V_{ref} = 7.0 V		10	–	–	–	–	0.5	–	–	
V_{AI} = 0 to 12.0 V, V_{ref} = 12.0 V		15	–	–	–	–	0.5	–	–	

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic		Symbol	V_{DD} V	Min	Typ	Max	Unit
Output Rise Time—Comparator	(MC14447 only)	t_{TLH}	5.0	–	120	240	ns
			10	–	75	150	
			15	–	65	130	
Output Fall Time—Comparator		t_{THL}	5.0	–	250	500	ns
			10	–	350	700	
			15	–	650	1300	
Propagation Delay Time—Comparator	MC14443 (R_L = 10 k to V_{DD})	t_{PLH}	5.0	–	550	1100	ns
			10	–	500	1000	
			15	–	550	1100	
		t_{PHL}	5.0	–	350	700	ns
			10	–	300	600	
			15	–	300	600	
	MC14447	t_{PLH}	5.0	–	600	1200	ns
			10	–	475	950	
			15	–	500	1000	
		t_{PHL}	5.0	–	450	980	ns
			10	–	540	1080	
			15	–	750	1500	
Multiplexer Propagation Delay		t_M	5.0	–	180	360	ns
			10	–	125	250	
			15	–	110	220	
Ramp Start Delay Time		t_{TS}	5.0	–	40	80	ns
			10	–	25	50	
			15	–	20	40	
Acquisition Time* C = 1000 pF R_{ref} = 100 kΩ		t_A	5.0	–	30	60	μs
			10	–	15	30	
			15	–	14	28	

* Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

2

PIN DESCRIPTIONS

A2, A1, A0, ANALOG MUX ADDRESS INPUTS (PINS 2, 1, 16) — These inputs determine the input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 2.

Ramp Start, RAMP START (PIN 3) — When Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When Ramp Start is brought high, the connection to the input channel is broken and the capacitor begins to ramp toward V_{SS}. See Figure 4.

Ramp Cap, RAMP CAPACITOR (PIN 4) — The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current. A polystyrene or mylar capacitor is recommended. The value should be ≥ 100 pF so that the board and stray capacitances have negligible effects. Large values of capacitance with the associated large leakage currents are not recommended because the leakage current must be insignificant in comparison to the minimum reference current (10 μA).

V_{SS}, NEGATIVE POWER SUPPLY (PIN 5) — This is system ground.

Ref Current, REFERENCE CURRENT (PIN 6) — To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{ref}) to a positive supply from Pin 6. Typical current is equal to $(V_{DD} - V_{ref})/R_{ref}$.

Comp Out, COMPARATOR OUTPUT (PIN 7) — This output is low when the capacitor has reached the discharged voltage and is high otherwise. The MC14443 requires a pull-up resistor on Pin 7 due to the open-drain configuration. The MC14447 does not require a pull-up resistor.

Ref Voltage, REFERENCE VOLTAGE (PIN 8) — This is the known voltage to which the unknown is compared.

INPUT CHANNELS (PINS 9, 10, 11, 12, 13, 15) — Input channels 1 through 6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

V_{DD}, POSITIVE POWER SUPPLY (PIN 14) — This pin is the package positive power supply pin.

FIGURE 1 – VOLTAGE TO PULSE WIDTH CONVERSION

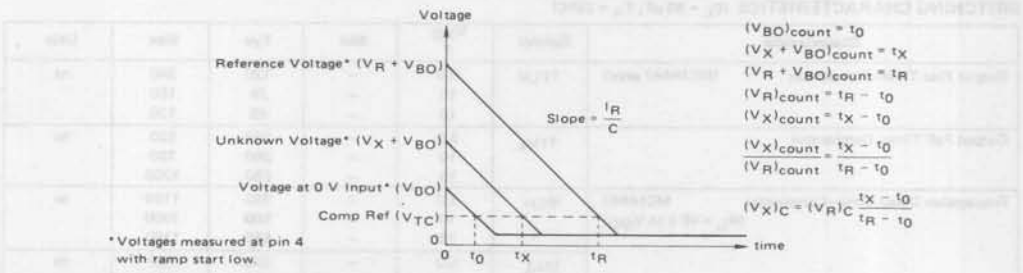


FIGURE 2 – TRUTH TABLE

A2	A1	A0	Input Selected	
0	0	0	V_{SS}	Channel 0 (ground)
0	0	1	Ch1	Channel 1
0	1	0	Ch2	Channel 2
0	1	1	Ch3	Channel 3
1	0	0	Ch4	Channel 4
1	0	1	Ch5	Channel 5
1	1	0	Ch6	Channel 6
1	1	1	V_{ref}	Channel 7 (External Reference)

FIGURE 3 – TYPICAL APPLICATIONS CIRCUIT

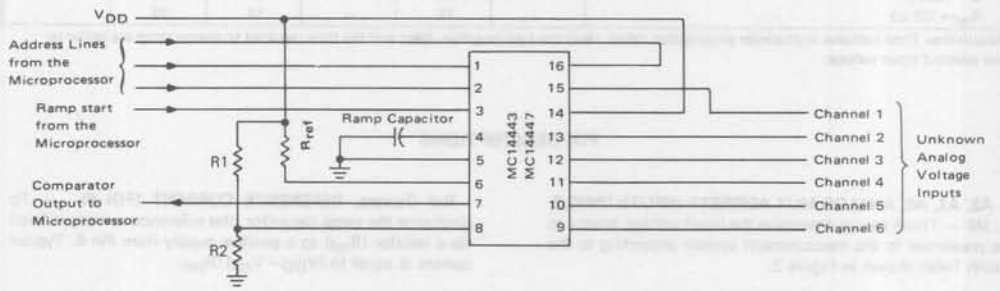


FIGURE 4 – SOFTWARE FLOW (CONVERSION SEQUENCE)

Step No.	A2	A1	A0	Ramp Start	Comment
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)
2.	1	1	1	1	Record time until Pin 7 goes low
3.	0	0	0	0	Channel 0 Selected (Ground)
4.	0	0	0	1	Record time until Pin 7 goes low
5.	0	0	1	0	Channel 1 Selected
6.	0	0	1	1	Record time until Pin 7 goes low
Calculate $t_{Ch7} - t_{Ch0} = t_{Ch7}'$ Step 2 – Step 4					
Calculate $t_{Ch1} - t_{Ch0} = t_{Ch1}'$ Step 6 – Step 4					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch1}'/t_{Ch7}')$*					
7.	0	1	0	0	Channel 2 Selected
8.	0	1	0	1	Record time until Pin 7 goes low
Calculate $t_{Ch2} - t_{Ch0} = t_{Ch2}'$					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch2}'/t_{Ch7}')$†					
etc.					

*Weighting of the analog signal on Channel 1.
†Weighting of the analog signal on Channel 2.

MOTOROLA

MC14444

CMO

(LOW-POW GATE
COMPL MOS)

MICROPRO -COMPATIBLE
ANALOG TAL CONVERTER

ANALOG-TO-DIGITAL CONVERTER (ADC)

The MC14444 ADC is a 40-pin bus-compatible 8-bit A/D converter with additional digital I/O capability. The device operates from a single 5 V supply and provides direct interface to the MPU data bus used with all Motorola M6800 family parts. It performs an 8-bit conversion in 32 machine cycles at 1 MHz and allows for up to 15 analog inputs. In addition, the part has a 3-bit digital I/O port and can accept up to 9 digital inputs. Six of these inputs are designed to be either analog or digital inputs. All necessary logic for software configuration, channel selection, conversion control, bus interface and maskable interrupt capability is included.

- Direct Interface to M6800 Family MPUs
- Dynamic Successive Approximation A/D
- 32 μs Conversion at f_E = 1.0 MHz
- Ratiometric Conversion
- Completely Programmable
- Polled or Interrupt Driven Operation
- 3 Dedicated Digital Inputs
- 3-Bit Digital I/O Port
- 9 Dedicated Analog Inputs
- 6 Inputs Usable for Either Analog or Digital Signals
- Completely TTL Compatible Inputs at Full Spe pply Voltage of 5 V ± 10%

P SUFFIX
PLASTIC PACKAGE
CASE 711

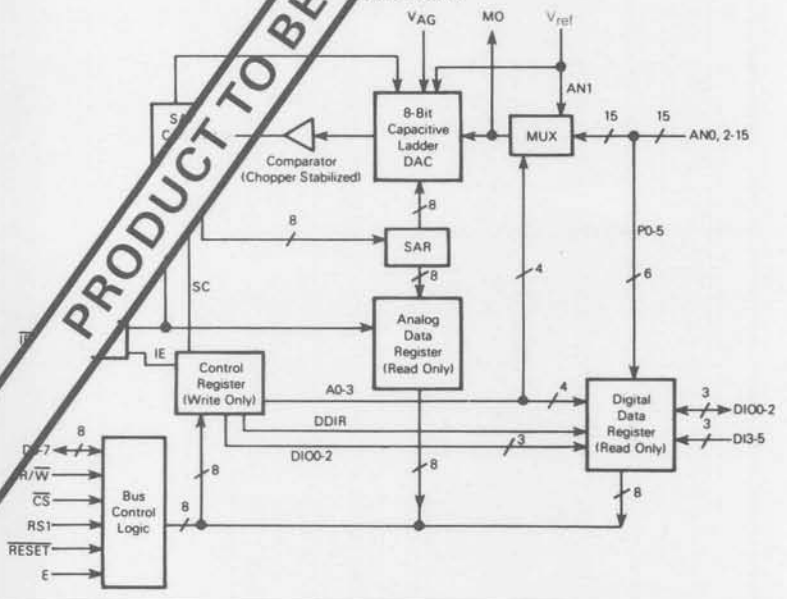
ORDERING INFORMATION

MC14XXX

	Suffix Denotes
L	Ceramic Package
P	Plastic Package

2

CK DIAGRAM



MOTOROLA

MC144110/1

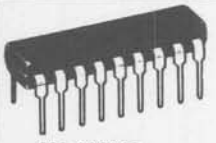
CMOS

QUAD & HEX
D/A CONVERTERS

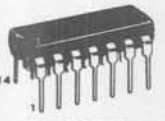
QUAD & HEX D/A CONVERTERS

The MC 144110 and MC 144111 are hex and quad static, D/A converters realised in CMOS technology. Each converter, featuring 6-bit resolution, consists of a 6-bit shift register, 6-bit latch and a static D/A converter.

- 4/6 direct R-2R network outputs
- 4/6 emitter follower outputs
- MPU compatible input levels
- Serial data input
- Data cascade output
- Wide operating voltage range of 4.5 to 15 Vdc



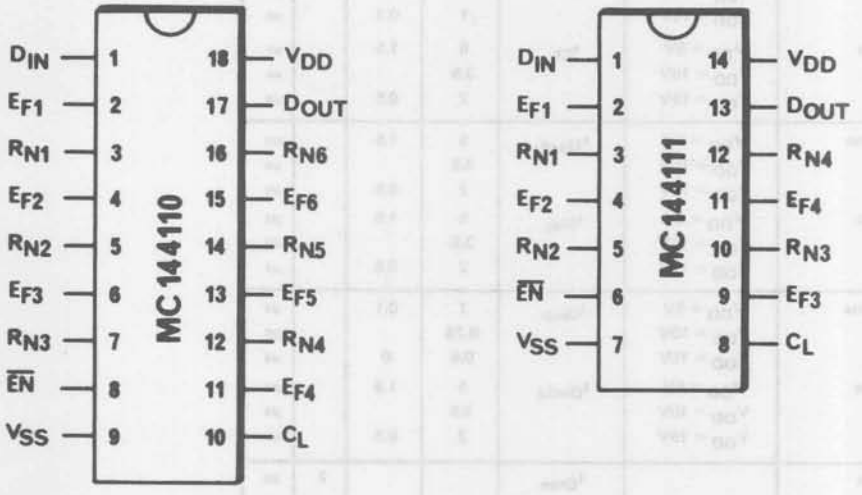
MC 144110
P SUFFIX
PLASTIC PACKAGE
CASE 707-02



MC 144111
PLASTIC PACKAGE
CASE 646 (TO-116)

2

FIGURE 1 – PIN ASSIGNMENTS



Issue 4

MAXIMUM RATINGS ($T_A = 25\,^{\circ}C$)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to −0.5	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
Input Current, All Inputs	I_{in}	10	mAdc
Operating Temperature Range	T_A	0 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

2

SWITCHING CHARACTERISTICS ($T_A = 0 \ldots 85\,^{\circ}C$)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Clock high time	V_{DD} = 5V	t_{CH}	2	0.2		µs
	V_{DD} = 10V		1.5			µs
	V_{DD} = 15V		1	0.1		µs
Clock low time	V_{DD} = 5V	t_{CL}	5	1.5		µs
	V_{DD} = 10V		3.5			µs
	V_{DD} = 15V		2	0.5		µs
Enable lead time	V_{DD} = 5V	t_{Elead}	5	1.5		µs
	V_{DD} = 10V		3.5			µs
	V_{DD} = 15V		2	0.5		µs
Enable lag time	V_{DD} = 5V	t_{Elag}	5	1.5		µs
	V_{DD} = 10V		3.5			µs
	V_{DD} = 15V		2	0.5		µs
Data Set-up time	V_{DD} = 5V	t_{Dsup}	1	0.1		µs
	V_{DD} = 10V		0.75			µs
	V_{DD} = 15V		0.5	0		µs
Data Hold time	V_{DD} = 5V	t_{Dhold}	5	1.5		µs
	V_{DD} = 10V		3.5			µs
	V_{DD} = 15V		2	0.5		µs
Clock rise time		t_{Crise}			2	µs
Clock fall time		t_{Cfall}			2	µs

ELECTRICAL CHARACTERISTICS ($T_A = 0 - 85\,^{\circ}C$, $V_{DD} = 4.5 - 15V$)

Characteristic		Pin[1]	Symbol	Min	Typ	Max	Unit
DC Supply Voltage		18	V_{DD}	4.5		15	V DC
DC Supply Current	MC 144110	(14)	I_{DD}			12	mA DC
	MC 144111					8	mA DC
Input low level		1, 8, 10	D_{IN}			0.8	V
High level	$V_{DD} = 5V$	(1, 6, 8)	CL	3.0			V
	$V_{DD} = 10V$		$\overline{EN}$	3.5			V
	$V_{DD} = 15V$			4.0			V
Current	$V_{IN} = V_{DD}$		I_{IN}			1	μA
Output Sink	$V_{OL} = 0.5V$	17	I_{OL}	200			μA
Source	$V_{OH} = V_{DD} - 0.5V$	(13)	I_{OH}	− 200			[1] μA
D/A Characteristics							
Network Resistance			R	7	10	15	kΩ [2]
Precision		3, 5, 7, 12					
(w.c. at $V_{RN} = V_{DD/2}$)	$V_{DD} = 5V$	14, 16	V_{NONL}[2]		20	100	mV
	$V_{DD} = 10V$	(3, 5, 10,				200	mV
	$V_{DD} = 15V$	12)			120	300	mV
Step Size[3]				− 75 %	$V_{DD}/64$	+ 75 %	
MC 144110							
NPN Emitter Follower Current Gain							
$I_E = 0.1 - 10mA$ at 25°C		2, 4, 6,	h_{fe}	40	100		
Emitter leakage Current $V_{RN} = 0V$		11, 13				10	μA
V_{BE} at $I_E = 1mA$			V_{BE}	0.4		0.7	V
Max Dissipation		15					
per output	$T_{Amax} = 85\,^{\circ}C$		P_E			10	mW
all 6 outputs			P_{Etot}			25	mW
per output	$T_{Amax} = 70\,^{\circ}C$		P_E			30	mW
all 6 outputs			P_{Etot}			100	mW
MC 144111							
NPN Emitter Follower Current Gain		2, 4, 9,					
$I_E = 0.1 - 10mA$ at 25°C		11	h_{fe}	40	100		
Emitter Leakage Current $V_{RN} = 0V$						10	μA
V_{BE} at $I_E = 1mA$			V_{BE}	0.4		0.7	V
Max Dissipation							
per output	$T_{Amax} = 85\,^{\circ}C$		P_E			20	mW
all 4 outputs			P_{Etot}			50	mW
per output	$T_{Amax} = 70\,^{\circ}C$		P_E			50	mW
all 4 outputs			P_{Etot}			150	mW

[1] Pin numbers in brackets () refer to MC 144111

[2] See Figure 4

[3] See Figure 5

2

FIGURE 2a – SERIAL INPUT, POSITIVE CLOCK

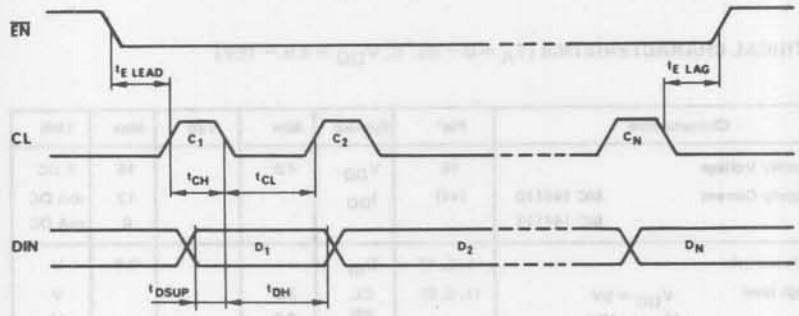
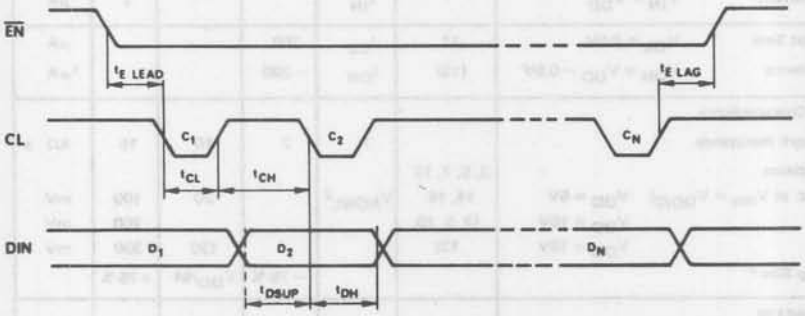
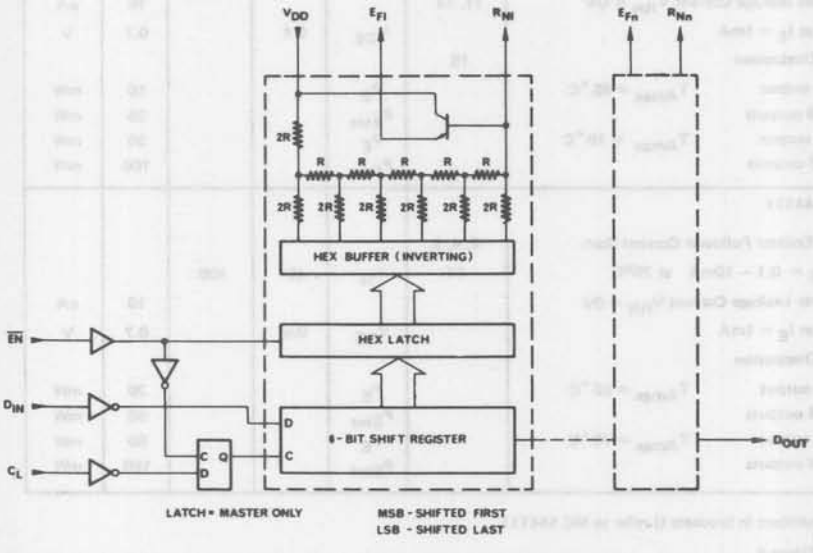


FIGURE 2b – SERIAL INPUT, NEGATIVE CLOCK



2

FIGURE 3 – BLOCK DIAGRAM



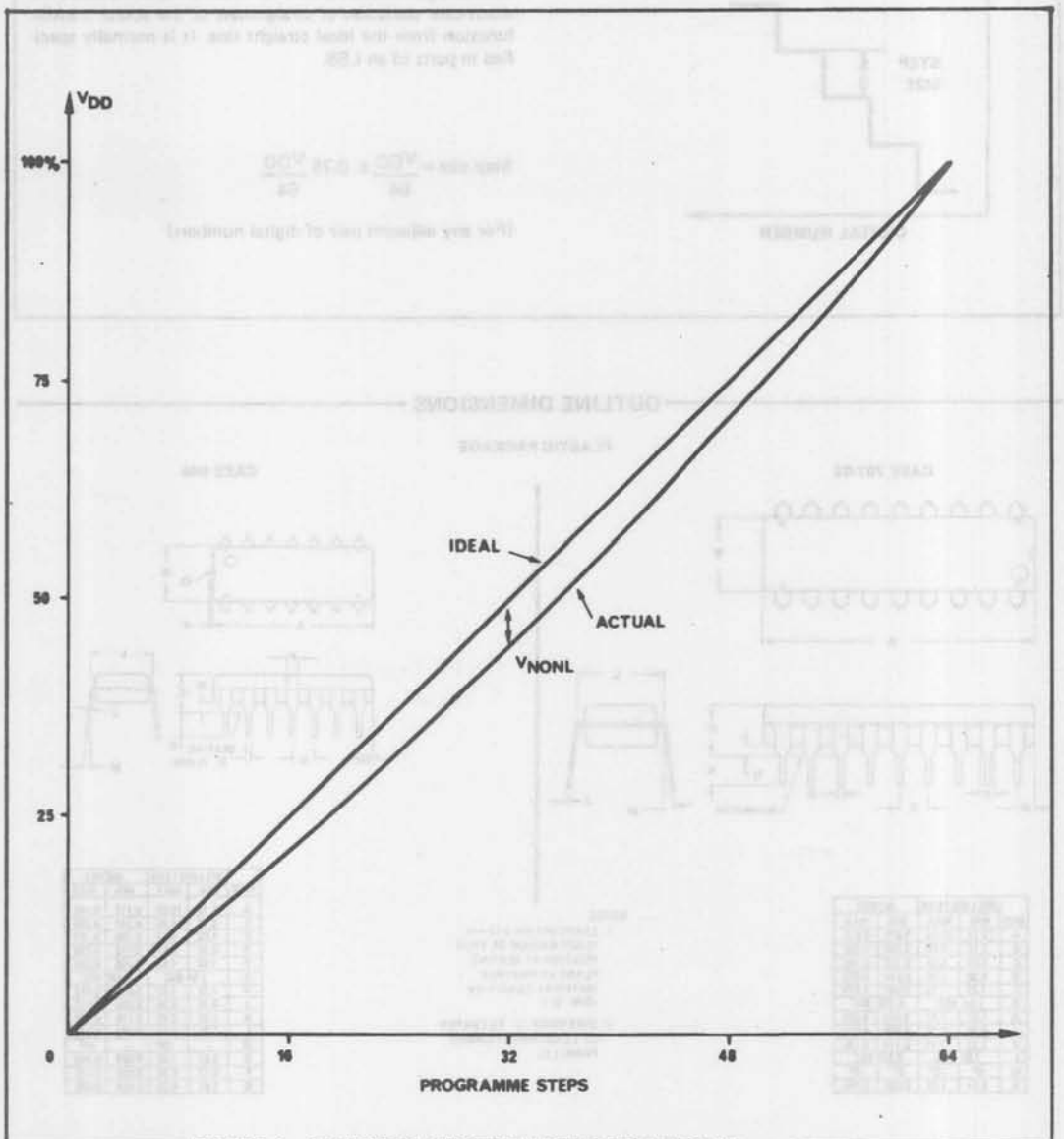
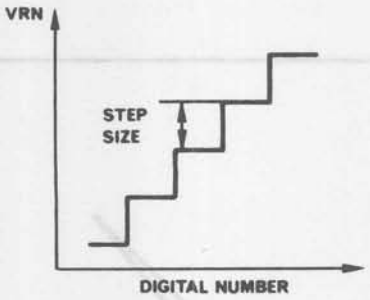


FIGURE 4 – TRANSFER FUNCTION LINEARITY ERROR (V_{NONL})

FIGURE 5 – DEFINITION OF STEP SIZE



LINEARITY ERROR (integral linearity). A measure of how straight a device's transfer function is, it indicates the worst-case deviation of straightness of the actual transfer function from the ideal straight line. It is normally specified in parts of an LSB.

$$\text{Step size} = \frac{V_{DD}}{64} \pm 0.75\frac{V_{DD}}{64}$$

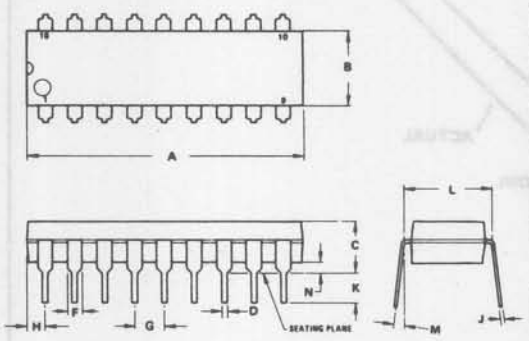
(For any adjacent pair of digital numbers)

OUTLINE DIMENSIONS

2

PLASTIC PACKAGE

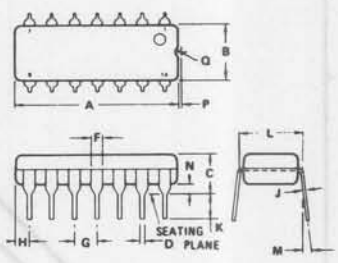
CASE 707-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUM OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (DIM "G").
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

CASE 646



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MOTOROLA

MC145040
MC145041

Advance Information

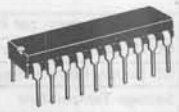
8-Bit A/D Converters With Serial Interface

Silicon-Gate CMOS

The MC145040 and MC145041 are low-cost 8-bit A/D Converters with serial interface ports to provide communication with microprocessors and microcomputers. The converters operate from a single power supply with a maximum nonlinearity of ± ½ LSB over the full temperature range. No external trimming is required.

The MC145040 allows an external clock input (A/D CLK) to operate the dynamic A/D conversion sequence. The MC145041 has an internal clock and an end-of-conversion signal (EOC) is provided.

- Operating Voltage Range: V_{DD} = 4.5 to 5.5 Volts
- Successive Approximation Conversion Time:
  MC145040 — 10 μs (with 2 MHz A/D CLK)
  MC145041 — 20 μs Maximum (Internal Clock)
- 11 Analog Input Channels with Internal Sample and Hold
- 0- to 5-Volt Analog Input Range with Single 5-Volt Supply
- Ratiometric Conversion
- Separate V_{ref} and V_{AG} Pins for Noise Immunity
- Wide V_{ref} Range
- No External Trimming Required
- Direct Interface to Motorola SPI and National MICROWIRE Serial Data Ports
- TTL/NMOS-Compatible Inputs May Be Driven with CMOS
- Outputs are CMOS, NMOS, or TTL Compatible
- Very Low Reference Current Requirement
- Low Power Consumption: 11 mW
- Internal Test Mode for Self Test



CERAMIC CASE 732 — PLASTIC CASE 738

PLASTIC LEADED CHIP CARRIER (PLCC) CASE 775

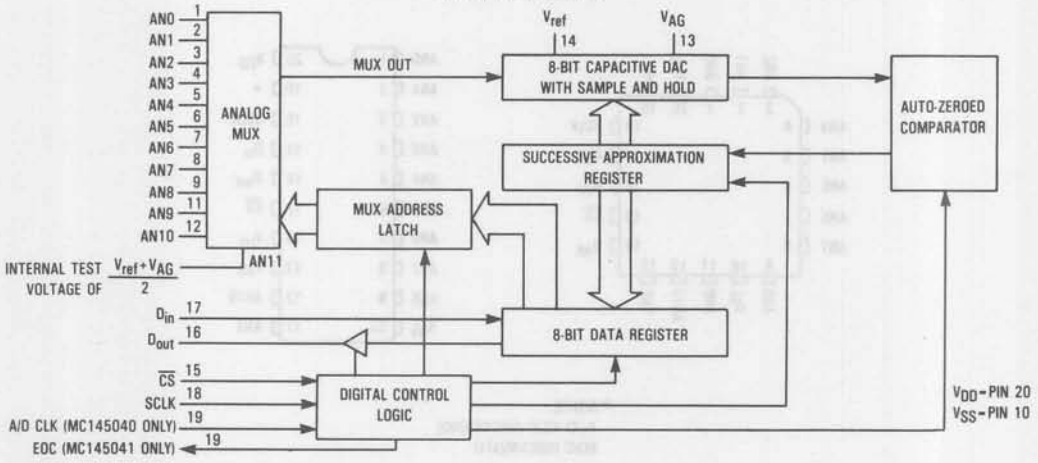
ORDERING INFORMATION

MC14XXXX

Suffix
- 1 2.5 V ≤ V_{ref} ≤ V_{DD}
- 2 V_{ref} = V_{DD}
- P Plastic (−40 to +85°C)
- L Ceramic (−55 to +125°C)
- FN PLCC (−40 to +85°C)

2

BLOCK DIAGRAM



MICROWIRE is a trademark of National Semiconductor.

This document contains information on a new product. Specification and information herein are subject to change without notice.

MAXIMUM RATINGS* (For all product grades)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	−0.5 to +7.0	V
V_{ref}	DC Reference Voltage	V_{AG} to V_{DD}+0.1	V
V_{AG}	Analog Ground	V_{SS}−0.1 to V_{ref}	V
V_{in}	DC Input Voltage, Any Analog or Digital Input	V_{SS}−1.5 to V_{DD}+1.5	V
V_{out}	DC Output Voltage	V_{SS}−0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{DD},I_{SS}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}.) Unused outputs must be left open.

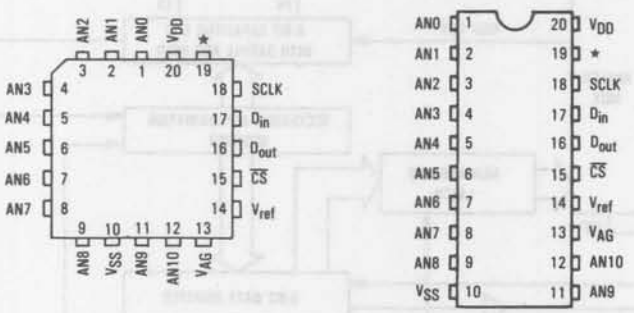
OPERATION RANGES (Applicable to Guaranteed Limits for all product grades)

Symbol	Parameter	Suffix				Unit
		L1	L2	P1, FN1	P2, FN2	
V_{DD}	DC Supply Voltage (Referenced to V_{SS})	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	4.5 to 5.5	V
V_{ref}	DC Reference Voltage (Note 1)	V_{AG}+2.5 to V_{DD}	V_{DD}	V_{AG}+2.5 to V_{DD}	V_{DD}	V
V_{AG}	Analog Ground (Note 1)	V_{SS} to V_{ref}−2.5	V_{SS}	V_{SS} to V_{ref}−2.5	V_{SS}	V
V_{AI}	Analog Input Voltage (Note 2)	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V_{AG} to V_{ref}	V
V_{in}, V_{out}	Digital Input Voltage, Output Voltage	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V_{SS} to V_{DD}	V
T_A	Operating Temperature	−55 to +125	−55 to +125	−40 to +85	−40 to +85	°C

NOTES:
1. Reference voltages down to 1.0 V ($V_{ref} - V_{AG}$ = 1.0 V) are functional, but the A/D Converter Electrical Characteristics are not guaranteed.
2. $V_{SS} \le V_{AI} \le V_{AG}$ produces an output of $00 and $V_{ref} \le V_{AI} \le V_{DD}$ produces an output of $FF. See V_{AG} and V_{ref} pin descriptions.

2

PIN ASSIGNMENTS



★NOTE:
A/D CLK (MC145040)
EOC (MC145041)

DC ELECTRICAL CHARACTERISTICS

(Voltages Referenced to V_{SS}, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Symbol	Parameter	Test Conditions	Guaranteed Limit	Unit
V_{IH}	Minimum High-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		2.0	V
V_{IL}	Maximum Low-Level Input Voltage (D_{in}, SCLK, $\overline{CS}$, A/D CLK)		0.8	V
V_{OH}	Minimum High-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	$I_{out} = -200\ \mu A$ $I_{out} = -100\ \mu A$ $I_{out} = -20\ \mu A$	2.4 2.4 $V_{DD} - 0.1$	V
V_{OL}	Maximum Low-Level Output Voltage (D_{out}) (EOC) (D_{out}, EOC)	$I_{out} = +1.6$ mA $I_{out} = +1.0$ mA $I_{out} = 20\ \mu A$	0.4 0.4 0.1	V
I_{in}	Maximum Input Leakage Current (D_{in}, SCLK, $\overline{CS}$, A/D CLK)	$V_{in} = V_{SS}$ or V_{DD}	±2.5	μA
I_{OZ}	Maximum Three-State Leakage Current (D_{out})	$V_{out} = V_{SS}$ or V_{DD}	±10	μA
I_{DD}	Maximum Power Supply Current	$V_{in} = V_{SS}$ or V_{DD}, All Outputs Open MC145040: A/D CLK = 2 MHz	2	mA
I_{ref}	Maximum Static Analog Reference Current (V_{ref})	$V_{ref} = V_{DD}$ $V_{AG} = V_{SS}$	10	μA
I_{AI}	Maximum Analog Mux Input Leakage Current between all deselected inputs and any selected input. (AN0-AN10)	$V_{AI} = V_{SS}$ to V_{DD}, L1 and L2 Suffix P1,P2, FN1, FN2 Suffix	±1000 ±400	nA

A/D CONVERTER ELECTRICAL CHARACTERISTICS

(MC145040: 1 MHz ≤ A/D CLK ≤ 2 MHz, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Characteristic	Definition and Test Conditions	Guaranteed Limit	Unit
Minimum Resolution	Number of bits resolved by the A/D	8	Bits
Maximum Nonlinearity	Maximum deviation from the best straight line through the A/D transfer characteristic	± ½	LSB
Maximum Zero Error	Difference between the output of an ideal and an actual A/D for zero input voltage	± ½	LSB
Maximum Full-Scale Error	Difference between the output of an ideal and an actual A/D for full-scale input voltage	± ½	LSB
Maximum Total Unadjusted Error	Maximum sum of Nonlinearity, Zero Error, and Full-Scale Error	± ½	LSB
Maximum Quantization Error	Uncertainty due to converter resolution	± ½	LSB
Absolute Accuracy	Difference between the actual input voltage and the full-scale weighted equivalent of the binary output code, all error sources included	±1	LSB
Maximum Conversion Time	Total time to perform a single analog-to-digital conversion MC145040 MC145041	20 20	A/D CLK cycles μs
Maximum Data Transfer Time	Total time to transfer digital serial data into and out of the device	8	SCLK cycles
Maximum Sample Acquisition Time	Analog input acquisition time window MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC140541: SCLK = 1 MHz	 10 16	μs
Maximum Total Cycle Time	Total time to transfer serial data, sample the analog input, and perform the conversion MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC145041: SCLK = 1 MHz	 24 40	μs
Maximum Sample Rate	Rate at Which Analog Inputs May be Sampled MC145040: A/D CLK = 2 MHz, SCLK = 1 MHz MC145041: SCLK = 1 MHz	 41 25	kHz

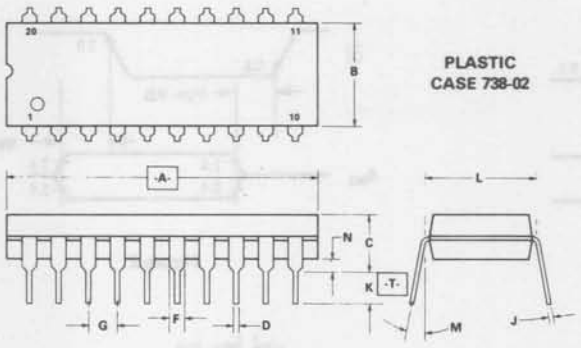
2

AC ELECTRICAL CHARACTERISTICS ($t_r = t_f = 6$ ns, Full Temperature and Voltage Ranges Per Operation Ranges Table)

Figure	Symbol	Parameter		Guaranteed Limit	Unit
1	f	Maximum Clock Frequency (50% Duty Cycle), SCLK		1.1	MHz
1 (same as SCLK)	f	Clock Frequency (50% Duty Cycle), A/D CLK (MC145040)	Minimum Maximum	1.0 2.1	MHz
1,7	t_{PLH}, t_{PHL}	Maximum Propagation Delay, SCLK to D_{out}		400	ns
1,7	t_h	Minimum Hold Time, SCLK to D_{out}		10	ns
2,7	t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}		150	ns
2,7	t_{PZL}, t_{PZH}	Maximum Propagation Delay, $\overline{CS}$ to D_{out}	MC145040 MC145041	3 A/D CLK cycles + 400 ns 3.4	μs
3	t_{su}	Minimum Setup Time, D_{in} to SCLK		400	ns
3	t_h	Minimum Hold Time, SCLK to D_{in}		0	ns
4,7,8	t_d	Maximum Delay Time, EOC to D_{out} (MSB)	MC145041	400	ns
5	t_{su}	Minimum Setup Time, $\overline{CS}$ to SCLK	MC145040 MC145041	3 A/D CLK cycles + 800 ns 3.8	μs
5	t_h	Minimum Hold Time, 8th SCLK to $\overline{CS}$		0	ns
6,8	t_{PHL}	Maximum Propagation Delay, 8th SCLK to EOC		500	ns
1	t_r, t_f	Maximum Input Rise and Fall Times, Any Digital Input		100	ns
1,4,6,7,8	t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output		300	ns
–	C_{in}	Maximum Input Capacitance	AN0-AN10 A/D CLK, SCLK, $\overline{CS}$, D_{in}	55 15	pF
–	C_{out}	Maximum Three-State Output Capacitance	D_{out}	15	pF

2

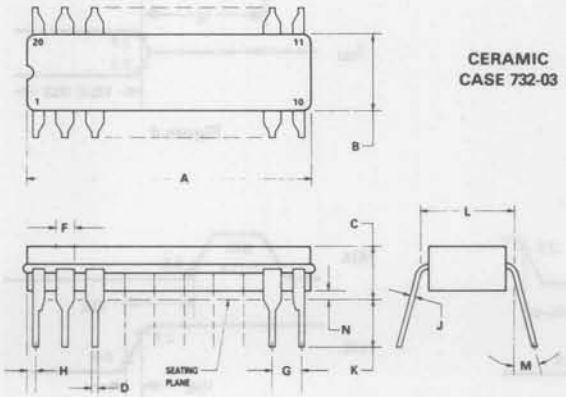
PACKAGE DIMENSIONS



PLASTIC
CASE 738-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

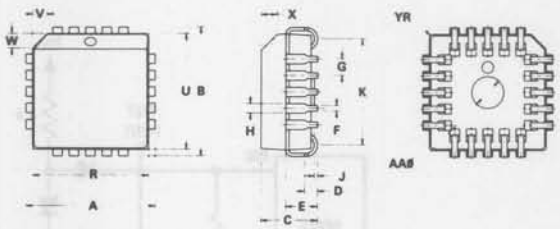
NOTES:
1. DIM -A- IS DATUM
2. POSITIONAL TOL FOR LEADS
   ⌖ ⌀ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE
4. DIM "B" DOES NOT INCLUDE MOLD FLASH
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973



CERAMIC
CASE 732-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15
N	0.25	1.02	0.010	0.040

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL
3. DIM A AND B INCLUDES MENISCUS



NOTES:
1. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: INCH

PLASTIC LEADED
CHIP CARRIER (PLCC)
CASE 775

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.78	10.02	0.385	0.395
B	9.78	10.02	0.385	0.395
C	4.19	4.57	0.165	0.180
D	0.64	1.01	0.025	0.040
E	2.16	2.79	0.085	0.110
F	0.33	0.53	0.013	0.021
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.13	0.38	0.005	0.015
K	7.37	8.38	0.290	0.330
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	0.00	0.50	0.000	0.020
AA	2.34	2.71	0.088	0.107

2

SWITCHING WAVEFORMS

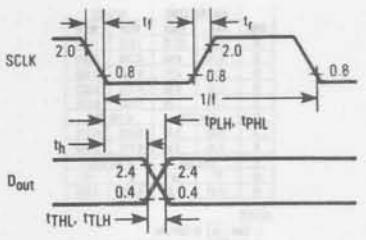


Figure 1

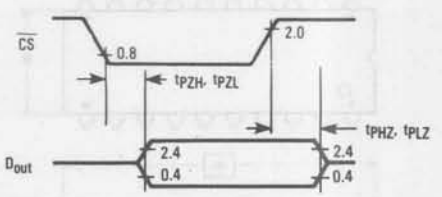


Figure 2

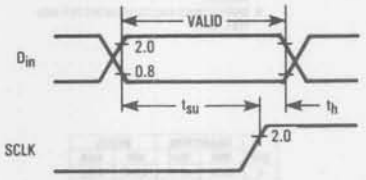


Figure 3

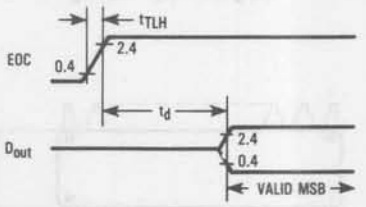


Figure 4

2

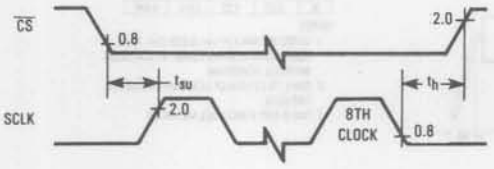


Figure 5

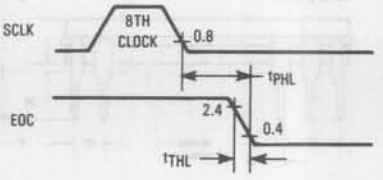


Figure 6

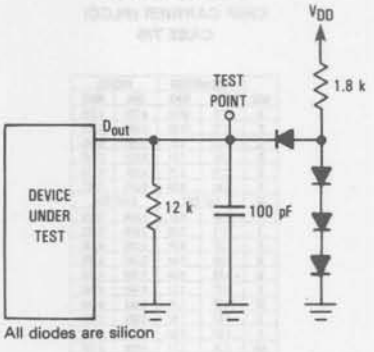


Figure 7. Test Circuit

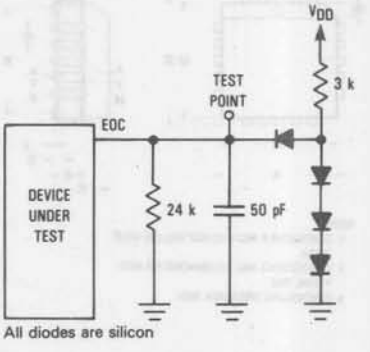


Figure 8. Test Circuit

PIN DESCRIPTIONS

DIGITAL INPUTS AND OUTPUTS

$\overline{CS}$ (Pin 15)

Active-low chip select input. $\overline{CS}$ provides three-state control of D_{out}. $\overline{CS}$ at a high logic level forces D_{out} to a high-impedance state. In addition, the device recognizes the falling edge of $\overline{CS}$ as a serial interface reset to provide synchronization between the MPU and the A/D converter's serial data stream. To prevent a spurious reset from occurring due to noise on the $\overline{CS}$ input, a delay circuit has been included such that a $\overline{CS}$ signal of duration $\leq$1 A/D CLK period (MC145040) or $\leq$500 ns (MC145041) is ignored. A valid $\overline{CS}$ signal is acknowledged when the duration is $\geq$3 A/D CLK periods (MC145040) or $\geq 3\ \mu s$ (MC145041).

CAUTION

A reset aborts a conversion sequence, therefore high-to-low transitions on $\overline{CS}$ must be avoided during the conversion sequence.

D_{out} (Pin 16)

Serial data output of the A/D conversion result. The 8-bit serial data stream begins with the most significant bit and is shifted out on the high-to-low transition of SCLK. D_{out} is a three-state output as controlled by $\overline{CS}$. However, D_{out} is forced into a high-impedance state after the eighth SCLK, independent of the state of $\overline{CS}$. See Figures 9, 10, 11, or 12.

D_{in} (Pin 17)

Serial data input. The 4-bit serial data stream begins with the most significant address bit of the analog mux and is shifted in on the low-to-high transition of SCLK.

SCLK (Pin 18)

Serial data clock. The serial data register is completely static, allowing SCLK rates down to DC in a continuous or intermittent mode. SCLK need not be synchronous to the A/D CLK (MC145040) or the internal clock (MC145041). Eight SCLK cycles are required for each simultaneous data transfer, the low-to-high transition shifting in the new address and the high-to-low transition shifting out the previous conversion result. The address is acquired during the first four SCLK cycles, with the interval produced by the remaining four cycles being used to begin charging the on-chip sample-and-hold capacitors. After the eighth SCLK, the SCLK input is inhibited (on-chip) until the conversion is complete.

A/D CLK (Pin 19, MC145040 only)

A/D clock input. This pin clocks the dynamic A/D conversion sequence, and may be asynchronous and unrelated to SCLK. This signal must be free running, and may be obtained from the MPU system clock. Deviations from a 50% duty cycle can be tolerated if each half period is > 238 ns.

EOC (Pin 19, MC145041 only)

End-of-conversion output. EOC goes low on the negative edge of the eighth SCLK. The low-to-high transition of EOC indicates the A/D conversion is complete and the data is ready for transfer.

ANALOG INPUTS AND TEST MODE

AN0 through AN10 (Pins 1-9, 11, 12)

Analog multiplexer inputs. The input AN0 is addressed by loading $0 into the serial data input, D_{in}. AN1 is addressed by $1, AN2 by $2 . . . AN10 via $A. The mux features a break-before-make switching structure to minimize noise injection into the analog inputs. The source impedance driving these inputs must be $\leq$10 kΩ. NOTE: $B addresses an on-chip test voltage of $(V_{ref} + V_{AG})/2$, and produces an output of $80 if the converter is functioning properly. However, a ±1 LSB deviation from $80 occurs in the presence of sufficient system noise (external to the chip) on V_{DD}, V_{SS}, V_{ref}, or V_{AG}.

POWER AND REFERENCE PINS

V_{SS} and V_{DD} (Pins 10 and 20)

Device supply pins. V_{SS} is normally connected to digital ground; V_{DD} is connected to a positive digital supply voltage. $V_{DD} - V_{SS}$ variations over the range of 4.5 to 5.5 volts do not affect the A/D accuracy. Excessive inductance in the V_{DD} or V_{SS} lines, as on automatic test equipment, may cause A/D offsets > ½ LSB.

V_{AG} and V_{ref} (Pins 13 and 14)

Analog reference voltage pins which determine the lower and upper boundary of the A/D conversion. Analog input voltages $\geq V_{ref}$ produce an output of $FF and input voltages $\leq V_{AG}$ produce an output of $00. CAUTION: The analog input voltage must be $\geq V_{SS}$ and $\leq V_{DD}$. The A/D conversion result is ratiometric to $V_{ref} - V_{AG}$ as shown by the formula:

$$V_{in} = \left[\frac{\text{output code}}{\$FF} \times (V_{ref} - V_{AG})\right] + \frac{\text{quantizing}}{\text{error}} + \frac{\text{linearity}}{\text{error}}$$

V_{ref} and V_{AG} should be as noise-free as possible to avoid degradation of the A/D conversion. Noise on either of these pins will couple 1:1 to the analog input signal, i.e. a 20 mV change in V_{ref} can cause a 20 mV error in the conversion result. Ideally V_{ref} and V_{AG} should be single-point connected to the voltage supply driving the system's transducers.

2

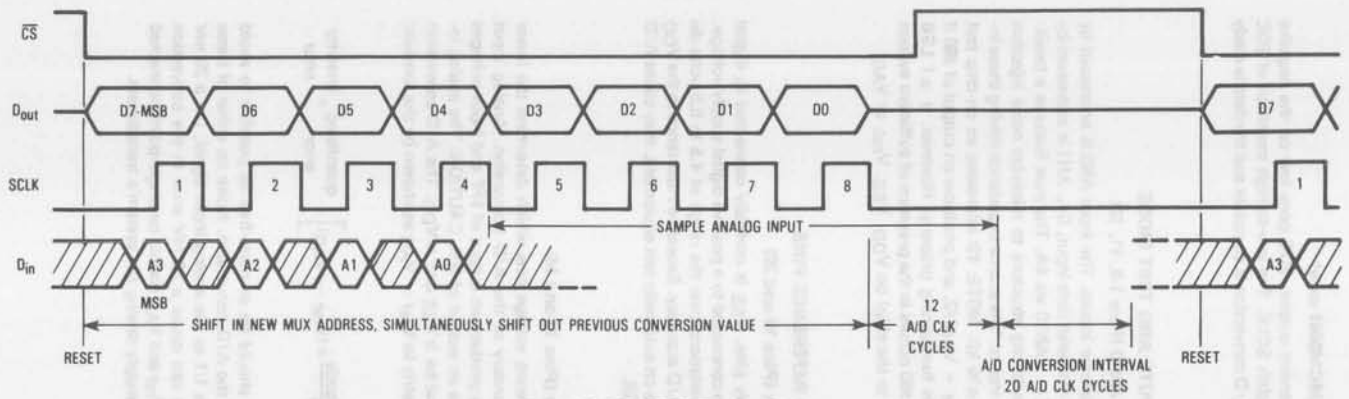


Figure 9. MC145040 Timing Diagram
Utilizing $\overline{CS}$ to Three-State D_{out}

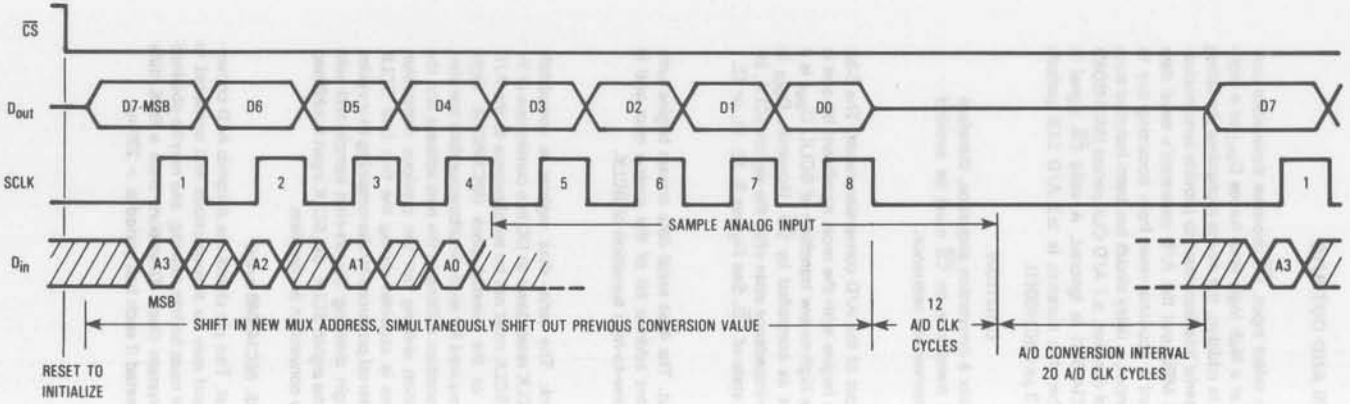


Figure 10. MC145040 Timing Diagram
Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

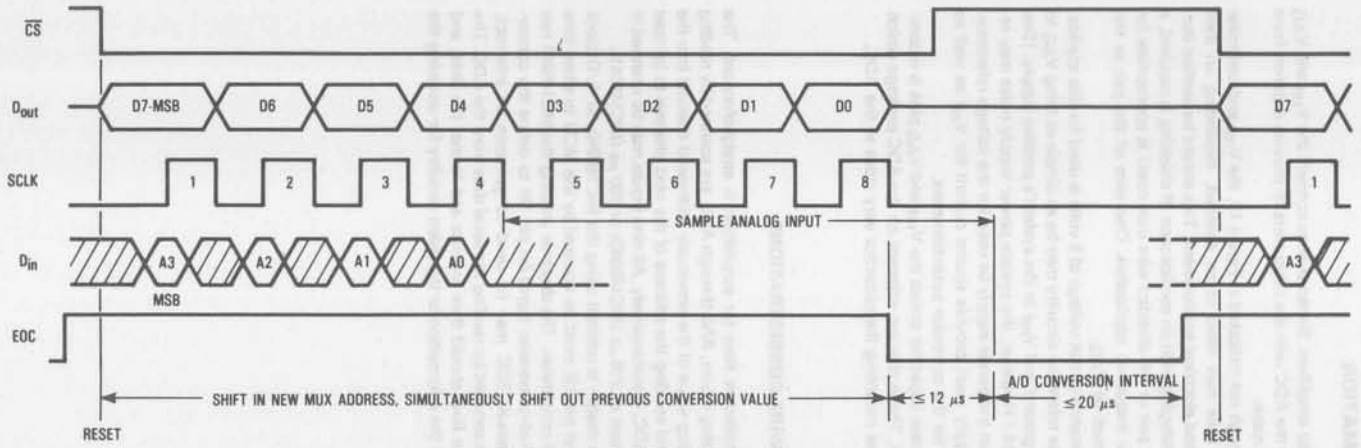


Figure 11. MC145041 Timing Diagram
Utilizing $\overline{CS}$ to Three-State D_{out}

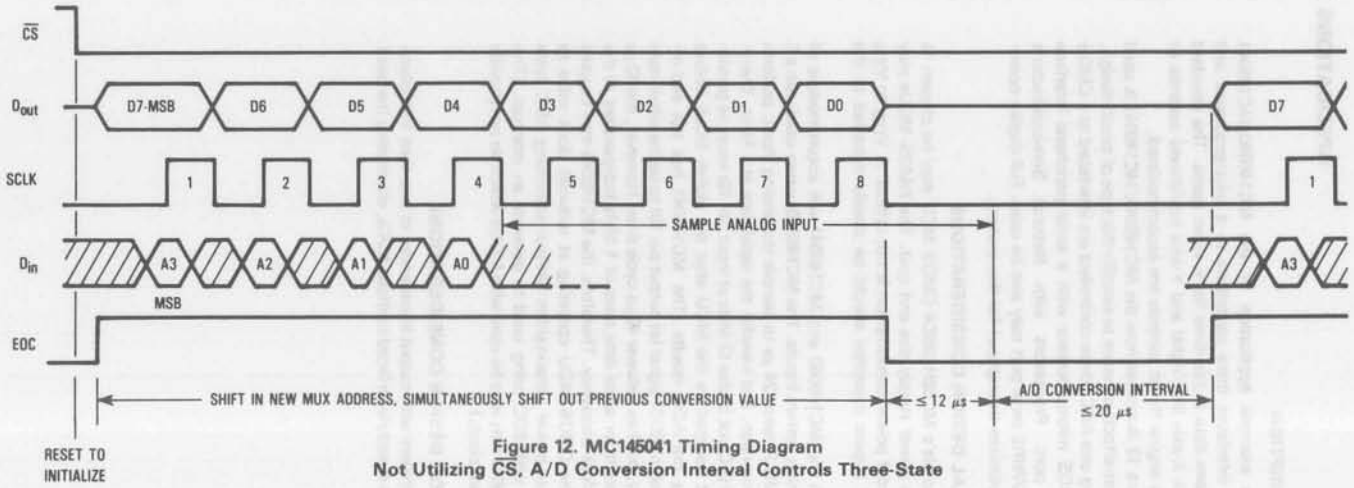


Figure 12. MC145041 Timing Diagram
Not Utilizing $\overline{CS}$, A/D Conversion Interval Controls Three-State

NOTES:
D7, D6, D5 . . . D0 = The result of the previous A/D conversion.
A3, A2, A1, A0 = The mux address for the next A/D conversion.

APPLICATIONS INFORMATION

DESCRIPTION

This example application of the MC145040/MC145041 ADCs interfaces three controllers to a microprocessor and processes data in real-time for a video game. The standard joystick X-axis (left/right) and Y-axis (up/down) controls as well as engine thrust controls are accommodated.

Figure 13 illustrates how the MC145040/MC145041 is used as a cost-effective means to simplify this type of circuit design. Utilizing one ADC, three controllers are interfaced to a CMOS or NMOS microprocessor with a serial peripheral interface (SPI) port. Processors with National Semiconductor's MICROWIRE serial port may also be used. Full duplex operation optimizes throughput for this system.

DIGITAL DESIGN CONSIDERATIONS

Motorola's MC68HC05C4 CMOS MCU may be chosen to reduce power supply size and cost. The NMOS MCUs may be used if power consumption is not critical. A V_{DD} to V_{SS} 0.1 μF bypass capacitor should be closely mounted to the ADC.

Both the MC145040 and MC145041 will accommodate all the analog system inputs. The MC145040, when used with a 2 MHz MCU, takes 24 μs to sample the analog input, perform the conversion, and transfer the serial data at 1 MHz. Thirty-two A/D Clock cycles (2 MHz at input pin 19) must be provided and counted by the MCU after the eighth SCLK before reading the ADC results. The MC145041 has the end-of-conversion (EOC) signal (at output pin 19) to define when data is ready, but has a slower 40 μs cycle time. However, the 40 μs is constant for serial data rates of 1 MHz independent of the MCU clock frequency. Therefore, the MC145041 may be used with the CMOS MCU operating at reduced clock rates to minimize power consumption without sacrificing ADC cycle times, with EOC being used to generate an interrupt. (The MC145041 may also be used with MCUs which do not provide a system clock.)

ANALOG DESIGN CONSIDERATIONS

Controllers with output impedances of less than 10 kilohms may be directly interfaced to these ADCs, eliminating the need for buffer amplifiers. Separate lines connect the V_{ref} and V_{AG} pins on the ADC with the controllers to provide isolation from system noise.

Although not indicated in Figure 13, the V_{ref} and controller output lines may need to be shielded, depending on their length and electrical environment. This should be verified during prototyping with an oscilloscope. If shielding is required, a twisted pair or foil-shielded wire (not coax) is appropriate for this low frequency application. One wire of the pair or the shield must be V_{AG}.

A reference circuit voltage of 5 volts is used for this application. The reference circuitry may be as simple as tying V_{AG} to system ground and V_{ref} to the system's positive supply. (See Figure 14.) However, the system power supply noise may require that a separate supply be used for the voltage reference. This supply must provide source current for V_{ref} as well as current for the controller potentiometers.

A bypass capacitor across the V_{ref} and V_{AG} pins is recommended. These pins are adjacent on the ADC package which facilitates mounting the capacitor very close to the ADC.

SOFTWARE CONSIDERATIONS

The software flow for acquisition is straightforward. The nine analog inputs, AN0 through AN8, are scanned by reading the analog value of the previously addressed channel into the MCU and sending the address of the next channel to be read to the ADC, simultaneously. All nine inputs may be scanned in a minimum of 216 μs (MC145040) or 360 μs (MC145041).

If the design is realized using the MC145040, 32 A/D clock cycles (at pin 19) must be counted by the MCU to allow time for A/D conversion. The designer utilizing the MC145041 has the end-of-conversion signal (at pin 19) to define the conversion interval. EOC may be used to generate an interrupt, which is serviced by reading the serial data from the ADC. The software flow should then process and format the data, and transfer the information to the video circuitry for updating the display.

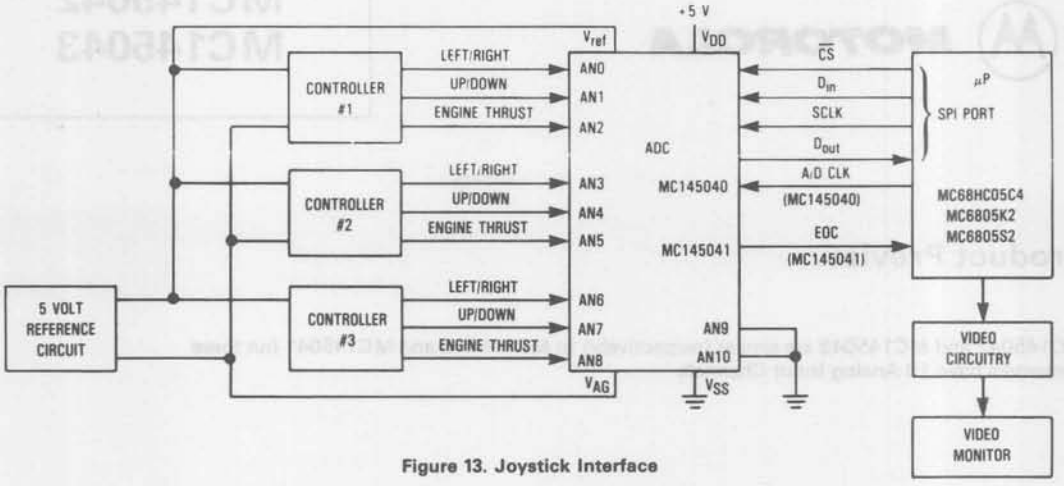


Figure 13. Joystick Interface

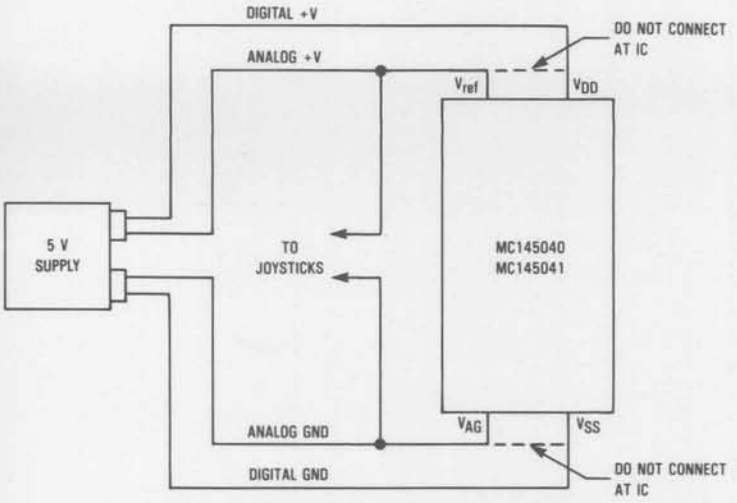


Figure 14. Alternate Configuration Using the Digital Supply for the Reference Voltage

2

MOTOROLA

MC145042
MC145043

Product Preview

MC145042 and MC145043 are similar (respectively) to MC145040 and MC145041 but these converters have 19 Analog Input Channels.

2

MOTOROLA

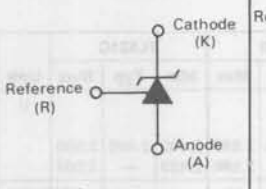
TL431,A Series

Specifications and Applications Information

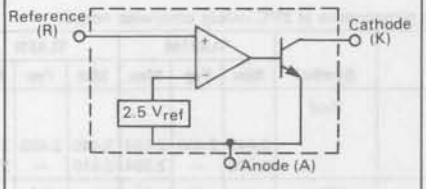
PROGRAMMABLE PRECISION REFERENCES

The TL431,A integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 volts with two external resistors. These devices exhibit a wide operating current range of 1.0 to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 volt reference makes it convenient to obtain a stable reference from 5.0 volt logic supplies, and since the TL431,A operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

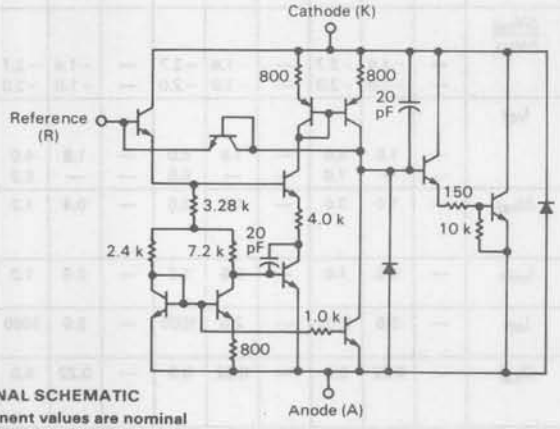
- Programmable Output Voltage to 36 Volts
- Voltage Reference Tolerance: ±1.0% (TL431,A)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage



SYMBOL



FUNCTIONAL BLOCK DIAGRAM



INTERNAL SCHEMATIC
Component values are nominal

PROGRAMMABLE PRECISION REFERENCES

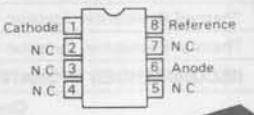
SILICON MONOLITHIC INTEGRATED CIRCUITS

LP SUFFIX
CASE 29-02
TO-226AA
(TO-92)

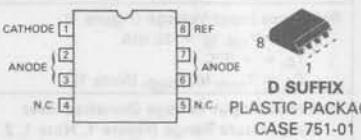
Pin 1. Reference
2. Anode
3. Cathode

P SUFFIX
PLASTIC DUAL-IN-LINE PACKAGE
CASE 626

(Top View)



JG SUFFIX
CERAMIC DUAL-IN-LINE PACKAGE
CASE 693



D SUFFIX
PLASTIC PACKAGE
CASE 751-01
SOP-8

SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP,ACLP	0 to +70°C	Plastic TO-92
TL431CP,ACP	0 to +70°C	Plastic DIP
TL431CD,ACD	0 to +70°C	SOP-8
TL431CJG	0 to +70°C	Ceramic DIP
TL431ILP,AILP	−40 to +85°C	Plastic TO-92
TL431IP,AIP	−40 to +85°C	Plastic DIP
TL431IJG	−40 to +85°C	Ceramic DIP
TL431MJG	−55 to +125°C	Ceramic DIP

DS9578R1

2

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode To Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	−100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	−0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I, TL431AI TL431C, TL431AC	T_A	 −55 to +125 −40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.70 1.10 1.25	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

THERMAL CHARACTERISTICS

Characteristics	Symbol	D, LP Suffix Package	P Suffix Package	JG Suffix package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

2

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode To Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	V_{ref}	 2.440 2.396	 2.495 —	 2.550 2.594	 2.440 2.410	 2.495 —	 2.550 2.580	 2.440 2.423	 2.495 —	 2.550 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	 — —	 −1.4 −1.0	 −2.7 −2.0	mV/V
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞ T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	 — —	 1.8 —	 4.0 7.0	 — —	 1.8 —	 4.0 6.5	 — —	 1.8 —	 4.0 5.2	μA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C unless otherwise noted)

Characteristic	Symbol	TL431AI			TL431AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA	V_{ref}							V
T_A = +25°C		2.470	2.495	2.520	2.470	2.495	2.520	
$T_A = T_{low}$ to T_{high} (Note 4)		2.440	—	2.550	2.453	—	2.537	
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Note 1, 2) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref}	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	—	−1.4	−2.7	—	−1.4	−2.7	mV/V
ΔV_{KA} = 36 V to 10 V		—	−1.0	−2.0	—	−1.0	−2.0	
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞	I_{ref}							μA
T_A = +25°C		—	1.8	4.0	—	1.8	4.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	6.5	—	—	5.2	
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	0.8	2.5	—	0.4	1.2	μA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	Ω

Note 1:
T_{low} = −55°C for TL431MJG
= −40°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

T_{high} = +125°C for TL431MJG
= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

FIGURE 1 — TEST CIRCUIT FOR $V_{KA} = V_{ref}$

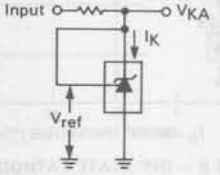


FIGURE 2 — TEST CIRCUIT FOR $V_{KA} > V_{ref}$

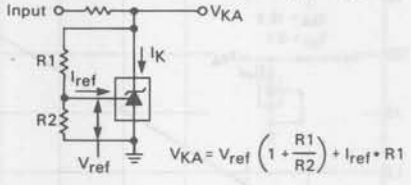
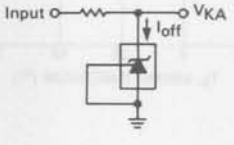
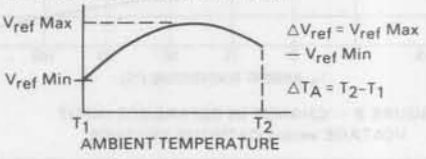


FIGURE 3 — TEST CIRCUIT FOR I_{off}



Note 2:
The deviation parameter ΔV_{ref} is defined as the differences between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\alpha V_{ref} \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6)

Example: ΔV_{ref} = 8.0 mV and slope is positive, V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ ppm/°C$$

2

Note 3:
The dynamic impedance Z_{ka} is defined as:

$$|Z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{ka}'| \approx |Z_{ka}| \left(1 + \frac{R1}{R2}\right)$$

Note 4:
This test is not applicable to surface mount (D suffix) devices.

FIGURE 4 — CATHODE CURRENT versus CATHODE VOLTAGE

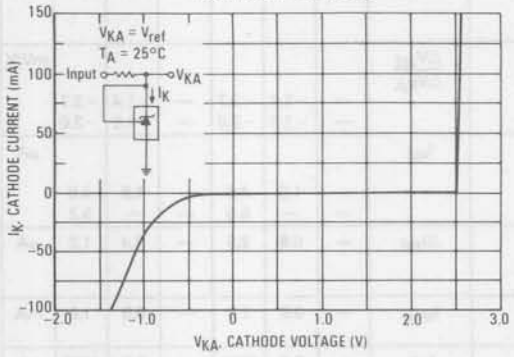


FIGURE 5 — CATHODE CURRENT versus CATHODE VOLTAGE

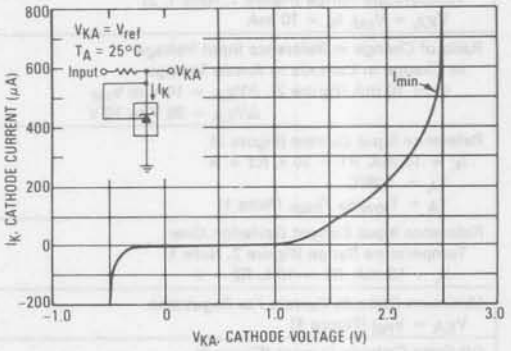


FIGURE 6 — REFERENCE INPUT VOLTAGE versus AMBIENT TEMPERATURE

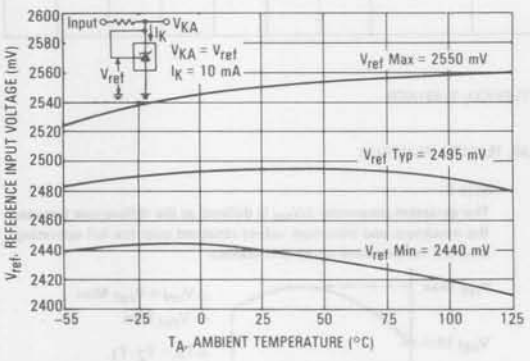


FIGURE 7 — REFERENCE INPUT CURRENT versus AMBIENT TEMPERATURE

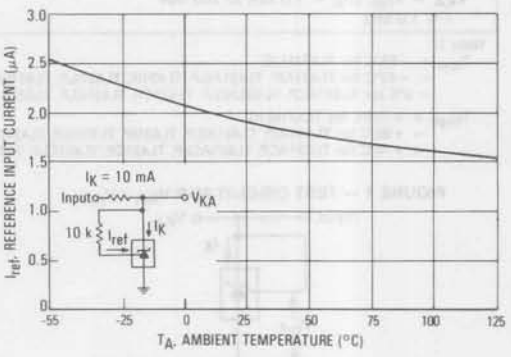


FIGURE 8 — CHANGE IN REFERENCE INPUT VOLTAGE versus CATHODE VOLTAGE

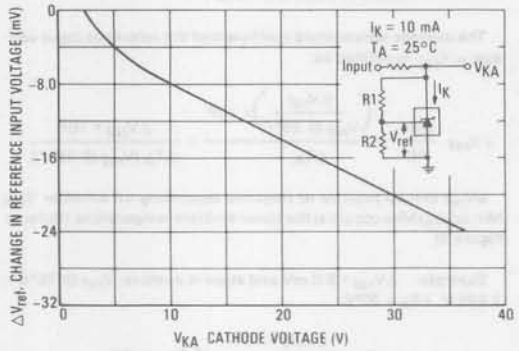


FIGURE 9 — OFF-STATE CATHODE CURRENT versus AMBIENT TEMPERATURE

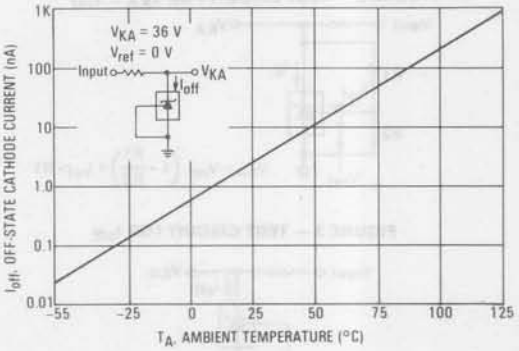


FIGURE 10 — DYNAMIC IMPEDANCE versus FREQUENCY

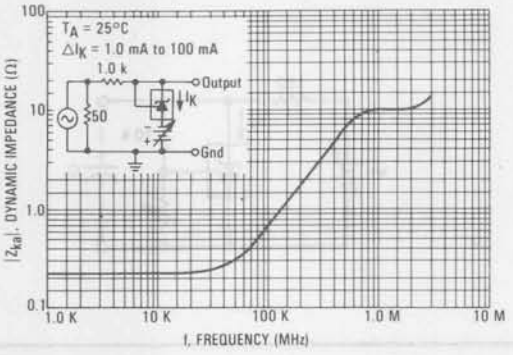


FIGURE 11 — DYNAMIC IMPEDANCE versus AMBIENT TEMPERATURE

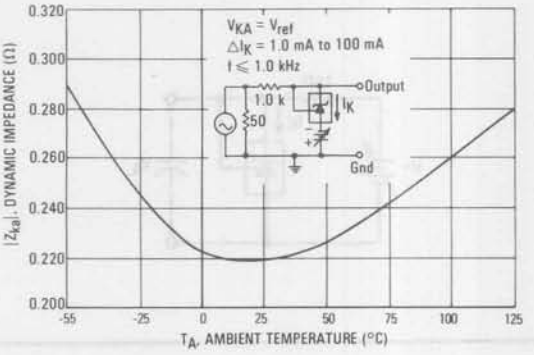


FIGURE 12 — OPEN LOOP VOLTAGE GAIN versus FREQUENCY

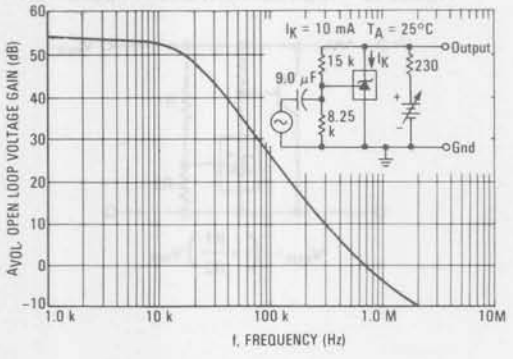


FIGURE 13 — SPECTRAL NOISE DENSITY

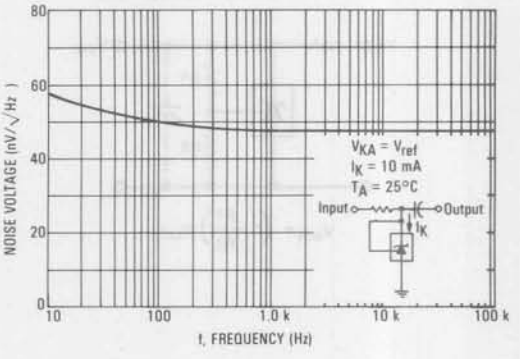


FIGURE 14 — PULSE RESPONSE

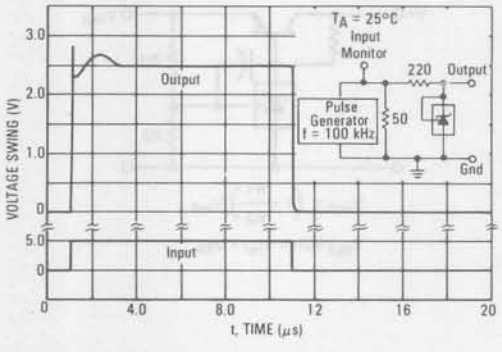
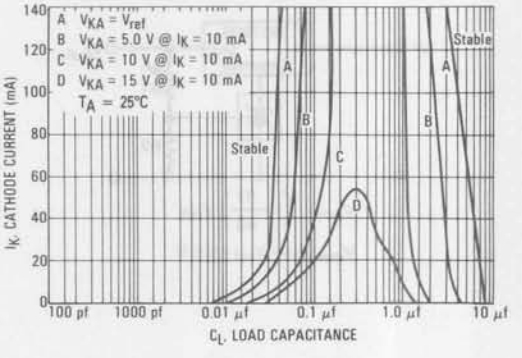


FIGURE 15 — STABILITY BOUNDARY CONDITIONS



2

FIGURE 16 — TEST CIRCUIT FOR CURVE A OF STABILITY BOUNDARY CONDITIONS

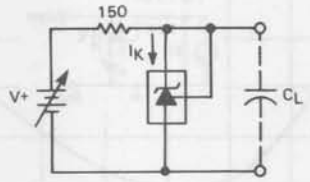
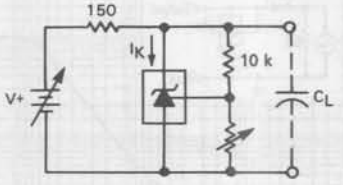
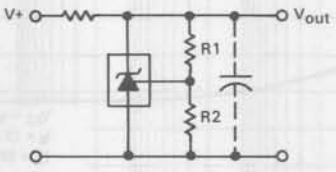


FIGURE 17 — TEST CIRCUIT FOR CURVES B, C, AND D OF STABILITY BOUNDARY CONDITIONS



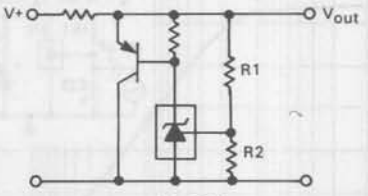
TYPICAL APPLICATIONS

FIGURE 18 — SHUNT REGULATOR



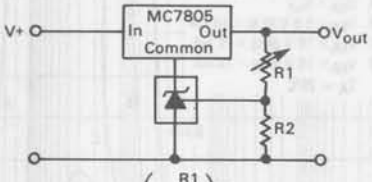
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

FIGURE 19 — HIGH CURRENT SHUNT REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

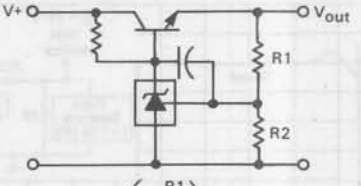
FIGURE 20 — OUTPUT CONTROL OF A THREE-TERMINAL FIXED REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + 5.0 V

FIGURE 21 — SERIES PASS REGULATOR



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

V_{out} Min = V_{ref} + V_{be}

FIGURE 22 — CONSTANT CURRENT SOURCE

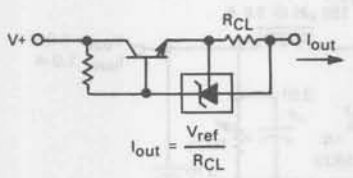


FIGURE 23 — CONSTANT CURRENT SINK

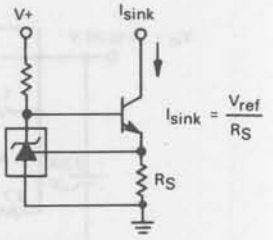


FIGURE 24 — TRIAC CROWBAR

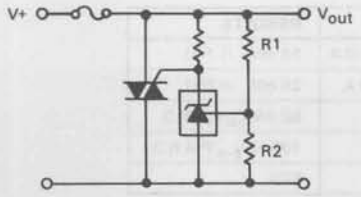


FIGURE 25 — SCR CROWBAR

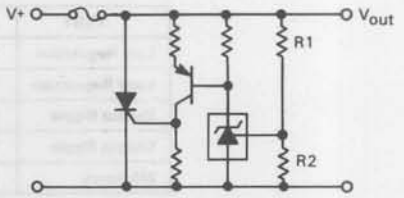
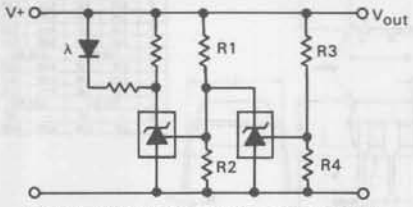


FIGURE 26 — VOLTAGE MONITOR

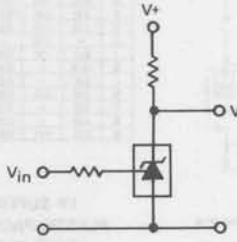


L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right)V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right)V_{ref}$$

FIGURE 27 — SINGLE-SUPPLY COMPARATOR WITH TEMPERATURE-COMPENSATED THRESHOLD



$V_{th} = V_{ref}$

V_{in}	V_{out}
$<V_{ref}$	V+
$>V_{ref}$	≈ 2.0 V

FIGURE 28 — LINEAR OHMMETER

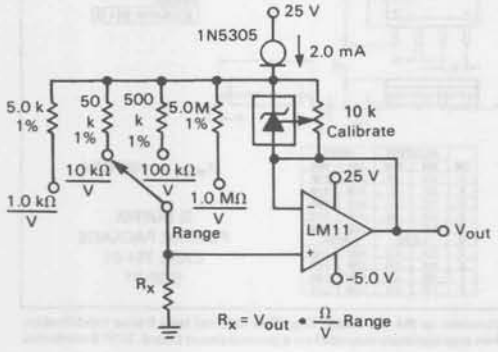


FIGURE 29 — SIMPLE 400 mW PHONO AMPLIFIER

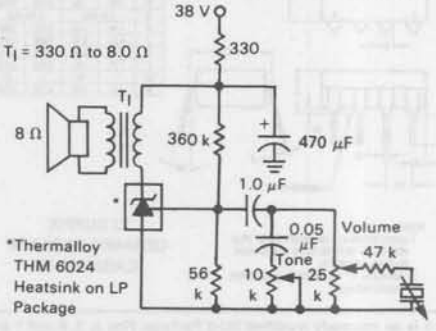
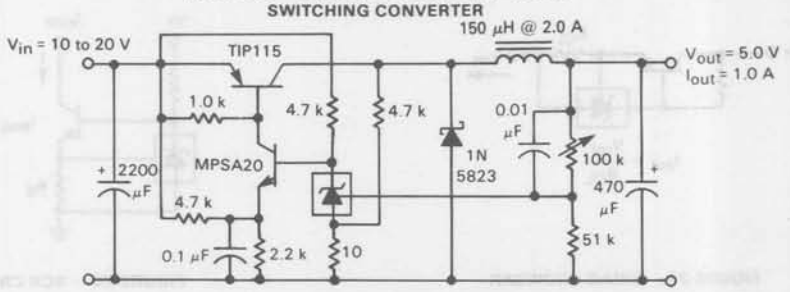
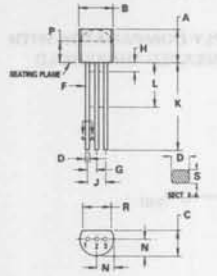


FIGURE 30 — HIGH EFFICIENCY STEP-DOWN SWITCHING CONVERTER



TEST	CONDITIONS	RESULTS
Line Regulation	V_{in} = 10 V to 20 V, I_o = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_o = 0A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_o = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_o = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_o = 1.0 A	82%

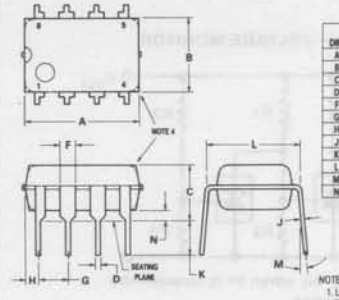
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	—	2.54	—	0.100
J	2.41	2.67	0.095	0.105
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.03	2.67	0.080	0.105
P	2.92	—	0.115	—
R	3.43	—	0.135	—
S	0.36	0.41	0.014	0.016

NOTES:
1. CONTOUR OF PACKAGE BEYOND ZONE "P" IS UNCONTROLLED.
2. DIM "F" APPLIES BETWEEN "H" AND "L". DIM "D" & "S" APPLIES BETWEEN "L" & 12.70 mm (0.5") FROM SEATING PLANE. LEAD DIM IS UNCONTROLLED IN "H" & BEYOND 12.70 mm (0.5") FROM SEATING PLANE.

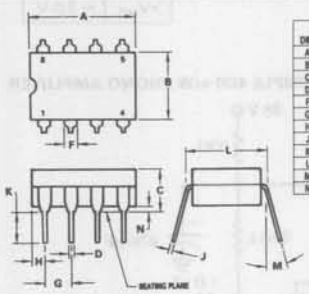
LP SUFFIX
PLASTIC PACKAGE
CASE 29-02
TO-226AA (TO-92)
$R_{\theta JA}$ = 200°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE:
⌖ ⌀ 0.13 (0.005) Ⓜ T A Ⓜ B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

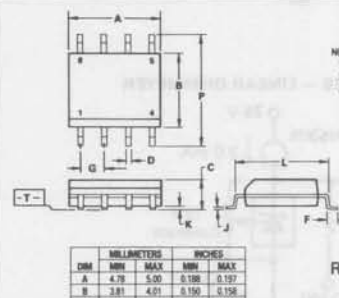
P1 SUFFIX
PLASTIC PACKAGE
CASE 626-04



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	—	15°	—	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

U SUFFIX
CERAMIC PACKAGE
CASE 693-02



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	1.75	0.053	0.069
D	0.35	0.48	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.19	0.22	0.007	0.008
K	0.10	0.20	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.20	0.228	0.244

NOTES:
1. -T- IS SEATING PLANE.
2. DIMENSION A IS DATUM.
3. POSITIONAL TOLERANCE FOR LEADS:
⌖ 0.25 (0.010) Ⓜ A Ⓣ

$R_{\theta JA}$ = 180°C/W

D SUFFIX
PLASTIC PACKAGE
CASE 751-01
SOP-8*

*SOP-8 is an internally modified SO-8 Package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP-8 conforms to all external dimensions of the standard SO-8 Package.

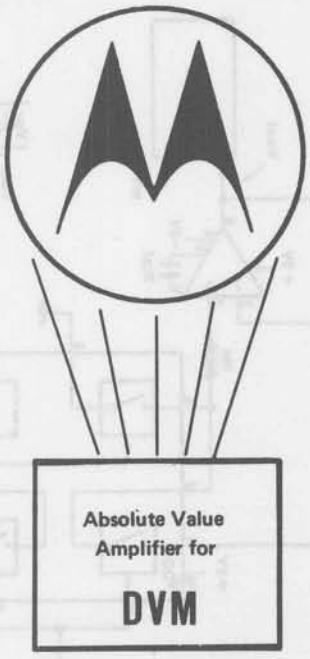
Section 3 — Application Notes

3

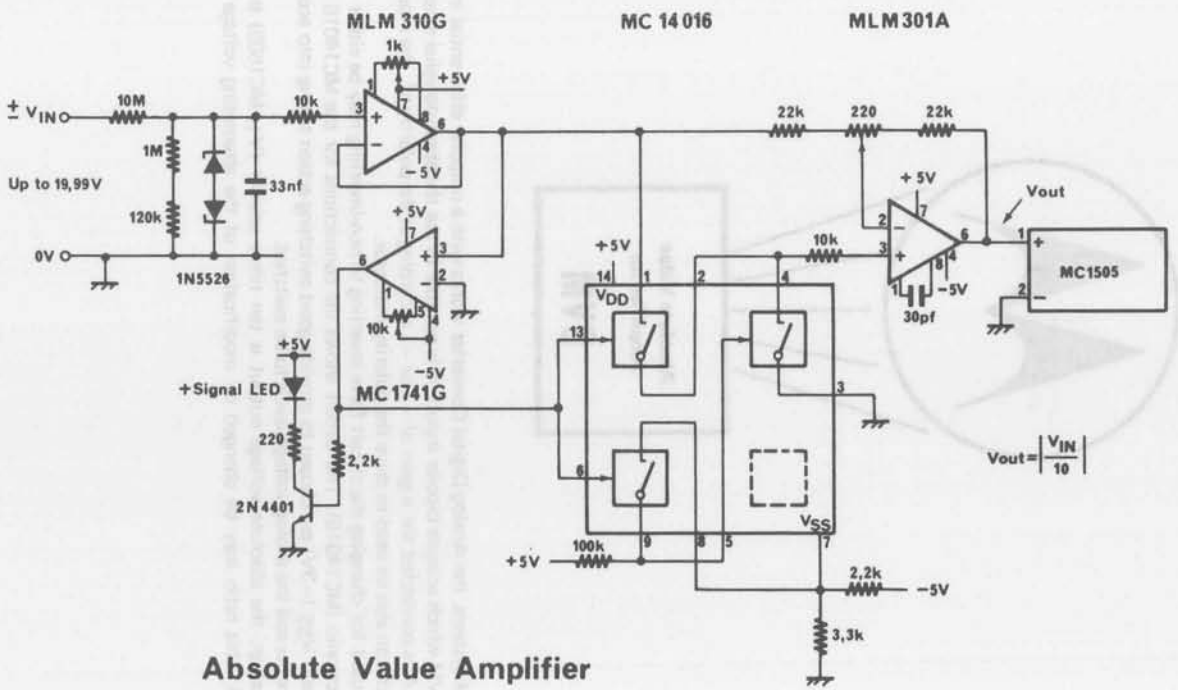
3

the ONE page

APPLICATION IDEA **FROM *MOTOROLA***



In many DVM systems, the Analog Digital Converter works with a unipolar differential input voltage. In order to obtain a DVM which accepts bipolar inputs, it is possible to use the absolute value amplifier shown here.
The MLM301A is connected for a gain of +1 or −1 according ot the polarity of the input, as detected by the MC1741, which can also be used to drive the polarity indicator.
The switches used for changing the circuit form inverting to non-inverting may be either mechanical (e.g. reed relays) or electronic (MC14016). The circuit shows the connections for the MC14016. The supply voltages V_{DD} (5V) and V_{SS} (−3V) are chosen to provide good switching action taking into account both the switch drive requirements and the analog voltage levels to be switched.
In this application, the absolute voltage output is ten times smaller (V_1, MC1505) than the input voltage (V_{IN}) applied. This ratio may be changed by modification of the alternating voltage divider at the input terminal.



Absolute Value Amplifier

APPLICATION IDEA FROM MOTOROLA

2.5% Resolution Analog Voltage Indicator

Digital voltmeters are accurate measuring devices but in some cases the display is not practical.
The Analog Voltage Indicator described here is ideal as an inexpensive display and is easy to build.

Description of the circuit

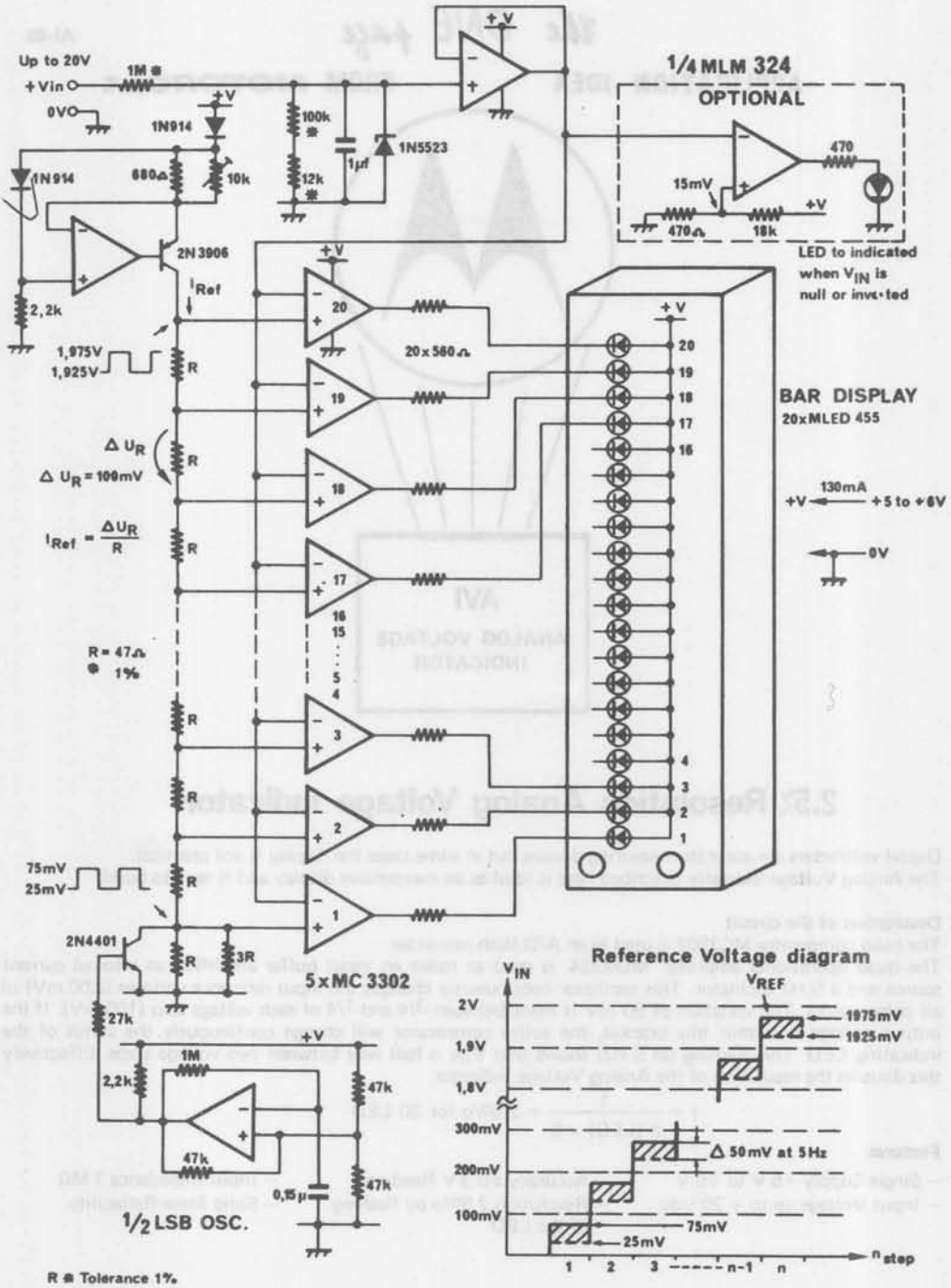
The quad comparator MC3302 is used as an A/D flash converter.
The quad operational amplifier MLM324 is used to make an input buffer amplifier, an internal current source and a 5 Hz oscillator. This oscillator continuously changes the input reference voltages (Δ50 mV) of all comparators. The variation of 50 mV is made between 3/4 and 1/4 of each voltage step (100 mV). If the output voltage is within this bracket, the active comparator will change continuously the status of the indicating LED. This flashing (at 5 Hz) shows that V_{IN} is half way between two voltage steps. Effectively this doubles the resolution of the Analog Voltage Indicator.

$$r = \frac{1}{n\,(LED) \times 2} = 2{,}5\%\ \text{for 20 LED}$$

Features

- Single Supply +5 V to +6 V
- Input Voltage up to + 20 Vdc
- Accuracy ± 0.3 V Reading
- Resolution 2.5% by flashing of the LED
- Input Impedance 1 MΩ
- Solid State Reliability

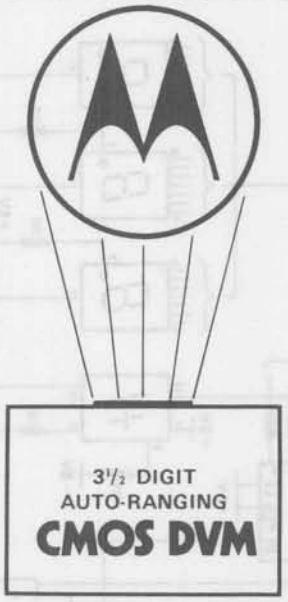
3



Analog Voltage Indicator

the ONE page

APPLICATION IDEA FROM *MOTOROLA*

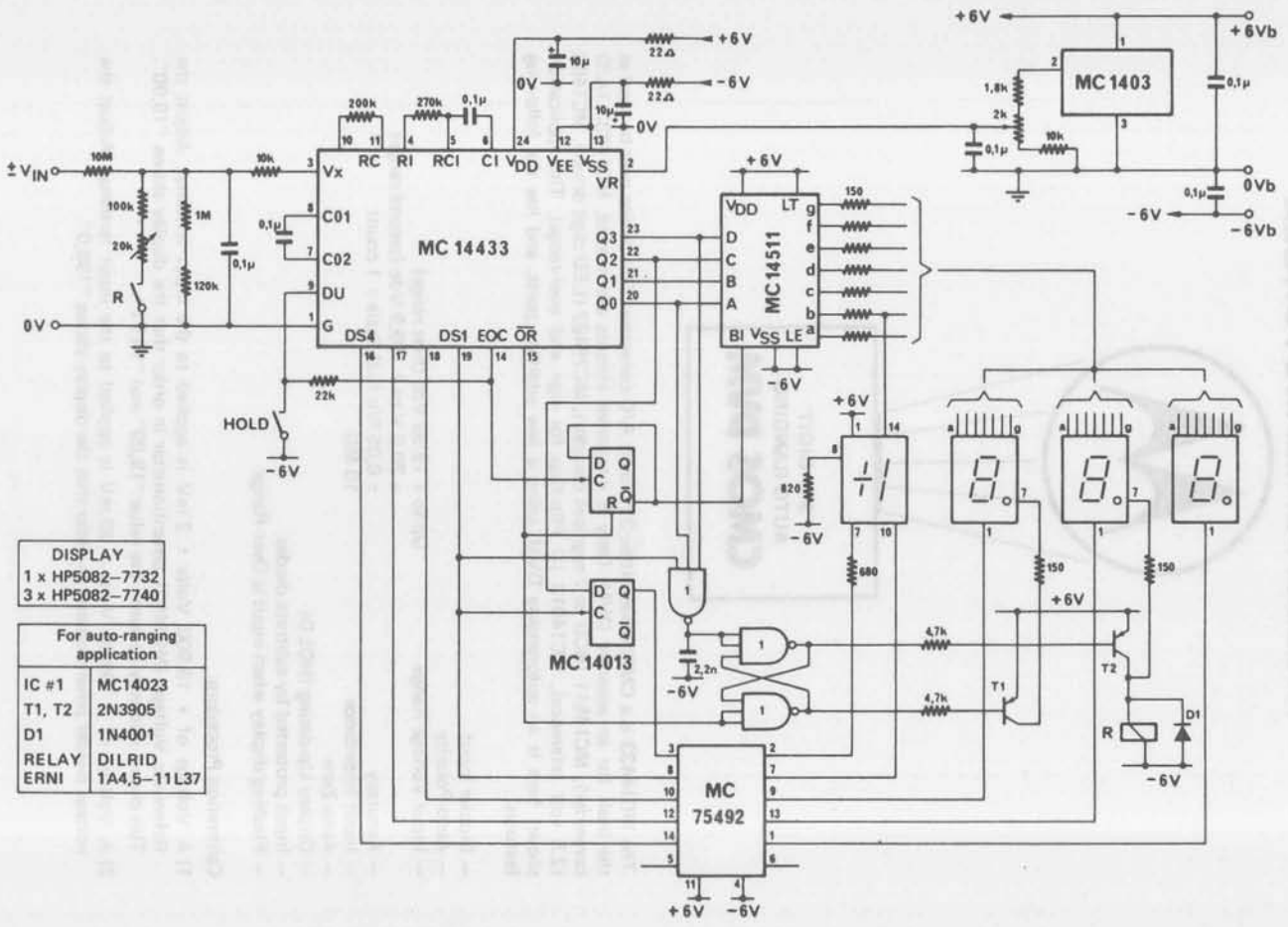


The MC14433 is a CMOS monolithic 3½ digit A/D converter. This device may be used as the basis for an accurate DVM. Only 5 integrated circuits are needed, MC14433 (A/D converter), MC14511 (BCD to 7-segment decoder), MC75492 (LED digit driver), MC1403 (2.5 volt reference), MC14013 (D Flip-flop for sign and over-range). The application shown here is an autoranging DVM, using a few addition parts, and has the following features:

- Bipolar input
- Auto-Polarity
- Input Voltage Range — Up to ± 19,99 Vdc (first range)
  ± 20,0 V to ± 199,9 Vdc (second range)
- Accuracy — ± 0,05 o/o Full Scale ± 1 count
- Input Impedance — 10 MΩ
- Auto-Zero
- Display Up-dating (HOLD)
- Input protected by subtrate diodes
- Flashing display when input is Over-Range

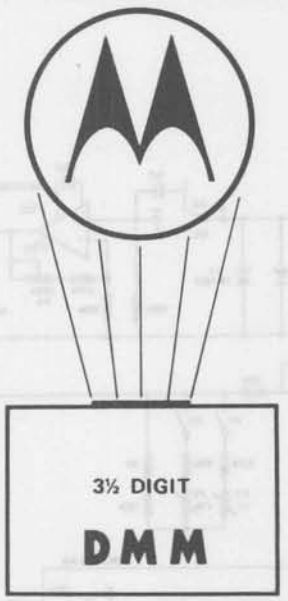
Calibration Procedure:

1) A Voltage of ± 19,900 Volts ± 2 mV is applied to the input terminal. Adjust the Reference Voltage (MC1403) potentiometer in order that the display shows "19,90". This occurs mid-way between the value "19,89" and "19,91".
2) A Voltage of ± 199,00 Volts ± 20 mV is applied to the input terminal. Adjust the voltage divider potentiometer in order that the display shows "199,0".


MC 14433
MC14511
MC 14013
MC 75492
MC 1403
HOLD
DISPLAY
1 x HP5082–7732
3 x HP5082–7740
For auto-ranging application
IC #1 MC14023
T1, T2 2N3905
D1 1N4001
RELAY ERNI DILRID 1A4,5–11L37

the ONE page

APPLICATION IDEA FROM *MOTOROLA*



The application shown here is an auto-ranging DMM for measuring voltages, currents, resistances and temperatures. The features are:

Voltage

AC or Bipolar DC
- up to 19,99 V
- 20,0 V to 199,9 V
- 200 V to 1000 V

} Three scale auto-ranging

Current

AC or Bipolar DC up to 1999 mA (Drop Voltage max. 0,36 V)

Resistance

- up to 1,999 KΩ
- 2 KΩ to 19,99 KΩ
- 20 KΩ to 199,9 KΩ

} Three scale auto-ranging

Temperature

−10 °C to +100,0 °C (Transistor Sensor)

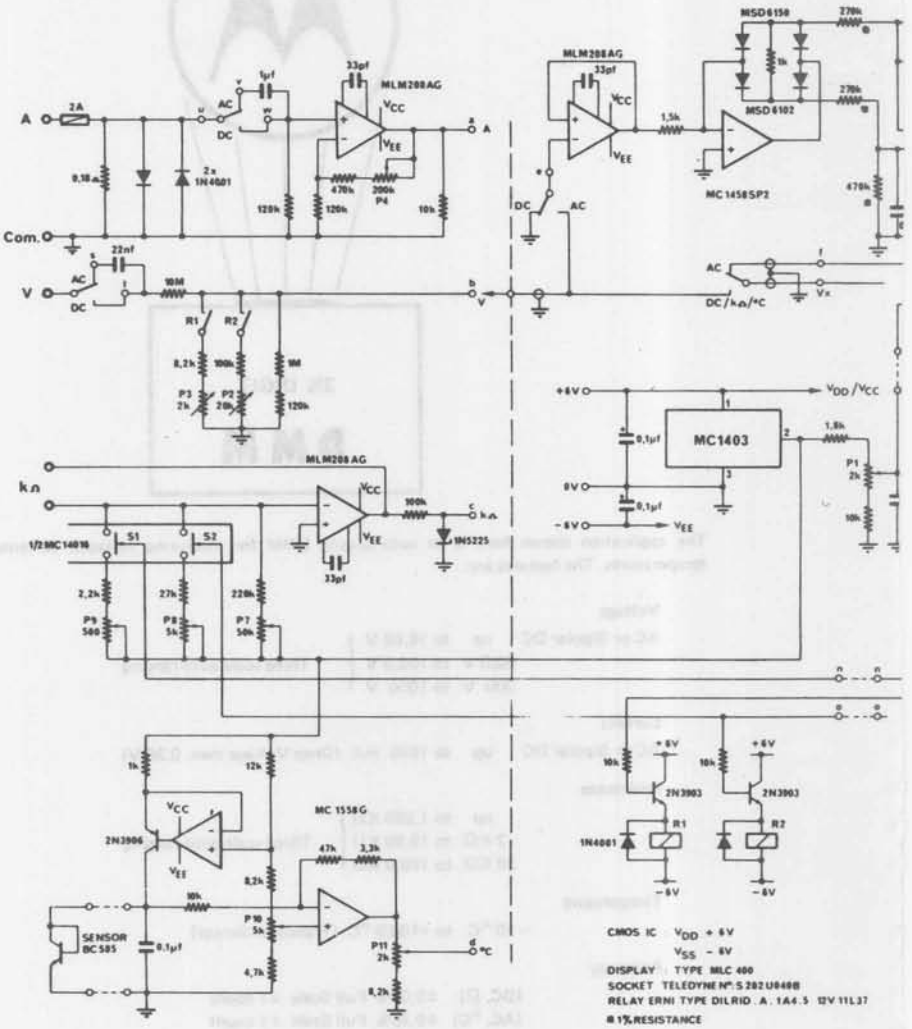
Accuracy

(DC, Ω) ±0,05% Full Scale ±1 count
(AC, °C) ±0,25% Full Scale ±1 count

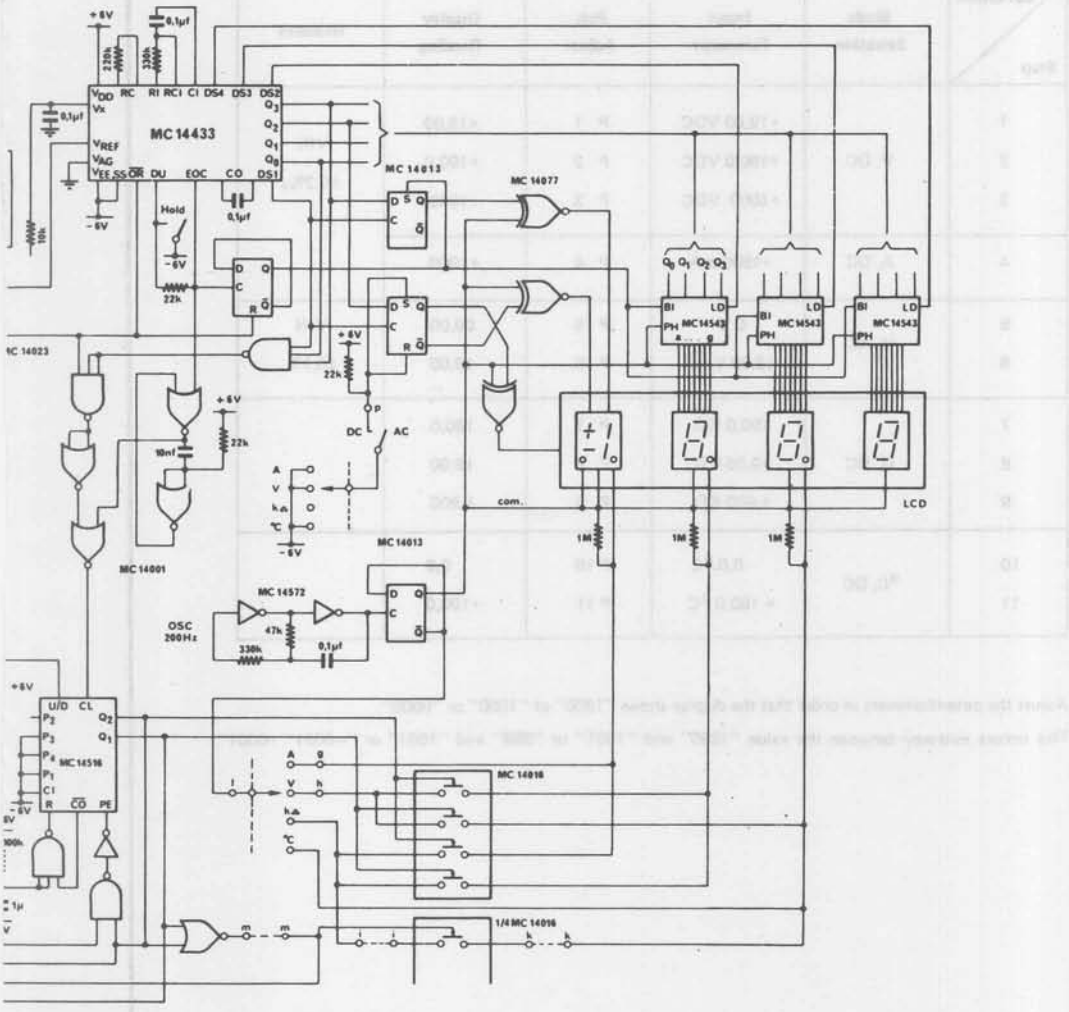
Display UP-dating (HOLD)

Flashing display when input is Over-Range

Low Consumption max. 200 mW


MLM208AG
MSD6150
MSD6102
MC1458P2
MC1403
MC1558G
MLM208AG
1/2MC14016
SENSOR BC585
2N3906
2N3903
2N3903
1N4001
1N5225
CMOS IC V_{DD} + 6V
V_{SS} - 6V
DISPLAY : TYPE MLC 400
SOCKET TELEDYNE N°: S 282 U 040 B
RELAY ERNI TYPE DILRID . A . 1A4 . 5 12V 11L37
1% RESISTANCE

3½ DIGIT MUL


MC14433
MC 14013
MC 14077
MC 14543
MC 14001
MC 14572
MC 14516
MC 14016
1/4 MC 14016
MC 14023
OSC
200Hz
Hold
DC
AC
com.
LCD
+6V
-6V
0,1µf
22k
47k
330k
10nf
1M

V.A.Ω. °C.

3

CALIBRATION PROCEDURE

Condition / Step	Mode Selection	Input Parameter	Pot. Adjust	Display Reading	Remarks
1	V, DC	+19,00 VDC	P 1	+19,00	VIN ±0,2‰
2		+190,0 VDC	P 2	+190,0	
3		+1000 VDC	P 3	+1000	
4	A, DC	+1900 mA	P 4	+1900	
5	V, AC	0 V	P 5	00,00	VIN ±0,1%
6		19,00 VAC	P 6	19,00	
7	Ω, DC	190,0 KΩ	P 7	190,0	
8		19,00 KΩ	P 8	19,00	
9		1,900 KΩ	P 9	1,900	
10	°C, DC	0,0 °C	P 10	0,0	
11		+ 100,0 °C	P 11	+100,0	

Adjust the potentiometers in order that the display shows "1900" or "1000" or "0000".

This occurs mid-way between the value "1899" and "1901" or "999" and "1001" or "−0001" +0001".

3

the ONE page

APPLICATION IDEA FROM MOTOROLA

- **Accuracy**
  ± 0.05% FS ± 1 count (DC)
  ± 0.2% FS ± 1 count (AC)
- **Resolution**
  3½ digit
- **Consumption** 200 mW
- **Display** UP-dating (hold)

AUTOMATIC
PORTABLE
DVM

- **Auto-Selection**
  of AC and DC
- **Auto-Ranging**
  up to 199.9 V
  200 to 1999 V
- **Auto-Polarity**

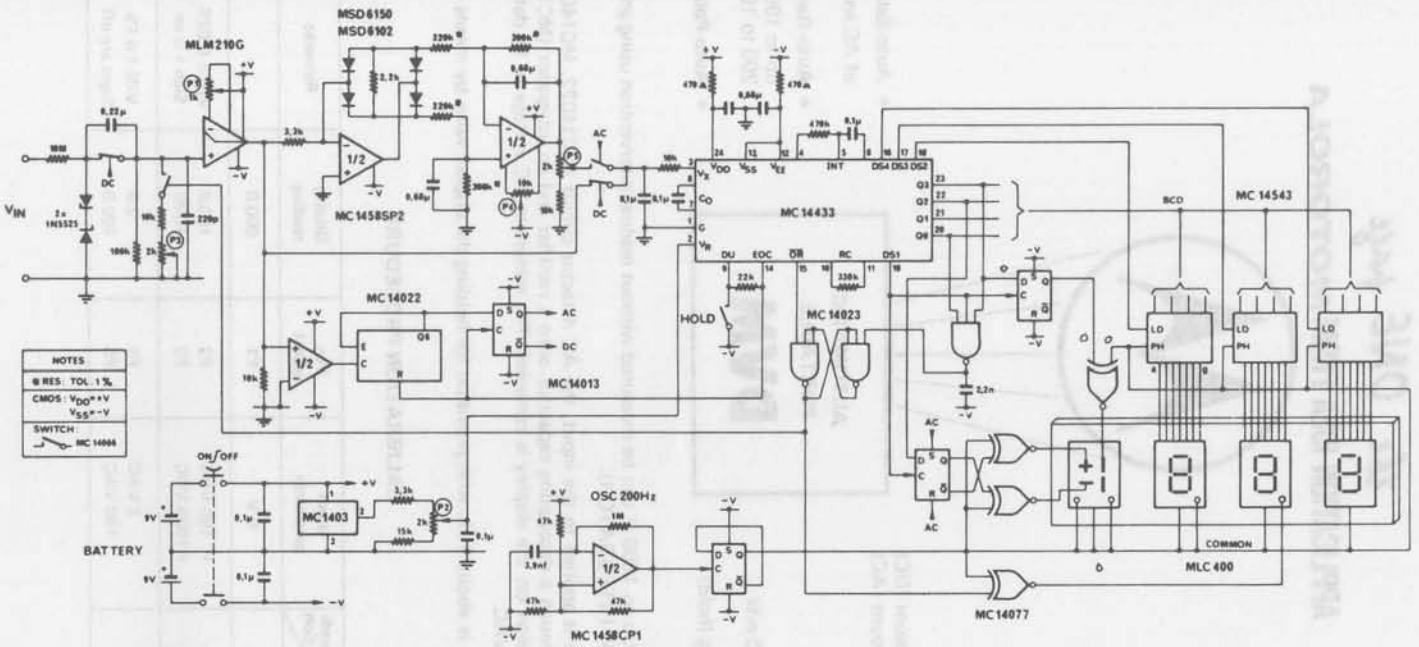
AC or DC voltages Up to 1000 V can be measured without manual intervention using an AC detector circuit (OVER FLOW INTEGRATOR).

When an AC voltage is applied to the input, the AC detector circuit (MC14022, MC14013) switches the inputs signal through a decoupling capacitor onto a rectifier and an integrator (MC1458SP2). At the same time the sign on the display is removed. The minimum AC voltage to be detected by the circuit is about 0,5 VAC.

The conversion rate is about 4 Hz with provision for holding the display value by means of the switch (hold).

CALIBRATION PROCEDURE

Step \ Condition	Input parameter	Pot. adjust	Display reading	Remarks
1	0 V	P1	000.0	
2	+ 190 VDC	P2	190.0	VIN ± 0.02%
3	+ 1000 VDC	P3	1000	Sign + is on
4	2 VAC	P4	2.0	VIN ± 0.1%
5	190 VAC	P5	190.0	Signs are off



PORTABLE AUTOMATIC DVM (AC and DC) UP to 1000 V

the ONE page

APPLICATION IDEA FROM MOTOROLA

Resolution 0.1 °C

PORTABLE DIGITAL THERMOMETER

–40 °C to +99.9 °C

Accuracy
± 0.3 °C at
Tamb = 0 °C to 50 °C

An accurate digital thermometer can be built with a transistor sensor (BC585) and an analog-to-digital converter (MC14433). The transistor sensor has a temperature coefficient of about –2 millivolts/° C. So with a Δt of 100 °C, the ΔV of the sensor will be 200 mV. Using the ratio-metric function of the MC14433 it is easy to calibrate the thermometer.

$$\underset{\text{(display)}}{\text{Vout}} = 2000 \frac{(V_X - V_{AG})}{(V_R - V_{AG})} \quad \text{where } V_X - V_{AG} = \Delta V \text{ (sensor)}$$

The voltage between V_{AG} and V_{EE} is calculated according to the specification on the Data Sheet, the resistance tolerance of 5% and a temperature of 0 °C for the sensor. The voltage between V_R and V_{AG} will be about 400 mV, according to the formula shown above.

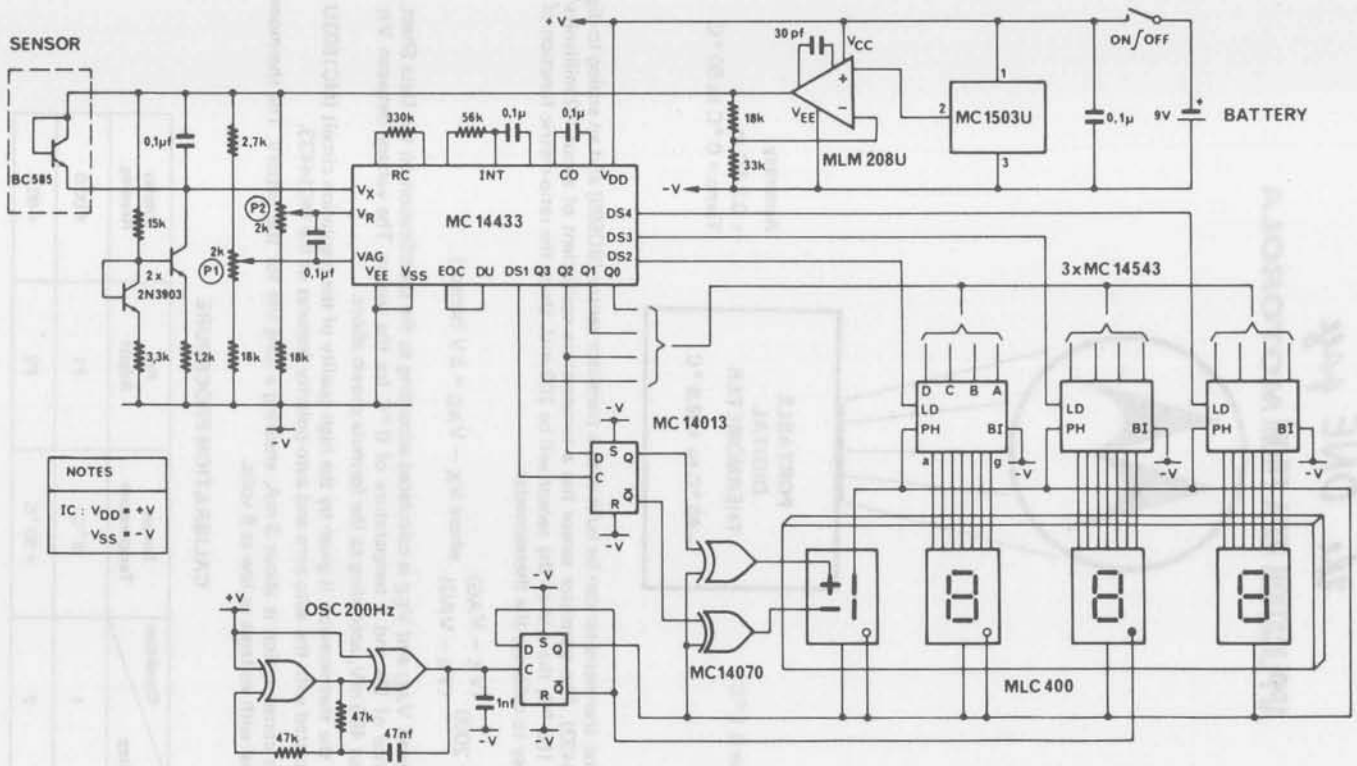
The accuracy of the thermometer is given by the high quality of the regulation circuit (MC1503U and MLM208U) associated with the auto-zero and auto-polarity features of the MC14433.

The total current consumption is about 3 mA, ensuring a long life for the battery. The thermometer remains functional with voltages as low as 8 volts.

3

CALIBRATION PROCEDURE

Step \ Condition	Sensor Temperature	Pot Adjust	Display Reading
1	0 °C	P1	± 00.0
2	+ 90 °C	P2	+ 90.0



PORTABLE DIGITAL THERMOMETER (-40°C to +99.9°C)

AN-321

Application Note

The acquisition and recovery of analog signals in a M6800 data processing system

Some practical examples of the interfacing required in analog data processing with microprocessors are discussed. A multi-channel process control data acquisition module and the graphic display of digital data on a standard X-Y chart recorder are presented as typical interface units.

3

The acquisition and recovery of analog signals in a M6800 data processing system

INTRODUCTION

The fundamental circuits used in processing analog signals by conventional methods include the operations of filtering and detection. These are, in fact, simplified electronic circuit realisations for the operations of convolution and correlation. The introduction of the digital computer into the realm of signal processing permits these mathematical operations to be performed in practice. Once the analog signal has been transformed into digital format, any required sequence of operations for processing the signal may be performed, simply by programming the computer accordingly.

On-line computation can now be envisaged, since computers are available as circuit components. However, the limitation remains, that total calculation time must be more rapid than the rate of data acquisition. The relatively slow speed of performing digital arithmetic operations therefore limits the on-line microprocessor system to applications in the audio and subsonic area (e.g. physiological signals, vibration analysis, servo-motor controllers) at present.

Since data acquisition can usually be performed faster than the rate of calculation, the techniques of off-line and batch processing can be advantageously employed in treating higher frequency signals. To illustrate this facility, we consider here the problem of data acquisition to meet the requirements of a process control application. The time delay and/or change of time scale implied in off-line processing often necessitates visual displays (e.g. CRT, chart recorder) of computed signal parameters over defined time windows. The example of such a graphic display using an X-Y recorder is discussed later.

In considering these particular examples, the basic features of sampled data processing must be understood. A brief description is included in the Appendix.

DATA ACQUISITION

3

The particular example taken here concerns multi-channel data acquisition for an on-line process control application using an M6800 system. A large number of slowly varying analog parameters have to be made available as inputs for the control algorithm being evaluated by the digital microprocessor. The control algorithm may call for any of the analog variables to be available in digital representation with an access time that is compatible with the response time of the control loop (including the calculation time of the processor). This restriction makes it impossible to use conventional data logging[1] owing to the long conversion time of an integrating analog-to digital converter. The requirement here is that an analog variable should be available for digital data manipulation by the M6800, with a minimum time delay after the appropriate software instruction. The solution adopted is to use successive approximation analog-to-digital conversion with a digitally controlled channel selector.

The specifications taken for a data acquisition module are the following:

- 8 single ended analog input channels (extension possible to 16).
- Input voltage excursion +5 to −5 Volts.
- Conversion accuracy 0.5‰ (10 bits with sign).
- Digital output compatible with M6800 bus.
- Conversion time less than 100 microseconds after software "request" for any analog variable (channel).

The input voltage variations are assumed to be less than ½ LSB (2,5 millivolt) during the inter-sampling period (100 microseconds). This obviates the need for a "sample and hold" circuit at the input to the converter.

The multi-channel analog to digital converter is to be interfaced with the M6800 bus structure. Several combinations using the MC6820, Peripheral Interface Adapter, have been described elsewhere[2]. However the organisation of hardware/software to achieve the specifications defined above, precludes the use of the MC6820, owing to access time limitations. This leads to the adoption of a multiplexed successive approximation register converter[3]

The interface to the M6800 system may still be realised a number of different ways, three of which will now be discussed in more detail.

(a) Direct Memory Access (DMA) is a means of entering the digital data from the converter directly into the M6800 system RAM without going through the MPU registers (for a detailed description, see the M6800 Applications Manual). In this case, the A/D conversion is free-running, converting the analog channels in a pre-determined order. (hardwired). Whenever a channel of digital data is ready for transfer into RAM via the data bus, the assigned address corresponding to that data channel must be generated externally for the MPU address bus.

The M6800 bus structure can be forced into 3-state (high impedance) condition, in order to accept the data, by using the GO/HALT line. Alternatively, the TSC line may be used and the clock generator stretched to permit "cycle stealing". More efficient still is to use rapid 3-state buffers to isolate the RAM (which must also have rapid access time for this application) from the rest of the MPU system. During clock cycle phase Ø1, the data may be written into the RAM, without affecting the MPU in any way.

The information transferred into the RAM by DMA will be the latest converted value, so is always available to the MPU by a standard software read command (LDA). This technique has the disadvantage that the analog multiplexing is not under MPU control. The rate of updating the RAM for one particular channel (analog bandwith) depends then on the rate and sequence of scanning the channels.

[1] Data acquisition networks with NMOS and CMOS - Motorola Application Note AN-770.

[2] Analog to digital conversion techniques with M6800 Microprocessor System – Motorola Application Note AN-757.

[3] Sucessive approximation A/D conversion - Motorola Application Note AN-716.

(b) Interrupt (IRQ) routines can be used to transfer a completed analog-to-digital conversion into the MPU registers. The free-running converter signals the end of the conversion (EOC) to the M6800 via the IRQ line. An interrupt service routine is used to store the result in a defined RAM location before returning to the original program. The updated value can be accessed from the RAM by a software read command (LDA). However when using interrupts, it should be remembered that the time between the IRQ occuring and access to the interrupt routine may be as long as 23 μs. Returning to the original program will take a further 10 μs. So much permanent dead time will seriously affect the computational speed and significantly reduce the response time, if the system is part of a control loop.

(c) Software command of the data acquisition system may be realised if the analog channel selection/analog-to-digital converter is hardwire coded so that it can be addressed directly by the MPU bus. The software request to read a desired analog channel will connect that analog channel to the A/D converter and trigger the start of conversion. When conversion is complete the result is transferred into the accumulator and computation proceeds.

Although some dead time is involved in waiting for the conversion to be performed. this only occurs while the software request for analog data is being serviced. In a real system, such requests will probably occur relatively infrequently at irregular intervals (compared with the A/D conversion time), so the loss of computing time may not be significant.

In view of the above discussion, the last technique as chosen for this application.

The requirement for working to an accuracy of 0.5‰ implies the use of a 10 bit successive approximation register converter. For convenience, two consecutive MPU data bytes are used, since the data bus in only 8 bits wide. The timing sequence of the latched bits of a successive approximation converter is well defined by the clock, so it is possible to handle the two most significant bits in one MPU data byte while the remaining eight bits are being determined by the converter. These latter 8 bits are then transferred as one byte into the MPU system. The "pipeline" organisation of the system is shown in figure 1.

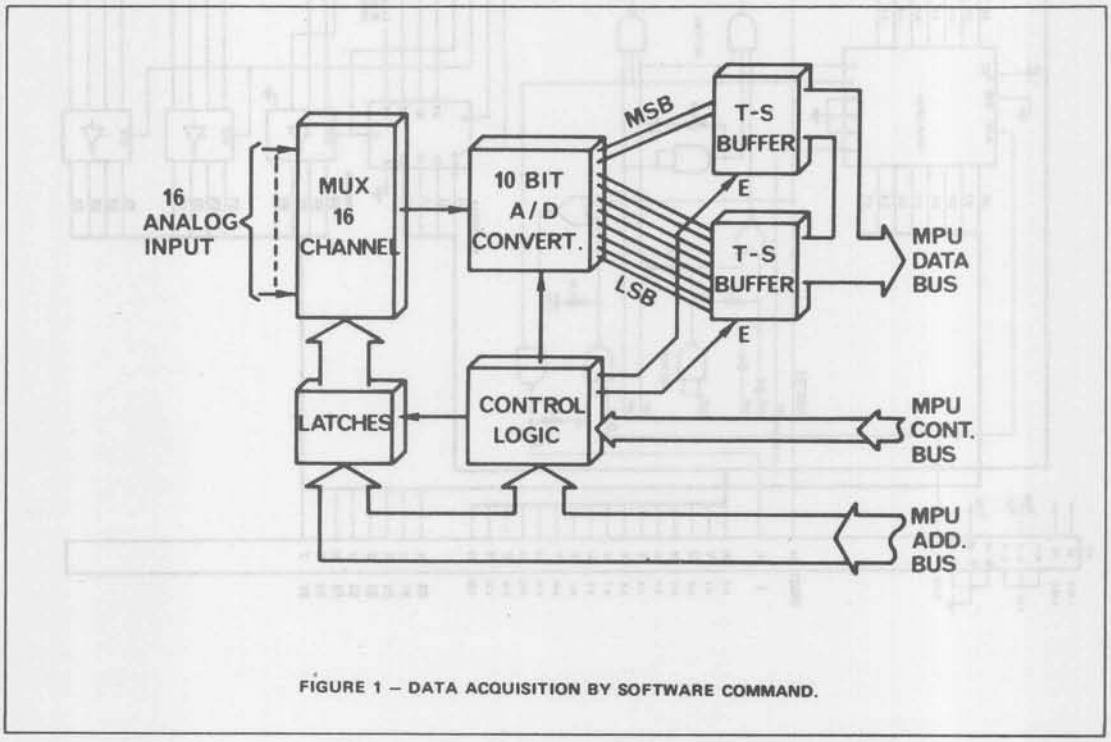


FIGURE 1 – DATA ACQUISITION BY SOFTWARE COMMAND.

To illustrate the use of this technique with a real example, an 8-channel data acquisition system has been built on an EXORciser card. The A/D converter (10 bit with sign) is not synchronous with the MPU clock. The circuit diagram of the board is shown in figure 2. This circuit permits the micro-computer (not shown) to request, by means of LDA software instructions, the two byte digital value of a desired analog channel. The result is made available in the A (LSB) and B (MSB) accumulators and also is stored in defined locations in the MCM6810 (random access memory) on the card.

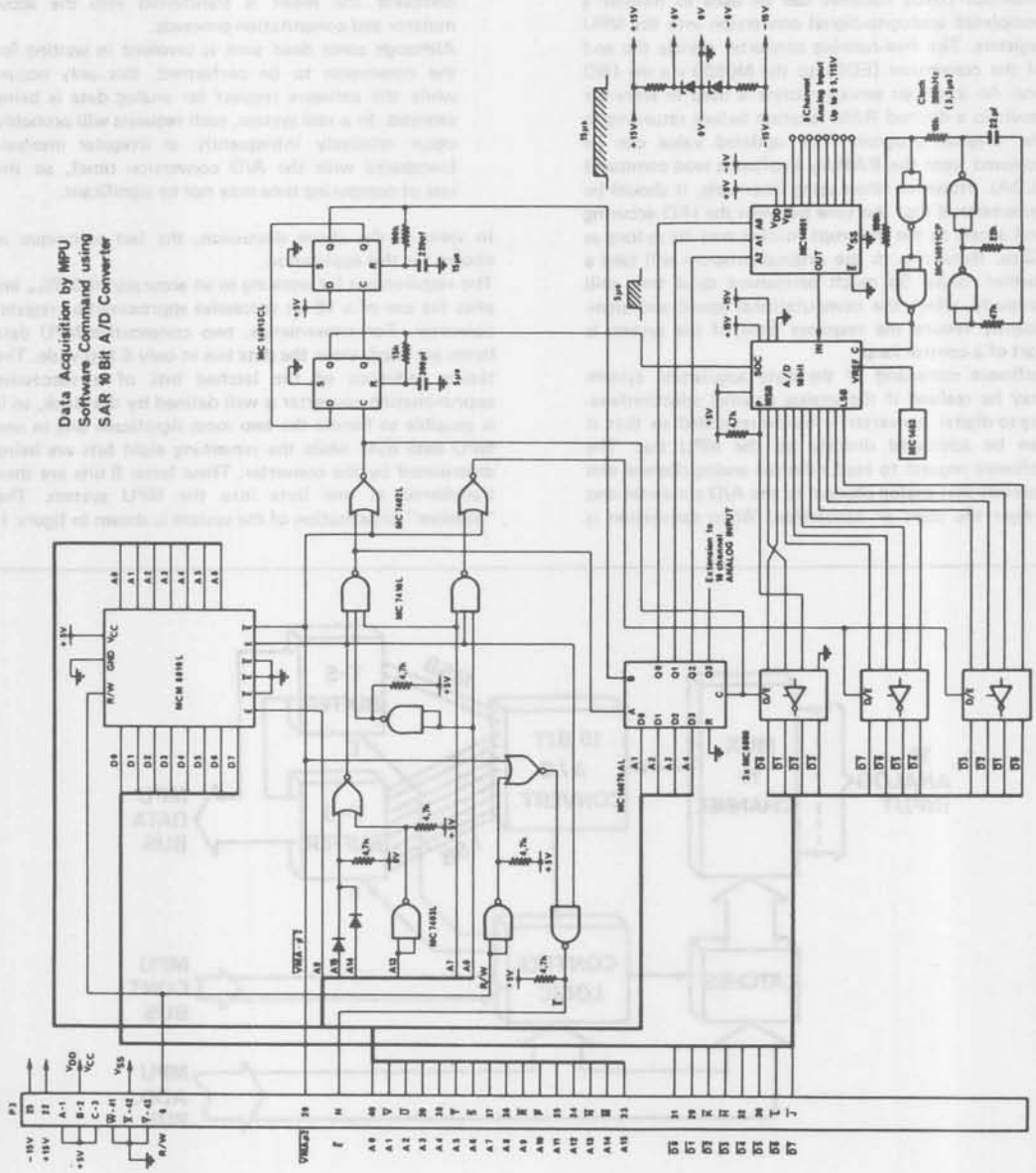


FIGURE 2 – BLOCK DIAGRAM

In this example, the following address assignments were used:

CHANNEL 1	2080/2081
CHANNEL 2	2082/2083
.	.
.	.
.	.
CHANNEL 8	208E/208F
RAM	2100/217F

A software instruction to read (LDA) any channel address is decoded on the card and starts the A/D converter (SOC line) with the analog multiplexer latched to the appropriate channel.

The timing diagram relevant to the sequence of operations is shown in figure 3. The conversion is completed approximately 55 μs after the first read instruction initiates the converter. An example of the use of this data acquisition card is in storing (in the RAM) the values of the 8 analog channels in rapid sequence. The software for this is shown here where the program is intended for use as a subroutine, with retrieval of index and accumulators included.

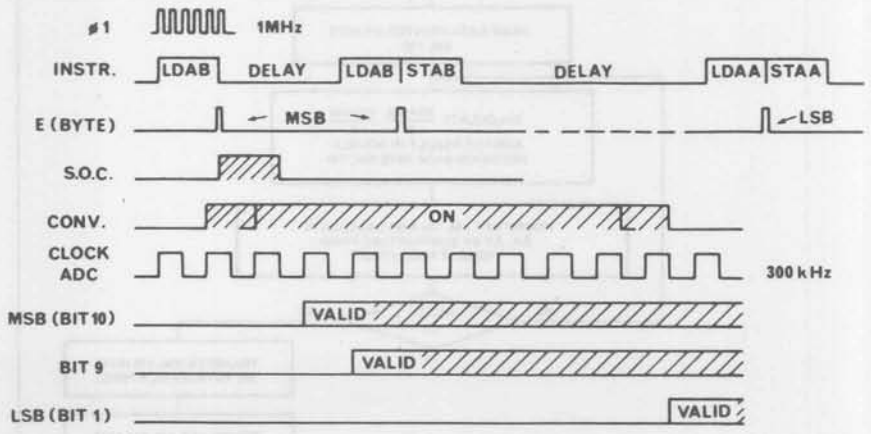


FIGURE 3 – TIMING DIAGRAM OF ONE CONVERSION

```
START   SEI                         Interrupt request masked
        PSH   A                     Save ACC.A
        PSH   B                     Save ACC.B
        STX           $2120         Save Index Register
        LDX           #$2080
        LDA   B       00,X          Start of Conversion (SOC)
        PSH   A                     Delay 4 μs
        PUL   A                     Delay 4 μs
LOOP1   NOP                         Delay 2 μs
        LDA   B       00,X          MSB BYTE Valid, SOC locked
        STA   B       $80,X         Final Data Memory (RAM)
        INX                         Prepare LSB BYTE Address
        PSH   A                     Delay 4 μs
        PUL   A                     Delay 4 μs
        PSH   A                     Delay 4 μs
        PUL   A                     Delay 4 μs
        LDA   A       00,X          LSB BYTE Valid
        STA   A       $80,X         Final Data Memory (RAM + 1)
        INX                         Prepare next channel input
        LDA   B       00,X          Next channel SOC
        CPX           #$2090        Need 16 BYTE for 8 channel
        BNE           LOOP1
        PUL   B                     Restore ACC.B
        PUL   A                     Restore ACC.A
        LDX           $2120         Restore Index Register
        NOP
        CLI                         Clear Interrupt Mask
        RTS                         Return
END
```

Note: that if a 16 channel multiplexer is used, then the CPX instruction must be raised by 16 more bytes (to $20A0).

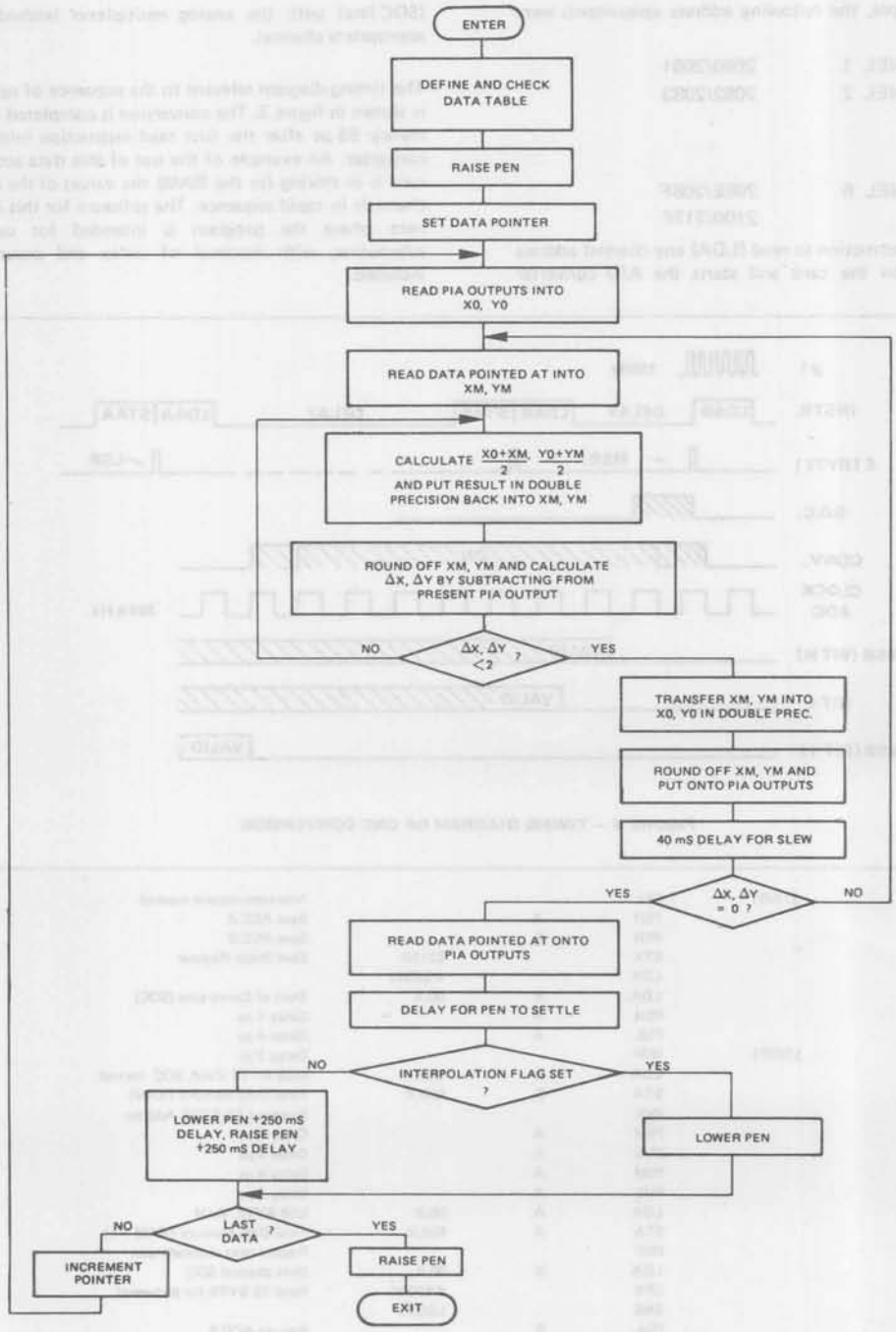


FIGURE 4 – CHART PLOTTER FLOW CHART

A distinct advantage of the system just described is that, once the digitisation process has been initiated, it is possible to predict exactly when the data will become available. The microcomputer could therefore be made to do useful work (not just stack shifting as shown in this example) during this time interval.

DISPLAY FOR DATA/GRAPHICS

Although acquisition, data manipulation, and output are now purely digital, a display of some parameters in analog form is very often needed. As pointed out in the Appendix, provided the data is defined at regular time intervals, respecting the Nyquist criterion, then complete signal recovery is possible by convoluting the digital data with the appropriate sinc function. Examining the more general case though, where the time intervals are not regular, which may occur when the data held in the memory represents discontinuous signals of graphic information, then the above procedure cannot be used to generate a visual display. The general case will now be treated in more detail, since it is also applicable to the specific case of signal display where the signal has been stored again after the convolution process has been performed. The two most common displays are the CRT (usually for on-line) or X-Y chart plotter where off-line hard-copies are required. This latter display will now be considered in more detail, since it is easily compatible with the M6800 as far as speed is concerned. The electro-mechanical parts of X-Y plotters are usually controlled either by stepper motors (digital pulse train inputs) or analog servo-motors (analog voltage inputs). In either case a dedicated interface circuit is usually employed, which relieves the host computer of the inefficient task of generating the slowly varying signals required to drive the pen correctly. A digital differential analyser (DDA) may be used, which generates incremental X and Y control signals based on the co-ordinates and graphic "primitive" information calculated by the host computer. Owing to the slow writing speed of standard X-Y recorders, a microcomputer can provide, at low cost, a viable general purpose interface which can easily calculate and generate the pen drive signals itself. The classical method would be to use it to calculate the characteristic co-efficients of the chosen "primitive" and evaluate the pen coordinates as X or Y (as appropriate) are slowly incremented. This procedure involve the formal operations of multiplication and division. For simplicity, the graphic "primitives" used here are restricted to straight line segments between points, so a less formal algorithm of "continuous averaging" is used to generate the pen movements, as discussed below.

The X, Y co-ordinates of the mid-point between the two points to be joined are calculated by subtraction and a right shift (in double precision). If the pen would have to move more than 1 bit to reach this point, the mid-point of the actual pen position and the previous average is calculated. This procedure is repeated until the difference is only one bit; the pen is then advanced to the calculated point. Averaging starts again, to obtain the next point; this continues repetitively until the pen is within one bit of the defined X, Y co-ordinates held in memory. The pen is finally advanced to this point, finishing the straight line traverse between the two sets of co-ordinates.

The flow chart describing this operation is shown here in figure 4.

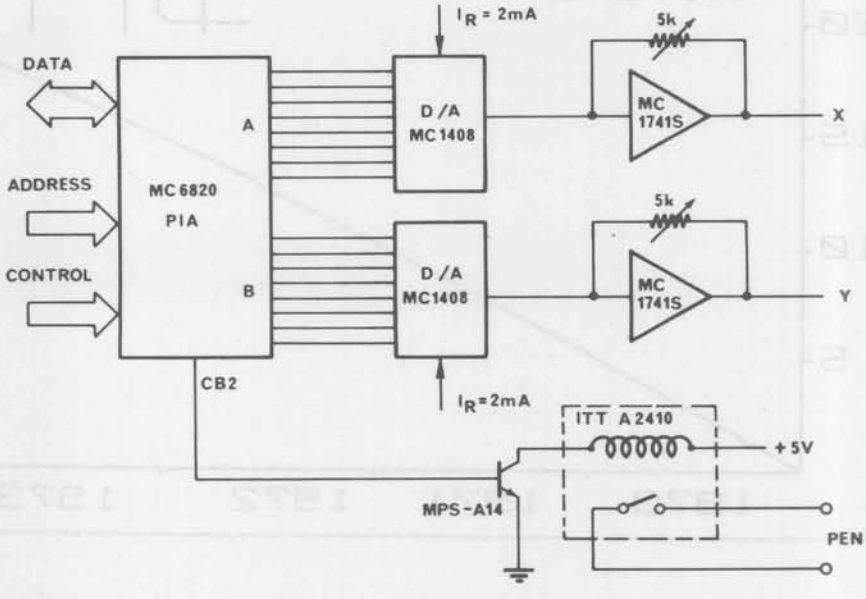


FIGURE 5 – GRAPHIC PLOTTER INTERFACE

A typical display unit is a Hewlett-Packard 7035B chart recorder. For this plotter, the precision of positioning the pen (±0.2%) is of the same order as the resolution of the 8 bit data bus. The display unit therefore only requires that two (X and Y) D/A converters (MC1408) be interfaced to the MPU bus via a PIA (MC6820). The circuit is shown in figure 5 where the peripheral control line, CB2, is also used to provide the pen-lift function. The gain of the X and Y channels may be adjusted independantly so as to obtain graphics suited to the particular paper size used.

If more than 8 bit precision is required (i.e. a more accurate plotter), double precision (2-byte) data becomes necessary. Both hardware and software now become more complex, but the same principle is applied in the interpolation for the pen movement.

A program for use with the HP7035B recorder has been written to allow one of three modes of operation to be selected by the user.

OPTION I – Plots straight lines between adjacent points specified by the co-ordinates held in memory. The data is unsigned and assumed to be in memory as a table; the lowest address specifies the first Y co-ordinate and the highest, the last X co-ordinate. Pen movement is slowed to 25 mm/sec. by software delay in order to avoid slewing errors.

OPTION P – Plots individual co-ordinate points with the pen lifted between points while traversing. Otherwise, identical to Option I.

OPTION T – Plots alphanumeric text as a series of straight lines. Part of the memory table contains the co-ordinates for alphanumerics. The appropriate addresses are called up by the ASCII code for the character required. Three possible sizes of character may be specifed by the user as well as the starting point for every line of text.

These three options are illustrated by the plot shown here in figure 6.

The basic program consists of about 700 bytes, while the alphanumeric ASCII character look-up table occupies another 700 memory bytes.

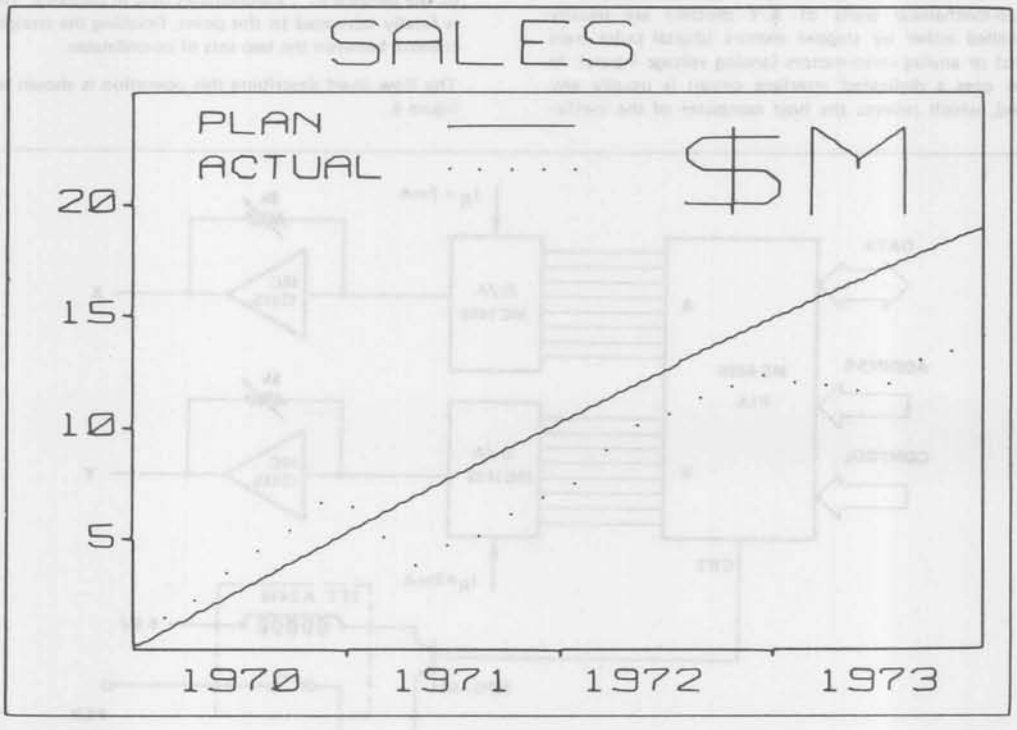


FIGURE 6

CONCLUSION

With suitable A/D and D/A conversion circuits, the microcomputer can be considered as a general purpose circuit component in the same sense as an operational amplifier. The defined task is specified by external components for an operational amplifier, while this function is performed by the software program in the case of the microcomputer. When processing analog signals, the advantages of using digital computation are in the stability and high accuracy achieved; the disadvantage is the speed restriction imposed in handling the sampled-data signals, so limiting the operational band-width. However, the impact of the microcomputer will be felt most in areas where the procedures used call for long storage time and for versatile algorithms which are adaptable in real time. In the low-frequency part of the spectrum, microcomputer calculations can be performed sufficiently rapidly to implement processing in real time. Higher frequency signals however can be treated off-line requiring an understanding of efficient data acquisition and display methods. The two examples described in this note are intended to be practical without resorting to discussions that may be too generalised.

APPENDIX

SAMPLED DATA SYSTEM CONSIDERATIONS

The input to a digital signal processor is a series of discrete quantized data points. In order that a continuously varying analog signal be compatible with the processor, an interface is needed which will make available the quantized values (with the required precision) at accurately known time intervals. For the purposes of this discussion it will be assumed that the quantisation is multi-level (binary coding) and that the time intervals are all identical. These are real restrictions, since a number of other useful representations do exist. However, accepting the above assumption, leads to the simplification that the interface has two functions, which can be considered separately. One is the data sampling function (sample and hold) while the other is the analog to digital converter. Both of these are well known to electronic engineers and the various possible implementations will not be discussed further here.

The decision to use regular sampling intervals imposes constraints on the analog input signal which is to be processed. From basic sampling theory developed by Shannon, any analog variable can be completely specified as a discrete time series, provided that sampling is performed at a frequency higher than the "Nyquist frequency". That is, above twice the frequency of the highest frequency component present in the analog signal. If the analog signal does not conform to this limitation then an over-lapping phenomenon known as "aliasing" can occur. In practice, the analog input signal is band-limited by using a suitable low-pass filter to attenuate the higher frequency components, so avoiding digitising incorrect values due to under-sampling.

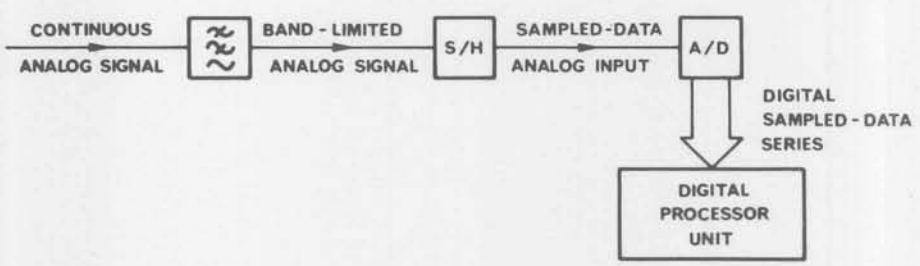


FIGURE 7 – SAMPLED DATA INPUT

The above procedure, illustrated in figure 7, describes a simple technique for entering data into a digital processor. However, the problems encountered in the inverse procedure for the reconstitution of analog signals from the digital processor output are not so widely appreciated. Continuous analog signals may be generated from a discrete time series by interpolation, the inverse procedure to sampling. Mathematically this necessitates the convolution of the output time series with the "sinc" function[4]. The convolution may be performed by an ideal low-pass linear phase analog filter, as shown in figure 8.
Such an ideal filter is not easy to realise; the usually adopted approximation is to use a first or second order low pass filter. This has to be designed so as to limit the interpolation distortion due to phase non-linearity to the same order as the precision of the D/A converter which preceeds it, a relatively simple task.

If the output signal is to be presented slowly enough (as when using off-line display) the convolution may be carried out in digital form by the processor itself. This necessitates the evaluation of the convolution process being performed faster than the slew-rate of the display device. Such a system, eliminating the analog low-pass filter, is a realistic possibility for the case of a chart recorder display.
The particular arithmetic manipulations carried out on the digital time series between digitisation and analog recovery will not be considered here. The actual processes are defined by algorithms usually in the time domain (e.g. Z-transforms) which are realized entirely by the software program, thereby giving the versatility and on-line adaptability which characterises this form of signal processing.

[4] $\text{sinc } x \triangleq \frac{\sin \pi x}{\pi x}$

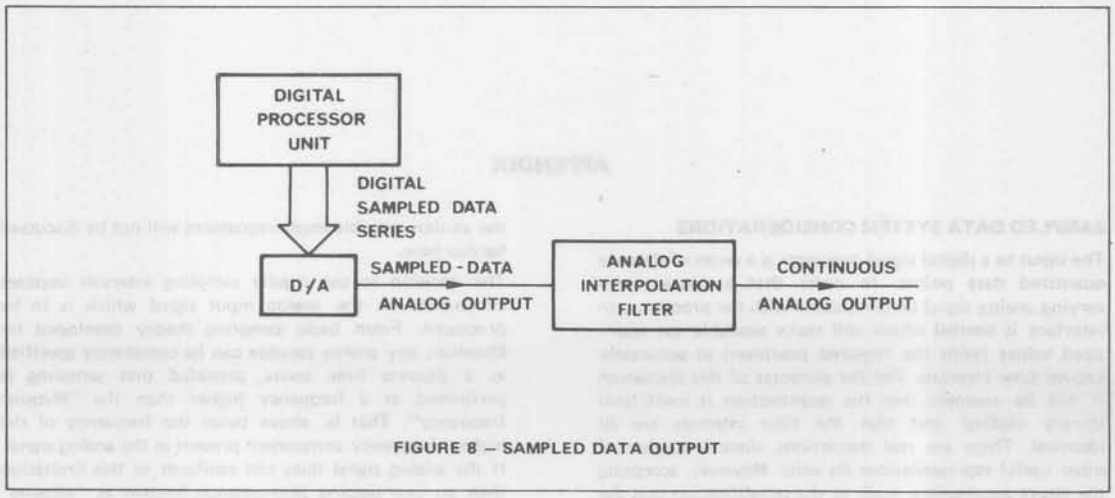


FIGURE 8 – SAMPLED DATA OUTPUT

A/D CONVERSION SERIES – Part IV

HIGH SPEED DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL TECHNIQUES

A brief overview of some of the more popular techniques for accomplishing D/A and A/D techniques. In particular those techniques which lead themselves to high speed conversion.

HIGH SPEED DIGITAL-TO-ANALOG AND ANALOG-TO-DIGITAL TECHNIQUES

INTRODUCTION

The world in which we live is truly an analog world. Data taken from anything that is tested or measured will usually appear in analog form and is difficult to handle, process, or store for later use without introducing considerable error. If data is taken frequently from a large number of sources, it will accumulate at such a rate that it becomes a burden and a major problem to the laboratory running the test. A digital computer has the capability of processing such data at rates comparable to those at which it was produced; however, the data must first be converted into a form usable by the digital computer. Then after the digital processing is complete, the digits must be reconverted to analog form to interface with the real world.

Although a pure analog system is capable of better accuracy than an analog-digital system, its accuracy is rarely completely usable because it is presented in a form that cannot be easily read, recorded, or interpreted with high accuracy. Digital data, however, is readily presented in numerical form regardless of the number of bits, and is just as easily manipulated, processed, and stored. Once data is converted into digital form it may be processed mathematically, sorted, analyzed, and used for control much more accurately and rapidly than with the analog data. If data must be "handled" much after it is acquired, it is safer to digitize it because there is little chance of error accumulation in successive manipulation. Further, digital data can be stored in many non-volatile types of memory devices.

The applications of A/D and D/A converters are almost unlimited. As the state-of-the-art of semiconductor technology advances, the cost of these conversion systems will continue to drop, and more system designers will be able to use A/Ds and D/As, which were before economically or physically impractical. A few current uses include: space telemetry systems, all digital voltmeters, voice security systems, closed loop process control systems (i.e., chemical plants, steel mills, etc.), in-flight checkout systems (to code the output of sensors so that a small computer on board can process the information), and hybrid computers use both A/D and D/A converters as a means of interfacing analog and digital computers to solve large system simulation problems. The listed applications indicate the versatility and represents only a small portion of the actual uses.

It should be obvious that the A/D converter that controls the ambient temperature of a large supermarket cannot encode the video information from an optical scanner; obviously, the system requirements are as different as night and day. There are many ways of performing A/D and D/A conversion, from very slow, inexpensive techniques to ultra-fast expensive ones. For the rest of this note, only the latter category will be discussed.

Appendix A is a glossary of terms pertaining to the subject of A/D and D/A conversion, and may benefit the reader in understanding the author's interpretation of some key terms.

Appendix B discusses several of the more common digital codes used with A/D and D/A conversion.

HIGH SPEED D/A CONVERTERS

Digital-to-Analog conversion can be accomplished by quite a number of methods. It is not the purpose of this discussion to give an exhaustive description of each type, but merely to mention a few of the more popular techniques and point out where they fit into the more specialized category of high speed D/A converters.

Voltage Output D/As

The output of a D/A converter can be an analog voltage or current. The voltage output types will be discussed first, since they are used most commonly and are easiest to understand.

Figure 1 shows the block diagram of a 3-bit voltage output D/A using weighted resistors and a summing amplifier. The summing resistors of an operational amplifier are weighted in binary fashion and are connected via an electronic switch to the reference or to ground, depending upon the state of each individual digital input. A digital "1" connects the resistor to the reference, and thus adds in its respective binary weighted increment. Although double-throw switches are shown, conceptually it is unnecessary to switch the resistor to ground when not connected to the reference. However, when single pole switches are utilized, the gain of the amplifier varies with the digital input and this affects bandwidth, dc offset, and drift. This variation is eliminated by the more expensive double throw switch.

A significant disadvantage of the simple weighted resistor approach of Figure 1 is that the accuracy and

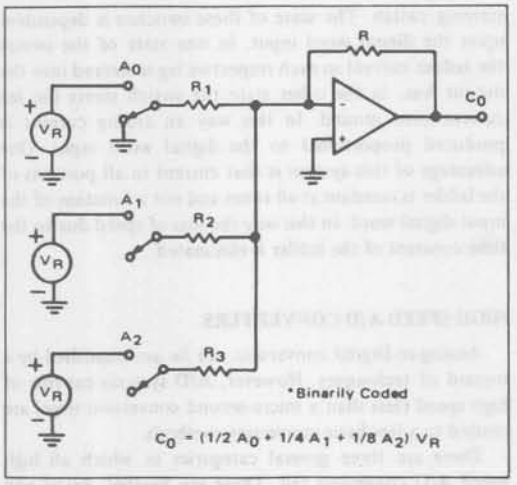


FIGURE 1 – Voltage Output Weighted Resistor Summing D/A

stability of this type of DAC is dependent upon the absolute accuracy of the resistors and their ability to track each other versus temperature. Since the input resistors all have different values, it is difficult to obtain identical tracking characteristics. Furthermore, since each input resistor's value is twice the preceding one, the absolute values become quite large. For higher resolution DACs it is also difficult, or at least expensive to get good stable resistors at such values. The high impedances, as well as the speed limitations of voltage switches and operation amplifiers, result in the voltage output DAC being relatively slow.

To overcome the problems relating primarily to the resistors, an alternate technique utilizing an R-2R resistive "ladder" network, shown in Figure 2, is generally used. Note, that if one leg of the ladder is connected to the reference by the electronic switch and the remaining are all grounded, a current is produced in the leg which "travels" through the ladder and gets divided by a factor of two at each junction. Thus, the contribution of current from that leg (e.g., bit) at the summing junction is binarily weighted in accordance with the number of junctions through which it has passed. The LSB (least significant bit) is therefore on the left in Figure 2.

One of the most significant advantages of the R-2R ladder approach is that the impedance as seen from the input to the op-amp is constant (equal to R). Hence, bandwidth, etc., do not change with digital setting. Of more significance, however, is the fact that all the resistors are either R or 2R. Note that the accuracy is *not* dependent upon the absolute value of all the Rs, but rather only their differences. Similarly, temperature effects are only significant with respect to how well all the Rs and 2Rs *track* each other, respectively. Since the value of R can be any convenient value (0.1 k to 50 k), ladder networks are a natural for monolithic diffusion or deposition, which further improve their tracking capability. Also, the impedance levels can be kept sufficiently low to minimize bandwidth limitations due to stray capacitance.

Another type of R-2R ladder, voltage output D/A, is shown in Figure 3. This circuit is very similar to the one just described, except equal value current sources are switched into the nodes of the ladder rather than switching the "legs" of the ladder between voltages. Simply network theory will show that the effect of each current, at e_0, is the same as in the previous circuit, hence they are binarily weighted.

For several reasons, currents may be switched much more rapidly than voltages. This gives the current source D/A an increase in speed by at least one order of magnitude. Because of this switched current-source R-2R ladder D/A is one of the types most often used in high speed voltage-output D/As. This technique, because of the R-2R ladder and current switching, lends itself to monolithic fabrication.

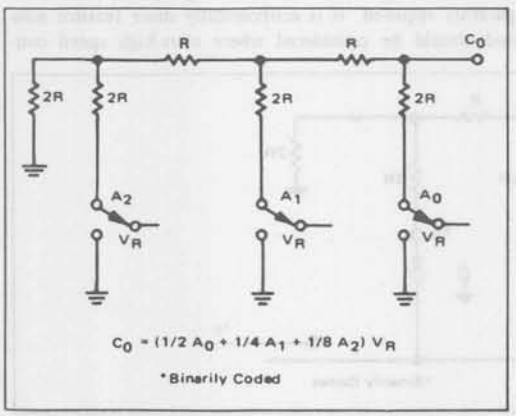


FIGURE 2 – Switched Voltage Source R-2R Ladder D/A

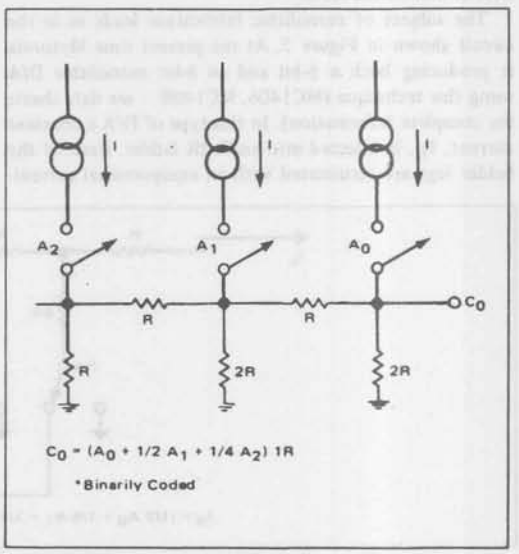


FIGURE 3 – Switched Current Source R-2R Ladder

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Current Output D/As

This type of D/A can be implemented by generating binarily-weighted currents, preferably from active sources, and summing these on a common bus. Figure 4 shows a block diagram of a D/A using this principle.

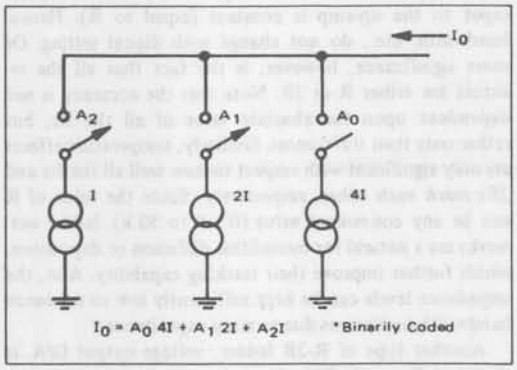


FIGURE 4 – Current Output D/A Using Weighted Current Sources

In an actual circuit the switches controlled by the digital word input, would simply be current steering circuits, not on-off switches as shown. Current from a current source would either be steered into the output bus or into another node of the circuit. This type of switching is the fastest method of current switching available; switching speeds of less than a nanosecond are possible with emitter coupled logic (MECL).

The weighted current source D/A technique is also a method that can easily be implemented in monolithic form. It is the opinion of this author that this system offers the best possibility of producing a truly high-speed D/A in monolithic form.

The subject of monolithic fabrication leads us to the circuit shown in Figure 5. At the present time Motorola is producing both a 6-bit and an 8-bit monolithic D/A using this technique (MC1406, MC1408 – see data sheets for complete information). In this type of D/A a constant current, I_L, is injected into an R-2R ladder. Each of the ladder legs are terminated with an equipotential current-steering switch. The state of these switches is dependent upon the digital word input. In one state of the switch the ladder current in each respective leg is steered into the output bus, in the other state the switch steers the leg current into ground. In this way an analog current is produced proportional to the digital word input. One advantage of this system is that current in all portions of the ladder is constant at all times and not a function of the input digital word. In this way the loss of speed due to the time constant of the ladder is eliminated.

HIGH SPEED A/D CONVERTERS

Analog-to-Digital conversion can be accomplished by a myraid of techniques. However, A/D systems capable of high speed (less than a micro-second conversion time) are limited to a few basic conversion methods.

There are three general categories in which all high speed A/D converters fall. These are Parallel, Serial and Combination. In a parallel conversion technique, all of the bits are converted simultaneously by many circuits in parallel. In a serial type of A/D each bit is converted sequentially one at a time. The third category, combination, is simply a combination of the previous two.

In general the parallel systems are faster and more complex than the serial types. The combination types are simply a compromise between speed and complexity.

The Parallel A/D (Flash)

In the parallel method, all bits of the digital representation are determined simultaneously. It is called the parallel method because of the configuration; a bank of voltage comparators, each responding to a different level of input voltage. This method is also called "Flash" encoding. Figure 6 shows the block diagram.

Characteristic of this configuration, it can be shown that for n-bits of binary information the system requires 2^n-1 comparators, and each comparator determines one LSB level. Unitl recent advances in the state-of-the-art of integrated circuits, this method was prohibitive if "n" were very large because of the large quantity of comparators required. It is economically more feasible now and should be considered where ultra-high speed con-

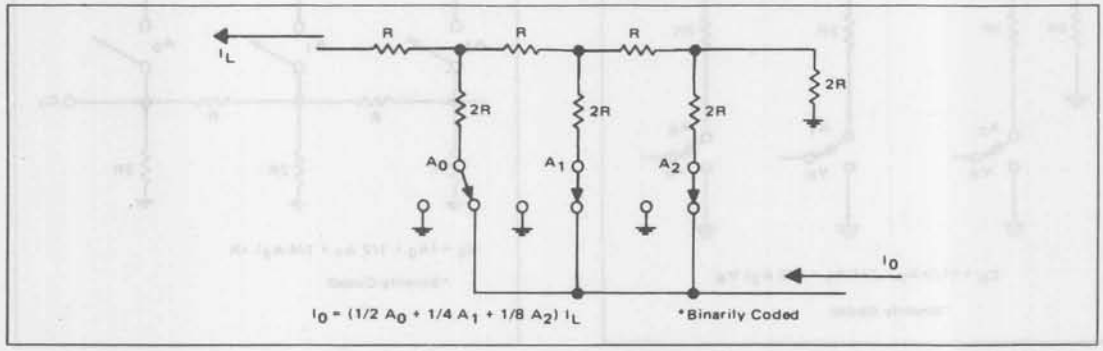


FIGURE 5 – Current Output R-2R Ladder D/A

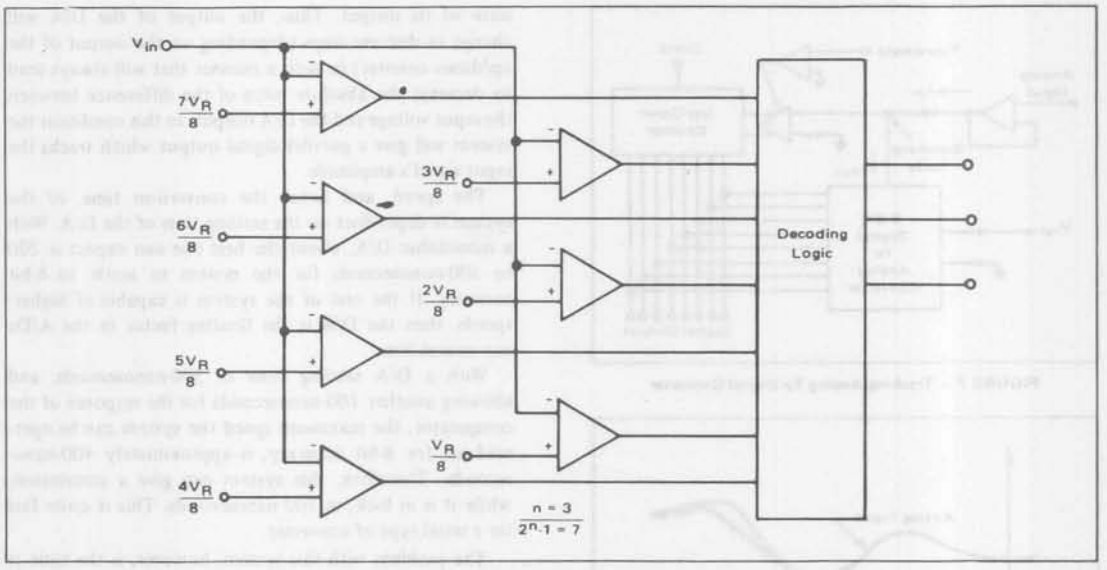


FIGURE 6 – Parallel A/D Block Diagram (Flash)

version is required. As MSI and LSI circuits become more and more common, it is very likely that a semiconductor manufacturer could produce a one chip A/D of 4-6 bits on one monolithic IC. It is the opinion of this author that this is an interim solution at best because the performance of such a device could not match those of the discrete circuits. And there are other techniques, some of which will be discussed later, that suggest more attractive performance specifications per nano-acre than that of the Flash system at lower cost.

One disadvantage of this system is that the output of the comparator bank is not directly usable information. These 2^n-1 outputs must be converted to binary information in some sort of binary code. (For more information on coding, see Appendix B.) For large values of n, the massiveness of the conversion logic not only increases cost and complexity, but requires more successive stages, thus increasing the conversion time.

The parallel converter is essentially asynchronous by the nature of its construction, and can be used effectively in both multiplexing or continuous tracking mode. It should be noted that often times a set of latches and a clock are added to this system to store and up-date the output in a clocked manner. This is done because the output of the Flash system can give erroneous glitches during a change from one value to another.

Specific requirements of the complete system determine the type of comparator needed. With this system since 2^n-1 comparators are used, the total input bias current of the system is one of the comparator's input bias currents multiplied by 2^n-1. This figure can be quite high if "n" is on the order of 6 to 8 bits.

Most comparators and digital logic circuits have a relatively fixed propagation delay. If parts are selected with this feature, the system can be preloaded. This means that a new signal can be injected to the system before the system has had time to completely convert the previous signal. While one signal is propagating through the digital logic a new signal is applied to the comparators. The digital logic operates on this signal while the comparators convert a new signal. This procedure will, in effect, decrease the total conversion time. However, it must be attempted with great care, since timing problems can arise in this sort of configuration.

Tracking Type of A/D

The Tracking A/D derives its name from the fact that the digital output continuously "tracks" the analog input voltage. This type of A/D is usually used in communications systems or some other application where the input is a continuously varying signal.

The Tracking type of A/D is one of several systems that use a Digital-to-Analog converter (D/A) in a feedback path to make an A/D. With this type of converter the accuracy can be no better than the D/A being used, (usually 6-10 bits).

Figure 7 shows the block diagram of the Tracking type A/D. There are two operating modes of the Tracking A/D. The first of these is when the A/D is "locked" on the signal and is "tracking" with it. The system will stay "locked" onto the signal as long as the signal does not increase or decrease in amplitude faster than the A/D system can "track" with it. The other mode of operation occurs when the system is just turned on or the signal has changed amplitude faster than the A/D could follow. When this occurs the system is "out of lock" and the A/D generates a staircase, in the direction of the input siganl change, until it again reaches the input voltage and acquires "lock" again. Figure 8 shows the waveform generated by

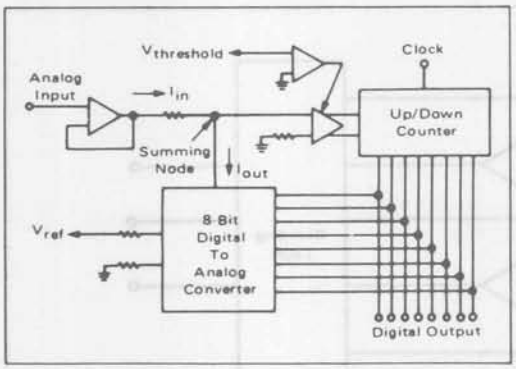


FIGURE 7 – Tracking Analog To Digital Converter

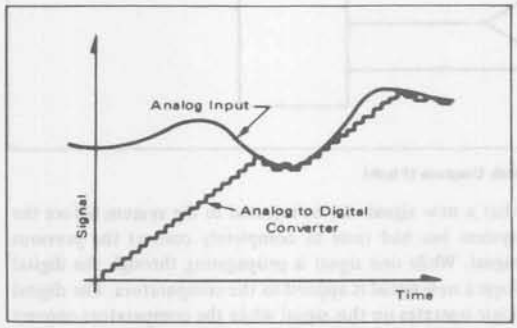


FIGURE 8 – Tracking Analog To Digital Converter Waveforms

the output of the D/A and the input signal plotted on the same set of axes. This figure shows both the "locked" and "out of lock" conditions.

Conversion time, for this type of A/D is a very nebulous thing. As long as the A/D is "locked" onto the signal, the conversion time is now the time required for the system to acquire lock again. This time will vary, depending on the absolute value difference between the output voltage of the D/A and the input signal. One can see from this that this system would be good if the requirement is to continuously monitor a slowly changing signal. If, however, the input signal varies in steps, as the case of several different signals being multiplexed, this particular system would not be a proper choice.

In operation the D/A generates a voltage output with a possible 2^n discrete step, the value of this voltage being directly proportional to the digital "word" that is on the digital inputs of the D/A. A comparator in the system compares the output of the D/A to the input voltage and gives an output signifying whether the input is above or below the D/A voltage.

Also included in the system is an n-bit up/down counter and a free-running oscillator or clock. The "n" outputs of the up/down counter are connected to the input of the D/A, thus determining its output voltage. The "n" outputs of the counters are also the digital output of the A/D.

The output of the comparator causes the up/down counter to count either up or down, depending on the state of its output. Thus, the output of the D/A will change in discrete steps (depending on the output of the up/down counter) in such a manner that will always tend to decrease the absolute value of the difference between the input voltage and the D/A output. In this condition the system will give a parallel digital output which tracks the input signal's amplitude.

The speed, and hence the conversion time, of the system is dependnet on the settling time of the D/A. With a monolithic D/A, about the best one can expect is 200 to 300-nonoseconds for the system to settle to 8-bit accuracy. If the rest of the system is capable of higher-speeds, then the D/A is the limiting factor in the A/Ds conversion time.

With a D/A settling time of 300-nanoseconds, and allowing another 100-nanoseconds for the response of the comparator, the maximum speed the system can be operated at, for 8-bit accuracy, is approximately 400-nanoseconds. Therefore, this system can give a conversion, while it is in lock, in 500 nanoseconds. This is quite fast for a serial type of converter.

The problem with this system, however, is the time it takes the A/D to reacquire lock once the signal is lost. In the absolute worst case, it could take 2^n clock pulses! This is very poor indeed. In order to prevent this condition in operation, the slew rate of the input signal must be limited.

In most applications, the operational characteristics of the Tracking A/D are undesirable. However, there are applications where its "unique" features are not detrimental and in these cases the Tracking type of A/D can be a very powerful, economical system.

Motorola will soon offer a new IC which is useful in implementing the Tracking A/D converter technique. The type MC1507L contains a high-speed op amp and a dual threshold comparator with separate UP and DOWN outputs. Both thresholds may be adjusted simultaneously by varying a reference voltage input.

Combining the MC1507 with either a MC1506L or MC1508L-8 D/A Converter and a pair of UP/DOWN counters produces a relatively inexpensive tracking converter. The MC1507 data sheet also shows a method of speeding up the clock to hasten the conversion time under the conditions when the system gets out of lock. This option requires use of a second MC1507 function block.

Successive Approximation A/D

The Successive Approximation (S/A) type of A/D is a serial system which uses a D/A in a feedback loop. It is relatively slow compared to other types of high-speed A/Ds, but its low cost, ease of construction, and system operational features more than make up for its lack of speed in many applications. It is by far the most widely used A/D system in use today.

Figure 9 shows the block diagram of the system. In operation, the system enables the bits of the D/A one at a time, starting with the most significant bit (MSB). As each bit is enabled, the comparator gives an output

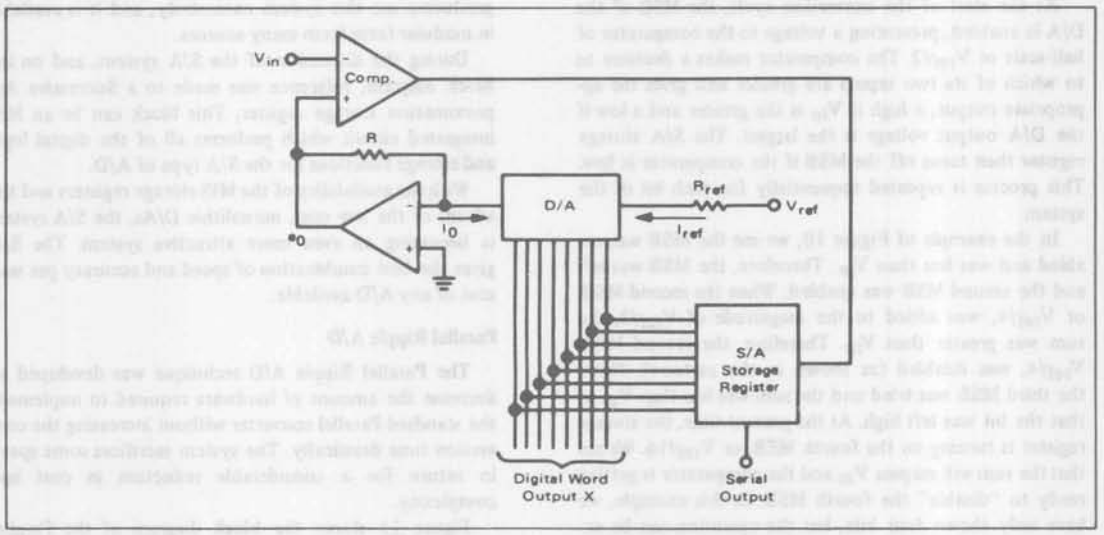


FIGURE 9 – Successive Approximation Block Diagram

signifying that the input signal is greater or less in amplitude than the output of the D/A. If the D/A output is greater than the input signal, the bit is "reset" or turned off. The system does this with the MSB first, then the next most significant bit, then the next, etc. After all the bits of the D/A have been tried, the conversion cycle is complete. At this time, another conversion cycle is started. The operation of the system can easily be understood by referring to Figure 10. This cartoon shows the system in actual operation.

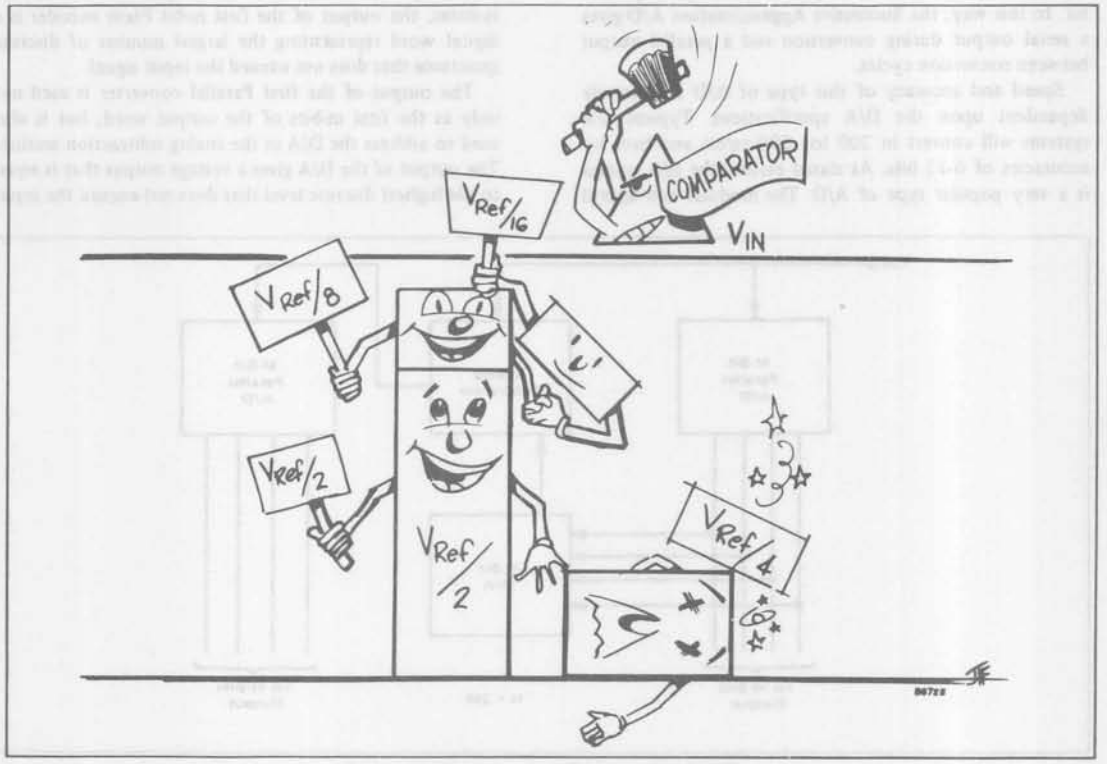


FIGURE 10 – Successive Approximation

At the start of the conversion cycle, the MSB of the D/A is enabled, presenting a voltage to the comparator of half-scale or $V_{ref}/2$. The comparator makes a decision as to which of its two inputs are greater and gives the appropriate output, a high if V_{in} is the greater and a low if the D/A output voltage is the largest. The S/A storage register then turns off the MSB if the comparator is low. This process is repeated sequentially for each bit of the system.

In the example of Figure 10, we see the MSB was enabled and was less than V_{in}. Therefore, the MSB was left and the second MSB was enabled. When the second MSB, or $V_{ref}/4$, was added to the magnitude of $V_{ref}/2$, the sum was greater than V_{in}. Therefore, the second MSB, $V_{ref}/4$, was disabled (as shown in the cartoon). Next, the third MSB was tried and the sum was less than V_{in} so that the bit was left high. At the present time, the storage register is turning on the fourth MSB, or $V_{ref}/16$. We see that the sum will surpass V_{in} and the comparator is getting ready to "disable" the fourth MSB. In this example, we have only shown four bits, but the operation can be extended to as many as desired. After the conversion cycle has completed the address of the D/A is the parallel binary word output of the A/D.

The serial output of the system is taken from the output of the comparator. While the system is in the conversion cycle, the comparator output will be either low or high, corresponding to the digital state of the respective bit. In this way, the Successive Approximation A/D gives a serial output during conversion and a parallel output between conversion cycles.

Speed and accuracy of this type of A/D are directly dependent upon the D/A specifications. Typical S/A systems will convert in 200 to -500-ns/bit and have bit accuracies of 6-12 bits. As stated earlier, the S/A system is a very popular type of A/D. The modular and hybrid producers use this system extensively, and it is available in modular form from many sources.

During the discussion of the S/A system, and on the block diagram, reference was made to a Successive Approximation storage register. This block can be an MSI integrated circuit which performs all of the digital logic and storage functions for the S/A type of A/D.

With the availability of the MIS storage registers and the advent of the low cost, monolithic D/As, the S/A system is becoming an even more attractive system. The S/A gives the best combination of speed and accuracy per unit cost of any A/D available.

Parallel Ripple A/D

The Parallel Ripple A/D technique was developed to decrease the amount of hardware required to implement the standard Parallel converter without increasing the conversion time drastically. The system sacrifices some speed in return for a considerable reduction in cost and complexity.

Figure 11 shows the block diagram of the Parallel Ripple type of A/D. Basically, the system consists of two each, m-bit Parallel converters, and an m-bit D/A. The total system has an n-bit output, where n = 2m. In this system both the parallel converters and the D/A-subtraction circuits must be n-bit accurate!.

In operation, the A/D converts the first m-bits of the output by the standard flash technique. As in most A/D systems, the output of the first m-bit Flash encoder is a digital word representing the largest number of discrete quantums that does not exceed the input signal.

The output of the first Parallel converter is used not only as the first m-bits of the output word, but is also used to address the D/A in the analog subtraction section. The output of the D/A gives a voltage output that is equal to the highest discrete level that does not exceed the input

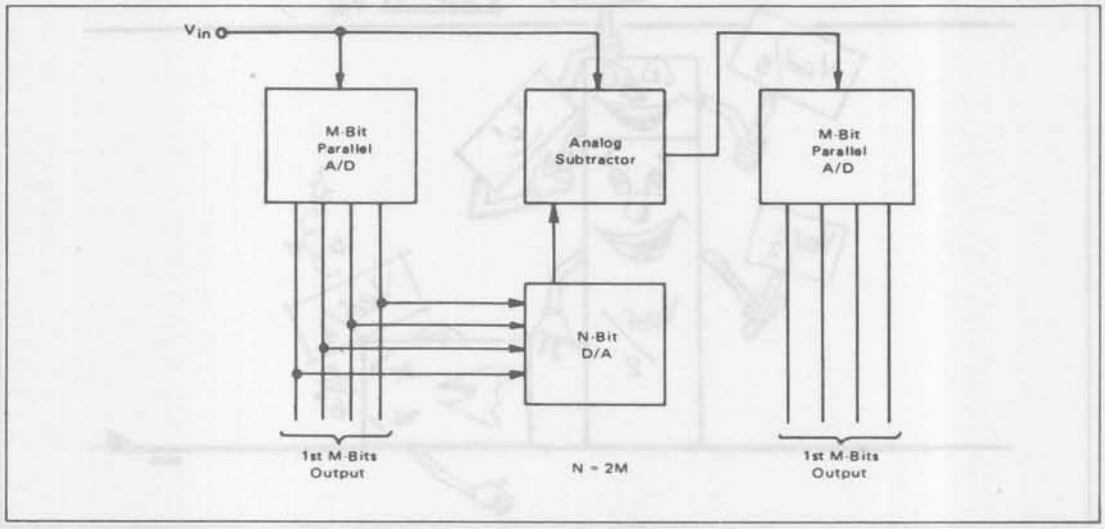


FIGURE 11 – Block Diagram of Parallel Ripple A/D

signal. This voltage is subtracted, by analog means, from the input signal. The remainder is then fed to another m-bit Flash encoder which converts the remaining m-bits of the system. In an actual system, either the thresholds of the second set of 2^m-1 comparators must be scaled down by a factor of 2^m, or the remainder signal must be amplified by 2^m.

As can easily be seen, the time required to complete a conversion is the sum of:

1. Time required for first m-bit conversion
2. Time for D/A to settle to required accuracy
3. Time to complete analog subtraction
4. Time required for second m-bit conversion

Since the first m-bits arrive at the output ahead of the second, and the system uses the Parallel technique, the name of Parallel Ripple was coined.

As stated earlier, at the present time no one is producing a monolithic A/D of any type. However, this scheme, and the other types of A/Ds about to be described, offer the possibility of monolithic fabrication of an A/D system. With present technology the system would probably have to be divided into several parts, each of which could be integrated. As the capabilities of the manufacturers continue to increase, a one chip, high speed A/D becomes more and more feasible.

VTF A/D System

The Variable Threshold Flash A/D converter is a clockless, non-synchronous type of A/D which gives a binary output, requires only one comparator per bit, and needs no decoding of the comparator outputs.

Primarily, the advantage of the VTF system over other types of A/Ds is the capability of high speed conversion coupled with low parts count and low cost. Also, the unique method that the system uses for conversion gives it added versatility. More will be said about this later. In addition to the above, the VTF type of A/D lends itself to monolithic fabrication.

Basically the VTF system is a "flash" approach with the addition of feedback. The addition of the feedback reduces the number of comparators required for an n-bit system from 2^n-1 to n. Like the flash method, n comparators have their thresholds initially set at the binary weightings of the reference voltage. That is, the threshold of the MSB is set at $V_{ref}/2$; the threshold of the second MSB is set at $V_{ref}/4$, etc.* (See AN-471).

In VTF operation, however, the comparator threshold voltages are changed at appropriate times and in such manner that their outputs are made to count in the proper code. Note that the VTF system may be set up to count standard "binary", Grey code, BCD or several other codings.

Figure 12 shows a block diagram of a 3-bit A/D using the VTF principle. Operation of the system may be easily understood if we look at each of the threshold determining circuits as a D/A converter. Note that only a one-bit D/A is needed for the MSB, a two-bit D/A is required for the second MSB, a three-bit for the third MSB, etc. The reason for this is shown in Figures 13(a) and 13(b). Figure 13(a)

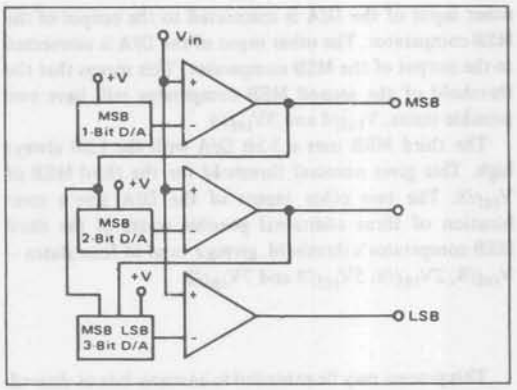
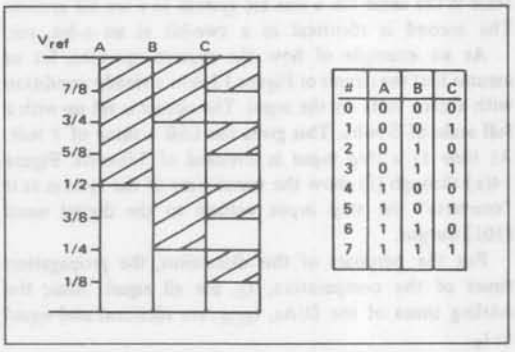


FIGURE 12 – Block Diagram of Variable Threshold Flash



#	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

FIGURE 13 – VTF Threshold Levels

lists all of the possible states of a three-bit binary code. Figure 13(b) shows the level where each respective bit is high; the shaded areas representing the input voltage range for which the bit is high and the non-shaded areas the range of a low state.

It can be seen that there are 2^n separate areas for each bit, counting both shaded and non-shaded areas, where "n" is the bit number starting with the MSB as 1. An n bit D/A has 2^n possible output levels. Therefore, the system requires an n-bit D/A for bit number "n". This can be generalized to any number of bits.

Figure 13(b) shows that the first (lowest) transition of bit number n, occurs at the level of $V_{ref}/2^n$. Therefore, the lowest value of the comparator threshold for the bit is $V_{ref}/2^n$. This corresponds to the level out of the D/A with the least significant bit energized. For this reason the LSB of each D/A is always left on.

Using the above rules, the MSB uses a 1-bit D/A which is always on. This gives, in effect, a constant voltage equal to $V_{ref}/2$ as the threshold voltage of the MSB comparator. As can be seen in Figures 12 and 13, the threshold of the MSB does not change.

The second most significant bit uses a 2-bit D/A, (no pun intended). The LSB of this D/A is always on, giving a threshold of $V_{ref}/4$ to the second MSB comparator. The

other input of the D/A is connected to the output of the MSB comparator. The other input of the D/A is connected to the output of the MSB comparator. This means that the threshold of the second MSB comparator will have two possible states, $V_{ref}/4$ and $3V_{ref}/4$.

The third MSB uses a 3-bit D/A with the LSB always high. This gives nominal threshold for the third MSB of $V_{ref}/8$. The two other inputs of the D/A give a combination of three additional possible states of the third MSB comparator's threshold, giving a total of four states – $V_{ref}/8$, $2V_{ref}/8$, $5V_{ref}/8$ and $7V_{ref}/8$.

This process may be extended to as many bits as desired. Note that the addition of more bits to the system increases the compleixty of the additional bits only. The MSB is the same for a one-bit system as a ten-bit system. The second is identical in a two-bit as an n-bit, etc.

As an example of how the system operates, let us assume that the circuit of Figure 12 is in a steady condition with a zero volts on the input. The circuit is set up with a full scale of 8-volts. This gives the LSB a value of 1 volt. At time t_1 a step input is initiated of 5.0-volts. Figure 14(a) through (f) show the waveforms of the system as it "converts" the step input voltage to the digital word (101) output.

For the purposes of this discussion, the propagation times of the comparators, t_c, are all equal. Also, the settling times of the D/As, $t_{d/A}$, are identical and equal to t_c.

Figure 14(a) shows the threshold of the MSB comparator and the input voltage, V_{in}. The output of the MSB is shown in Figure 14(b). Figures 14(c) and (d) and 14(e) and (f) show the same points for each of the other two bits respectively.

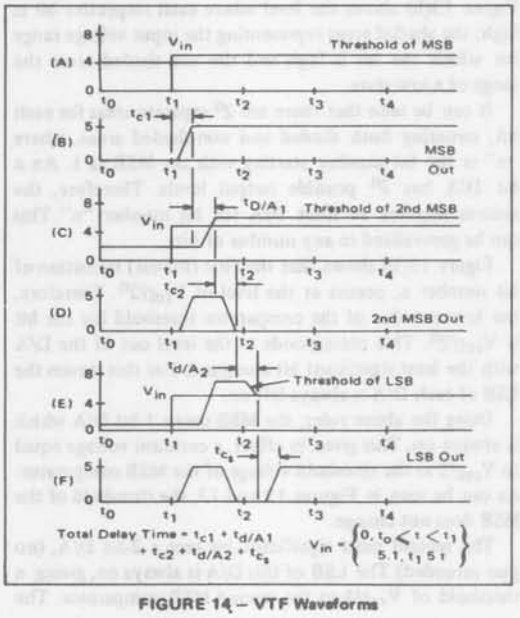


FIGURE 14 – VTF Waveforms

From time t_0 to t_1 the input voltage to the system V_{in} is zero volts. The threshold of the comparators are at their lowest states, namely, 4, 2, and 1-volt respectively. As the input voltage is below all of the thresholds the outputs of the comparators are all low.

At time, t_1, the input voltage is stepped to 5.0-volts. The input being greater than each of the respective threshold voltages, causes all of the outputs to go high. Therefore at time, $t_1 + t_{c1}$, all of the bits are high. The output of the MSB is one input to each of the D/As on the two least significant bits. Also, the output of the second MSB is one input of the LSB's D/A. These voltages on the D/A inputs cause the threshold of the second MSB to go to six volts and the LSB threshold to go to seven volts. At time, $t_1 + t_c + t_{d/A}$, the thresholds of the two least significant bits are at 6 and 7-volts respectively.

Since at this time the input voltage is less than the 2nd MSB's comparator and LSB's thresholds, both of the two least significant bits of the A/D go to a low. Because the output of the second MSB is an input to the LSB's D/A, the threshold of the LSB again changes. At time, $t_1 + t_{c1} + t_{d/A1} + t_{c2} + t_{d/A2}$ the threshold of the LSB is at 5.0-volts. As 5.0 is less than the 5.1-volts input, the output of the LSB goes high. The conversion is complete at time $t_1 + t_{c1} + t_{d/A1} + t_{c2} + t_{d/A2} + t_{c3}$. Thus, at this time, the data on the outputs of the comparators is the digital representation of the input voltage.

The data at the output of the MSB is valid one comparator delay after the input has been applied. The reason for this is the fact that the threshold of the MBS never changes.

The threshold of the second MSB is dependent on the state of the MSB. Therefore, the threshold voltage of the second MSB cannot be assumed to be accurate until one D/A settling time after the MSB reaches its final state. The output of the second MSB requires one comparator delay in addition to this. Because of this, the output of the second MSB cannot be guaranteed to be valid until two comparator delays and one D/A settling time after the input has been applied.

This process can be repeated through all of the stages of an n-bit system, giving a time necessary to guarantee the accuracy of a given bit. It is, however, easy to generalize the process by the formula:

$$t = nt_c + (n-1)\, t_{d/A} \qquad (1)$$

where n is the bit number, t_c is the propagation delay time of a comparator and $t_{d/A}$ is the settling time of a D/A.

Because of the above phenomenon, in operation the VTF A/D system converts the most significant bit first, then the second, etc. This means that if the output were taken before the A/D had completely converted the answer, the error would be in the least significant bits only. This appears as error and rolls off the amplitude of the signal output so that it appears as though the system were bandwidth limited. This means that the converter can give useful information before the A/D system has had

time to guarantee a complete conversion. Most A/D converters of this speed capability will give a completely unpredictable answer if the output is taken before the system has completely converted.

It should be noted here that the VTF A/D does not always require the time given by equation (1). The system can give the correct answer in as little as one comparator delay. The time required to give the complete conversion is a function of the amount of change of V_{in} since the last conversion. For example, if V_{in} only changes 1 LSB, the worst-case conversion time is two comparator delays and one D/A settling time.

The system as described here is a clockless, non-synchronous type of A/D. In this type of system, the converter output follows the input and the output can go through false states during the conversion. If desired, the VTF A/D system could be made into a completely synchronous, clocked type of system by adding digital delay circuits plus an analog delay time.

Synchronous VTF A/D System

Figure 15 shows the VTF system in a clock synchronous configuration. This circuit is identical to the one described earlier and shown in Figure 12, except for the addition of the D-type flip-flops and the analog delay lines. The advantages of this system is that after an initial n-clock period propagation delay, the output of the A/D gives a complete conversion every clock pulse thereafter. The only requirements being that the delay of the analog delay line must be equal to the clock period, and that period must be greater than the sum of one comparator delay and one D/A settling time.

The purpose of the analog and digital delay circuits is to allow the more significant bits to make another comparison before the least significant bits have completely converted. For example, let us assume the circuit is setting at zero and a signal input is applied as a step function. The value of the step input changes every clock period to a new value. This waveform is shown in Figure 16(b).

As described in the non-synchronous system, the MSB comparator output is valid after one comparator delay. This output is fed to all of the successive stages to change the other bit's respective thresholds. In the non-synchronous system the input signal must remain constant until the system has had time to complete the conversion. However, in the synchronous system the output is stored in a flip-flop and the output of the flip-flop is fed to the successive stages. This allows the MSB to give a new output without waiting for the rest of the system to complete the conversion.

This process is repeated through all of the stages of the A/D. In this manner the A/D can, after an initial n-clock period delay, give a complete conversion every clock period.

Figures (a) through (n) show waveforms of the system in operation. The delays are shown and one can see how the system gives a complete conversion every clock period.

As can be seen from the block diagrams of the systems and the above discussion, the VTF technique gives the simplest, lowest cost, and lowest parts count, high speed A/D that can be built with today's technology. Also, the

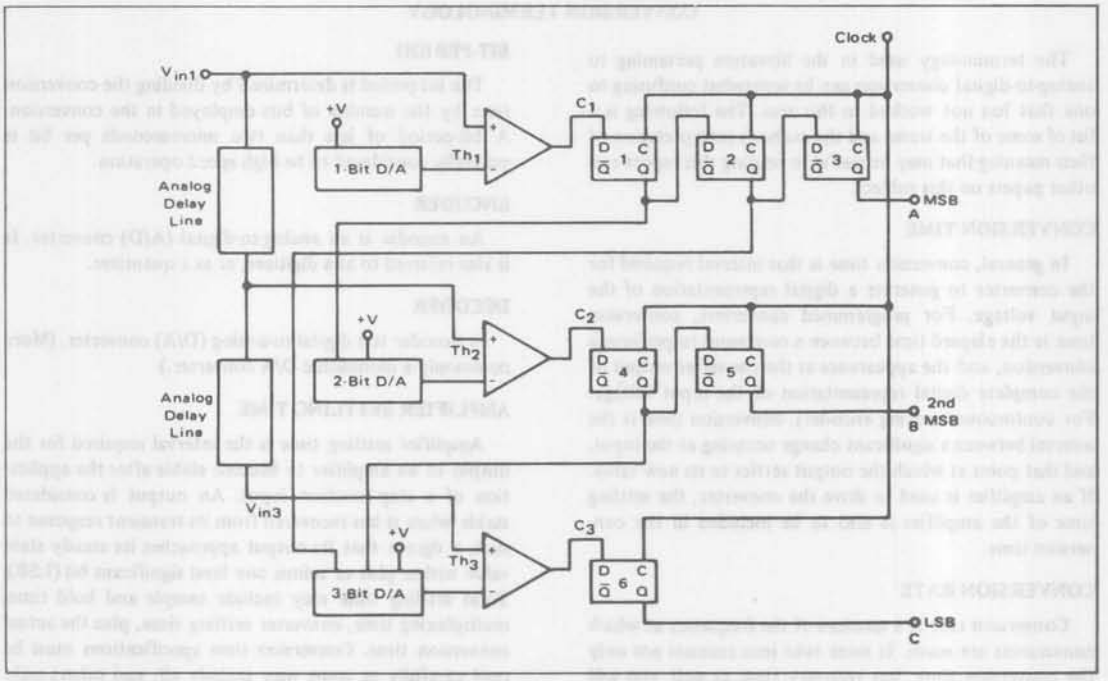


FIGURE 15 – Block Diagram of Synchronous VTF

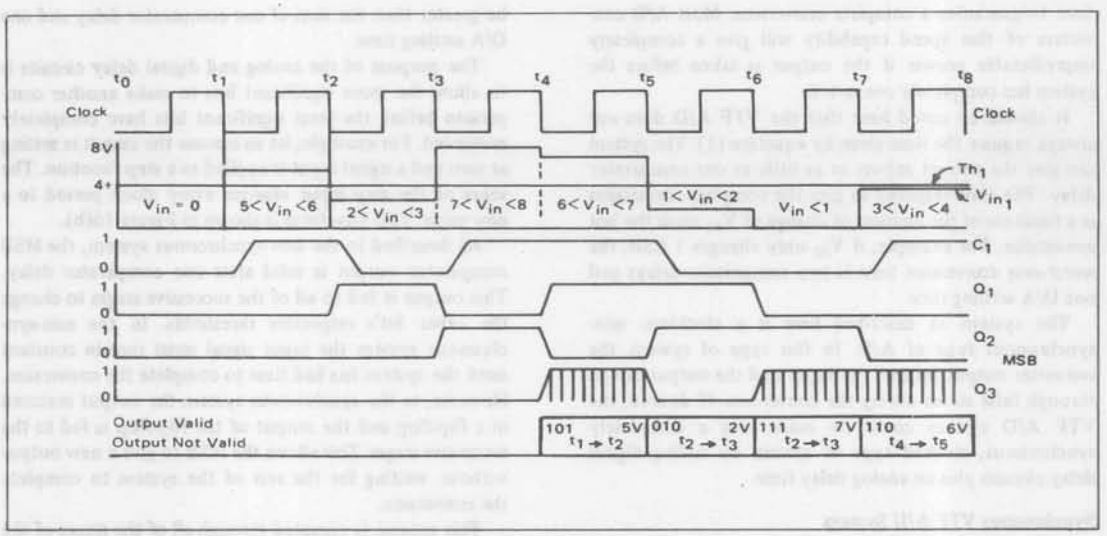


FIGURE 16 – MSB Waveforms For Synchronous VTF

fact that the VTF A/D can be built in monolithic form could give the system an added benefit to the user who desired to fabricate a high-speed A/D.

A 6-bit A/D using the non-synchronous system has been constructed at Motorola's Application Facility. Using MECL III Comparators and discrete part D/As, a worst-case conversion time of 60 nanoseconds was achieved. It is not unreasonable to expect the synchronous system to give an 8-bit conversion in 15 ns, at a cost of less than $250!

APPENDIX A
GLOSSARY OF ANALOG-TO-DIGITAL CONVERSION TERMINOLOGY

The terminology used in the literature pertaining to analog-to-digital conversion can be somewhat confusing to one that has not worked in this area. The following is a list of some of the terms and the author's interpretation of their meaning that may be useful in reading this report and other papers on this subject.

CONVERSION TIME

In general, conversion time is that interval required for the converter to generate a digital representation of the input voltage. For programmed converters, conversion time is the elapsed time between a command to perform a conversion, and the appearance at the converter output of the complete digital representation of the input voltage. For continuous tracking encoders, conversion time is the interval between a significant change occuring at the input, and that point at which the output settles to its new value. If an amplifier is used to drive the converter, the settling time of the amplifier is also to be included in the conversion time.

CONVERSION RATE

Conversion rate is a measure of the frequency at which conversions are made. It must take into account not only the conversion time, but recovery time as well, and will usually be less than the reciprocal of conversion time.

BIT-PERIOD

The bit-period is determined by dividing the conversion time by the number of bits employed in the conversion. A bit-period of less than two microseconds per bit is generally considered to be high speed operation.

ENCODER

An encoder is an analog-to-digital (A/D) converter. It is also referred to as a digitizer, or as a quantizer.

DECODER

A decoder is a digital-to-analog (D/A) converter. (More commonly a monolithic D/A converter.)

AMPLIFIER SETTLING TIME

Amplifier settling time is the interval required for the output of an amplifier to become stable after the application of a step-function input. An output is considered stable when it has recovered from its transient response to such a dgreee that its output approaches its steady state value within plus or minus one least significant bit (LSB). Total settling time may include sample and hold time, multiplexing time, converter settling time, plus the actual conversion time. Conversion time specifications must be read carefully as some may include all, and others only part of the above mentioned.

Note that in a 15-bit system, the RC time constants must be multiplied by at least 12 before the settling time error can be ignored. With each time constant period, the error decreases about 36%. After ten time constants, an exponential voltage is 0.005% away from the full value.

APERTURE

Aperture is the amount of uncertainty about the exact time when the encoder input was at the value represented by a given output code. In general, the aperture is equal to the conversion time. However, with the use of a sample-and-hold circuit as an input network, the aperture can be reduced, since more information is known about when the input sample was obtained relative to the timing of the output result.

QUANTUM LEVEL

In an n-bit encoder there are exactly 2^n different states. If the analog reference voltage is divided into 2^n parts then one part represents a quantum of voltage. The reference voltage is quantized into 2^n quantum levels where each quantum level is represented by one of the 2^n binary states in an n-bit quantizer.

The error of quantization is a function of the number of bits in the converter. An A/D converter is normally adjusted for the center of each of the binary weighted steps; hence, the error of quantization is at most one-half of a significant bit (1/2 LSB).

RESOLUTION

Resolution is the ability of the converter to distinguish between adjacent values of the quantity being measured. Normally the resolution would be considered to be limited only by the number of bits carried. In practice, however, the ultimate resolution of a given design is limited by the noise in the various analog and switching circuits, and by the linearity and monotonicity of the converter. Specifications for the resolution of a converter should be compatible with the number of bits and vice-versa, otherwise the specification would imply that the readings convey a higher degree of resolution than could actually exist.

ACCURACY

Accuracy must include all of the sources of errors (quantization, non-linearily, noise, and short term drift). Relative accuracy is often defined as the deviation from a straight line passing through zero and the nominal full scale value (very similar to linearity). A typical accuracy specification might be 0.05% ± 1/2 LSB at +25°C.

Long term stability, not included in the accuracy specification, defines the additional error introduced because of component aging. It is measured over a period of time (generally one to three months) at a fixed ambient temperature. A typical long term stability specification might be ±0.005%/90 days at +25°C.

PRECISION

Precision relates to the repeatability of successive measurements. Precision is limited in practice by noise and a small but finite quantization error that always exists in some "dead band" at each successive numerical value. When the unknown analog voltage lies within any of the dead bands around each of the possible values, the repeatability can never be greater than plus or minus one least-significant-bit. One measure of the quality of the high speed analog-to-digital converter is the ratio of the dead band to the full quantization level for each value across the entire range.

MONOTONICITY

Monotonicity relates to an increasing output for every increasing value of input voltage. Another way of saying this is that the derivative of the output with respect to the input is always positive. A converter must be capable of producing every coded value within the input range defined. The accuracy of the various resistors in the digital-to-analog converter ladder network and the offser voltage in the switching electronics must be minimized, so that the sum of the errors for any given number of successive lesser significant bits is less than the error produced by the next most significant bit; otherwise, it would be possible to force non-uniform spacing of the quantum levels and miss some of the output codes altogether. Absolute requirements for monotonicity are that all codes are obtainable and that the quantization level of each code be within one-half of one least-significant-bit of the ideal, linear-related quantization level.

LINEARITY

Linearity is a measure of the deviation from a straight line of a plot of the input-output radio of an analog-to-digital converter over its operating range and is usually expressed in a percent of full scale.

STABILITY

The factor of stability simply relates to the ability of the converter to maintain the characteristics (relative accuracy, resolution, precision, etc.) over a defined operating interval. Lack of stability occurs primarily for two reasons: drift in the voltage reference and the resistors, and drift in the conversion switching networks.

CONVERSION ERROR

The discrepancy between the actual output of an analog-to-digital converter and the exact digital representation of the quantity being measured at the instant of measurement is conversion error. It is generally one-half of the value represented by the least-significant-bit.

INPUT IMPEDANCE

The input impedance of the converter system is the amount of load that the ADC represents to its source, the quantity being measured. A typical comparator with a 50 MΩ input resistance will load a source resistance of 1 kΩ sufficiently to introduce an error of 0.002%.

SYSTEM TEMPERATURE COEFFICIENT

The system temperature coefficient in the worst case is the sum of the contributions of each of the component temperature coefficients. One must be careful in reading A/D converter specifications to avoid being misled by the "RMS-trick". RMS calculations are good when a large number of terms are included, but are not valid when only a few elements are present. Consider the following as an example of this mis-specification:

Voltage Reference TC = 0.0006%/°C
Voltage Comparator TC = 0.0005%/°C
Ladder Resistor TC = 0.0003%/°C

Algebraic Total = 0.0014%/°C
$(\text{rms total})^2 = (0.006)^2 + (0.005)^2 + (0.003)^2$
$= 0.00000070$
rms total 0.0008%/°C

The RMS total is obviously a misleading specification when the algebraic total could quite possibly occur since the probability that a few things could occur simultaneously is not too small.

APPENDIX B
CODES AND NUMBERING SYSTEMS USED IN A/D AND D/A CONVERSION

Several computational codes or number systems are used in data handling machines, the majority of which may be categorized as positional notations. Positional notation means that any integar may be represented by the sum of a number of digits, weighted in value according to their position in the notation.

Using this notation, it is possible to express any integer (A) as

$$A = a_n B^n + a_{n-1} Bn-1 + \ldots + a_0 B^0 \quad (1)$$

where B is the base or radix of the number system, and a_n is an integer number. A fractional number may likewise be expressed in the form of equation 1 by using negative exponential powers. The three commonly used bases are 10 (decimal system), 8 (octal system), and 2 (binary system).

One of the basic requirements of all positional notations is that the base of the code equal the total number of digit symbols, all possible values of a_n, used to represent the coded numbers, a_n is a digit between 0 and (B-1), where again B is the radix of the number system.

Decimal

The decimal system uses 10 symbols (0, 1, 2, 3, ..., 8, 9); therefore, from our previous discussion the base of the decimal system is 10, and any integer (A) can be represented as

$$A = a_n 10^n + a_{n-1} 10^{n-1} + a_{n-2} 10^{n-2} + \ldots + a_0 10^0 \quad (2)$$

Where a_i is an integer between and including 0 and 9. As an example, the number 15 to the base 10, which symbolically is $(15)_{10}$, is represented as shown below.

$$(15)_{10} = 1 \times 10^1 + 5 \times 10^0 \quad (3)$$

Because of its early development and its natural association to man (i.e., 10 fingers, 10 toes), the decimal system is universally used for human computation. However, when the decimal system is used for notational purposes in high speed data systems, it becomes clumsy, inconvenient, and very inefficient.

Using the decimal system, electronic circuitry would be required to accurately represent ten different states corresponding to the ten digit symbols. Circuitry of this type is currently unavailable. However, many methods now exist for representing two independent states electrically.

Binary

The binary number system was developed to take advantage of the convenience of the 2-state concept which was just discussed. This system uses the number base 2 which means that only two digits (0 and 1) can be used to represent all coded numbers (a_i's). As an example, the number $(15)_{10}$ represented in base-2 notation is:

$$(15)_{10} = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = (1111)_2 \quad (4)$$

This illustrates that the binary code sacrifices length of notation for simplicity of digital symbolism.

When the machine language is completely binary, communication between man and machine is frequently impossible and at very best, messy. To overcome this problem a coding system is needed which combines the ease of machine computation of the binary system with the familiarity of the decimal system. A coding technique that combines these features into one code is the binary-coded decimal (BCD) system which uses an arbitrary four-digit binary code to represent each of the decimal digits (0 through 9).

Binary-Coded Decimal

One specific binary-coded decimal code is formed by using the binary representations of the decimal numbers 0 through 9. This is commonly called the 8-4-2-1 code. The first 16 decimal numbers and their representations in the binary and binary-coded decimal system are shown in columns one through three in Table I, included at the end of this appendix. Using the binary-coded decimal code, the decimal number 715 is written as

7	1	5	
0111	0001	0101	(5)

or

$$(715)_{10} = (011100010101)_{BCD} \quad (6)$$

To convert from binary-coded decimal (BCD) to decimal numbers, one has only to make the coded number into four digit sections, starting with the least significant digit and proceeding to the left, and then apply the definition of the binary numbers 0 through 9 to each section.

Gray

One binary-coded decimal code which finds wide application in analog-to-digital converters is the unit-distance code (also called the Gray Code, after its inventor, and also commonly called the "cyclic" or the "Reflected Binary Code".

The Gray Code has the unique property that its states are a unit-distance apart. That is in going from any decimal number (i.e., 11) to any adjacent decimal number (10 or 12) only one binary digit will change value. The fourth column of Table I illustrates the Gray code representations for the decimal number 0 through 15.

As a matter of general information, the generating equation for the magnitude of each one (1) in the Gray code is

$$\sum_{j=0}^{j=n} 2^j \qquad (7)$$

where n represents the digit column in which the one (1) appears. The most significant one (1) has a positive sign and each of the succeeding ones (1's) to the right will have an alternate sign. As an illustration, consider the Gray-coded number 1110.

$$(1110)_G = \sum_{j=0}^{3} 2^j - \sum_{j=0}^{2} 2^j + \sum_{j=0}^{1} 2^j$$

$$= 2^0 + 2^1 + 2^2 + 2^3 - 2^0 - 2^1 - 2^2 + 2^0 + 2^1$$

$$= 2^3 + 2^0 + 2^1 = (11)_{10} \qquad (8)$$

TABLE I

The Binary, Binary-Coded Decimal, and Gray Code Equivalents of the First 16 Decimal Numbers

Decimal	Binary	Binary Coded Decimal	Gray Code
0	0000	0000 0000	0000
1	0001	0000 0001	0001
2	0010	0000 0010	0011
3	0011	0000 0011	0010
4	0100	0000 0100	0110
5	0101	0000 0101	0111
6	0110	0000 0110	0101
7	0111	0000 0111	0100
8	1000	0000 1000	1100
9	1001	0000 1001	1101
10	1010	0001 0000	1111
11	1011	0001 0001	1110
12	1100	0001 0010	1010
13	1101	0001 0011	1011
14	1110	0001 0100	1001
15	1111	0001 0101	1000

Hence, the Gray code for the decimal 11 is 1110. The Gray code for the decimal 12 is 1010. Only the second most significant digit (bit) changes between the successive numbers (11 and 12) allowing no ambiguity to exist in the digital readout. The point is of reasonable significance when decoding is required and erroneous spikes cannot be tolerated.

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AN-713

Application Note

BINARY D/A CONVERTERS CAN PROVIDE BCD-CODED CONVERSION

This note describes the application and use of integrated circuit D/A converters for use in providing a BCD-coded conversion. The technique is illustrated using a 2-1/2 digit digital voltmeter.

3

Binary D/A converters can provide BCD-coded conversion

You can use IC D/A converters, even though they're binary coded, to do BCD-to-analog conversion. It just takes a few extra parts.

Monolithic digital-to-analog (D/A) converters have become very popular because of their versatility and low cost. They have one limitation, however, and that is that they are all binary coded. Thus, they cannot be used directly for the many applications where a binary-coded decimal (BCD) conversion is required. It is possible, though, by adding some external components to make a binary-coded D/A converter perform as a BCD code converter.

Two-digit converter

A 2-digit, BCD-coded voltage-output D/A converter is shown in **Fig. 1**. To understand its operation, note the 4-bit binary code and corresponding one digit of BCD code shown in **Table 1**. The BCD code and the 0-to-9 of the binary code are exactly the same. The 4-bit binary code sequences through all 16 steps before the next most-significant bit (fifth bit) increments one step. However, when counting in BCD the 4-bit code will only sequence through ten steps before the next most-significant bit increments once. This means that 10 least-significant bit steps in BCD equal 16 least-significant bit steps in binary, assuming the next most-significant bit of both codes is the same magnitude.' Therefore, by making the four least-significant bits of the binary-weighed D/A converter appear larger, such that 10 least-significant bit steps equal the magnitude of the next significant bit, a BCD-coded D/A converter can be effectively produced.

To make the four least-significant bits of the D/A appear larger than normal (**Fig. 1**), current from the node connecting the output of the D/A converter and the virtual ground of the op amp is used. This virtual ground of the op amp provides a very good summing junction.

In implementing the technique it was found that the hardware available made it much easier to switch currents into the node than out of it. This problem was circumvented by taking a constant current out of the node and switching currents into it.

The output of the binary D/A is a current sink, with the amount of current depending on the reference current input, I_{ref}, and the digital word on its input lines. This is empirically given by:

$$I_o = I_{ref}\left(\frac{X}{256}\right)$$

$$I_{ref} = \frac{V_{ref}}{R_{ref}}$$

where I_o is the output current, I_{ref} is the reference current and x is the digital word input.

The op-amp feedback resistor changes analog current I_o to an analog voltage, e_o, where:

$e_o = I_o R$

Thus, e_o is directly proportional to I_o, namely R times.

The outputs of the CMOS NOR gates appear as voltage sources, with 750Ω output impedances. In

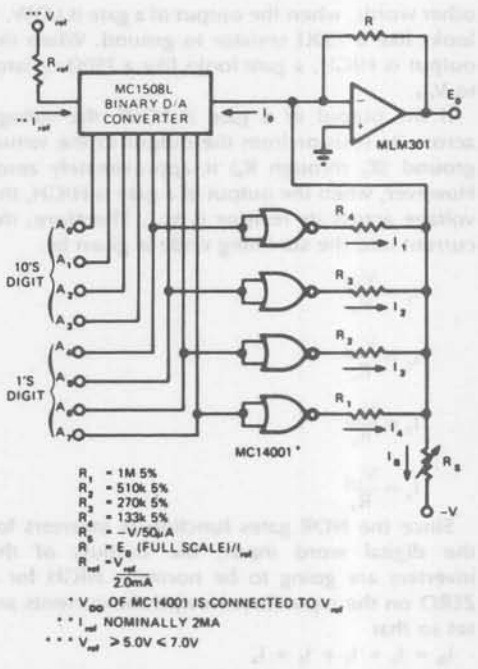

Fig. 1—Two-digit BCD D/A converter uses a binary-coded monlithic D/A converter as its basic conversion element.

TABLE 1 – 4-BIT BINARY VS 1-DIGIT BCD

	BINARY				BCD			
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	0
3	0	0	1	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	1	0	0	1
10	1	0	1	0	———			
11	1	0	1	1	———			
12	1	1	0	0	———			
13	1	1	0	1	———			
14	1	1	1	0	———			
15	1	1	1	1	———			

other words, when the output of a gate is LOW, it looks like a 750Ω resistor to ground. When the output is HIGH, a gate looks like a 750Ω resistor to V_{ref}.

If the output of a gate is LOW, the voltage across its resistor from the output to the virtual ground (R_1 through R_4) is approximately zero. However, when the output of a gate is HIGH, the voltage across its resistor is V_{ref}. Therefore, the current into the summing node is given by:

$$I_1 = \frac{V_{ref}}{R_1}$$

$$I_2 = \frac{V_{ref}}{R_2}$$

$$I_3 = \frac{V_{ref}}{R_3}$$

$$I_4 = \frac{V_{ref}}{R_4}$$

Since the NOR gates function as inverters for the digital word input, the outputs of the inverters are going to be normally HIGH for a ZERO on the input line. Now, if the currents are set so that

$I_B = I_1 + I_2 + I_3 + I_4$

when the input word is all ZEROs, no net current will be taken from or added to the summing node. If one of the four least-significant bits is turned ON, the output of that inverter goes LOW and the current through the resistor to the summing junction is zero. This requires a net current, equal to the amount that was being injected into the summing junction by the resistor, to be drawn out of the summing junction, causing that bit of the D/A to appear larger than it really is. The other three bits work in exactly the same manner.

The only problem now is to determine the values of the resistors for proper operation.

Since the output of the D/A is a direct function of the reference current, it follows that the added currents must be also. The most-significant current of the D/A is $I_{ref}/2$. The second most-significant bit current is $I_{ref}/4$ and so on. **Table 2** shows the value for the current of each bit of the D/A and also gives the values needed for BCD operation. The difference between the binary value and the BCD value must be taken from the node to make the binary-weighed D/A behave as though it were BCD coded.

It is interesting to note that making the D/A converter act as if it were BCD coded could also be achieved if the four most-significant bits of the D/A were made to look smaller than normal. The reason the system is set up as described is that the least-significant bit currents do not have to be as accurate as the most-significant bit currents. This means that the magnitude of the current subracted from the summing junction using the least-significant bits is not critical.

Determining allowable current error

If the BCD-coded D/A converter is to be

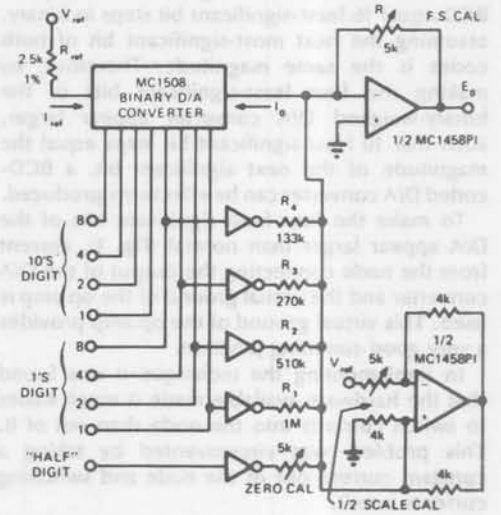

Fig. 2—Addition of a current source and current switch expands the 2-digit BCD converter of **Fig. 1** into a 2-1/2-digit converter.

accurate, the maximum amount that any of the bit currents can deviate from the ideal value is 50% of the least-significant bit current. Since the least-significant bit current is larger for BCD than for binary, a less accurate D/A is required to give 2-digit BCD accuracy (100 steps) than for 8-bit binary (256 steps).

Table 2 shows that the value of the least-significant bit current for BCD is 0.125 mA. So to give the required accuracy, each bit current must not deviate from the ideal value by more than ±0.00625 mA, or 6.25 μA.

For an 8-bit binary D/A, assuming a 2 mA ladder current, the maximum error that any bit may have is 3.9 μA. Assuming the 8-bit D/A to have the worst allowable error on each of the least-significant bits, that leaves an error of 6.25 μA minus 3.9 μA, or 2.35 μA to be introduced by the injected currents. In other words, to insure that the 2-digit BCD-coded D/A is accurate, the injected currents must be kept within ±2.35 μA of their ideal value.

It is easy now to determine the accuracy required for the injected currents. The percentage of accuracy is simply the amount of deviation allowed, 2.35 μA, divided by the amount of injected current. This is given by:

$$\% \text{ allowable error} = \frac{2.35\ \mu A}{\text{amount current injected}} \times 100$$

Using this formula, the injected currents' allowable errors are:

LSB; 50%
2nd LSB; 25%
3rd LSB; 12.5%
4th LSB; 6.25%

This shows that 5% tolerance resistors are more than adequate. **Fig. 1** gives the resistor values for a 5.0V reference voltage. These values are sufficient to neglect the output impedance of the NOR gates.

Calibration of the circuit of **Fig. 1** is as follows: First, V_{ref} or R_{ref} is adjusted to give a half-scale reading of e_o with only the most-significant bit ON. Next, with all bits turned OFF, R_s is adjusted so that e_o is zero. The D/A is now calibrated.

TABLE 2 – BIT CURRENTS

BIT	NUMBER	BINARY	BCD	DIFFERENCE
A_0	MSB	1.000MA*	1.000MA*	0
A_1	2ND	0.5000	0.5000	0
A_2	3RD	0.2500	0.2500	0
A_3	4TH	0.1250	0.1250	0
A_4	5TH	0.0625	0.1000	0.0375
A_5	6TH	0.0312	0.0500	0.0188
A_6	7TH	0.0158	0.0250	0.0094
A_7	LSB	0.0078	0.0125	0.0047

* I_{ref} = 2.0000mA

2-1/2-digit converter

In many applications, a 2-1/2-digit BCD-coded converter is desired. That is, a circuit that will count to 199 rather than to 99. Once the basic 2-digit circuit has been designed, it is relatively easy to add the half digit. **Fig. 2** shows such a 2-1/2-digit circuit. It is identical to the 2-digit configuration, except for the addition of a current source and a current switch to produce the 1/2 digit.

In operation, the circuit should sequence through steps 0 to 99 while the 1/2 digit is LOW and through steps 100 to 199 while the 1/2 digit is HIGH. This means that the 1/2-digit current is equal to 100 least-significant bits of current. If the least-significant bit current in the 2-1/2-digit circuit is the same as the least-significant bit current in the 2-digit circuit previously described, the value for the 1/2 digit is 1.250 mA (100×0.0125 mA). Therefore, the circuit will act as a 2-1/2-digit BCD-coded D/A if the 1/2-digit switch sinks zero current for the first 100 counts (0 to 99) and sinks 1.250 mA for the second 100 counts (100 to 199).

The 1/2-digit current is added in the same manner as the least-significant bit currents were added in the 2-digit system. Namely, a constant current, I_H, is sunk from the summing node, and the various currents, I_1 through I_5, are switched into the node. For the 2-1/2-digit circuit, I_H is obtained by:

$I_H = I_1 + I_2 + I_3 + I_4 + I_5$

where I_1 through I_4 are identical with their 2-digit system counterparts.

The tolerance of I_H to assure that the D/A remains accurate is 2.35 μA. This is the same value as that derived in the 2-digit section. Since I_H is much larger for the 2-1/2-digit system, the percentage tolerance of I_H is much more critical. If the values for I_1 through I_4 shown in **Table 2** are summed with the value of I_5, we have;

I_H = 4.7 μA + 9.4 μA + 18.8 μA + 37.5 μA + 1250 μA = 1320 μA.

If I_H can only vary ±2.35 μA, its tolerance is ±0.18%.

In the 2-digit system, current I_H could be produced simply by a resistor from the summing node to the negative supply because the summing node is a virtual ground. Once the system is calibrated by adjusting R_5, current I_H is constant except for changes caused by variations in the negative supply voltage.

In the 2-1/2-digit system, a circuit is needed that will sink current from the summing node without being referenced to the negative supply voltage.

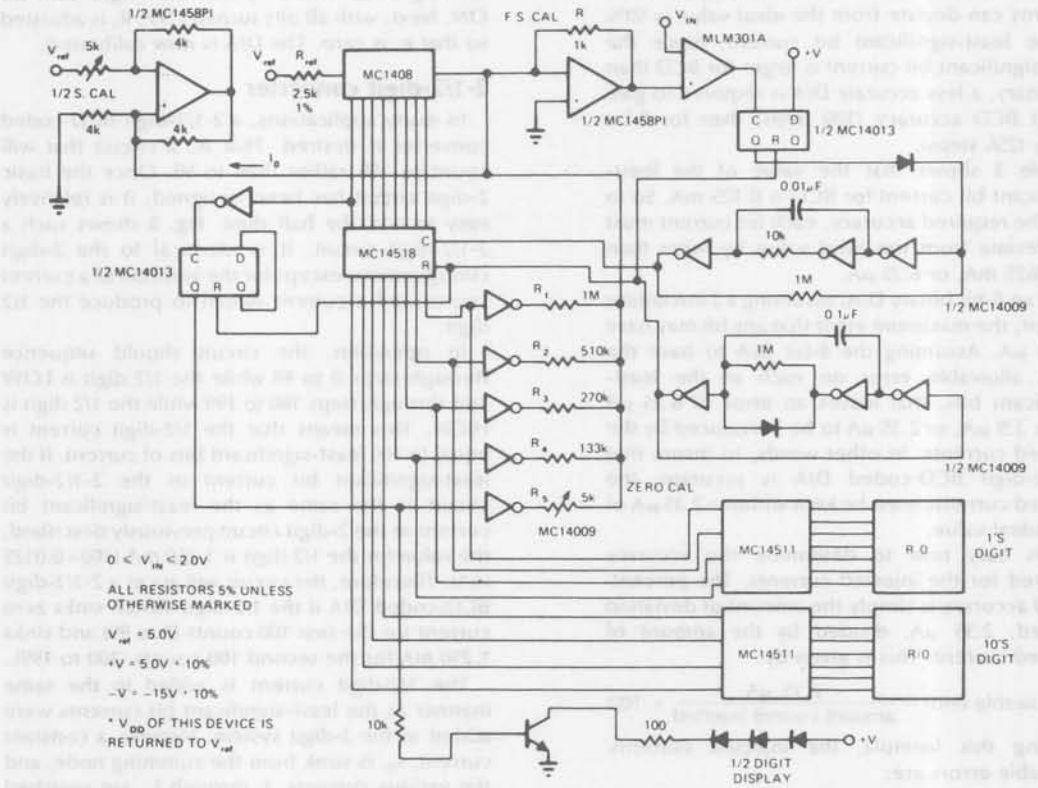

Fig. 3—2-1/2-digit DVM uses a binary D/A converter to accomplish conversion of a BCD digital input signal.

One circuit that fills the need is the operational-amplifier current source shown in **Fig. 2**.

There is one other difference between the basic 2-digit system and the 2-1/2-digit circuit. In the 2-1/2-digit implementation, a CMOS hex-inverter is used instead of a quad 2-input NOR gate package. This is because the 2-1/2-digit system requires five switches.

The 2-1/2-digit system is calibrated as follows:

a) Attach an accurate DVM to the output, e_o. With all inputs LOW, adjust ZERO CAL potentiometer for a zero reading of e_o.
b) Put a HIGH input only on the most-significant bit of the monolithic D/A (0 1000 0000), then read and record e_o.
c) Put a HIGH input only on the 1/2 digit and adjust the 1/2 SCALE CAL potentiometer to give exactly 1.25 times the reading of the previous step.
d) With all inputs LOW, readjust the ZERO CAL potentiometer for an e_o of exactly 0V.
e) Finally, input the BCD word for 199, (1 1001 1001) and adjust the F.S. CAL for the desired full-scale reading.

DVM shows application

Fig. 3 shows how the technique can be incorporated into a 2-1/2-digit digital voltmeter. The circuit uses the staircase type of conversion, with the staircase being produced by the 2-1/2-digit BCD-coded D/A and the BCD counters. The MLM301A is used as a comparator to compare the staircase to the input signal. □

A/D CONVERSION SERIES – PART 5

SUCCESSIVE APPROXIMATION A/D CONVERSION

Recent advances in integrated circuit design and technology have resulted in reduced cost of high performance successive approximation analog to digital converters. This note describes and illustrates two examples of how modern IC components have changed this well known technique.

A/D CONVERSION SERIES - PART V

SUCCESSIVE APPROXIMATION A/D CONVERSION

INTRODUCTION

This treatise concerns the Successive Approximation type of analog-to-digital converter. The questions of why, where, and how to use the S/A system will be discussed along with the basic theory of operation and analysis. In addition, some of the recent advances in monolithic state-of-the-art devices applied to the S/A system will be described.

HISTORY

Through the years the Successive Approximation type of A/D has established itself as the most popular system for medium speed applications; that is, conversion times on the order of 500 ns/bit. There are several reasons for the dominance of the Successive Approximation or S/A system. Namely, the system has some very desirable operational features in addition to a high speed/accuracy product. All this coupled with low system cost and ease of construction account for the system's popularity. Also, like all of the A/D systems which make use of a D/A converter in a feedback loop, the critical, accuracy determining components are in the D/A itself. This means one need only purchase a D/A with the desired speed and accuracy specifications and not have to be concerned with these parameters; a very desirable feature indeed!

With the advent of the monolithic D/A several years ago, the S/A system received an additional shot in the arm. Not only did the monolithic D/A's simplify the construction, but substantially decreased total system cost while increasing both reliability and temperature performance.

Recently another product has appeared on the market which makes the S/A system even more attractive. A digital MSI function known as the Successive Approximation storage Register or SAR. This block contains all of the logic and digital circuitry required to make an S/A type of A/D system. As with the case of the monolithic D/A, the SAR makes the S/A system more economical, easier to construct and increases the total system reliability. Another advantage of the SAR is that it reduces the total system power significantly.

THEORY OF OPERATION

As the theory of operation of the S/A type of A/D is quite well documented and available in many texts on A/D systems, it will not be dealt with rigorously here. However, a brief outline of the basic system operation will be given in order to define our terms for the succeeding portions of the article.

Figure 1 shows the basic block diagram of the system. In operation, the system enables the bits of the D/A one at a time, starting with the most-significant-bit: (MSB). As each bit is enabled, the comparator gives an output signifying that the input signal is greater or less in amplitude than the output of the D/A. If the D/A output is greater than the input signal, the bit is "reset" or turned off. The system does this with the MSB first, then the next most significant bit, then the next, etc. After all the bits of the D/A have been tried, the conversion cycle is complete. At this time, another conversion cycle is started.

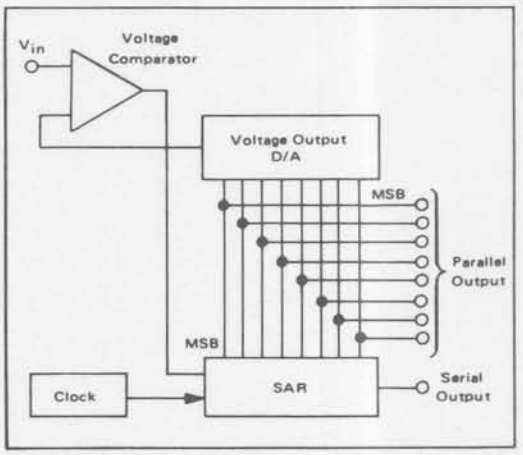

FIGURE 1 – Basic Block Diagram of Successive Approximation A/D System

The operation of the system can easily be understood by referring to Figure 2. This cartoon shows the system in actual operation.

At the start of the conversion cycle, the MSB of the D/A is enabled, presenting a voltage to the comparator of half-scale or $V_{ref/2}$. The comparator makes a decision as to which of its two inputs are greater and gives the ap-

propriate output, a high if V_{in} is the greater and a low if the D/A output voltage is the largest. The S/A storage register then turns off the MSB if the comparator is low. This process is repeated sequentially for each bit of the system.

In the example of Figure 2, we see the MSB was enabled and was less than V_{in}. Therefore, the MSB was left on and the second MSB was enabled. When the second MSB, or $V_{ref/4}$, was added to the magnitude of $V_{ref/2}$, the sum was greater than V_{in}. Therefore, the second MSB, $V_{ref/4}$, was disabled (as shown in the cartoon.) Next, the third MSB was tried and the sum was less than V_{in} so that bit was left high. At the present time, the storage register

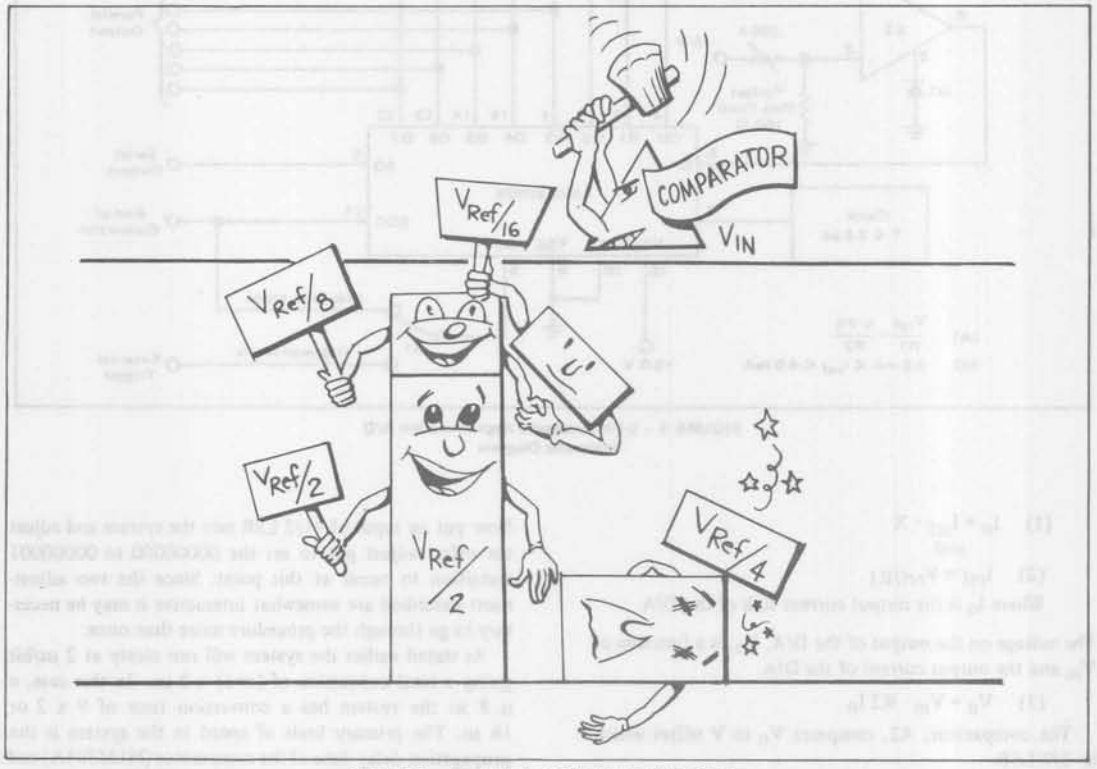

FIGURE 2 – Analogy of an S/A Type of A/D System

is turning on the fourth MSB, or $V_{ref/16}$. We see that the sum will surpass V_{in} and the comparator is getting ready to "disable" the fourth MSB. In this example, we have only shown four-bits, but the operation can be extended to as many as desired. After the conversion cycle has completed the address of the D/A is the parallel binary word output of the A/D.

The serial output of the system is taken from the output of the comparator. While the system is in the conversion cycle, the comparator output will be either low or high, corresponding to the digital state of the respective bit. In this way, the Successive Approximation A/D gives a serial output during conversion and a parallel output between conversion cycles.

IMPLEMENTATION

Figure 3 shows a schematic diagram of an S/A type A/D using a monolithic D/A and a CMOS SAR. The system requires a total of 4 IC's at a system cost of less than $20. As shown, the system operates on +5 and -15 volt supplies, requires approximately 200 mW of power, and will operate at 2 μs/bit conversion rates.

With the exception that a current output D/A is being used, the circuit shown in Figure 3 operates exactly as described in the theory of operations section.

In operation, the input voltage V_{in}, drives an MLM301A op amp connected as a non-inverting, unity-gain buffer. This is simply to translate impedances so that the impedance of the driving source has no affect on the A/D's output.

The output of the D/A is a current sink proportional to the reference current I_{ref} and the digital word on the address lines of the D/A; inputs A1 thru A8. The digital word input to the D/A will be represented by X.

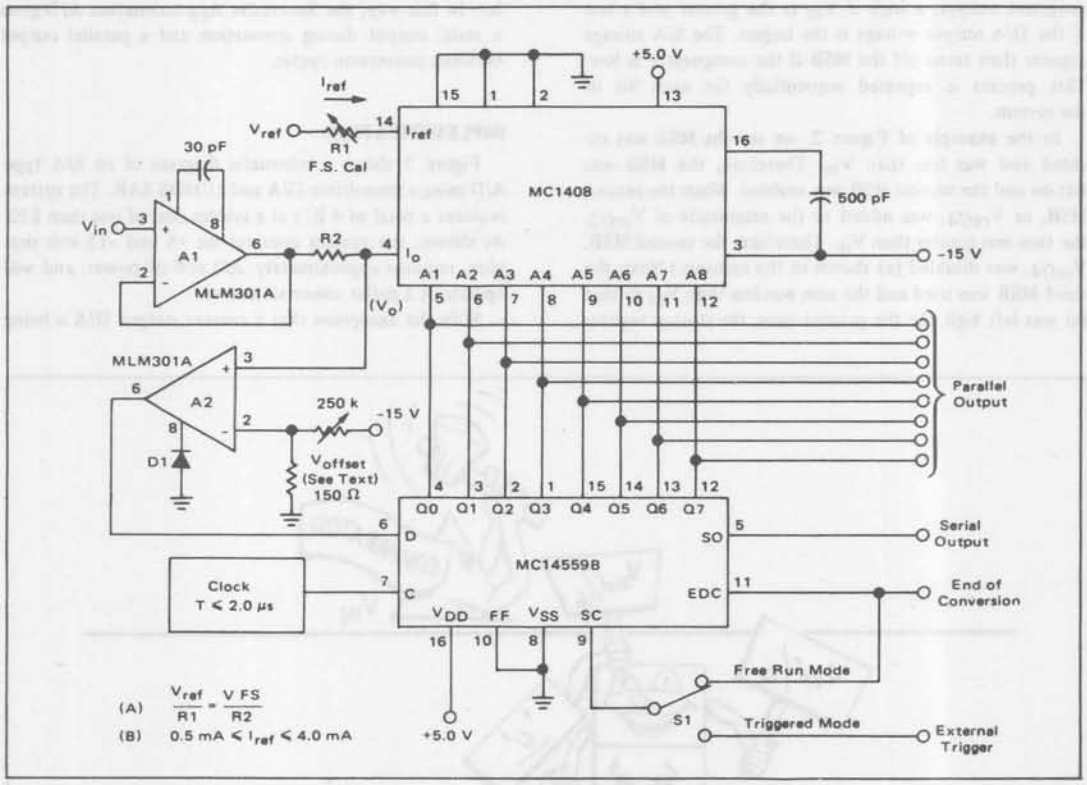

FIGURE 3 – 8-Bit Successive Approximation A/D Schematic Diagram

(1) $I_o = I_{ref} \cdot X$
and
(2) $I_{ref} = V_{ref}/R1$
Where I_o is the output current sink of the D/A.

The voltage on the output of the D/A, V_O, is a function of V_{in} and the output current of the D/A.

(3) $V_O = V_{in} \cdot R2\, I_o$

The comparator, A2, compares V_O to V offset which is -1/2 LSB.

If V_O is greater than V offset the output of the comparator is a "one".

Full scale voltage (11111111), of the system as set up was 2.56 volts. This gives each LSB a value of 10 mV. Any value of full scale could be chosen as long as one does not saturate the input buffer amplifier (input voltage must stay about 1 volt below the positive supply of the op-amp to keep it out of saturation), and the Equations (A) and (B) are followed. Equations (A) and (B) are shown with Figure 3.

Calibration of the system is very easy. Simply put a voltage of full scale minus 1/2 LSB into the input and adjust the full scale calibrate pot (R) to make the transition from 11111110 to 11111111 occur at this point. Now put an input of +1/2 LSB into the system and adjust the offset adjust pot to set the 00000000 to 00000001 transition to occur at this point. Since the two adjustment described are somewhat interactive it may be necessary to go through the procedure more than once.

As stated earlier the system will run nicely at 2 μs/bit giving a total conversion of (n+1) x 2 μs. In this case, n is 8 so the system has a conversion time of 9 x 2 or 18 μs. The primary limit of speed in the system is the propagation delay time of the comparator (MLM301A) and the SAR. The propagation delay time for the 301A is on the order of 1 μs with a 5 mV over drive. The propagation delay of the SAR is about 450 ns at 5 volts. Adding the prop delays gives about 1.5 μs. When the setting time of the D/A is added in, about 250 ns, we see the total is 1.75 μs. Hence the operational figure of 2 μs/bit. Operational waveforms are shown in Figures 5 and 6.

Figure 4 shows a schematic of another system which is very similar to the one in Figure 3 except that the SAR is running on +12 volts and a MC1710C comparator is used with a one transistor level translator on its output. At 12 volts V_{DD} on the SAR its prop delay is typically 135 ns. The comparator and level translator has a total prop delay of about 50 ns. Now the total delay time is

135 ns for the SAR, 50 ns for the comparator and the 250 ns for the D/A.

This gives a total time of 435 ns/bit or a 2 MHz clock rate. Total conversion time for this system is 500 ns x 9 or 4.5 μs. The cost of the high speed system is about the same as the lower speed version but it requires several more components and the addition of one more power supply, as well as requiring about 400 mW of power. Accuracy, calibration and operation of the high speed version are exactly the same as described for the lower speed system. Therefore, for clock speeds up to 500 kHz the circuit shown in Figure 3 is adequate. However where higher speeds are required, up to 2 MHz, the system shown in Figure 4 should be used.

would be truncated to 4-bits and the MC14549B used for the remaining 8. For more information on cascading of the SAR chips see the MC14559B data sheet.

In this treatise, only binary coded A/D systems have been discussed. All of the circuits shown here and the theory put forth apply equally well to systems of BCD coding, or in most cases to non-linearly weighted systems. The only stipulation being that the D/A used is monotonic. Everything in the circuits shown would be the same for these last two cases except that the D/A converters would have a different transfer function.

SYSTEM ACCURACY

The Successive Approximation A/D system has several

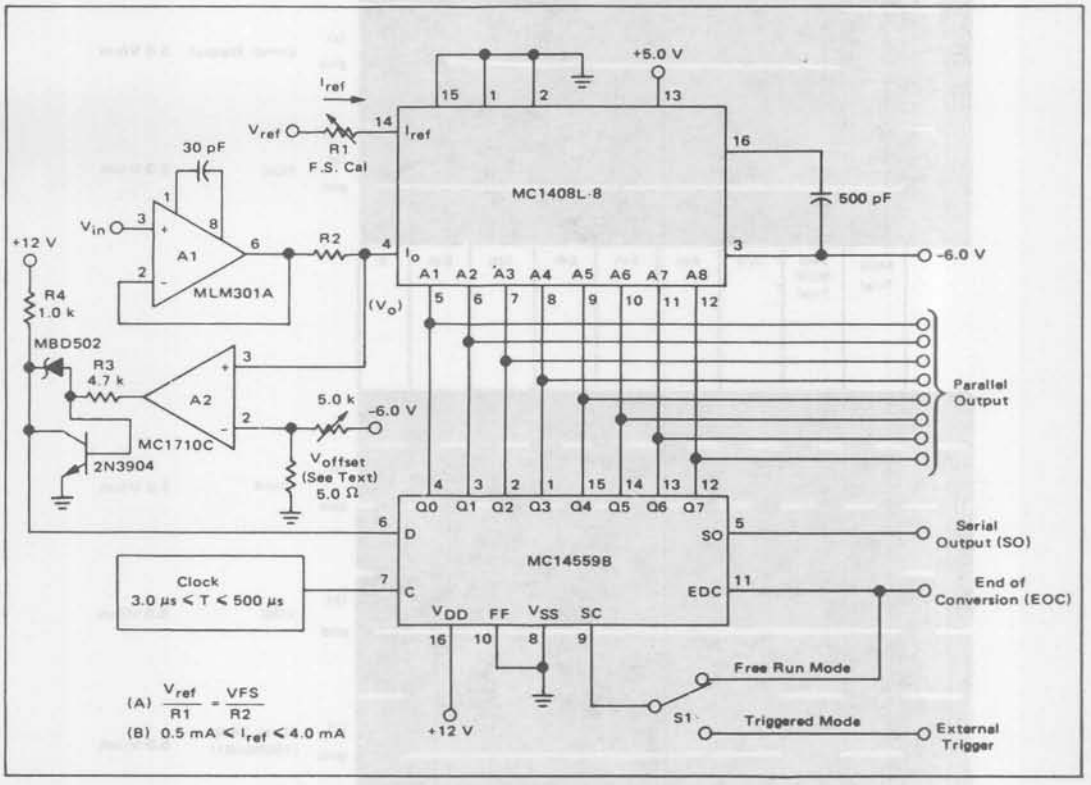

FIGURE 4 – 8-Bit Successive Approximation A/D Schematic Diagram, High Speed Version

Both of the A/D systems described in this paper are 8-bit systems. If desired a 4, 5, 6, or 7-bit system could be implemented using the same configuration as shown in Figure 3 or Figure 4. The only change being the truncation of the length of the SAR, see Figure 7. Note that for a 6-bit system only a 6-bit accurate D/A is required.

If a system of more than 8-bits is required, the MC14559B may be cascaded with the MC14549B to make an SAR of anything from 9 to 16-bits. For 12-bits the MC14559B

sources of error. They are; Quanitization error, D/A accuracy, Comparator gain, Offset voltages of components, and D/A settling time. To get a feel for the relative magnitude of each of these, they will be examined individually in detail.

Quanitization error is that error inherent in every A/D system. It comes from the fact that the smallest increment the system can resolve is ±1/2 of a quantization unit. That is; an n-bit A/D has 2^n equal quanitization levels.

FIGURE 5 –

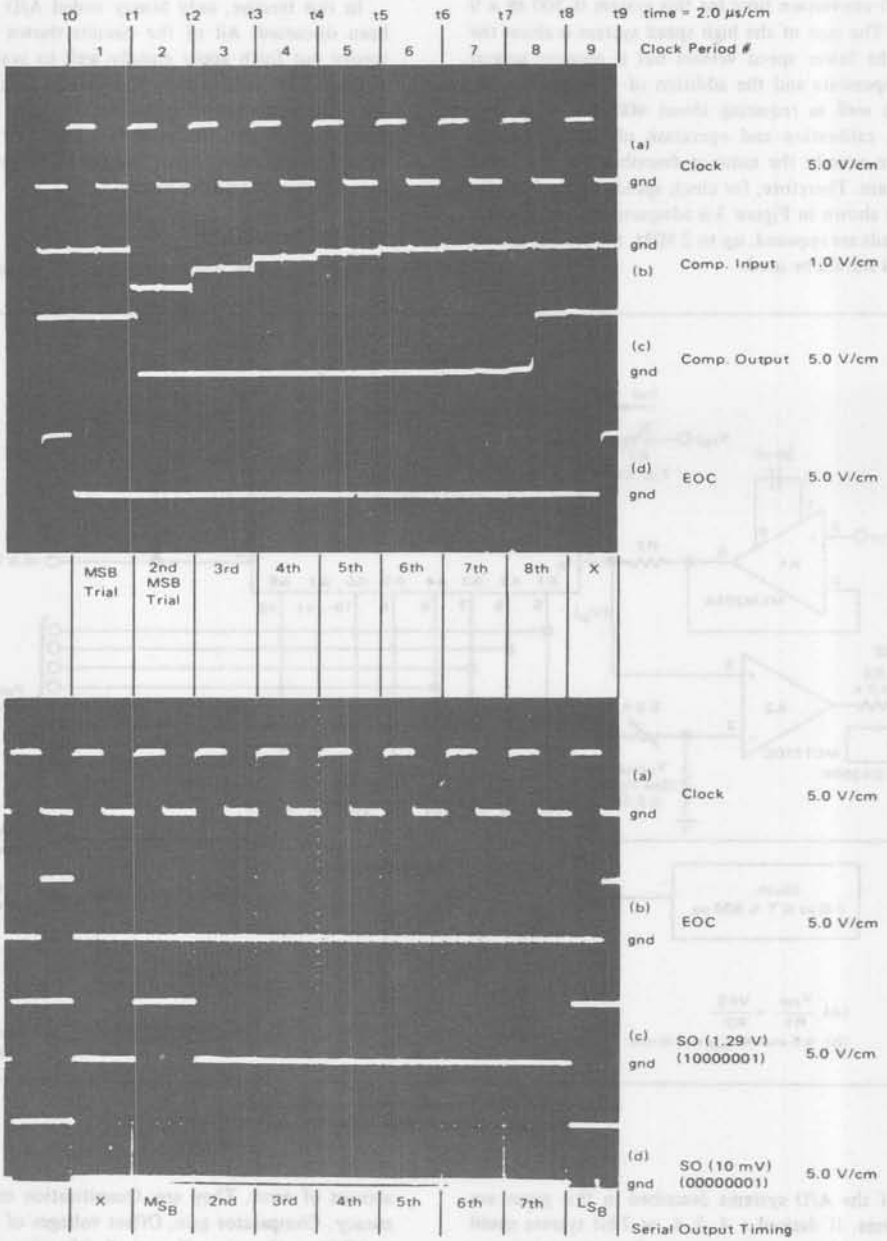

FIGURE 6 –

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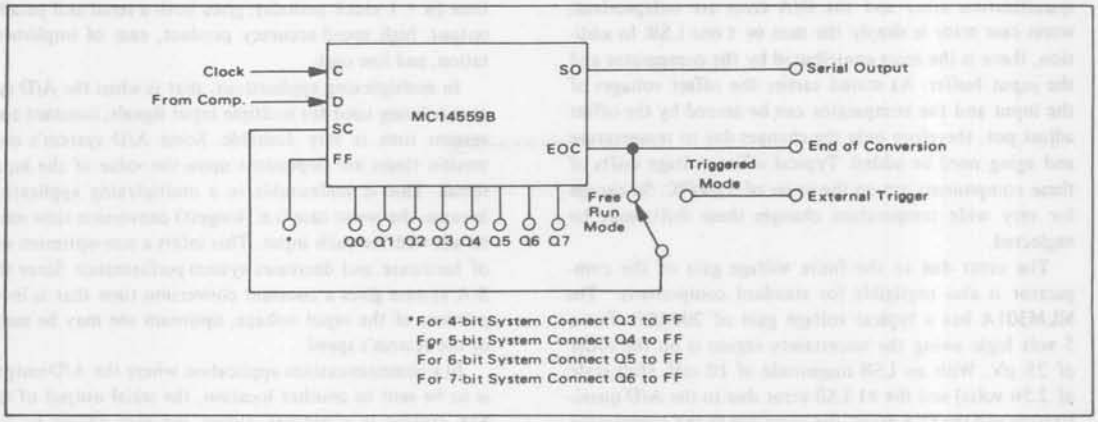

FIGURE 7 –

There are 2^n possible digital words the A/D can give as an output, each representing one of the 2^n discrete levels. Since there are no words in between these 2^n words, a voltage that is between two levels must be represented by one or the other, usually the closest one. For example, the actual value of the input voltage could be exactly halfway between two levels and the A/D would represent it with one or the other of the two words. In this case the system would be in error +1/2 quanitization unit if the upper level were read out, and -1/2 quanitization unit if the lower level were read out. The maximum error here is 1/2 quanitization unit. In most A/D systems, and in particular this one, the quanitization unit and the LSB are interchangable. Given this, the S/A type of A/D has a built in quanitization error of +1/2 LSB.

The digital-to-analog converter gives an analog output dependent upon the reference and the digital word on its inputs. The accuracy of the D/A depends on how closely the actual analog output of the D/A matches the ideal value described by the reference and the digital word input. In order for a D/A to be n-bit accurate, the analog output must not deviate from the ideal value by more than ±1/2 of the least significant bit. The value of the LSB is $1/2^n$ of reference.

The comparator is essentially a linear device and as such has a certain amount of voltage gain. If the voltage gain of the device is anything less than infinity, the differential input voltage required to switch the comparator output from one state to the other, call it V_d, is greater than zero. The value of V_d is simply the logic swing of the comparator divided by the open loop gain. If the differential input voltage to the comparator is less than V_d, the comparator's output cannot be guaranteed to be a logic one or zero. If we say the threshold of the comparator is half way through this uncertainty region, then we must allow an error of up to $V_d/2$ due to the comparator's finite gain.

There are three sources of offset voltage error in the system of Figure 3. One is the offset voltage of the input buffer amplifier. Another is the offset voltage of the comparator and the third is misadjustment of the offset adjust pot.

The first two offset voltages mentioned are inherent in the devices used and are fixed; usually they are on the order of about ±2 mV for commercial grade components. They are fixed and can be easily compensated for by the offset adjustment. Once they are adjusted for, one only need to be concerned with their changing value due to temperature or age.

In practice, the settling time of the D/A is usually not a source of error. It is mentioned here only as a word of caution because if the D/A is not given time to settle it can be a source of error. In D/A specifications, a figure of time is given for the D/A to settle to some specific amount of accuracy. This means that once the digital word on the input of the D/A has been changed, a certain minimum amount of time is required before the D/A's analog output can be guaranteed fall within given accuracy limits. Therefore when designing an S/A system, the clock period must be long enough to give the SAR and comparator time to function in addition to giving the D/A time to settle to the desired accuracy. Note also that all of these events are sequential. That is, the SAR must give the proper address to the D/A, then the D/A must be allowed to settle and then time must be allowed for the comparator to react. All this must be allowed to happen within one clock period.

Given the sources of error as explained earlier, let us now examine the circuit of Figure 3 and try to estimate the total system accuracy.

First of all, there is the quanitization uncertainty of ±1/2 LSB. In addition to this we must add the error due to the D/A converter. Usually a D/A has an error specification of ±1/2 LSB, although it could be better or worse, depending on the D/A.

In this example (Figure 3) the MC1408L can be purchased with accuracy specs of 6, 7 or 8-bits. 8-bit accuracy implies error of no more than ±1/2 of one part out of 256 or ± one part in 512. So for an 8-bit system as shown, the D/A contributes a maximum of ±1/2 LSB. Since the

quanitization error and the D/A error are independent, worst case error is simply the sum or ± one LSB. In addition, there is the error contributed by the comparator and the input buffer. As stated earlier the offset voltages of the input and the comparator can be zeroed by the offset adjust pot, therefore only the changes due to temperature and aging need be added. Typical offset voltage drifts of these components are on the order of 5 $\mu V/^{o}C$. So except for very wide temperature changes these drifts may be neglected.

The error due to the finite voltage gain of the comparator is also negligible for standard components. The MLM301A has a typical voltage gain of 200,000. For a 5 volt logic swing the uncertainty region is on the order of 25 μV. With an LSB magnitude of 10 mV, (full scale of 2.56 volts) and the ±1 LSB error due to the A/D quanitization and the D/A error, the error due to the comparator is virtually zero.

The offset adjust pot in the system does more than just zero out the offset voltages of the input buffer and comparator. The primary purpose of this adjustment is to offset the scale of the D/A output 1/2 LSB. The reason for this is quite straight forward. It can be seen that the output of the S/A type A/D system is always less than or equal to the input voltage. In some cases the output of the A/D can be exactly equal to the input voltage, while at other times it can be as much as one LSB low. (Quanitization error). When the +1/2 LSB error due to the D/A is added, we have a maximum system error of +1/2 LSB -1-1/2 LSB. In order to make the error of the A/D symmetrical we simply offset the reference input of the comparator a negative 1/2 LSB. (Offsetting the comparator a negative 1/2 LSB is identically equal to raising the D/A output waveform 1/2 LSB). Now the error of the A/D is ±1 LSB.

USES OF THE S/A

The Successive Approximation type of A/D system has a myriad of applications in the medium speed, medium accuracy A/D converter category. There are several reasons for its wide usage. Among these are, constant conversion time (n + 1 clock periods), gives both a serial and parallel output, high speed-accuracy product, ease of implementation, and low cost.

In multiplexing applications, that is when the A/D system is being used for multiple input signals, constant conversion time is very desirable. Some A/D system's conversion times are dependent upon the value of the input signal. This is undesirable in a multiplexing application because the worst case (i.e., longest) conversion time must be allowed for each input. This infers a non-optimum use of hardware and decreases system performance. Since the S/A system gives a constant conversion time that is independent of the input voltage, optimum use may be made of the system's speed.

In a communications application where the A/D output is to be sent to another location, the serial output of the S/A system is a natural. Unless the user desires to run multiple data lines, one for each bit of the A/D, the output of an A/D used in this manner must be changed from a parallel output to a serial output before the information can be sent to a remote location. As the S/A system inherently gives the serial output; a savings in both hardware and cost can be achieved.

The S/A system gives a very high speed-accuracy product. When one considers the speeds achievable coupled with the accuracies obtainable for a given cost system, the S/A has no peers in this category. For example, using the S/A system, an 8-bit A/D conversion can easily be accomplished in less than 5 μs, at a total cost of less than $20. When these same parameters are considered for other types of A/D's such as the Cyclic, Tracking, Parallel etc; the speed-accuracy product for a given system cost is considerably less.

As mentioned earlier, the new monolithic D/A's and SAR's have not only drastically reduced system cost, power, and size, but have increased reliability and temperature performance as well. The successive approximation type of A/D system was very popular before these components were available. Now, with the addition of these MSI building blocks the S/A system can do nothing but become more popular and its field of usage expand.

ANALOG-TO-DIGITAL CONVERSION TECHNIQUES WITH THE M6800 MICROPROCESSOR SYSTEM

This application note describes several analog-to-digital conversion systems implemented with the M6800 microprocessor and external linear and digital IC's. Systems consisting of an 8- and 10-bit successive approximation approach, as well as dual ramp techniques of 3½- and 4½-digit BCD and 12-bit binary, are shown with flow diagrams, source programs and hardware schematics. System tradeoffs of the various schemes and programs for binary-to-BCD and BCD-to-7 segment code are discussed.

Analog-To-Digital Conversion Techniques with the M6800 Microprocessor System

INTRODUCTION

The MPU (microprocessing unit) is rapidly replacing both digital and analog circuitry in the industrial control environment. It provides a convenient and efficient method of handling data, controlling valves, motors and relays, and in general, supervising a complete processing machine. However, much of the information required by the MPU for the various computations necessary in the processing system may be available as analog input signals instead of digitally formatted data. These analog signals may be from a pressure transducer, thermistor or other type of sensor. Therefore, for analog data an A/D (analog-to-digital) converter must be added to the MPU system.

Although there are various methods of A/D conversion, each system can usually be divided into two sections — an analog subsystem containing the various analog functions for the A/D and a digital subsystem containing the digital functions. To add an A/D to the MPU, both of the sections may be added externally to the microprocessor in the form of a PC card, hybrid module or monolithic chip. However, only the analog subsystem of the A/D need be added to the microprocessor, since by adding a few instructions to the software, the MPU can perform the function of the digital section of the A/D converter in addition to its other tasks. Therefore, a system design that already contains an MPU and requires analog information needs only one or two additional inexpensive analog components to provide the A/D. The microprocessor software can control the analog section of the A/D, determine the digital value of the analog input from the analog section, and perform various calculations with the resulting data. In addition, the MPU can control several analog A/D sections in a timeshare mode, thus multiplexing the analog information at a digital level.

Using the MPU to perform the tasks of the digital section provides a lower cost approach to the A/D function than adding a complete A/D external to the MPU. The information presented in this note describes this technique as applied to both successive approximation (SA) A/D and dual ramp A/D. With the addition of a DAC (digital-to-analog converter), a couple of operational amplifiers, and the appropriate MPU software, an 8- or 10-bit successive approximation A/D is available. Expansion to greater accuracies is possible by modifying the software and adding the appropriate D/A converter. The technique of successive approximation A/D provides medium speed with accuracies compatible with many systems. The second technique adds an MC1405 dual ramp analog subsystem to the MPU system and, if desired, a digital display to produce a 12-15 bit binary or a 3½- or 4½-digit BCD A/D conversion with 7-segment display readout. This A/D technique has a relatively slow conversion rate but produces a converter of very high accuracy. In addition to the longer conversion time, the MPU must be totally devoted to the A/D function during the conversion period. However, if maximum speed is not required this technique of A/D allows an inexpensive and practical method of handling analog information.

Figure 1 shows the relative merits of each A/D conversion technique. Listed in this table are conversion time, accuracy and whether interrupts to the MPU are allowed during the conversion cycle.

This note describes each method listed in Figure 1 and provides the MPU software and external system hardware schematics along with an explanation of the basic A/D technique and system peculiarities. In addition, the MPU interface connections for the external A/D hardware schemes are shown. These schemes are a complete 8-bit successive approximation and a 3½-digit dual ramp A/D system, both of which externally perform the conversion and transfer the digital data into the MPU system through a PIA.

For additional information on the MC6800 MPU system or A/D systems, the appropriate data sheets or other available literature should be consulted.

MPU

The Motorola microprocessor system devices used are the MC6800 MPU, MCM6810 RAM, MCM6830 ROM and MC6820 PIA (peripheral interface adapter). The following is a brief description of the basic MPU system as it pertains to the A/D systems presented later in this application note.

The Motorola MPU system uses a 16-bit address bus and an 8-bit data bus. The 16-bit address bus provides 65,536 possible memory locations which may be either storage devices (RAM, ROM, etc.) or interface devices (PIA, etc.). The basic MPU contains two 8-bit accumulators, one 16-bit index register, a 16-bit program counter, a 16-bit stack pointer, and an 8-bit condition code register. The condition code register indicates carry, half carry, interrupt, zero, minus, and 2's complement overflow. Figure 2 shows a functional block of the MC6800 MPU.

The MPU uses 72 instructions with six addressing modes which provide 197 different operations in the MPU. A summary of each instruction and function with the appropriate addressing mode is shown in Appendix A of this note.

Characteristic	Successive Approximation			Dual Ramp			
	8-Bit Software	10-Bit Software	8-Bit Hardware	12-Bit Software	3½-Digit Software	4½-Digit Software	3½-Digit Hardware
External Hardware	8-Bit DAC Op Amp Comparator	10-Bit DAC Op Amp Comparator	8-Bit DAC SAR* Op Amp Comparator	MC1405	MC1405	MC1405	MC1405 MC14435 MC14558 (for 7-segment display)
Conversion Rate	700 μs Constant	1.25 ms Constant	60 μs for MPU, plus A/D Conversion Time	165 ms (max) Variable	60 ms (max) Variable	600 ms (max) Variable	183 μs (min) for MPU, plus A/D Conversion Time
Interrupt Capability	Allowed	Allowed	Allowed	Not Allowed	Not Allowed	Not Allowed	Allowed
Number of Memory Locations Required (Including PIA Configuration)	106	145	42	84	296	328	58
Serial Output Available	Yes	Yes	Yes	No	No	No	No

*Successive Approximation Register

FIGURE 1 – Relative Merits of A/D Conversion Techniques

The RAMs used in the system are static and contain 128 8-bit words for scratch pad memory while the ROM is mask programmable and contains 1024 8-bit words. The ROM and RAM, along with the remainder of the MPU system components, operate from a single +5 volt power supply; the address bus, data bus and PIAs are TTL compatible.

The MPU system requires a 2ϕ non-overlapping clock with a lower frequency limit of 100 kHz and an upper limit of 1 MHz.

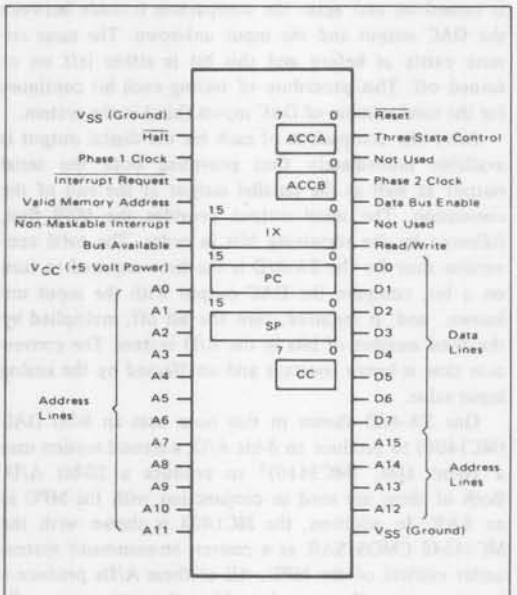

FIGURE 2 – MPU Pin Functions

The PIA is the interface device used between the address and data buses and the analog sections of the A/D. Each PIA contains two essentially identical 8-bit interface ports. These ports (A side, B side) each contain three internal registers that include the data register which is the interface from the data bus to the A/D, the data direction register which programs each of the eight lines of the data register as either an input or an output, and the control register which, in addition to other functions, switches the data bus between the data register and the data direction register. Each port to the PIA contains two addition pins, CA1 and CA2, for interrupt capability and extra I/O lines. The functions of these lines are programmable with the remaining bits in the control register. Figure 3 shows a functional block of the MC6820 PIA.

Each PIA requires four address locations in memory. Two addresses access either of the two (A or B sides) data/data direction registers while the remaining two addresses access either of the two control registers. These addresses are decoded by the chip select and register select lines of the PIA which are connected to the MPU address bus. Selection between the data register and data direction register is made by programming a "1" or "0" in the third least significant bit of each control register . A logic "0" accesses the data direction register while a logic "1" accesses the data register.

By programming "0"s in the data direction register each corresponding line performs as an input, while "1"s in the data direction register make corresponding lines act as outputs. The eight lines may be intermixed between inputs and outputs by programming different combinations of "1"s and "0"s into the data direction register. At the beginning of the program the I/O configuration is programmed into the data direction register, after which the control register is programmed to select the data register for I/O operation.

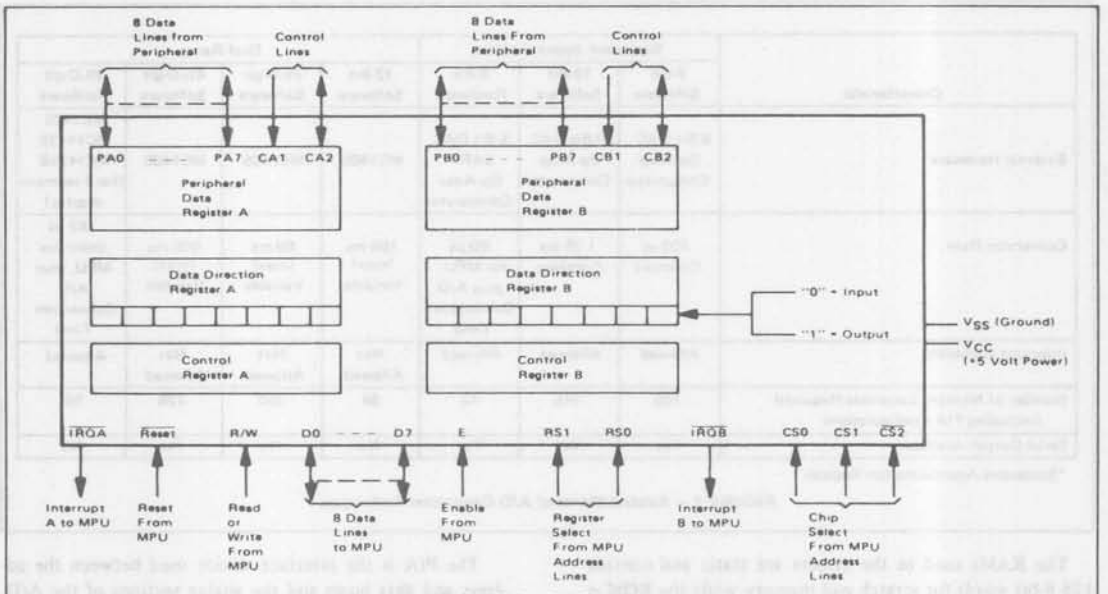

FIGURE 3 – PIA Functions

The printouts shown for each A/D program are the source instructions for the cross assembler from the Motorola timeshare. Since the MPU contains a 16-bit address bus and an 8-bit data bus, the hexadecimal number system provides a convenient representation of these numbers. Although the assembler output is in hexadecimal, the source input may be either binary, octal, decimal or hexadecimal. A dollar sign ($) preceding a number in the source instructions indicates hexadecimal, a percent sign (%) indicates binary and an at sign (@) indicates octal. No prefix indicates the decimal number system.

Only the beginning addresses of the program and labels are shown in the source programs. These beginning addresses may be changed prior to assembling the total system program or the programs may be relocated after assembly with little or no modification.

SUCCESSIVE APPROXIMATION TECHNIQUES

General

One of the more popular methods of A/D conversion is that of successive approximation. This technique uses a DAC (digital-to-analog converter) in a feedback loop to generate a known analog signal to which the unknown analog input is compared. In addition to medium speed conversion rates, it has the advantages of providing not only a parallel digital output after the conversion is completed but also the serial output during the conversion.

Figure 4 shows the block diagram and waveform of the SA-A/D. The DAC inputs are controlled by the successive approximation register (SAR) which is, as presented here, the microprocessor. The DAC output is compared to the analog input (V_{in}) by the analog comparator and its output controls the SAR. At the start of a conversion the MSB of the DAC is turned on by the SAR, producing an output from the DAC equal to half of the full scale value. This output is compared to the analog input and if the DAC output is greater than the input unknown, the SAR turns the MSB off. However, if the DAC output is less than the input unknown, the MSB remains on. Following the trial of the MSB the next most significant bit is turned on and again the comparison is made between the DAC output and the input unknown. The same criteria exists as before and this bit is either left on or turned off. This procedure of testing each bit continues for the total number of DAC inputs (bits) in the system.

After the comparison of each bit the digital output is available immediately thus providing both the serial output as well as the parallel output at the end of the conversion. The serial output provides the MSB first, followed by the remaining bits in order. The total conversion time for the SA-A/D is the time required to turn on a bit, compare the DAC output with the input unknown and, if required, turn the bit off, multiplied by the total number of bits in the A/D system. The conversion time is hence constant and unaffected by the analog input value.

One SA-A/D shown in this note uses an 8-bit DAC (MC1408) to produce an 8-bit A/D; a second version uses a 10-bit DAC (MC3410)* to produce a 10-bit A/D. Both of these are used in conjunction with the MPU as an SAR. In addition, the MC1408 is shown with the MC14549 CMOS SAR as a convert-on-command system under control of the MPU. All of these A/Ds produce a binary output. However, by adding the appropriate software a BCD output or 7-segment-display outputs are available. Also by using a BCD-weighted DAC, the BCD output can be produced directly.

*MC3410 to be announced

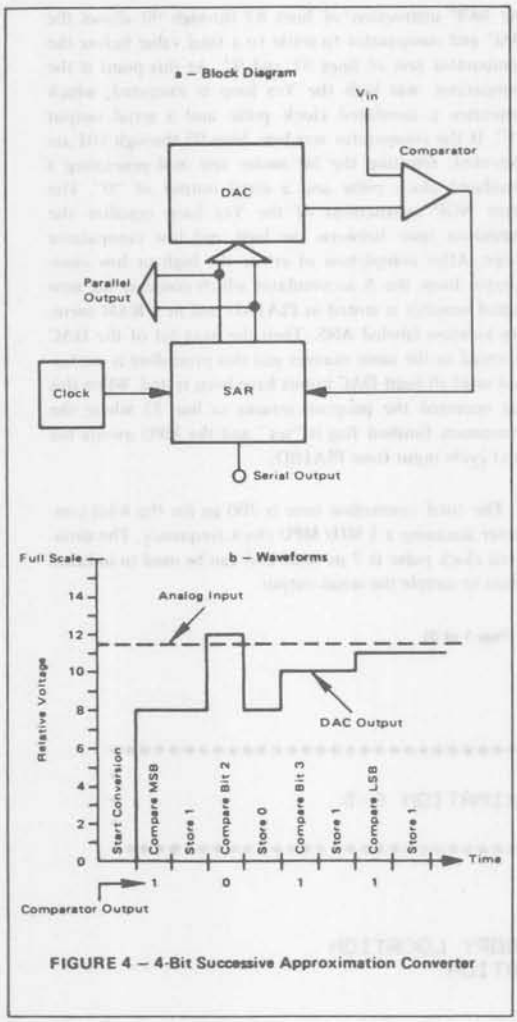

FIGURE 4 – 4-Bit Successive Approximation Converter

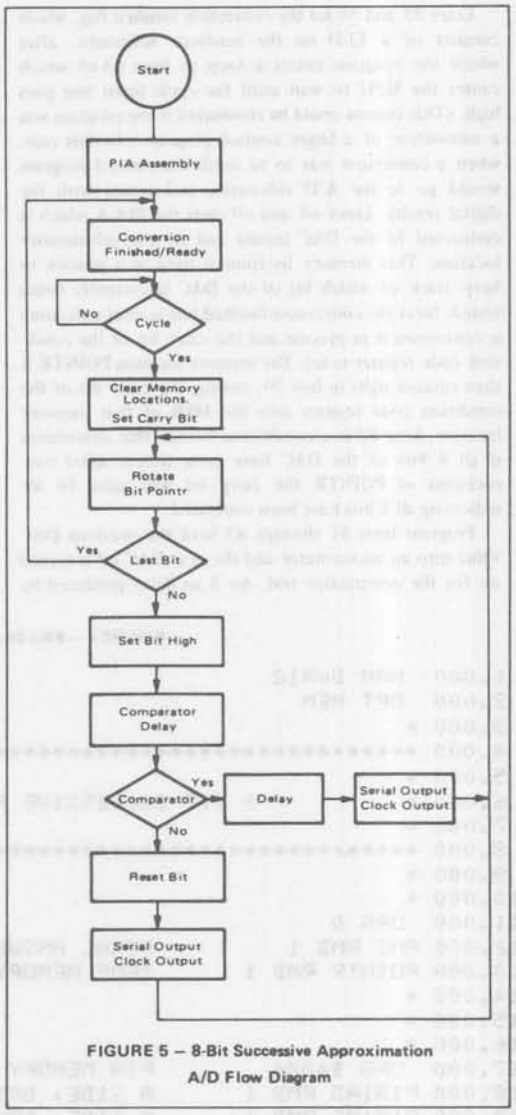

FIGURE 5 – 8-Bit Successive Approximation A/D Flow Diagram

8-Bit SA Program

The flow chart for the 8-bit MPU A/D system is shown in Figure 5; Figures 6 and 7 show the software and the hardware external to the microprocessor. The DAC used is the MC1408L-8 which has active high inputs and a current sink output. An uncompensated MLM301A operational amplifier is used as a comparator while an externally compensated MLM301A or internally compensated MC1741 operational amplifier is used as a buffer amplifier for the input voltage. The output voltage compliance of the DAC is ±0.5 volt; if the current required by the D/A does not match that produced from the output of the buffer amplifier through R1 and R2, then the DAC output will saturate at 0.5 volt above or below ground, thus toggling the comparator. The system is calibrated by adjusting R1 for 1 volt full scale, and zero calibration is set by adjusting R3.

The first MPU instruction for the 8-bit A/D is in line 45 of Figure 6. After assembly, this instruction will be placed in memory location $0A00 as defined in the assembler directive of line 42. The assembled code for this program is relocatable in memory as long as the PIA addresses and storage addresses are unchanged. The program as shown requires 106 memory bytes. Source program lines 45 through 53 configure the PIAs for the proper input/output configuration. PIA1BD is used for various control functions between the MPU system and the external hardware. The exact configuration of this PIA is shown in lines 28 through 33 of Figure 6. PIA1AD provides the 8-bit output needed for the DAC. Lines 51 through 53 set bit 3 of the PIA control register to access the data register for the actual A/D program.

Lines 55 and 56 set the conversion finished flag, which consists of a LED on the hardware schematic, after which the program enters a loop in lines 63-65 which causes the MPU to wait until the cycle input line goes high. (This feature could be eliminated if the program was a subroutine of a larger control program.) In this case, when a conversion was to be made the control program would go to the A/D subroutine and return with the digital results. Lines 68 and 69 clear the PIA-A which is connected to the DAC inputs and an internal memory location. This memory location is used as a pointer to keep track of which bit of the DAC is currently being tested. Next the conversion finished line is reset indicating a conversion is in process and the carry bit of the condition code register is set. The memory location POINTR is then rotated right in line 79, moving the carry bit of the condition code register into the MSB of that memory location. Line 80 is a conditional branch that determines if all 8 bits of the DAC have been tested. After nine rotations of POINTR the carry bit will again be set indicating all 8 bits have been compared.

Program lines 81 through 83 load the previous DAC value into an accumulator and the next DAC bit is turned on for the comparator test. An 8 μs delay produced by the NOP instruction of lines 87 through 90 allows the DAC and comparator to settle to a final value before the comparator test of lines 91 and 92. At this point if the comparator was high the Yes loop is executed, which generates a simulated clock pulse and a serial output "1". If the comparator was low, lines 95 through 101 are executed, resetting the bit under test and generating a simulated clock pulse and a serial output of "0". The three NOP instructions of the Yes loop equalize the execution time between the high and low comparator loops. After completion of either the high or low comparator loop, the A accumulator which contains the new digital number is stored in PIA1AD and in a RAM memory location labeled ANS. Then the next bit of the DAC is tested in the same manner and this procedure is continued until all eight DAC inputs have been tested. When this has occurred the program returns to line 55 where the conversion finished flag is "set" and the MPU awaits the next cycle input from PIA1BD.

The total conversion time is 700 μs for the 8-bit converter assuming a 1 MHz MPU clock frequency. The simulated clock pulse is 7 μs wide and can be used to indicate when to sample the serial output.

FIGURE 6 – 8-Bit SA Software (Page 1 of 3)

```
1.000  NAM DWA12
2.000  OPT MEM
3.000 *
4.000 ************************************************************
5.000 *                                                          *
6.000 *        8 BIT SUCCESSIVE APPROXIMATION A/D                *
7.000 *                                                          *
8.000 ************************************************************
9.000 *
10.000 *
11.000  ORG 0
12.000 ANS RMB 1        FINAL ANSWER MEMORY LOCATION
13.000 POINTR RMB 1     TEMP MEMORY LOCATION
14.000 *
15.000 *
16.000 *
17.000  ORG $4004       PIA MEMORY ADDRESSES
18.000 PIA1AD RMB 1     A SIDE, DATA REGISTER
19.000 PIA1AC RMB 1     A SIDE, CONTROL REGISTER
20.000 PIA1BD RMB 1     B SIDE, DATA REGISTER
21.000 PIA1BC RMB 1     B SIDE, CONTROL REGISTER
22.000 *
23.000 *                PIA1AD USED FOR DIGITAL OUTPUT TO DAC
24.000 *                PIA1BD USED FOR A/D CONTROL
25.000 *
26.000 *
27.000 *
28.000 ******************PIA1BD PIN CONNECTIONS******************
29.000 ************************************************************
30.000 * PB7  *  PB6 *  PB5 *  PB4 *  PB3 *  PB2 *  PB1 *  PB0 *
31.000 ************************************************************
32.000 * COMP  *  NC  *  SC  *  CF  *  SD  *  NC  * CYCLE * NC  *
33.000 ************************************************************
34.000 *                        *
35.000 *
```

FIGURE 6 – 8-Bit SA Software (Page 2 of 3)

```
36.000 *
37.000 * COMP-COMPARATOR,SC-SIMULATED CLOCK,SO-SERIAL OUTPUT
38.000 * CF-CONVERSION FINISHED, NC-NO CONNECTION
39.000 *
40.000 *
41.000 *
42.000  ORG $0A00          BEGINNING ADDRESS
43.000 *
44.000 *                              **PIA ASSEMBLY**
45.000  CLR PIA1AC
46.000  CLR PIA1BC
47.000  LDA A #$7C
48.000  STA A PIA1BD
49.000  LDA A #$0FF
50.000  STA A PIA1AD       A SIDE ALL OUTPUTS
51.000  LDA A #$04
52.000  STA A PIA1AC
53.000  STA A PIA1BC
54.000 *
55.000 RSTART LDA A #$10
56.000  STA A PIA1BD       SET CONVERSION FINISHED
57.000 *
58.000 *
59.000 *
60.000 *                              **CYCLE TEST**
61.000 *
62.000 *
63.000 CYCLE LDA A PIA1BD
64.000  AND A #$02
65.000  BEQ CYCLE
66.000 *
67.000 *
68.000  CLR PIA1AD
69.000  CLR POINTR
70.000 *
71.000 *
72.000 *
73.000  CLR PIA1BD        RESET CONVERSION FINISHED
74.000  SEC
75.000 *
76.000 *
77.000 *
78.000 *
79.000 CONVRT ROR POINTR
80.000  BCS RSTART
81.000  LDA A PIA1AD      RECALL PREVIOUS DIGITAL OUTPUT
82.000  ADD A POINTR
83.000  STA A PIA1AD      SET NEW DIGITAL OUTPUT
84.000 *
85.000 *                              **DELAY FOR COMPARATOR**
86.000 *
87.000  NOP
88.000  NOP
89.000  NOP
90.000  NOP
91.000  LDA A PIA1BD      COMPARATOR TEST
92.000  BMI YES
93.000 *
94.000 *                              **LOW COMPARATOR LOOP**
95.000  LDA A PIA1AD
96.000  SUB A POINTR
```

```
 97.000  LDA B #$20        SERIAL OUT OF "0", CLOCK SET
 98.000  STA B PIA1BD
 99.000  CLR B             CLOCK RESET
100.000  STA B PIA1BD
101.000  BRA END
102.000 ◆
103.000 ◆                              ◆◆HIGH COMPARATOR LOOP◆◆
104.000 YES LDA A PIA1AD
105.000  NOP
106.000  NOP               DELAY
107.000  NOP
108.000  LDA B #$28        SERIAL OUTPUT OF "1", CLOCK SET
109.000  STA B PIA1BD
110.000  LDA B #$08        CLOCK RESET
111.000  STA B PIA1BD
112.000 ◆
113.000 END STA A PIA1AD
114.000  STA A ANS
115.000  BRA CONVRT
116.000 ◆
117.000 ◆
118.000 ◆
119.000 ◆
120.000 ◆
121.000 ◆
122.000  MON
```

FIGURE 6 – 8-Bit SA Software (Page 3 of 3)

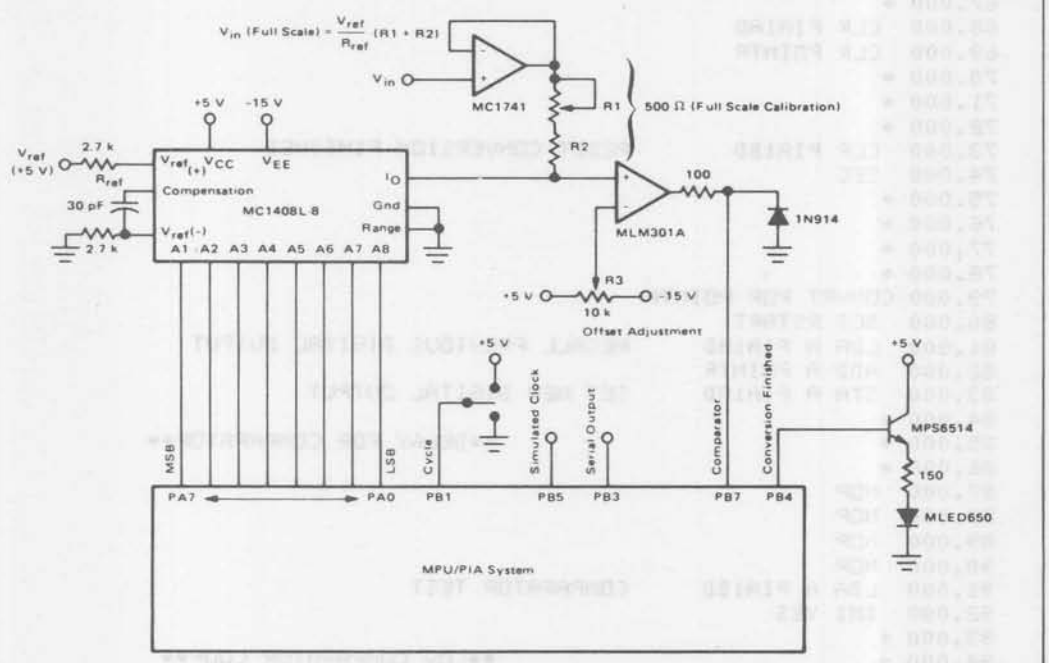

FIGURE 7 – 8-Bit SA Hardware

10-Bit SA Program

Figures 8 and 9 show the MPU software and external hardware for a 10-bit successive approximation A/D using the MC3410 DAC. The operation of this A/D is very similar to that of the 8-bit A/D. Both the A and B halves of a PIA are required for the DAC output while the control lines (comparator, conversion finished, etc.) are also identical to that of the 8-bit A/D previously discussed. The pointer for indicating which bit is currently under test is contained in two memory locations, PONTR1 and PONTR2. The pointer is initialized in lines 63 and 64 and as before, it is continuously shifted to the left as each bit is tested. Lines 72 through 77 and lines 89 through 101 operate on both halves of the PIA, "setting" and "resetting" the DAC bits under test. The final answer is stored in the two PIA memory locations as well as two internal memory locations (ANS1 and ANS2).

By using the appropriate DAC and changing line 63 of the software program, the 10-bit SA D/A can be modified for 9-16 bit A/D operation.

FIGURE 8 – 10-Bit SA Software (Page 1 of 3)

```
 1.000  NAM DWA40
 2.000  OPT MEM
 3.000 *
 4.000 ************************************************************
 5.000 *                                                          *
 6.000 *          10 BIT SUCCESSIVE APPROXIMATION A/D             *
 7.000 *                                                          *
 8.000 ************************************************************
 9.000 *
10.000 *
11.000  ORG 0
12.000 ANS1 RMB 1         FINAL ANSWER LOCATION (MSB)
13.000 ANS2 RMB 1         FINAL ANSWER LOCATION (LSB)
14.000 PONTR1 RMB 1       POINTER FOR BIT UNDER TEST
15.000 PONTR2 RMB 1       POINTER FOR BIT UNDER TEST
16.000 *
17.000 *
18.000  ORG $4006         PIA MEMORY ADDRESSES
19.000 PIA1BD RMB 1       B SIDE, DATA REGISTER
20.000 PIA1BC RMB 1       B SIDE, CONTROL REGISTER
21.000 PIA2AD RMB 1       A SIDE, DATA REGISTER
21.500 PIA2AC RMB 1       A SIDE, CONTROL REGISTER
22.000 PIA2BD RMB 1       B SIDE, DATA REGISTER
23.000 PIA2BC RMB 1       B SIDE, CONTROL REGISTER
24.000 *
25.000 *                  PIA1AD USED FOR DIGITAL OUTPUT TO DAC
26.000 *                  PIA1BD USED FOR A/D CONTROL
27.000 *
28.000 *
29.000 *
30.000 ********************PIA1BD PIN CONNECTIONS********************
31.000 ************************************************************
32.000 * PB7   *  PB6 *  PB5 *  PB4 *  PB3 *  PB2 *  PB1 *  PB0 *
33.000 ************************************************************
34.000 * COMP  *  NC  *  SC  *  CF  *  SO  *  NC  * CYCLE *  NC  *
35.000 ************************************************************
36.000 *                              *
37.000 *
38.000 *
39.000 * COMP-COMPARATOR,SC-SIMULATED CLOCK,SO-SERIAL OUTPUT
40.000 * CF-CONVERSION FINISHED, NC-NO CONNECTION
41.000 *
42.000 *
43.000 *
44.000 *
45.000 *
46.000  ORG $0A00          BEGINNING OF PROGRAM
47.000 *                        *PIA ASSEMBLY*
48.000  CLR PIA1BC
49.000  CLR PIA2AC
```

FIGURE 8 – 10-Bit SA Software (Page 2 of 3)

```
 50.000  CLR PIA2BC
 51.000  LDA A #$7C
 52.000  STA A PIA1BD
 53.000  LDA A #$0FF
 54.000  STA A PIA2AD
 55.000  STA A PIA2BD
 56.000  LDA A #$04
 57.000  STA A PIA1BC
 58.000  STA A PIA2AC
 59.000  STA A PIA2BC
 60.000 *
 61.000 RESTART LDA A #$10
 62.000  STA A PIA1BD          SET CONVERSION FINISHED
 63.000  CLR PONTR1
 64.000  CLR PONTR2
 65.000 *
 66.000 *
 67.000 *
 68.000 *                              *CYCLE TEST*
 69.000 *****************************************************
 70.000 *
 71.000 CYCLE LDA A PIA1BD
 72.000  AND A #$02
 73.000  BEQ CYCLE
 74.000 *                            *RESET DAC INPUTS*
 75.000  CLR PIA2AD
 76.000  CLR PIA2BD
 77.000 *
 78.000 *
 79.000 *
 80.000  CLR PIA1BD          RESET CONVERSION FINISHED
 81.000  LDA A #$04
 82.000  STA A PONTR1
 83.000 *
 84.000 *
 85.000 *
 86.000 *
 87.000 CONVRT ROR PONTR1
 88.000  ROR PONTR2
 89.000  BCS RESTART
 90.000  LDA A PIA2AD         RECALL PREVIOUS DIGITAL OUTPUT(8 LSB)
 91.000  ADD A PONTR1
 92.000  STA A PIA2AD         SET NEW DIGITAL OUTPUT
 93.000  LDA A PIA2BD         RECALL PREVIOUS DIGITAL OUTPUT(2 MSB)
 94.000  ADD A PONTR2
 95.000  STA A PIA2BD         SET NEW DIGITAL OUTPUT
 96.000 *****************************************************
 97.000 *                            *DELAY FOR COMPARATOR*
 98.000 *
 99.000  NOP
100.000  NOP
101.000  NOP
102.000  NOP
103.000  LDA A PIA1BD         COMPARATOR TEST
104.000  BMI YES
105.000 *
106.000 *
107.000 *                            *LOW COMPARATOR LOOP*
108.000  LDA A PIA2AD
109.000  SUB A PONTR1
110.000  STA A PIA2AD
111.000  STA A ANS1
112.000  LDA A PIA2BD
```

```
113.000  SUB A PONTR2
114.000  STA A PIA2BD
115.000  STA A ANS2
116.000  LDA B #$20          SERIAL OUTPUT (CLOCK ONLY)
117.000  STA B PIA1BD
118.000  CLR B               CLOCK RESET
119.000  STA B PIA1BD
120.000  BRA END
121.000 ◆
122.000 ◆
123.000 ◆                          ◆HIGH COMPARATOR LOOP◆
124.000 YES LDA A #$05      TIME EQUALIZATION
125.000 DELAY DEC A
126.000  BNE DELAY
127.000  LDA B #$28          SERIAL OUTPUT
128.000  STA B PIA1BD
129.000  LDA B #$08          CLOCK RESET
130.000  STA B PIA1BD
131.000  NOP
132.000  NOP
133.000 ◆
134.000 END BRA CONVRT
135.000 ◆
136.000 ◆
137.000 ◆
138.000  MON
```

FIGURE 8 – 10-Bit SA Software (Page 3 of 3)

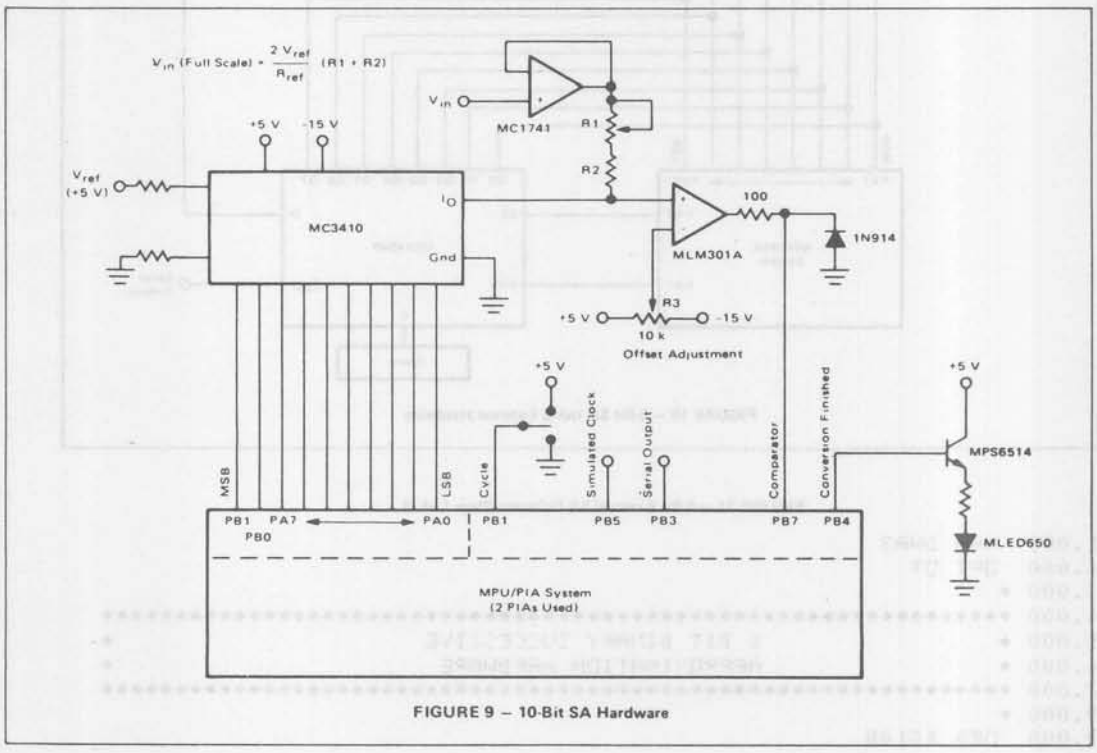

FIGURE 9 – 10-Bit SA Hardware

External SA System

The third successive approximation program, shown in Figures 10 and 11, uses an MC1408 DAC with the MC14549 CMOS SAR for a convert-on-command A/D system. This system is controlled by the MPU through the CA1 and CA2 PIA pins to start a conversion and store the results of this conversion in memory when the conversion is finished. The 8-bit data word from the A/D is brought in to the MPU system through PIA1AD. The advantages of this A/D system are that a minimum number of software instructions are required, a higher speed conversion is possible, and the MPU may be performing other tasks during the conversion. The disadvantage is a higher parts count and increased cost.

The program for this A/D, shown in Figure 11, is written as a subroutine of a larger program. This larger program is simulated with the instructions of lines 28 through 31. The subroutine starts in line 34, unmasking the interrupt input on CA1 and setting CA2 high. (For additional information on use of the CA1 and CA2 lines, see the MC6820 data sheet.) CA2 initiates the conversion. Line 35 is a dummy read statement necessary to clear the data register of the interrupt bit associated with the CA1 input line. Then a wait for interrupt instruction stores the stack in anticipation of the A/D conversion being completed. When the conversion is finished the CA1 line is toggled by the EOC output of the MC14549 and the program goes to line 43 where CA1 is masked and CA2 is set low, thus stopping any further conversion sequences by the A/D. The digital results are loaded into the A accumulator through PIA-A and stored in memory location TEMP. Then the MPU returns from the interrupt and finally returns from the subroutine.

The entire sequence requires 60 μs plus the conversion time of the A/D.

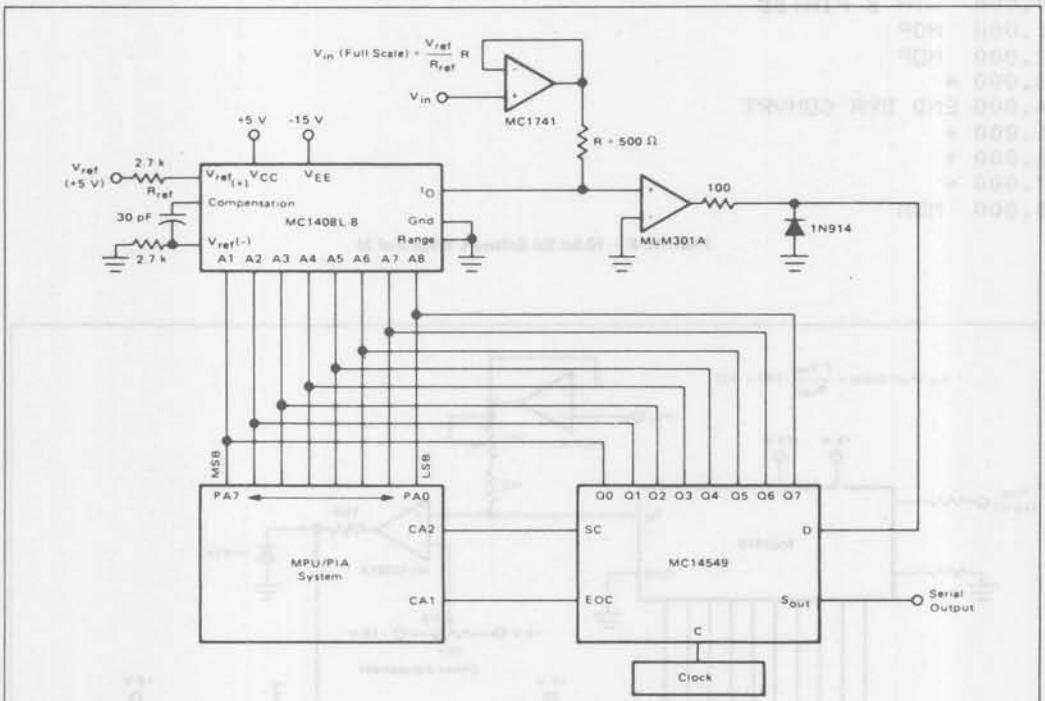

FIGURE 10 – 8-Bit SA Using External Hardware

FIGURE 11 – 8-Bit External SA Software (Page 1 of 2)

```
1.000  NAM DMA3
2.000  OPT OT
3.000  *
4.000  ********************************************************************
5.000  *                    8 BIT BINARY SUCCESSIVE                       *
6.000  *                    APPROXIMATION HARDWARE                        *
7.000  ********************************************************************
8.000  *
9.000  ORG $0100
```

```
10.000 TEMP RMB 1              8 BIT BINARY DATA
11.000 *
12.000 *
13.000  ORG $4004
14.000 PIA1AD RMB 1            DATA REGISTER
15.000 PIA1AC RMB 1            CONTROL REGISTER
16.000 *
17.000 *
18.000 *
19.000 *
20.000  ORG $0300
21.000  CLR PIA1AC             PIA ASSEMBLY
22.000  CLR PIA1AD
23.000  LDA A #$3C
24.000  STA A PIA1AC
25.000  LDS #$0020
26.000 *
27.000 *
28.000  NOP
29.000  JSR CONVRT
30.000 END NOP
31.000  BRA END
32.000 *
33.000 *                                CONVERSION SUBROUTINE
34.000 CONVRT LDA A #$3F                  CA1 UNMASKED,POS EDGE--CA2 HIGH
35.000  LDA B PIA1AD
36.000  STA A PIA1AC
37.000  WAI
38.000  RTS
39.000 *
40.000 *
41.000 *
42.000 *                                INTERRUPT PROGRAM
43.000 INTRPT LDA A #$36                  CA1 MASKED-CA2 LOW
44.000  STA A PIA1AC
45.000  LDA A PIA1AD
46.000  STA A TEMP
47.000  RTI
48.000 *
49.000 *
50.000 *
51.000  MON
```

FIGURE 11 – 8-Bit External SA Software (Page 2 of 2)

3

DUAL RAMP TECHNIQUES

General

Another commonly used method for A/D conversion is the dual ramp or dual slope technique. This approach has a longer conversion time than that of the successive approximation method. The conversion time period is also variable and input voltage dependent. However, this method yields an A/D converter of high accuracy and low cost.

As the name implies the dual ramp method consists of two ramp periods for each conversion cycle. Figure 12 shows the basic waveforms for the dual ramp A/D. The ratio in time of the ramp lengths provides a value representing the difference between a reference and an unknown voltage. During time period T1, the input unknown is integrated for a fixed time period (fixed number of clock cycles). The integrator voltage increases from the reference level to a voltage which is proportional to the input voltage. At the end of this time period a reference voltage is applied to the input of the integrator causing the integrator output voltage to decrease until the reference level is again reached. The number of clock cycles that are required to bring the integrator output voltage back to the reference level is proportional to the input unknown voltage.

The dual ramp converters discussed here use the MC1405 analog subsystem in conjunction with the M6800 MPU system. The MC1405 provides the integrator, comparator and reference voltage required for the analog functions of the dual ramp A/D. The analog device also adds an offset current to the integrator input during the ramp up time period to stabilize small voltage readings. The digital section of the A/D must subtract an equivalent number of counts to produce a zero reading display output for a zero input. The interface between the analog and digital subsystems consists of two control lines. These are the comparator output from the analog part, which indicates whether the ramp is above or below the reference level, and a ramp control output from the digital part to switch the integrator input between the input unknown voltage and the reference voltage. The control of these lines, offset subtraction, and calculations with the resulting data must be handled by the digital subsystem, which in this case is the MPU.

For additional information on the dual ramp technique for A/D, consult the data sheet for the MC1405.

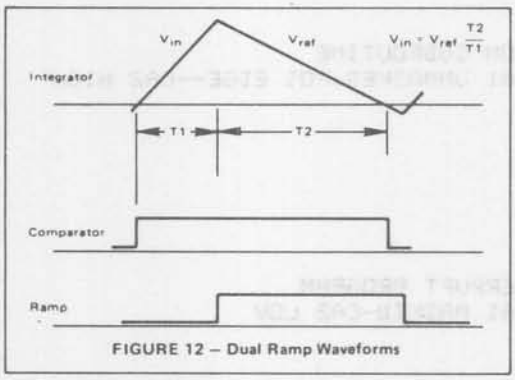

FIGURE 12 – Dual Ramp Waveforms

12-Bit Dual Ramp Program

This version of the dual ramp A/D generates a 12-bit binary output from a 1 volt full scale analog input. Figures 13, 14 and 15 show the flow chart, MPU software and external hardware. The interface of the PIAs used for this A/D is shown both on the schematic and in lines 16 through 22 of the source program. Lines 25 and 26 indicate the two memory locations where the final 12-bit binary result is stored. These locations are $0000 and $0001. The four most significant bits are in location $0000 while the remaining eight bits are in $0001.

Referring to the software of Figure 14, the first instructions (lines 37 through 42) initialize the PIA for its input/output configuration. Source program lines 46 through 49 set the ramp control line of the MC1405 and check the comparator output from the MC1405 to insure that the integrator output is below the reference level at the start of a conversion. Next the "conversion finished" flag is set indicating a conversion ready status. Then the MPU enters a loop (lines 55 through 57) waiting for a cycle input (PB1) from the PIA. When this condition occurs the conversion finished flag is reset while the ramp control line (PB2) goes low, thus starting a conversion cycle. In addition, the index register has been loaded with $2000 which will be decremented to provide the ramp up timing period. When the ramp crosses the threshold level the comparator (PB7) change from low to high causes the MPU to enter the timing cycle of lines 67 through 69. The index register is continuously decremented until reaching zero, at which point the ramp control line (PB2) to the MC1405 is set high (line 74) and the index register is incremented (line 75). This loop continues until the integrator output again reaches the threshold level. Line 76 of the ramp down cycle is a dummy statement included to equalize the timing between the ramp up and ramp down time periods. The proper timing ratio (2:1 in this example) must be maintained for correct A/D operation.

After the termination of the ramp down time period the content of the index register is stored in memory locations $0000 and $0001 (line 82). Next the offset counts are subtracted (512_{10}) from this result by subtracting $01 from memory location $0000. The result is

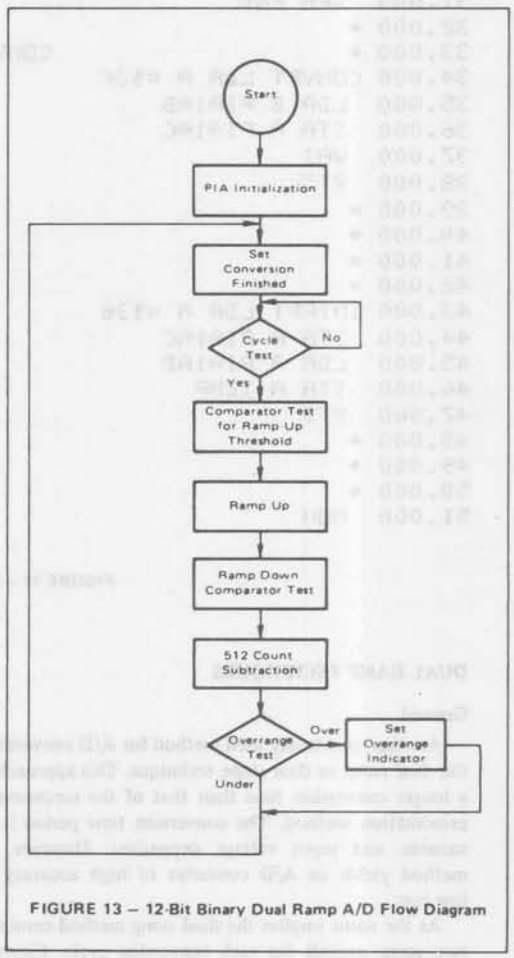

FIGURE 13 – 12-Bit Binary Dual Ramp A/D Flow Diagram

then stored back into the same memory location. Lines 86 and 87 check the contents of memory location TEST for a number greater than 4095_{10}. If this condition occurs, the overrange, conversion finished, and ramp control bits are set high. Otherwise the MPU branches back to line 50 where only the conversion finished and ramp control bits are set high. The program then checks the status of the cycle input waiting for the next conversion.

When assembled, the first instruction will be located at $0A00 with 84_{10} memory locations required. The full scale conversion time is 165 ms assuming a 1 MHz clock in the MPU system.

As with all MC1405 designs, the integration capacitor must be large enough to insure that the integrator does not saturate during the ramp up time period. The value of this capacitor depends upon the power supply voltage applied to the MC1405 and the ramp up time period. The MC1405 data sheet contains the equations for calculation of this capacitor. The MC1405 is capable of operating on a single +5 volt power supply; however, a +15 volt supply voltage is recommended to decrease the integrator capacitor size. When using 15 volts the comparator output must be clamped at 5 volts to prevent damaging the PIA inputs.

FIGURE 14 – 12-Bit Dual Ramp Software (Page 1 of 2)

```
 1.000  NAM DWA10
 2.000  OPT MEM
 3.000 *
 4.000 *
 5.000 *
 6.000 *
 7.000 *
 8.000 ************************************************************
 9.000 *                                                          *
10.000 *    12 BIT BINARY DUAL RAMP A/D USING THE MC1405          *
11.000 *          WITH THE MC6800 SERIES MPU SYSTEM               *
12.000 *                                                          *
13.000 ************************************************************
14.000 *
15.000 *
16.000 *                    INPUT/OUTPUT  PIA LOCATIONS
17.000 *
18.000 *                    RAMP CONTROL (OUTPUT)          PB2
19.000 *                    CYCLE (INPUT)                  PB1
20.000 *                    OVERRANGE (OUTPUT)             PB3
21.000 *                    CONVERSION FINISHED (OUTPUT)PB4
22.000 *                    COMPARATOR (INPUT)             PB7
23.000 *
24.000 *
25.000  ORG $0
26.000 TEST RMB 2          FINAL ANSWER MEMORY LOCATIONS
27.000 *
28.000  ORG $4004
29.000 PIA1AD RMB 1
30.000 PIA1AC RMB 1
31.000 PIA1BD RMB 1        B SIDE,DATA REGISTER
32.000 PIA1BC RMB 1        B SIDE,CONTROL REGISTER
33.000 *
34.000  ORG $0A00          BEGINNING ADDRESS
35.000 *
36.000 *                          **PIA ASSEMBLY**
37.000  CLR PIA1AC
38.000  CLR PIA1BC
39.000  LDA A #$7C
40.000  STA A PIA1BD       SET PIA TO HAVE 3 INPUTS AND 5 OUTPUTS
41.000  LDA A #$04         SET BIT 3 OF PIA CONTROL REGISTER
42.000  STA A PIA1BC
```

```
43.000 *
44.000 *
45.000 *
46.000  LDA A #$04
47.000  STA A PIA1BD      RAMP CONTROL HIGH
48.000 START LDA A PIA1BD   COMPARATOR TEST - INSURES RAMP IS LOW
49.000  BMI START                  TO START CONVERSION
50.000 RSTART LDA A #$14
51.000  STA A PIA1BD      CONVERSION READY , RAMP CONTROL HIGH
52.000 *
53.000 *
54.000 *                          **CYCLE TEST**
55.000 CYCLE LDA A PIA1BD
56.000  AND A #$02
57.000  BEQ CYCLE
58.000  LDX #$2000        INITIALIZATION FOR RAMP UP TIMING
59.000 *
60.000  CLR PIA1BD        RESET OVERRANGE AND CONVERSION FINISHED
61.000 *                          AND SET RC LOW
62.000 COMP LDA A PIA1BD
63.000  BPL COMP
64.000 *
65.000 *
66.000 *                          **RAMP UP TIMING CYCLE**
67.000 RAMPUP LDA B #$04
68.000  DEX
69.000  BNE RAMPUP
70.000 *
71.000 *                          **RAMP DOWN TIMING CYCLE**
72.000 *
73.000 *
74.000 RAMPDN STA B PIA1BD      RC HIGH
75.000  INX
76.000  CPX #0000         DUMMY STATEMENT FOR TIME DELAY
77.000  LDA A PIA1BD      COMPARATOR TEST
78.000  BMI RAMPDN
79.000 *
80.000 *
81.000 *
82.000  STX TEST
83.000  LDA A TEST        512 COUNT SUBTRACTION
84.000  SUB A #$02
85.000  STA A TEST
86.000  SUB A #$10        OVERRANGE TEST
87.000  BCS RSTART
88.000  LDA A #$1C        SET CONVERSION FINISHED,OVERRANGE
89.000  STA A PIA1BD          AND SET RAMP CONTROL HIGH
90.000  BRA CYCLE
91.000  MON
```

FIGURE 14 – 12-Bit Dual Ramp Software (Page 2 of 2)

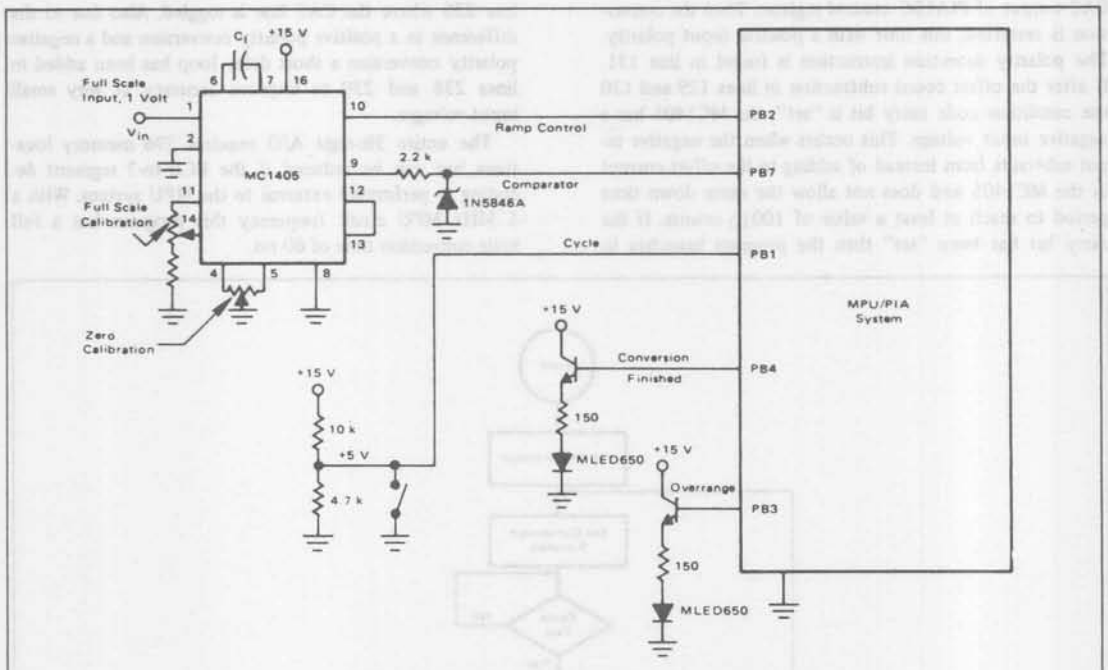

FIGURE 15 – 12-Bit Binary Dual Ramp A/D Hardware

3½-Digit Dual Ramp Program

The flow chart, source program and hardware for a 3½-digit system are shown in Figures 16, 17, and 18 respectively. Referring to Figure 17, the basic conversion routine of lines 96 through 135 in this program is similar to that of the previously discussed 12-bit binary system. The initialization of the index register in line 108 has been changed to increase the ramp up time period. The basic conversion results in a binary number as did the 12-bit version previously discussed. This binary result is converted by the software routine in lines 144 through 180 to produce 3½-digit BCD output. This routine converts up to a 16-bit binary number to the equivalent BCD value. Also the BCD result is converted to a 7-segment display code for use in a LED or LCD readout system. Another feature of the 3½-digit A/D program shown here is a polarity detection scheme. This allows the A/D to handle both positive and negative input voltages.

The external hardware for the 3½-digit A/D requires two full PIAs; one of the four ports is used for interface to the MC1405, cycle input, overrange flag, etc. An I/O configuration similar to that of the 12-bit binary A/D is used. The remaining three ports of the PIAs are used for the 3½-digit display, as shown in Figure 18b.

The conversion initially produces a binary result which is stored in memory locations MSB and MSB+1. This result has 100_{10} offset counts subtracted, and then a polarity check is made. If the polarity that is currently being applied to the input of the MC1405 is positive, the binary number is converted to a BCD number. The technique used for binary-to-BCD conversion is described in Appendix B. The BCD results are stored in memory locations UNTTEN and HNDTHD. Each of these memory locations contains two BCD words. Following the conversion, an overrange test is made in lines 183 through 186 which checks for a maximum of a BCD "1" in the upper four bits of memory location HNDTHD. If an overrange condition occurs, the program branches to lines 227 through 234 where a 1999_{10} is placed in the display and the overrange flag in PIA1BD is "set".

After the overrange test the BCD code is converted to a 7-segment code and stored in the memory location for each PIA port. Segments A through G use PIA outputs 0 through 6 while the half digit output uses PIA2BD output PB7. The conversion technique for BCD-to-7 segment utilizes a look-up table in line 251 with the indexed mode of addressing to access the table. Each of the three full BCD digits is converted to the 7-segment code by first separating the lower BCD and upper BCD word and using the BCD code as the least significant byte of a two byte address for the look-up table. This address is then loaded into the index register and used to locate the corresponding 7-segment code. In the case of the upper BCD digit of each BCD, the memory must be shifted left four times for correct addressing of the look-up table. Finally, the half digit output is added to PIA2BD in lines 197 through 226.

Should the MC1405 have the incorrect polarity on its input, a polarity reversing relay is operated by toggling the

CA2 output of PIA1BC control register. Then the conversion is restarted, this time with a positive input polarity. The polarity detection instruction is found in line 131. If after the offset count subtraction in lines 129 and 130 the condition code carry bit is "set", the MC1405 has a negative input voltage. This occurs when the negative input subtracts from instead of adding to the offset current in the MC1405 and does not allow the ramp down time period to reach at least a value of 100_{10} counts. If the carry bit has been "set" then the program branches to line 236 where the CA2 line is toggled. Also due to the difference in a positive polarity conversion and a negative polarity conversion a short delay loop has been added in lines 238 and 239 to improve accuracy at very small input voltages.

The entire 3½-digit A/D requires 296 memory locations but can be reduced if the BCD-to-7 segment decoding is performed external to the MPU system. With a 1 MHz MPU clock frequency this program has a full scale conversion time of 60 ms.

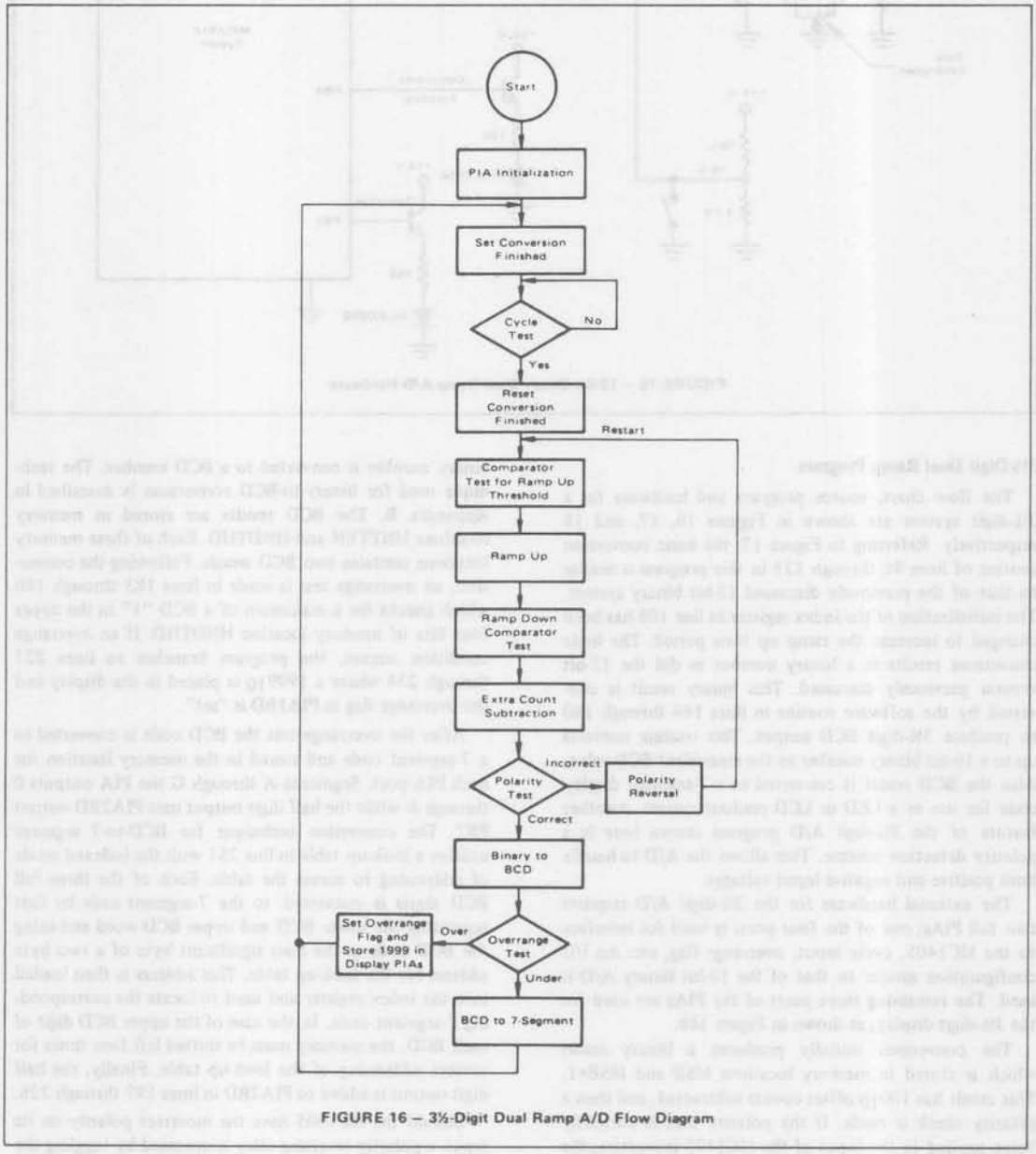

FIGURE 16 – 3½-Digit Dual Ramp A/D Flow Diagram

FIGURE 17 – 3½-Digit Dual Ramp Software (Page 1 of 5)

```
 1.000  NAM DWA25
 2.000  OPT MEM
 3.000 *
 4.000 *
 5.000 *        ************************************************
 6.000 *        *                                              *
 7.000 *        *            3 1/2 DIGIT A/D                   *
 8.000 *        *                                              *
 9.000 *        ************************************************
10.000 *
11.000 *
12.000 * THIS CONVERTER USES A MC1405 IN CONJUNCTION WITH THE
13.000 * MC6800 MPU TO PRODUCE A 3 1/2 DIGIT A/D.  THE
14.000 * DUAL RAMP METHOD OF A/D CONVERSION IS USED.
15.000 *
16.000 *   THE INPUTS TO THE MPU CONSIST OF
17.000 *
18.000 *        CYCLE SWITCH -LOCATED AT PIA1BD (PB1)
19.000 *        COMPARATOR   = LOCATED AT PIA1BD (PB7)
20.000 *
21.000 *   THE OUTPUTS FROM THE MPU CONSIST OF
22.000 *
23.000 *        RAMP CONTROL- LOCATED AT PIA1BD (PB2)
24.000 *        CONVERSION FINISHED = LOCATED AT PIA1BD (PB4)
25.000 *        OVERRANGE    - LOCATED AT PIA1BD (PB3)
26.000 *        POLARITY     - LOCATED AT PIA1BD (CA2)
27.000 *
28.000 *        7 SEGMENT OUTPUT
29.000 *          TENS   - PIA1AD
30.000 *          HUNDREDS - PIA2AD
31.000 *          THOUSANDS - PIA2BD
32.000 *          TENS OF THOUSANDS OR HALF DIGIT - PIA2BD (PB7)
33.000 *
34.000 *    THE BINARY ANSWER IS STORED AT MSB AND LSB
35.000 *
36.000 *    THE BCD ANSWER IS STORED AT UNITEN,HNDTHD,TENTSD
37.000 *
38.000 *    THE ANALOG INPUT FOR THE MC1405 MUST HAVE A 2 VOLT
39.000 *    MAXIMUM WHILE THE AUTOPOLARITY OUTPUT FROM THE MPU
40.000 *    MAY BE USED TO TOGGLE A RELAY TO PROVIDE NEGATIVE
41.000 *    INPUT CAPABILITY FOR THE A/D
42.000 *
43.000 *
44.000 *
45.000  ORG $0000
46.000 MSB RMB 1
47.000 LSB RMB 1
48.000 INDEX RMB 2
49.000 MSBTEM RMB 1              TEMP STORAGE OF BINARY ANSWER
50.000 LSBTEM RMB 1
51.000 *
52.000 *
53.000 *
54.000  ORG $0010
55.000 UNITEN RMB 1
56.000 HNDTHD RMB 1
57.000 *
58.000 *
59.000  ORG $4004
60.000 PIA1AD RMB 1          A SIDE DATA REGISTER
```

FIGURE 17 – 3½-Digit Dual Ramp Software (Page 2 of 5)

```
61.000 PIA1AC RMB 1          A SIDE CONTROL REGISTER
62.000 PIA1BD RMB 1          B SIDE DATA REGISTER
63.000 PIA1BC RMB 1          B SIDE CONTROL REGISTER
64.000 PIA2AD RMB 1          A SIDE DATA REGISTER
65.000 PIA2AC RMB 1          A SIDE CONTROL REGISTER
66.000 PIA2BD RMB 1          B SIDE DATA REGISTER
67.000 PIA2BC RMB 1          B SIDE CONTROL REGISTER
68.000 *
69.000 *
70.000  ORG $0A00
71.000 *
72.000 *                                  **PIA ASSEMBLY**
73.000  CLR PIA1AC
74.000  CLR PIA1BC
75.000  CLR PIA2AC
76.000  CLR PIA2BC
77.000  LDA A #$7C
78.000  STA A PIA1BD
79.000  LDA A #$0FF
80.000  STA A PIA1AD
81.000  STA A PIA2AD
82.000  STA A PIA2BD
83.000  LDA A #$34      SETS PIA CONTROL REGISTER BIT 3 HIGH
84.000  STA A PIA1AC
85.000  STA A PIA1BC
86.000  STA A PIA2AC
87.000  STA A PIA2BC
88.000 *
89.000  LDA A #$0C           FIRST TWO HEX DIGITS OF LOOK-UP
90.000  STA A INDEX               TABLE ADDRESSES
91.000 *                  ****************
92.000 *                  *  BASIC A/D   *
93.000 *                  ****************
94.000 *
95.000 *                                     INITIALIZATION
96.000  LDA A #$04
97.000  STA A PIA1BD   RC HIGH
98.000 START LDA A PIA1BD  COMPARATOR TEST
99.000  BMI START
100.000 CYCLE1 LDA A #$14
101.000  STA A PIA1BD   CONVERSION READY AND RC HIGH
102.000 *
103.000 *
104.000 *                                  **CYCLE TEST**
105.000 CYCLE LDA A PIA1BD
106.000  AND A #$02
107.000  BEQ CYCLE
108.000 RESTAR LDX #$07D0
109.000  CLR PIA1BD RESET OVERRANGE, CONVERSION FINISHED AND SET RC LOW
110.000 COMP LDA A PIA1BD
111.000  BPL COMP
112.000 *                                  **RAMP UP TIMING CYCLE**
113.000 RAMPUP LDA B #$04
114.000  DEX
115.000  BNE RAMPUP
116.000 *
117.000 *                                  **RAMP DOWN TIMING CYCLE**
118.000 *
119.000 *
120.000 RAMPDN STA B PIA1BD      RC HIGH
```

3

```
121.000  INX
122.000  CPX #0000           DUMMY STATEMENT FOR TIME DELAY
123.000  LDA A PIA1BD  COMPARATOR TEST
124.000  BMI RAMPDN
125.000 *
126.000  STX MSB
127.000  LDA A MSB+1
128.000  LDA B MSB
129.000  SUB A #$64
130.000  SBC B #$00
131.000  BCS POLRY1
132.000  STA A MSB+1
133.000  STA B MSB
134.000  STA A MSBTEM+1
135.000  STA B MSBTEM
136.000 *
137.000 *
138.000 *
139.000 *                  ******************
140.000 *                  * BINARY TO BCD *
141.000 *                  *   CONVERTER    *
142.000 *                  ******************
143.000 *
144.000  CLR UNTTEN
145.000  CLR HNDTHD
146.000  LDX #$0010
147.000 BEGIN LDA A UNTTEN
148.000  TAB
149.000  AND A #$0F
150.000  SUB A #$05
151.000  BMI AT
152.000  ADD B #$03
153.000 AT TBA
154.000  AND A #$0F0
155.000  SUB A #$50
156.000  BMI BT
157.000  ADD B #$30
158.000 BT STA B UNTTEN
159.000 *
160.000  LDA A HNDTHD
161.000  TAB
162.000  AND A #$0F
163.000  SUB A #$05
164.000  BMI CT
165.000  ADD B #$03
166.000 CT TBA
167.000  AND A #$0F0
168.000  SUB A #$50
169.000  BMI DT
170.000  ADD B #$30
171.000 DT STA B HNDTHD
172.000 *
173.000 *
174.000 *
175.000  ASL LSBTEM
176.000  ROL MSBTEM
177.000  ROL UNTTEN
178.000  ROL HNDTHD
179.000  DEX
180.000  BNE BEGIN
```

FIGURE 17 – 3½-Digit Dual Ramp Software (Page 3 of 5)

FIGURE 17 – 3½-Digit Dual Ramp Software (Page 4 of 5)

```
181.000 *
182.000 *                                   OVERRANGE TEST
183.000  LDA A HNDTHD
184.000  AND A #$20
185.000  SUB A #$10
186.000  BHI OVRNGE
187.000 *
188.000  BRA BCD
189.000 POLRY1 BRA POLARY   PATCH TO EXTEND RANGE OF BRANCHES
190.000 OVRNG1 BRA OVRNGE
191.000 *
192.000 *
193.000 *
194.000 *                  **********************
195.000 *                  * BCD TO 7 SEGMENT   *
196.000 *                  *   CONVERTER        *
197.000 *                  **********************
198.000 BCD LDA A UNTTEN
199.000  AND A #$0F
200.000  STA A INDEX+1
201.000  LDX INDEX
202.000  LDA A 0,X
203.000  STA A PIA1AD
204.000  LDA A UNTTEN
205.000  LSR A
206.000  LSR A
207.000  LSR A
208.000  LSR A
209.000  STA A INDEX+1
210.000  LDX INDEX
211.000  LDA A 0,X
212.000  STA A PIA2AD
213.000  LDA A HNDTHD
214.000  AND A #$0F
215.000  STA A INDEX+1
216.000  LDX INDEX
217.000  LDA A 0,X
218.000  STA A PIA2BD
219.000  LDA A HNDTHD
220.000  AND A #$10
221.000  SUB A #$10
222.000  BLT END1
223.000  LDA A #$80
224.000  ADD A PIA2BD
225.000  STA A PIA2BD
226.000 END1 JMP CYCLE1
227.000 *
228.000 OVRNGE LDA A #$1C
229.000  STA A PIA1BD
230.000  LDA A #$F3
231.000  STA A PIA1AD
232.000  STA A PIA2AD
233.000  STA A PIA2BD
234.000  JMP CYCLE
235.000 *
236.000 POLARY LDX #$0100
237.000 BR DEX
238.000  BNE BR
239.000  LDA A PIA1BC
240.000  COM A
```

```
241.000  AND A #$08
242.000  ADD A #$34
243.000  STA A PIA1BC
244.000  JMP RESTAR
245.000 *
246.000 *
247.000 *                    LOOK-UP TABLE FOR BCD TO 7 SEGMENT
248.000 *                            CONVERSION
249.000  ORG $0C00
250.000  FCB $7E,$30,$6D,$79,$33,$5B,$5F,$70,$7F,$73
251.000  END
252.000  MON
```

FIGURE 17 – 3½-Digit Dual Ramp Software (Page 5 of 5)

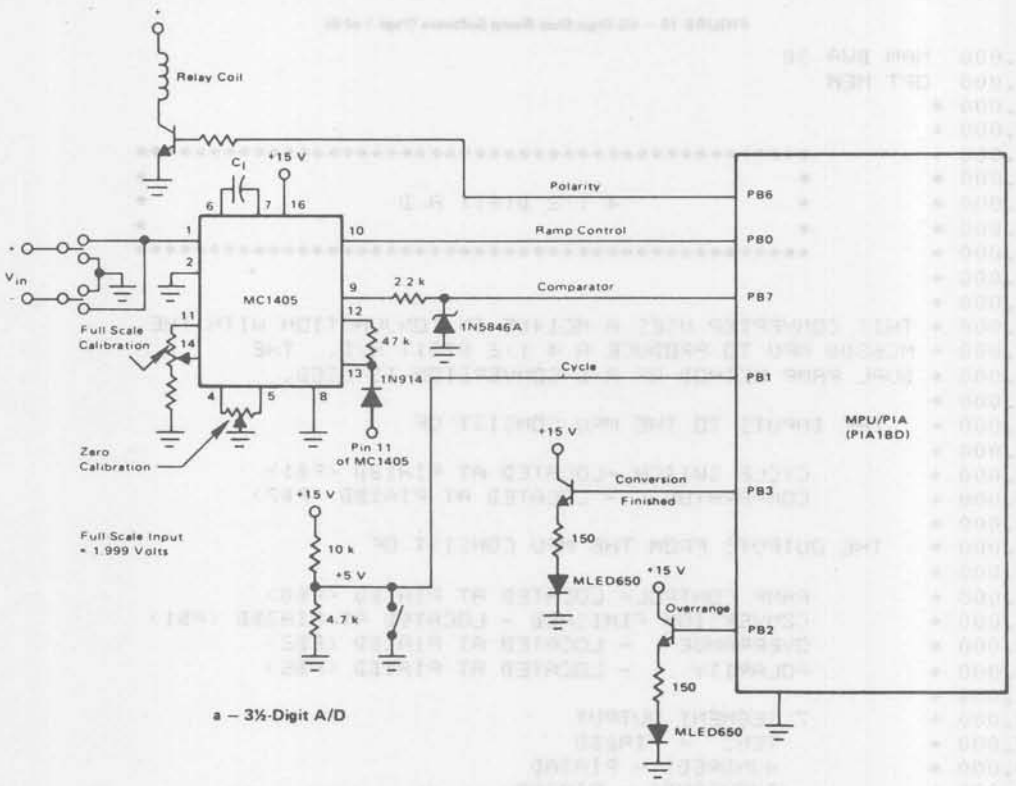

FIGURE 18 – 3½-Digit Dual Ramp A/D Hardware

4½-Digit Dual Ramp Program

The microprocessor software for a 4½-digit dual ramp A/D is shown in Figure 19. This program in an extension of the 3½-digit A/D just discussed and has a full scale input voltage of 1.9999 volts. Due to the addition of the extra digit, a fourth PIA port for the 7-segment display is required. The PIA port configuration used for ramp control, comparator, etc. is identical to that used in the 3½-digit A/D.

The addition of the extra digit also implies a longer ramp up time period which is produced by increasing the initialization of the index register in line 115. This longer ramp up time period also requires the change of the extra count subtraction statements of lines 137 and 138 to maintain the extra count subtraction of 10% ramp up time. Also, the longer ramp up time period will require a larger integration capacitor to prevent saturation of the MC1405 integrator. This is of course, assuming the same MPU clock frequency. The remainder of the A/D external hardware is unchanged except for the addition of the fourth full digital display. Figure 18a can be used for the 4½-digit A/D without modification, and Figure 18b can be used with only the addition of another digit.

The software for the binary-to-BCD converter remains the same for the 4½-digit A/D since it is capable of handling up to 16 bits. The conversion routine for BCD-to-7 segment code must be modified to handle the extra digit although the same basic technique is retained.

FIGURE 19 – 4½-Digit Dual Ramp Software (Page 1 of 5)

```
 1.000  NAM DWR 30
 2.000  OPT MEM
 3.000 *
 4.000 *
 5.000 *        ************************************************
 6.000 *        *                                              *
 7.000 *        *            4 1/2 DIGIT A/D                   *
 8.000 *        *                                              *
 9.000 *        ************************************************
10.000 *
11.000 *
12.000 * THIS CONVERTER USES A MC1405 IN CONJUNCTION WITH THE
13.000 * MC6800 MPU TO PRODUCE A 4 1/2 DIGIT A/D.  THE
14.000 * DUAL RAMP METHOD OF A/D CONVERSION IS USED.
15.000 *
16.000 *   THE INPUTS TO THE MPU CONSIST OF
17.000 *
18.000 *        CYCLE SWITCH -LOCATED AT PIA1BD (PB1)
19.000 *        COMPARATOR   - LOCATED AT PIA1BD (PB7)
20.000 *
21.000 *   THE OUTPUTS FROM THE MPU CONSIST OF
22.000 *
23.000 *        RAMP CONTROL- LOCATED AT PIA1BD (PB0)
24.000 *        CONVERSION FINISHED - LOCATED AT PIA3BD (PB1)
25.000 *        OVERRANGE   - LOCATED AT PIA1BD (PB2)
26.000 *        POLARITY    - LOCATED AT PIA1BD (PB6)
27.000 *
28.000 *        7 SEGMENT OUTPUT
29.000 *          TENS   - PIA2BD
30.000 *          HUNDREDS - PIA3AD
31.000 *          THOUSANDS - PIA3BD
32.000 *          TENS OF THOUSANDS OR HALF DIGIT -PIA3BD (PB7)
33.000 *
34.000 *    THE BINARY ANSWER IS STORED AT MSB AND LSB
35.000 *
36.000 *    THE BCD ANSWER IS STORED AT UNITTEN,HNDTHD,TENTSD
37.000 *
38.000 *    THE ANALOG INPUT FOR THE MC1405 MUST HAVE A 2 VOLT
39.000 *    MAXIMUM WHILE THE AUTOPOLARITY OUTPUT FROM THE MPU
40.000 *    MAY BE USED TO TOGGLE A RELAY TO PROVIDE NEGATIVE
41.000 *    INPUT CAPABILITY FOR THE A/D
42.000 *
43.000 *
44.000 *
45.000  ORG $0000
```

```
MSB RMB 1
LSB RMB 1
INDEX RMB 2
MSBTEM RMB 1            TEMP STORAGE OF BINARY ANSWER
LSBTEM RMB 1
*
*
*
 ORG $0010
UNTTEN RMB 1
HNDTHD RMB 1
TENTSD RMB 1
*
*
 ORG $4006
PIA1BD RMB 1          B SIDE, DATA REGISTER
PIA1BC RMB 1          B SIDE, CONTROL REGISTER
PIA2AD RMB 1          A SIDE, DATA REGISTER
PIA2AC RMB 1          A SIDE, CONTROL REGISTER
PIA2BD RMB 1          B SIDE, DATA REGISTER
PIA2BC RMB 1          B SIDE, CONTROL REGISTER
 ORG $4010
PIA3AD RMB 1          A SIDE, DATA REGISTER
PIA3AC RMB 1          A SIDE, CONTROL REGISTER
PIA3BD RMB 1          B SIDE, DATA REGISTER
PIA3BC RMB 1          B SIDE, CONTROL REGISTER
*
*
*
*                                   PIA ASSEMBLY
 ORG $0A00
 CLR PIA1BC
 CLR PIA2AC
 CLR PIA2BC
 CLR PIA3AC
 CLR PIA3BC
 LDA A #$4D
 STA A PIA1BD
 LDA A #$0FF     REMAINING PIA'S ALL OUTPUTS
 STA A PIA2AD
 STA A PIA2BD
 STA A PIA3AD
 STA A PIA3BD
 LDA A #$34       SETS PIA CONTROL REGISTER BIT 3 HIGH
 STA A PIA1BC
 STA A PIA2AC
 STA A PIA2BC
 STA A PIA3AC
 STA A PIA3BC
*
 LDA A #$0C          FIRST TWO HEX DIGITS OF LOOK-UP
 STA A INDEX                 TABLE ADDRESSES
*                   ****************
*                   *   BASIC A/D  *
*                   ****************
*
*                                  INITIALIZATION
 LDA A #$04
 STA A PIA1BD   PC HIGH
START LDA A PIA1BD  COMPARATOR TEST
```

FIGURE 19 – 4½-Digit Dual Ramp Software (Page 2 of 5)

FIGURE 19 – 4½-Digit Dual Ramp Software (Page 3 of 5)

```
106.000  BMI START
107.000 CYCLE1 LDA A #14
108.000  STA A PIA1BD   CONVERSION READY AND RC HIGH
109.000 *
110.000 *
111.000 *                                      CYCLE TEST
112.000 CYCLE LDA A PIA1BD
113.000  AND A #$02
114.000  BEQ CYCLE
115.000 RESTART LDX #$4E20          INITIALIZATION FOR RAMP UP
116.000 *                              TIMING
117.000  CLR PIA1BD RESET OVERRANGE, CONVERSION FINISHED AND SET RC LOW
118.000 COMP LDA A PIA1BD          COMPARATOR TEST
119.000  BPL COMP
120.000 *                                  RAMP UP TIMING CYCLE
121.000 RAMPUP LDA B #$04
122.000  DEX
123.000  BNE RAMPUP
124.000 *
125.000 *                              RAMP DOWN TIMING CYCLE
126.000 *
127.000 *
128.000 RAMPDN STA B PIA1BD      RC HIGH
129.000  INX
130.000  CPX #0000   DUMMY STATEMENT
131.000  LDA A PIA1BD  COMPARATOR TEST
132.000  BMI RAMPDN
133.000 *
134.000 *                              EXTRA COUNT SUBTRACTION
135.000  STX MSB
136.000  STX MSBTEM
137.000  LDA A MSB
138.000  SUB A #$04         EXTRA COUNT SUBTRACTION
139.000  BMI POLRY1         POLARITY TEST
140.000  STA A MSB
141.000  STA A MSBTEM
142.000 *
143.000 *
144.000 *
145.000 *                  ********************
146.000 *                  * BINARY TO BCD *
147.000 *                  *   CONVERTER    *
148.000 *                  ********************
149.000 *
150.000  CLR UNTTEN
151.000  CLR HNDTHD
152.000  CLR TENTSD
153.000  LDX #$0010
154.000 BEGIN LDA A UNTTEN
155.000  TAB
156.000  AND A #$0F
157.000  SUB A #$05
158.000  BMI AT
159.000  ADD B #$03
160.000 AT TBA
161.000  AND A #$0F0
162.000  SUB A #$50
163.000  BMI BT
164.000  ADD B #$30
165.000 BT STA B UNTTEN
```

```
166.000 *
167.000  LDA A HNDTHD
168.000  TAB
169.000  AND A #$0F
170.000  SUB A #$05
171.000  BMI CT
172.000  ADD B #$03
173.000 CT TBA
174.000  AND A #$0F0
175.000  SUB A #$50
176.000  BMI DT
177.000  ADD B #$30
178.000 DT STA B HNDTHD
179.000 *
180.000  LDA A TENTSD
181.000  TAB
182.000  SUB A #$05
183.000  BMI ET
184.000  ADD B #$03
185.000 ET STA B TENTSD
186.000 *
187.000 *
188.000  ASL LSBTEM
189.000  ROL MSBTEM
190.000  ROL UNTTEN
191.000  ROL HNDTHD
192.000  ROL TENTSD
193.000  DEX
194.000  BNE BEGIN
195.000 *
196.000  BRA BCD
197.000 OVRNG1 BRA OVRNGE
198.000  BRA BCD
199.000 *
200.000 POLRY1 BRA POLARY      BRANCH PATCH
201.000 *                   ********************
202.000 *                   * BCD TO 7 SEGMENT *
203.000 *                   *   CONVERTER      *
204.000 *                   ********************
205.000 BCD LDA A UNTTEN
206.000  AND A #$0F
207.000  STA A INDEX+1
208.000  LDX INDEX
209.000  LDA A 0,X
210.000  STA A PIA2AD
211.000  LDA A UNTTEN
212.000  LSR A
213.000  LSR A
214.000  LSR A
215.000  LSR A
216.000  STA A INDEX+1
217.000  LDX INDEX
218.000  LDA A 0,X
219.000  STA A PIA2BD
220.000  LDA A HNDTHD
221.000  AND A #$0F
222.000  STA A INDEX+1
223.000  LDX INDEX
224.000  LDA A 0,X
225.000  STA A PIA2AD
```

FIGURE 19 – 4½-Digit Dual Ramp Software (Page 4 of 5)

```
226.000  LDA A HNDTHD
227.000  LSR A
228.000  LSR A
229.000  LSR A
230.000  LSR A
231.000  STA A INDEX+1
232.000  LDX INDEX
233.000  LDA A 0,X
234.000  STA A PIA3BD
235.000  LDA A TENTSD
236.000  SUB A #$01
237.000  BLT END
238.000  LDA A #$80
239.000  ADD A PIA3BD
240.000  STA A PIA3BD
241.000 END JMP CYCLE1
242.000 *
243.000 OVRNGE LDA A #$0D ; OVERRANGE,RC HIGH, CON F
244.000  STA A PIA1BD
245.000  LDA A #$F3
246.000  STA A PIA2AD
247.000  STA A PIA2BD
248.000  STA A PIA3AD
249.000  STA A PIA3BD
250.000  JMP CYCLE
251.000 *
252.000 *
253.000 POLARY LDX #$0100
254.000 BR DEX
255.000  BNE BR
256.000  LDA A PIA1BC
257.000  COM A
258.000  AND A #$08
259.000  ADD A #$34
260.000  STA A PIA1BC
261.000  JMP RESTAR
262.000 *
263.000 *
264.000 *
265.000  ORG $0C00
266.000  FCB $7E,$30,$6D,$79,$33,$5B,$5F,$70,$7F,$73
267.000  END
268.000  MON
```

3

FIGURE 19 – 4½-Digit Dual Ramp Software (Page 5 of 5)

SUMMARY

Many MPU systems require analog information, which necessitates the use of an A/D converter in the microprocessor design. This note has presented two popular A/D techniques used in conjunction with the M6800 microprocessor system. These techniques, successive approximation and dual ramp, were shown using the MPU as the digital control element for the A/D system. This required dedication of the MPU to the A/D function during the conversion. Also shown were systems using the MPU to control the flow of data from an external A/D allowing the MPU to perform other tasks during the conversion.

The variety of programs presented allow the designer to make a selection based upon hardware cost, conversion speed, memory locations and interrupt capability. Although the A/D programs shown here are complete designs, they are general designs and may be tailored to fit each individual application. Also a variety of digital outputs are available including binary, BCD, and 7-segment. In conjunction with the BCD output a 16-bit binary to BCD conversion routine is presented in Appendix B.

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APPENDIX A
MPU INSTRUCTIONS

Accumulator and Memory Instructions

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	●	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	●	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	●	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	●	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	●	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	●	●	↕	↕	R	●
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	●	●	↕	↕	R	●
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	●	●	↕	↕	R	●
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	●	●	↕	↕	R	●
Clear	CLR							6F	7	2	7F	6	3				00 → M	●	●	R	S	R	R
	CLRA													4F	2	1	00 → A	●	●	R	S	R	R
	CLRB													5F	2	1	00 → B	●	●	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A − M	●	●	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B − M	●	●	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A − B	●	●	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				M̄ → M	●	●	↕	↕	R	S
	COMA													43	2	1	Ā → A	●	●	↕	↕	R	S
	COMB													53	2	1	B̄ → B	●	●	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 − M → M	●	●	↕	↕	①	②
	NEGA													40	2	1	00 − A → A	●	●	↕	↕	①	②
	NEGB													50	2	1	00 − B → B	●	●	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	●	●	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M − 1 → M	●	●	↕	↕	4	●
	DECA													4A	2	1	A − 1 → A	●	●	↕	↕	4	●
	DECB													5A	2	1	B − 1 → B	●	●	↕	↕	4	●
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	●	●	↕	↕	R	●
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	●	●	↕	↕	R	●
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	●	●	↕	↕	Ⓢ	●
	INCA													4C	2	1	A + 1 → A	●	●	↕	↕	Ⓢ	●
	INCB													5C	2	1	B + 1 → B	●	●	↕	↕	Ⓢ	●
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	●	●	↕	↕	R	●
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	●	●	↕	↕	R	●
Or Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	●	●	↕	↕	R	●
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	●	●	↕	↕	R	●
Push Data	PSHA													36	4	1	A → M_{SP}, SP − 1 → SP	○	●	●	●	●	●
	PSHB													37	4	1	B → M_{SP}, SP − 1 → SP	●	●	●	●	●	●
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	●	●	●	●	●	●
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	●	●	●	●	●	●
Rotate Left	ROL							69	7	2	79	6	3				M	●	●	↕	↕	Ⓢ	↕
	ROLA													49	2	1	A	●	●	↕	↕	Ⓢ	↕
	ROLB													59	2	1	B — C b7 b0	●	●	↕	↕	Ⓢ	↕
Rotate Right	ROR							66	7	2	76	6	3				M	●	●	↕	↕	Ⓢ	↕
	RORA													46	2	1	A	●	●	↕	↕	Ⓢ	↕
	RORB													56	2	1	B — C b7 b0	●	●	↕	↕	Ⓢ	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	●	●	↕	↕	Ⓢ	↕
	ASLA													48	2	1	A — C b7 b0 — 0	●	●	↕	↕	Ⓢ	↕
	ASLB													58	2	1	B	●	●	↕	↕	Ⓢ	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	●	●	↕	↕	Ⓢ	↕
	ASRA													47	2	1	A	●	●	↕	↕	Ⓢ	↕
	ASRB													57	2	1	B — b7 b0 C	●	●	↕	↕	Ⓢ	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	●	●	R	↕	Ⓢ	↕
	LSRA													44	2	1	A — 0 b7 b0 C	●	●	R	↕	Ⓢ	↕
	LSRB													54	2	1	B	●	●	R	↕	Ⓢ	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	●	●	↕	↕	R	●
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	●	●	↕	↕	R	●
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A − M → A	●	●	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B − M → B	●	●	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A − B → A	●	●	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A − M − C → A	●	●	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B − M − C → B	●	●	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	●	●	↕	↕	R	●
	TBA													17	2	1	B → A	●	●	↕	↕	R	●
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M − 00	●	●	↕	↕	R	R
	TSTA													4D	2	1	A − 00	●	●	↕	↕	R	R
	TSTB													5D	2	1	B − 00	●	●	↕	↕	R	R
																		H	I	N	Z	V	C

LEGEND:

- OP Operation Code (Hexadecimal);
- ~ Number of MPU Cycles;
- # Number of Program Bytes;
- + Arithmetic Plus;
- − Arithmetic Minus;
- · Boolean AND;
- M_{SP} Contents of memory location pointed to be Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- M̄ Complement of M;
- → Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ↕ Test and set if true, cleared otherwise
- ● Not Affected

Index Register and Stack Manipulation Instructions

POINTER OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN/ARITHMETIC OPERATION	5 H	4 I	3 N	2 Z	1 V	0 C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑦	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

Jump and Branch Instructions

OPERATIONS	MNEMONIC	RELATIVE OP	RELATIVE ~	RELATIVE #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BRANCH TEST	5 H	4 I	3 N	2 Z	1 V	0 C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										N ⊕ V = 0	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										Z + (N ⊕ V) = 0	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										Z + (N ⊕ V) = 1	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										N ⊕ V = 1	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										02	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		⑩					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt	WAI										3E	9	1		•	⑪	•	•	•	•

Condition Code Register Manipulation Instructions

OPERATIONS	MNEMONIC	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN OPERATION	5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0 → C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0 → I	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0 → V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1 → C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1 → I	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1 → V	•	•	•	•	S	•
Acmltr A → CCR	TAP	06	2	1	A → CCR	⑫					
CCR → Acmltr A	TPA	07	2	1	CCR → A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES:

(Bit set if test is true and cleared otherwise)

1 (Bit V) Test: Result = 10000000?
2 (Bit C) Test: Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non Maskable Interrupt is required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

APPENDIX B

BINARY-TO-BCD CONVERSION

A standard technique for binary-to-BCD conversion is that of the Add 3 algorithm. Figures B1 and B2 show a flow diagram and example of this algorithm. The technique requires a register containing the N-bit binary number and enough 4-bit BCD registers to contain the maximum equivalent BCD number for the initial binary number. The conversion starts by checking each BCD register for a value of 5 or greater. If this condition exists in one or all of these registers (initially this condition cannot exist), then a 3 is added to those registers where this condition exists. Next the registers are shifted left with the carry out of the previous register being the carry in to the next register. Again each BCD register is checked for values of 5 or greater. This sequence continues until the registers have been shifted N times, where N is the number of bits in the initial binary word. The BCD registers then contain the resulting BCD equivalent to the initial binary word. The example in Figure B2 starts with an 8-bit binary word consisting of all "1's." This word is converted to the BCD equivalent of 255 by this technique. After 8 shifts the last binary bit has been shifted out of the binary register and the hundreds, tens, and units registers contain a 255.

Figure B3 shows an MC6800 software routine for performing this technique of binary to BCD conversion. The initial binary number is a 16-bit number and occupies memory locations MSB and LSB; this binary number is converted to the equivalent BCD number in memory locations TENTSD, HNDTHD and UNTTEN. Each of these memory locations contains two BCD digits. Eighty-three memory locations are required for program storage with a maximum conversion taking 1.8 ms.

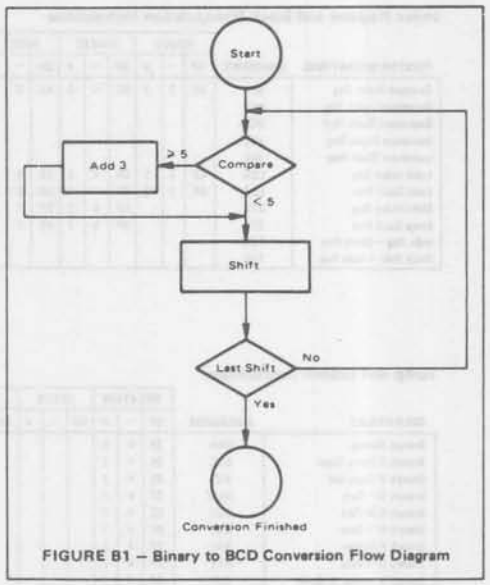

FIGURE B1 – Binary to BCD Conversion Flow Diagram

Hundreds	Tens	Units	8-Bit Binary	
			1 1 1 1 1 1 1 1	
		1	1 1 1 1 1 1 1	Shift
		1 1	1 1 1 1 1 1	Shift
		1 1 1	1 1 1 1 1	Shift
		1 0 1 0	1 1 1 1	Add 3 to Units
	1	0 1 0 1	1 1 1 1	Shift
	1	1 0 0 0	1 1 1 1	Add 3 to Units
	1 1	0 0 0 1	1 1 1	Shift
	1 1 0	0 0 0 1 1	1 1	Shift
	1 0 0 1	0 0 0 1 1	1 1	Add 3 to Tens
1	0 0 1 0	0 0 1 1 1	1	Shift
1	0 0 1 0	1 0 1 0 1	1	Add 3 to Units
1 0	0 1 0 1	0 1 0 1		Shift
2	5	5		Total Shifts 8

FIGURE B2 – Binary to BCD Conversion

FIGURE B3 – Binary-to-BCD Conversion Software (Page 1 of 2)

```
1.000  NAM DWA21
2.000  OPT MEM
3.000  *
4.000  ************************************************************
5.000  *                                                          *
6.000  *              BINARY TO BCD CONVERSION                    *
7.000  *                 ADD 3 ALGORITHM                          *
8.000  *                    16 BIT                                *
9.000  ************************************************************
10.000 *
11.000  ORG 0              INITIAL BINARY NUMBER
12.000 MSB RMB 1             MOST SIGNIFICANT 8 BITS
13.000 LSB RMB 1             LEAST SIGNIFICANT 8 BITS
14.000 *
15.000 *
16.000 *
17.000  ORG $0010          BCD RESULTS
18.000 UNTTEN RMB 1          UNITS AND TENS DIGITS
19.000 HNDTHD RMB 1          HUNDREDS AND THOUSANDS
20.000 TENTSD RMB 1          TENS OF THOUSANDS DIGIT
21.000 *
22.000 *
23.000 *
```

```
24.000  ORG $0F00       **BEGINNING OF PROGRAM**
25.000  CLR UNTTEN
26.000  CLR HNDTHD
27.000  CLR TENTSD
28.000  LDX #$0010
29.000 BEGIN LDA A UNTTEN      UNITS COMPARISON
30.000  TAB
31.000  AND A #$0F
32.000  SUB A #$05
33.000  BMI AT
34.000  ADD B #$03
35.000 AT TBA                  TENS COMPARISON
36.000  AND A #$0F0
37.000  SUB A #$50
38.000  BMI BT
39.000  ADD B #$30
40.000 BT STA B UNTTEN
41.000 *
42.000  LDA A HNDTHD           HUNDREDS COMPARISON
43.000  TAB
44.000  AND A #$0F
45.000  SUB A #$05
46.000  BMI CT
47.000  ADD B #$03
48.000 CT TBA
49.000  AND A #$0F0
50.000  SUB A #$50
51.000  BMI DT
52.000  ADD B #$30
53.000 DT STA B HNDTHD
54.000 *
55.000  LDA A TENTSD          TENS OF THOUSANDS COMPARISON
56.000  TAB
57.000  SUB A #$05
58.000  BMI ET
59.000  ADD B #$03
60.000 ET STA B TENTSD
61.000 *
62.000 *
63.000  ASL LSB
64.000  ROL MSB
65.000  ROL UNTTEN
66.000  ROL HNDTHD
67.000  ROL TENTSD
68.000  DEX
69.000  BNE BEGIN              END OF CONVERSION CHECK
70.000 *
71.000 *
72.000 *
73.000 *
74.000  END
75.000  MON
```

FIGURE B3 – Binary-to-BCD Conversion Software (Page 2 of 2)

AUTORANGING DIGITAL MULTIMETER USING THE MC14433 CMOS A/D CONVERTER

This application note describes an autorange digital multimeter using the MC14433. The multimeter includes ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A full scale, and resistance ranges from 2 kΩ to 2 MΩ full scale.

AUTORANGING DIGITAL MULTIMETER USING THE MC14433 CMOS A/D CONVERTER

This article describes an autorange digital multimeter using the MC14433. The multimeter includes ac and dc voltage ranges from 200 mV to 200 V, ac and dc current from 2 mA to 2 A full scale, and resistance ranges from 2 kΩ to 2 MΩ full scale. The MC14433 DVM chip used provides a 3-1/2-digit A/D converter with autopolarity, autozero and a high input impedance. The chip has overrange and underrange information available to simplify the design of the autoranging meter. Only two input jacks are required for all ranges and functions, eliminating the need for changing leads on the instrument when changing ranges or functions. Although only four ranges are provided for each function, the technique used may be expanded to more ranges if desired.

Range switching is done with the use of mechanical relays. The relays may be replaced with solid-state analog switches; however it was felt that the mechanical relays would provide a higher degree of reliability due to the high voltage and currents being measured with the multimeter.

MC14433 A/D CONVERTER

The MC14433 is a single-chip 3-1/2-digit A/D converter using a modified dual ramp technique of A/D conversion. Housed in a 24-pin package, it features autopolarity, autozero and a high input impedance. Figure 1 shows the pin diagram of the MC14433.

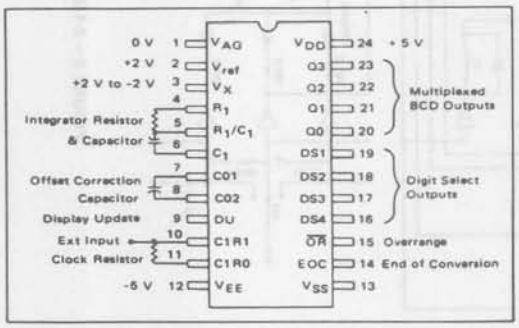

FIGURE 1 – MC14433 Pin Assignment

The output of the MC14433 is 3-1/2-digit multiplexed BCD with the MSD containing not only the half digit but also the polarity of the input, overrange and underrange information. Figure 2 shows the decoding for the MSD. The digit selects for the multiplexed BCD have interdigit blanking to ensure correct BCD data during the time that the digit select is true.

The converter is ratiometric and requires an external

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding	
+0	1	1	1	0	Blank	
–0	1	0	1	0	Blank	
+0 UR	1	1	1	1	Blank	
–0 UR	1	0	1	1	Blank	
+1	0	1	0	0	4 → 1	Hook up
–1	0	0	0	0	0 → 1	only seg b
+1 OR	0	1	1	1	7 → 1	and c to
–1 OR	0	0	1	1	3 → 1	MSD

Notes for Truth Table
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

FIGURE 2 – MSD Coding

reference voltage. This voltage is 2.000 volts for the 1.999 volt range and 200 mV for the 199.9 mV full scale input. Both the unknown and reference inputs and analog ground are high-impedance inputs. External components required are two resistors and two capacitors.

The MC14433 has an End of Conversion (EOC) pin for indicating the end of one conversion and the start of the next conversion by a positive pulse 1/2 clock period long. The device also contains a display update pin which allows the data to be strobed into the output latches. If at least one positive edge is received prior to the ramp down cycle, new data is strobed to the display. Normally this pin is tied to EOC to allow a data update each conversion cycle.

The MC14433 requires two power supplies. The total voltage must not exceed 18 volts. Pin 13 is the reference level for the output of the MC14433. If this pin is tied to 0 volts, the BCD output, digit selects and EOC will swing from 0 volts to V_{DD}. If, however, pin 13 is tied to V_{EE}, the output swing will be from V_{EE} to V_{DD}.

The clock for the MC14433 is internal to the chip, requiring only a single external resistor to set the frequency. An external clock may be used by driving pin 10. The total conversion time for the MC14433 is approximately 16400 clock periods. This conversion time includes the autozero cycle and the unknown input measurement cycle.

AUTORANGING CIRCUITRY

Figure 3 shows the autoranging DMM. The heart of the autoranging circuitry is an MC14035B CMOS shift

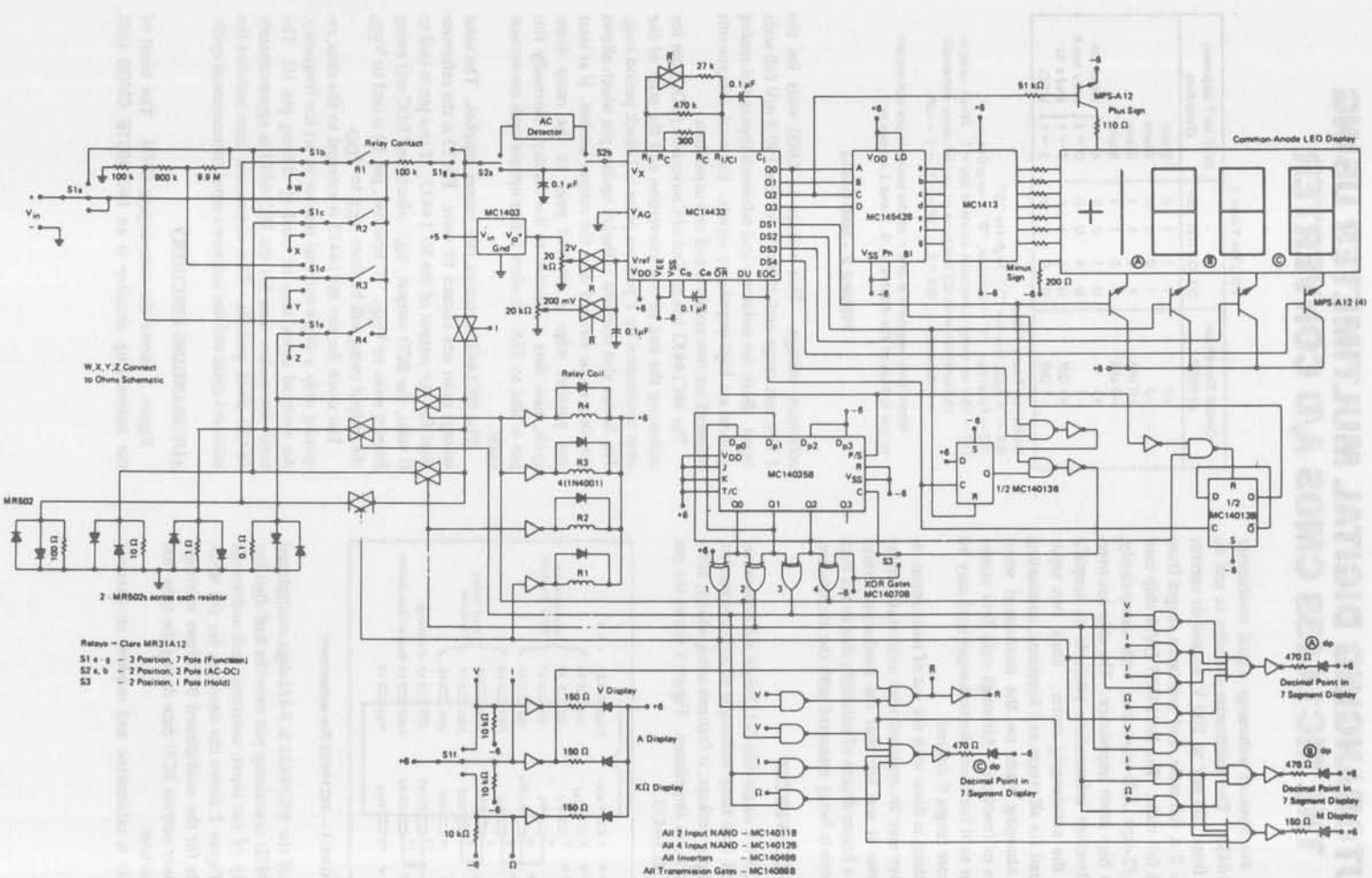

FIGURE 3 – 3-1/2-Digit Autoranging Multimeter

register which can be configured to shift either right or left. The direction of the shift is dependent upon whether an overrange or underrange signal is received at the end of each conversion. If the meter is in range, no shift signal is received. For an overrange condition, a high level is clocked to the right, and for an underrange condition the high level is clocked to the left (see Figure 4). The Exclusive OR gates decode the shift register output to produce only one output high. This output is used to turn on the corresponding range relays.

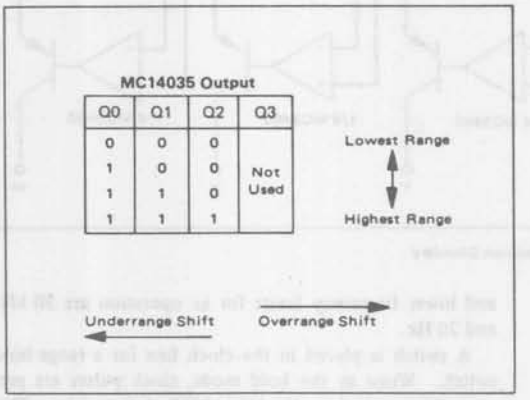

FIGURE 4 – Shift Register Operation for Autoranging DMM

If at the end of the next conversion the MC14433 is still either overrange or underrange, the shift register receives another clock pulse and thus the next range is selected. When an extreme overrange or underrange condition occurs the register is filled with all "ones" or all "zeros" which selects continuously either the highest or lowest range. Input voltages that exceed 200 volts as well as complete overrange conditions for the other functions cause the display to blink on and off. This feature is provided by the second half of the MC14013 flip-flop. The blinking rate is at half the conversion rate.

Figure 5 describes the functional operation for each range and function for the multimeter. The 2-volt reference is used for the ohms function, which means that 2 volts are developed across the unknown resistors at full scale. All current ranges use the 200-mV reference, while for voltage both the 200-mV and the 2-volt reference are used.

MC14066B transmission gates are used to switch between the 2-volt reference and the 200-mV reference. A transmission gate is also used to reduce the integrator resistor for the 200-mV range. In the current mode, transmission gates are used to switch the input of the MC14433 to the appropriate current-measuring resistor. This is necessary to eliminate the problem of measuring the voltage across the contact resistance of the function switch and relays in addition to the voltage across the current resistor. MR501 rectifiers are placed across the current resistors to limit the power dissipation during overrange conditions.

A ±6-volt power supply is used for the multimeter, with the logic sections referenced to the -6-volt level. This power supply is shown in Figure 6 and uses the MC7806 and MC7906 three-terminal regulators.

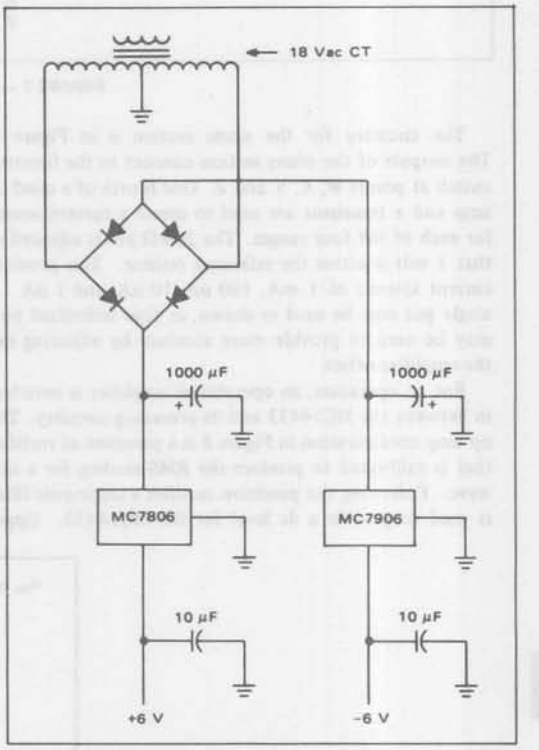

FIGURE 6 – ±6-Volt Power Supply

Relay	Voltage					Current					Resistance				
	Range	dp	Ref Used	Function Display	Resistor Divider	Range	dp	Ref Used	Function Display	Measurement Resistor	Range	dp	Ref Used	Function Display	Current Source
R1	200 mV	199.9	200 mV	mV	1:1	2 mA	1.999	200 mV	mA	100 Ω	2 kΩ	1.999	2 V	kΩ	1 mA
R2	2 V	1.999	2 V	V	1:1	20 mA	19.99	200 mV	mA	10 Ω	20 kΩ	19.99	2 V	kΩ	100 µA
R3	20 V	19.99	2 V	V	10:1	200 mA	199.9	200 mV	mA	1 Ω	200 kΩ	199.9	2 V	kΩ	10 µA
R4	200 V	199.9	2 V	V	100:1	2 A	1.999	200 mV	A	0.1 Ω	2000 kΩ	1999	2 V	kΩ	1 µA

FIGURE 5 – Functional Operation

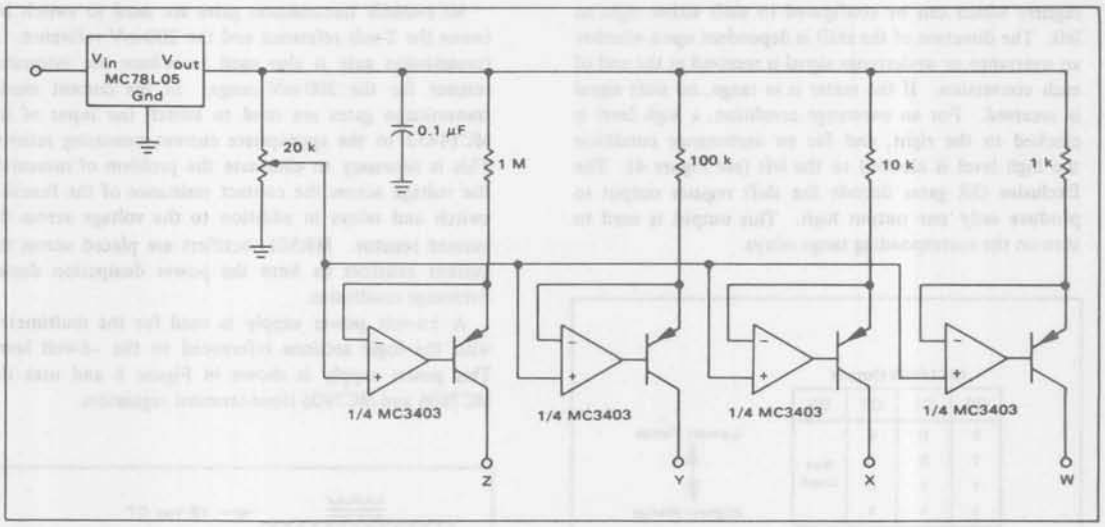

FIGURE 7 – Ohms Section Circuitry

The circuitry for the ohms section is in Figure 7. The outputs of the ohms section connect to the function switch at points W, X, Y and Z. One-fourth of a quad op amp and a transistor are used to create a current source for each of the four ranges. The 20-kΩ pot is adjusted so that 1 volt is across the reference resistor. This provides current sources of 1 mA, 100 μA, 10 μA, and 1 μA. A single pot may be used as shown, or four individual pots may be used to provide more accuracy by adjusting out the amplifier offset.

For ac operation, an operational amplifier is switched in between the MC14433 and its preceding circuitry. The op amp configuration in Figure 8 is a precision ac rectifier that is calibrated to produce the RMS reading for a sine wave. Following the precision rectifier a single-pole filter is used to provide a dc level for the MC14433. Upper and lower frequency limits for ac operation are 30 kHz and 20 Hz.

A switch is placed in the clock line for a range hold switch. When in the hold mode, clock pulses are prevented from clocking the MC14035B shift register. This feature allows several measurements to be made on a high range without the multimeter switching back to the low range between measurements.

The meter must not only be protected from destroying itself during overrange conditions but must also continue to make proper overrange measurements so that the next range may be selected. The analog input to the MC14433 is internally diode protected. The multimeter has a 100-kΩ resistor in series with this input to limit the current during overvoltage measurements.

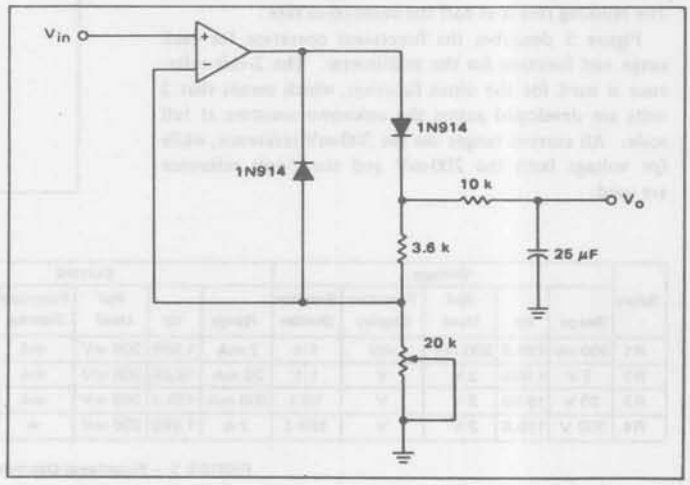

FIGURE 8 – AC Circuitry

DATA ACQUISITION NETWORKS WITH NMOS AND CMOS

This article describes an eight-channel data acquisition network (DAN) using the Motorola MC14433 CMOS A/D converter and the M6800 microprocessor family. The A/D conversion technique used with the MC14433 is a modified dual ramp featuring auto-zero, auto-polarity, and high input impedance. Both hardware and M6800 software are shown for the DAN.

DATA ACQUISITION NETWORKS WITH NMOS AND CMOS

LSI technology is making it easier and less expensive to design and build complex electronic systems. This fact holds true for Data Acquisition Networks (DANs) due to the new single chip A/Ds and microprocessor systems. Thus, it is now feasible to build your own data acquisition network instead of buying a completed system, and thereby save money.

This article discusses an eight-channel DAN using the Motorola MC14433 CMOS A/D converter and the M6800 microprocessor. The number of channels can be expanded or reduced very simply. In addition to the eight channel DAN the program for a single channel system is shown. The inputs to the system, positive or negative polarity, are multiplexed with a CMOS analog multiplexer.

MC14433 A/D CONVERTER

The MC14433 is a single chip 3½ digit A/D converter using a modified dual ramp technique of A/D conversion. Housed in a 24 pin package it features auto-polarity, auto-zero and a high input impedance. Figure 1 shows the pin diagram of the MC14433.

The output of the MC14433 is 3½ digit multiplexed BCD with the MSD containing not only the half digit but also polarity of the input, overrange and underrange information. Figure 2 describes the decoding for the MSD. The digit selects for the multiplexed BCD have interdigit blanking to ensure correct BCD data during the time that the digit select is true.

The A/D converter is ratiometric and requires an external reference voltage. This reference voltage is 2.000 volts for the 1.999 volt range and 200 mV for a 199.9 mV full scale input. Both the unknown and reference inputs and analog ground are high impedance inputs. Other external components required are clock resistor, integrator resistor and capacitor, and offset capacitor. Precision components are not required.

Of particular interest for the data acquisition systems are the display update (DU) and the end of conversion (EOC) pins. The EOC pin indicates the end of one conversion cycle and the start of the next conversion by a positive pulse one-half clock period long. The display update pin is an input to the chip which allows the data to be strobed into the output latches. If at least one positive edge is received prior to the ramp down cycle, new data is strobed to the display. In a stand alone A/D system, EOC is connected to DU.

Also of significance to the data acquisition network is the input polarity detection sequence for the MC14433. Polarity for the current conversion cycle is determined in the previous conversion cycle. Thus if the polarity is reversed, a second conversion cycle must be made in order to obtain a correct measurement.

The MC14433 requires two power supplies. The total voltage across the device must not exceed 18 volts. Pin 13 is the reference level for the output circuitry of the MC14433. If this pin is tied to 0 volts, the BCD output, digit select and EOC will swing from 0 volts to V_{DD}. If however, pin 13 is tied to V_{EE}, the output swing will be from V_{EE} to V_{DD}.

The clock for the MC14433 is internal to the chip, requiring only a single external resistor to set the frequency. An external clock may be used by driving pin 10.

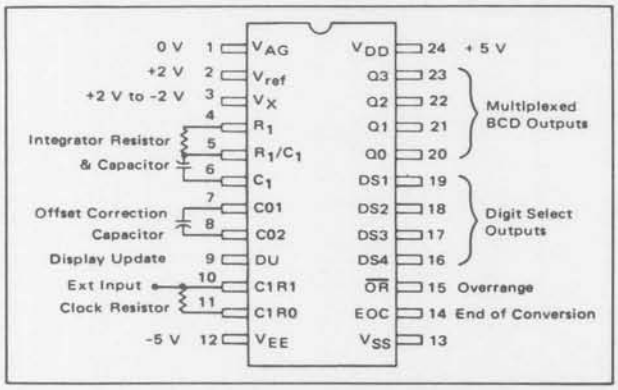

FIGURE 1 – MC14433 Pin Assignment

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding
+0	1	1	1	0	Blank
−0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
−0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 } Hook up
−1	0	0	0	0	0 → 1 } only seg b
+1 OR	0	1	1	1	7 → 1 } and c to
−1 OR	0	0	1	1	3 → 1 } MSD

Notes for Truth Table
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

FIGURE 2 – MSD Coding

The total conversion time for the MC14433 is approximately 16400 clock periods. This conversion time includes the auto-zero cycle and the unknown input measurement cycle. The clock frequency may be operated up to about 400 kHz producing a conversion time of 40 ms.

MPU

The Motorola microprocessor system devices used are the MC6800 MPU, MCM6810 RAM, MCM6830 ROM and MC6820 PIA (peripheral interface adapter). The following is a brief description of the basic MPU system as it pertains to the A/D systems presented later in this application note.

The Motorola MPU system uses a 16-bit address bus and an 8-bit data bus. The 16-bit address bus provides 65,536 possible memory locations which may be either storage devices (RAM, ROM, etc.) or interface devices (PIA, etc.). The basic MPU contains two 8-bit accumulators, one 16-bit index register, a 16-bit program counter, a 16-bit stack pointer, and an 8-bit condition code register. The condition code register indicates carry, half carry, interrupt, zero, minus, and 2's complement overflow. Figure 3 shows a functional block of the MC6800 MPU.

The MPU uses 72 instructions with six addressing modes which provide 197 different operations in the MPU. A summary of each instruction and function with the appropriate addressing mode is shown in the MC6800 data sheet.

The RAMs used in the system are static and contain 128 8-bit words for scratch pad memory while the ROM is mask programmable and contains 1024 8-bit words. The ROM and RAM, along with the remainder of the MPU system components, operate from a single +5 volt power supply; the address bus, data bus and PIAs are TTL compatible.

The MPU system requires a 2ϕ non-overlapping clock such as the MC6875* with a lower frequency limit of 100 kHz and an upper limit of 1 MHz.

*MC6875 to be introduced second quarter 1977

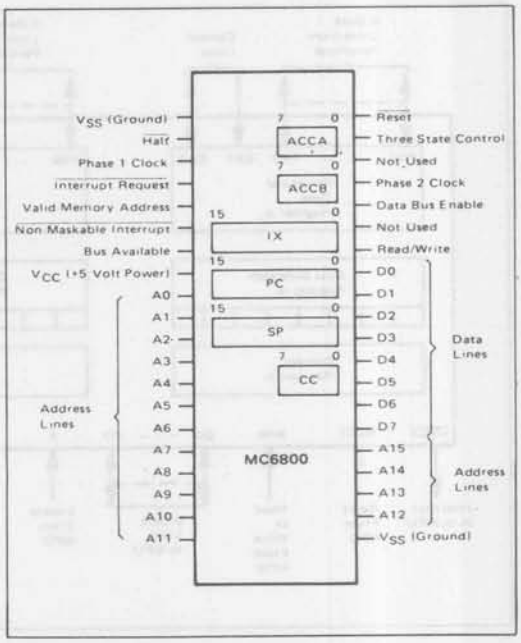

FIGURE 3 – MPU Pin Functions

The PIA is the interface device used between the address and data buses and the analog sections of the A/D. Each PIA contains two essentially identical 8-bit interface ports. These ports (A side, B side) each contain three internal registers that include the data register which is the interface from the data bus to the A/D, the data direction register which programs each of the eight lines of the data register as either an input or an output, and the control register which, in addition to other functions, switches the data bus between the data register and the data direction register. Each port to the PIA contains two addition pins, CA1 and CA2, for interrupt capability and extra I/O lines. The functions of these lines are programmable with the remaining bits of the control register. Figure 4 shows a functional block of the MC6820 PIA.

Each PIA requires four address locations in memory. Two addresses access either of the two (A or B sides) data/data direction registers while the remaining two addresses access either of the two control registers. These addresses are decoded by the chip select and register select lines of the PIA which are connected to the MPU address bus. Selection between the data register and data direction register is made by programming a "1" or "0" in the third least significant bit of each control register. A logic "0" accesses the data direction register while a logic "1" accesses the data register.

By programming "0"s in the data direction register each corresponding line performs as an input, while "1"s in the data direction register make corresponding lines act as outputs. The eight lines may be intermixed between inputs and outputs by programming different combinations of

3

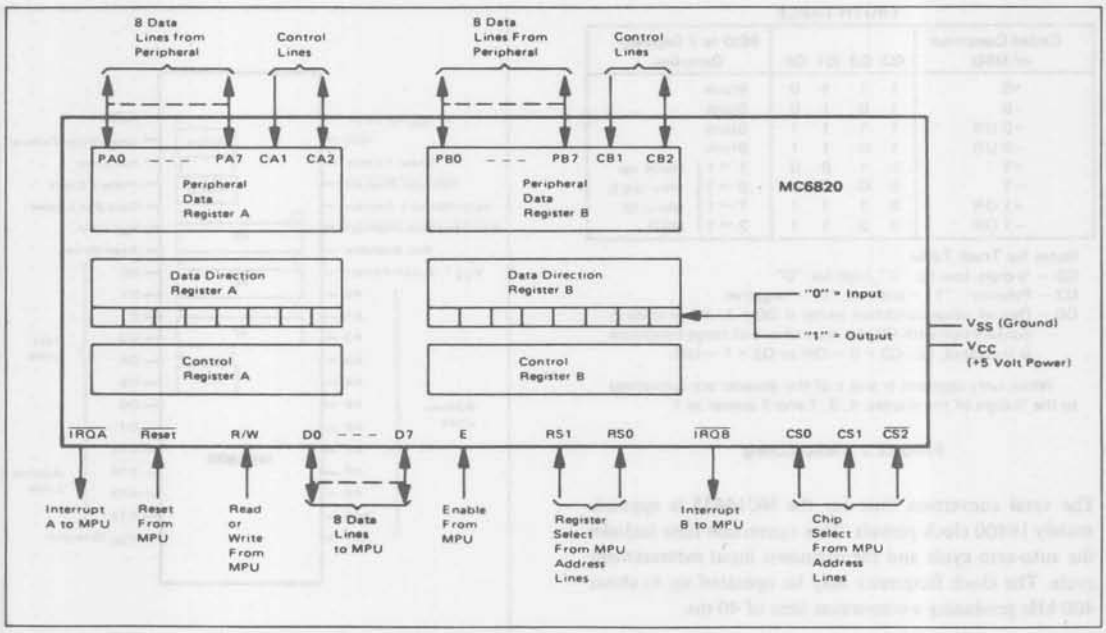

FIGURE 4 – PIA Functions

"1"s and "0"s into the data direction register. At the beginning of the program the I/O configuration is programmed into the data direction register, after which the control register is programmed to select the data register for I/O operation.

8-CHANNEL DATA ACQUISITION NETWORK

Figures 5 and 6 are the flow diagram for the 8-channel data acquisition network. Figure 5 shows the basic operation of the program while Figure 6 provides more detail on the A/D conversion routine. These flow diagrams relate to the actual software shown in Figure 8. The hardware required for the data acquisition is shown in Figure 9; as can be seen, it is fairly simple, consisting of the MC14433, MC1403* reference, MC14051B analog multiplexer, and an MC6820 PIA. The PIA is used as the interface between the microprocessor address and the data bus to the A/D. The microprocessor and associated memory are not shown due to a wide variety of forms possible depending upon the task that the total system is performing.

The reference for the MC14433 is an MC1403 bandgap reference which provides an output voltage of 2.5 volts. This voltage is divided down by the 20 kΩ pot to the 2.000 volt reference required by the MC14433. If a 200 mV reference is used, full scale for the DAN will be 199.9 mV.

The analog multiplexing required to handle the eight input channels is provided by a MC14051B CMOS multiplexer. This device selects one of eight inputs with a 3-bit binary code. The device is capable of switching dual polarity (plus or minus inputs) with a single polarity control voltage.

*MC1403 to be introduced first quarter 1977.

The MC14433 BCD output and digit select outputs are connected to the B side of the PIA as shown in lines 21-28 of the software routine. These lines of the software are comment lines only and do not result in code for the microprocessor. The B side data register of the PIA is labeled throughout the program as PIA1BD while the control register is labeled PIA1BC. The control I/O lines (CB1 and CB2) of the B side PIA are connected to EOC and DU of the MC1433.

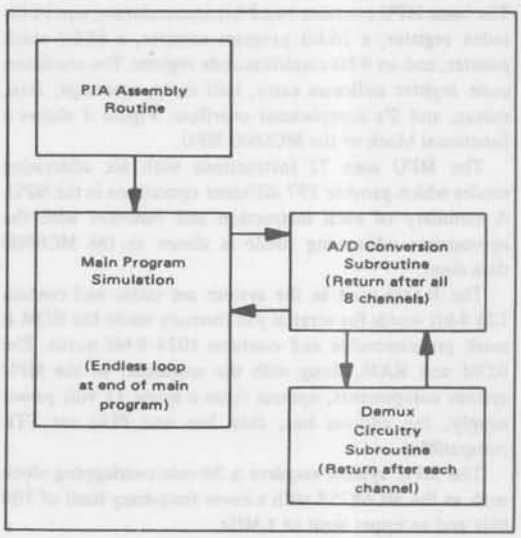

FIGURE 5 – Basic Operation of 8 Channel DAN

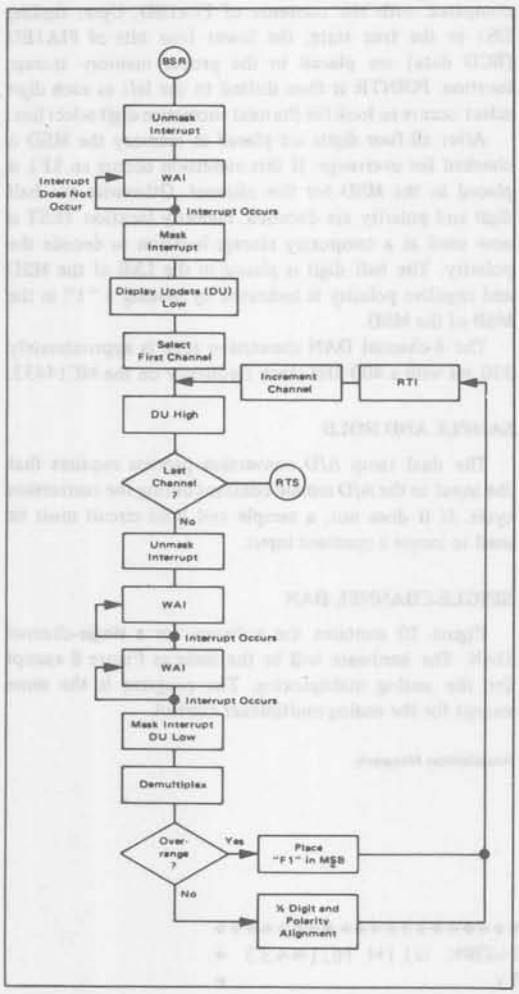

FIGURE 6 – A/D Conversion Subroutine Flow Chart

The first executable instruction for the program is in line 55 and starts a section called PIA assembly. The PIA sets the A side data register as all outputs and the B side data register as all inputs. From there the program goes to the main program simulation which, as its name implies, is a simulation of the user's main program. At such time in the user's program that some analog information is required, the A/D conversion subroutine starting in line 75 is executed. This routine synchronizes the program with the A/D conversion cycle and selects the first channel to be measured.

After the A/D conversion cycle for the first channel is completed the microprocessor is interrupted by the EOC of the MC14433. The interrupt program of line 88 is then executed; this demultiplexes the BCD output of the MC14433 and stores the data in memory. After completing he interrupt program the microprocessor returns to the A/D conversion subroutine and the next channel is selected. When the measurement of channel 2 is completed, the interrupt program is then executed and the resulting data stored away in memory. This procedure is repeated until all eight channels are read, after which the MPU returns to the main program. At this point the data obtained in the A/D conversion subroutine may be processed as required.

Looking at the software for the 8-channel data acquisition network in more detail, program storage of the final results begins in memory location $0010. Each BCD character is stored in the four LSBs of these memory locations. See Figure 7 for explanation of data storage. Each of the eight channel readings requires four memory

Channel Number	Memory Address	Digit	Data Example	Input Voltage
1	0010	MSD	01	1.729 V
	0011		07	
	0012		02	
	0013	LSD	09	
2	0014	MSD	F1	Overrange
	0015		09	
	0016		09	
	0017	LSD	09	
3	0018	MSD	08	-0.130 V
	0019		01	
	001A		03	
	001B	LSD	00	
4	001C	MSD	09	-1.130 V
	001D		01	
	001E		03	
	001F	LSD	00	
5	0020	MSD	00	0.000 V
	0021		00	
	0022		00	
	0023	LSD	00	
6	0024	MSD	01	1.000 V
	0025		00	
	0026		00	
	0027	LSD	00	
7	0028	MSD	F1	Overrange
	0029		09	
	002A		09	
	002B	LSD	09	
8	002C	MSD	09	-1.000 V
	002D		00	
	002E		00	
	002F	LSD	00	

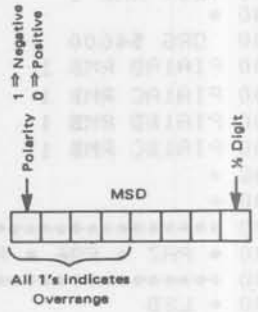

FIGURE 7 – Data Storage Definition

cycle the index register points to the MSD of that channel. This address is also stored at memory location called STORL.

Memory location TEST has two purposes; the first is for keeping track of which WAI was executed when the MPU was in the interrupt routine. This is required since more than one A/D conversion cycle is required for each channel. For the first channel three EOC pulses are required, while the remaining channels require only two A/D conversion cycles. The extra A/D conversion cycle in the first channel is used to synchronize the A/D converter to the MPU system. The second A/D conversion cycle in the first channel and the first conversion cycle of the remaining channels ensure that the polarity is correct for the current input. This is required since the MC14433 determines polarity in the previous conversion cycle.

Since the display update pin is edge triggered it must be taken high and low again in each conversion cycle when the data is to read by the MPU. The DU pin is taken high prior to the WAI for the measurement and low in the interrupt routine after the EOC occurs.

As mentioned previously, the multiplexed BCD data from the MC14433 is demultiplexed in the interrupt routine. A "1" is placed in bit 4 of POINTR which is select occurs to look for the next successive digit select line.

After all four digits are placed in memory the MSD is checked for overrange. If this condition occurs an $F1 is placed in the MSD for this channel. Otherwise the half digit and polarity are decoded. Memory location TEST is now used as a temporary storage location to decode the polarity. The half digit is placed in the LSB of the MSD and negative polarity is indicated by placing a "1" in the MSB of the MSD.

The 8-channel DAN conversion time is approximately 320 ms with a 400 kHz clock frequency on the MC14433.

SAMPLE AND HOLD

The dual ramp A/D conversion process requires that the input to the A/D remain constant during the conversion cycle. If it does not, a sample and hold circuit must be used to insure a constant input.

SINGLE-CHANNEL DAN

Figure 10 contains the software for a single-channel DAN. The hardware will be the same as Figure 8 except for the analog multiplexing. The program is the same except for the analog multiplexer control.

FIGURE 8 – 8-Channel Data Acquisition Network

```
 1.000  NAM DWA36
 2.000  OPT MEM,OTAPE
 3.000 *
 4.000 *
 5.000 *******************************************************
 6.000 * 8 CHANNEL DATA AQUISTION NETWORK WITH MC14433      *
 7.000 *              WITH AUTOPOLARITY                      *
 8.000 *******************************************************
 9.000 *
10.000  ORG $0000
11.000 STORL RMB 2          POINTER FOR DATA STORAGE LOCATION
12.000 POINTR RMB 1               POINTER FOR DIGIT SELECT
13.000 TEST RMB 1
14.000 *
15.000  ORG $4000
16.000 PIA1AD RMB 1             A SIDE,DATA REGISTER
17.000 PIA1AC RMB 1             A SIDE,CONTROL REGISTER
18.000 PIA1BD RMB 1             B SIDE,DATA REGISTER
19.000 PIA1BC RMB 1             B SIDE,CONTROL REGISTER
20.000 *
21.000 *                     **PIA CONFIGURATION**
22.000 *******************************************************
23.000 * PA7 * PA6 * PA5 * PA4 * PA3 * PA2 * PA1 * PA0 *
24.000 *******************************************************
25.000 * LSD                MSD * MSB                 LSB *
26.000 *******************************************************
27.000 *    DIGIT SELECT       *        BCD             *
28.000 *******************************************************
```

```
29.000 *
30.000 *          RESULTS STORED IN LOCATIONS $0010-$002F.
31.000 *             EACH CHANNEL OCCUPIES FOUR CONSECUTIVE
32.000 *             MEMORY LOCATIONS WITH MSD FIRST.
33.000 *             NEGATIVE POLARITY INDICATED VIA A
34.000 *             "1" IN MSB OF THE MSD.
35.000 *             OVERRANGE INDICATION VIA AN "F1" IN
36.000 *             MSD OF EACH CHANNEL.
37.000 *
38.000 *
39.000 *
40.000 *          CHANNEL SELECTION VIA PIA1AD.
41.000 *             CHANNEL NUMBER IS CODED IN A BINARY
42.000 *             FORM FOR CHANNELS 0-7.
43.000 *
44.000 *
45.000 *
46.000 *
47.000 *
48.000 *
49.000 *
50.000 *
51.000 *
52.000 *
53.000 *
54.000 *
55.000  ORG $0300                    PIA ASSEMBLY
56.000  CLR TEST
57.000  CLR PIA1BC                   PIA ASSEMBLY
58.000  CLR PIA1BD           B SIDE INPUTS
59.000  CLR PIA1AC
60.000  LDA A #$FF
61.000  STA A PIA1AD         A SIDE OUTPUTS
62.000  LDA A #$34
63.000  STA A PIA1BC
64.000  STA A PIA1AC
65.000  LDS #$08F0
66.000  CLI
67.000 *
68.000 *
69.000  NOP                          MAIN PROGRAM SIMULATION
70.000  JSR CONVRT
71.000 END NOP
72.000  BRA END
73.000 *
74.000 *
75.000 CONVRT LDX #$000C             CONVERSION SUBROUTINE
76.000  STX 0000
77.000  LDA B #$04
78.000  STA B TEST
79.000  LDA A PIA1BD
80.000  LDA A #$37
81.000  STA A PIA1BC
82.000  WAI
```

FIGURE 8 – 8-Channel Data Acquisition Network

```
 83.000  LDA B #$07
 84.000 N STA B PIA1AD
 85.000  LDA A #$02
 86.000  STA A TEST
 87.000  LDA A #$37
 88.000  STA A PIA1BC
 89.000  WAI
 90.000  NOP
 91.000  WAI
 92.000  DEC B
 93.000  BPL N
 94.000  RTS
 95.000 *
 96.000 *
 97.000 *
 98.000  ORG $0850                    INTERRUPT ROUTINE
 99.000  LDA A #$3F
100.000  STA A PIA1BC
101.000  LSR TEST
102.000  BCC FIRST
103.000  LDA A #$34
104.000  STA A PIA1BC
105.000 BEGIN LDA A #$10
106.000  STA A POINTR
107.000  LDX $0000
108.000 NEXT LDA A PIA1BD
109.000  ROR TEST
110.000  ADD B TEST
111.000  TAB
112.000  AND A POINTR
113.000  BEQ NEXT
114.000  ASL POINTR
115.000  AND B #$0F
116.000  STA B 4,X
117.000  INX
118.000  BCC NEXT
119.000  LDA A 0,X                 OVERRANGE TEST
120.000  TAB
121.000  AND A #$0B
122.000  CMP A #$03
123.000  BEQ OVRNGE
124.000  CLR TEST              HALF DIGIT AND POLARITY
125.000  AND B #$0C                ALIGNMENT
126.000  LSR B
127.000  LSR B
128.000  LSR B
129.000  ROR TEST
130.000  ADD B TEST
131.000  COM B
132.000  AND B #$81
133.000  STA B 0,X
134.000  BRA FINE
135.000 OVRNGE LDA A #$F1          OVERRANGE ROUTINE
136.000  STA A 0,X
```

FIGURE 8 – 8-Channel Data Acquisition Network

```
137.000 FINE STX STORL
138.000  RTI
139.000 FIRST LDA A PIA1BD   DUMMY LOAD TO CLR INTERRUPT
140.000  RTI
141.000  ORG $0350              HARDWARE INTERRUPT VECTOR
142.000  FDB $03F0
143.000  MON
```

FIGURE 8 – 8-Channel Data Acquisition Network

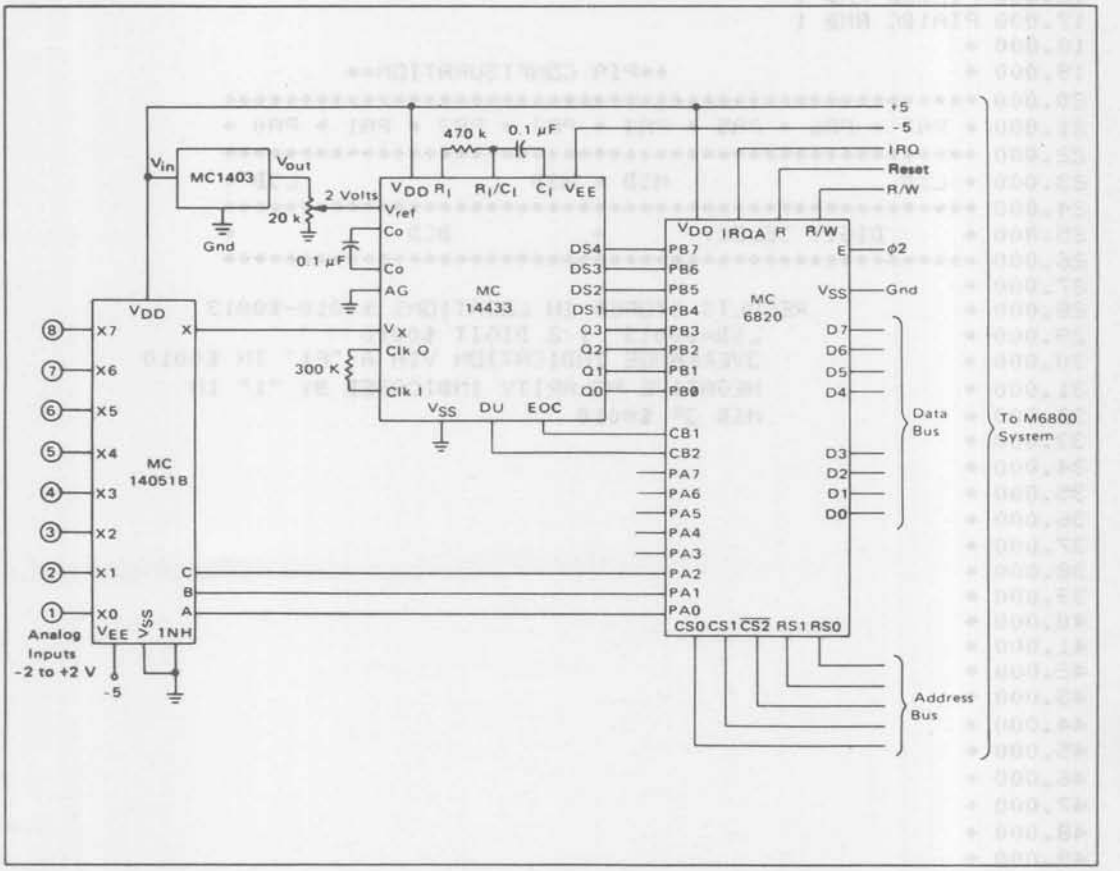

FIGURE 9 – 8-Channel Data Acquisition Hardware

```
 1.000  NAM DWA35
 2.000  OPT MEM,OTAPE
 3.000 *
 4.000 *                    *********
 5.000 *                    *MC14433*
 6.000 *****************************************************
 7.000 * SINGLE CHANNEL DATA ACQUISITION NETWORK WITH *
 8.000 *                   AUTOPOLARITY                    *
 9.000 *****************************************************
10.000 *
11.000  ORG $0002
12.000 POINTR RMB 1          POINTER FOR DIGIT SELECT
13.000 TEST RMB 1
14.000 *
15.000  ORG $4002
16.000 PIA1BD RMB 1
17.000 PIA1BC RMB 1
18.000 *
19.000 *                    **PIA CONFIGURATION**
20.000 *****************************************************
21.000 * PA7 * PA6 * PA5 * PA4 * PA3 * PA2 * PA1 * PA0 *
22.000 *****************************************************
23.000 * LSD                MSD * MSB              LSB *
24.000 *****************************************************
25.000 *     DIGIT SELECT      *          BCD          *
26.000 *****************************************************
27.000 *
28.000 *          RESULTS STORED IN LOCATIONS $0010-$0013
29.000 *             LSD=$0013  1/2 DIGIT $0010
30.000 *             OVERRANGE INDICATION VIA A "F1" IN $0010
31.000 *             NEGATIVE POLARITY INDICATED BY "1" IN
32.000 *             MSB OF $0010
33.000 *
34.000 *
35.000 *
36.000 *
37.000 *
38.000 *
39.000 *
40.000 *
41.000 *
42.000 *
43.000 *
44.000 *
45.000 *
46.000 *
47.000 *
48.000 *
49.000 *
50.000 *
51.000 *
52.000 *
53.000 *
54.000 *
```

FIGURE 10 – Single-Channel Data Acquisition Network

```
 55.000 *
 56.000 *
 57.000 *
 58.000  ORG $0800
 59.000  CLR TEST
 60.000  CLR PIA1BC                  PIA ASSEMBLY
 61.000  CLR PIA1BD
 62.000  LDA A #$34
 63.000  STA A PIA1BC
 64.000  LDS #$08F0
 65.000  CLI
 66.000 *
 67.000 *
 68.000  NOP                         MAIN PROGRAM SIMULATION
 69.000  JSR CONVRT
 70.000 END NOP
 71.000  BRA END
 72.000 *
 73.000 *
 74.000 CONVRT LDX #$0010     CONVERSION SUBROUTINE
 75.000  LDA B #$04
 76.000  STA B TEST
 77.000  LDA A PIA1BD DUMMY LOAD TO CLEAR INTERRUPT
 78.000  LDA A #$3F
 79.000  STA A PIA1BC
 80.000  WAI
 81.000  NOP
 82.000  WAI
 83.000  NOP
 84.000  WAI
 85.000  RTS
 86.000 *
 87.000 *
 88.000  ORG $0850              BEGINING OF INTERRUPT PROGRAM
 89.000  CLC
 90.000  LSR TEST
 91.000  BCC DELAY
 92.000  LDA A #$34
 93.000  STA A PIA1BC
 94.000 BEGIN LDA A #$10
 95.000  STA A POINTR
 96.000 NEXT LDA A PIA1BD
 97.000  TAB
 98.000  AND A POINTR
 99.000  BEQ NEXT
100.000  ASL POINTR
101.000  AND B #$0F
102.000  STA B 0,X
103.000  INX
104.000  BCC NEXT
105.000  LDA A $0010          OVERRANGE CHECK
106.000  TAB
107.000  AND A #$0B
108.000  CMP A #$03
```

FIGURE 10 – Single-Channel Data Acquisition Network

```
109.000  BEQ OVRNGE
110.000  CLR TEST          HALF DIGIT AND POLARITY
111.000  AND B #$0C         ALIGNMENT
112.000  LSR B
113.000  LSR B
114.000  LSR B
115.000  ROR TEST
116.000  ADD B TEST
117.000  COM B
118.000  AND B #$81
119.000  STA B $0010
120.000  BRA FINE
121.000 OVRNGE LDA A #$F1          OVERRANGE ROUTINE
122.000  STA A $0010
123.000 FINE STX STORL
124.000  RTI
125.000 DELAY LDA A PIA1BD
126.000  RTI
127.000  ORG $08F8
128.000  FDB $0850
129.000  MON
```

FIGURE 10 – Single-Channel Data Acquisition Network

REFERENCES

Aldridge, Don: *"Analog-To-Digital Conversion Techniques with the M6800 Microprocessor System"*, AN757, Motorola Semiconductor Products Inc.

M6800 Microprocessor Applications Manual, Motorola Semiconductor Products Inc.

M6800 Microprocessor Programming Reference Manual, Motorola Semiconductor Products Inc.

MC6800, MC6820 Data Sheets, *M6800 Microcomputer System Design Data*, Motorola Semiconductor Products Inc.

MC1403/1503 Data Sheet, Motorola Semiconductor Products Inc.

MC14051B Data Sheet, Motorola Semiconductor Products Inc.

MC14433 Data Sheet, Motorola Semiconductor Products Inc.

MOTOROLA

AN963

Interfacing The MC6108 A/D To a Microprocessor —

It's Easier Than You Think!

Prepared by
Dennis R. Morgan
Motorola, Inc. Analog IC Division

INTRODUCTION

This application note will supplement information in the MC6108 data sheet by describing the detailed requirements for interfacing the Analog-to-Digital converter to a microprocessor. The hardware requirements, and the programming necessary to execute a conversion and read the data, in several different configurations, will be discussed. The microprocessor used in developing this application note is the MC6802 (operating off a 3.58 MHz crystal), a representative sample of the MC6800 family.

Because of the short conversion time of the MC6108, "Wait" states and "Wait for Interrupt" instructions are generally not needed with most microprocessors. The microprocessor can issue a CONVERT instruction, and immediately thereafter, issue a READ instruction, regardless of whether the MC6108 is read through a port (MC6821), or read off the bus directly.

MC6108 OPERATION

The MC6108 is a high-speed, 8-bit, A/D converter using the familiar Successive Approximation technique. Referring to the block diagram in Figure 1, the device includes the SAR, 8-bit DAC, comparator, 2.5 volt precision reference, matched resistors for +10, +5 and ±5 volt inputs, and control logic.

By connecting the internal temperature stable 2.5 volt reference to the Gain R pin, a reference current of ≈1 mA is supplied to the DAC. That current is gained up by x4 by the DAC, and then attenuated by the digital code from the SAR. The analog input signal is applied to R_{in} (for 0 to +10 volts), or R_{off} for 0 to +5 volts, and the current from that signal is compared with the DAC's output current by the comparator during the successive approximation process. The converter will accept a ±5 volt input by connecting the 2.5 volt reference to R_{off}.

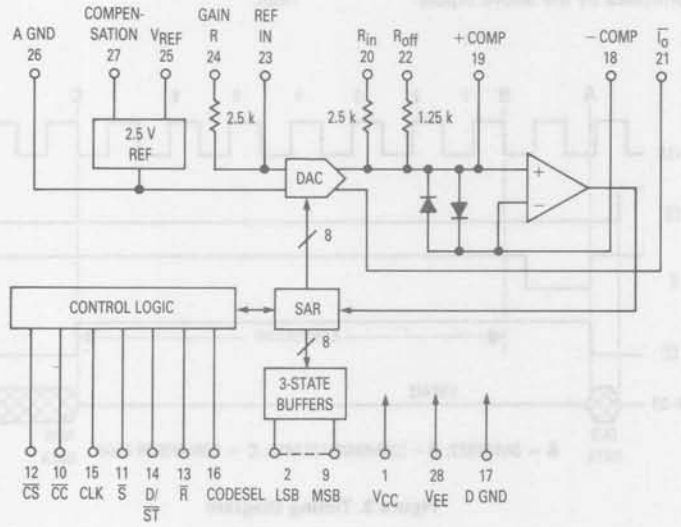

Figure 1. Block Diagram

3

and the input to R_{in}. Other input voltages can be accommodated by using external resistors at Ref In and +Comp, instead of the internal resistors, and grounding Gain R, R_{in}, and R_{off}. In the circuits tested for this application note, the analog side of the MC6108 was configured as shown in Figure 2.

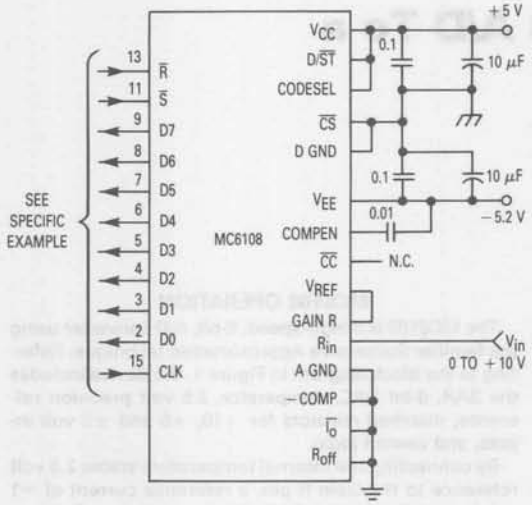

Figure 2. Analog Connections

Proper operation with a 5 MHz clock is guaranteed, although with careful attention to detail, clock rates as high as 10 MHz can be used. The control signals include Chip Select ($\overline{CS}$), Clock, Read ($\overline{R}$), Start ($\overline{S}$), Conversion Complete ($\overline{CC}$), Data/Status (D/$\overline{ST}$), and Code Select (CodeSel). The digital inputs and outputs are TTL compatible, with 3-state capability controlled by the above inputs.

Figure 3 shows the timing of the MC6108 during a conversion. The clock need not be synchronous with the other signals, and can run continuously. $\overline{CS}$ enables the device, and $\overline{S}$ must receive an active low pulse to initiate the conversion. The timing requirements are two: 1) $\overline{CS}$, $\overline{S}$, and Clock must be simultaneously low for a minimum of 50 ns (they may go low in any sequence); and 2) at least one low-to-high clock transition must occur during the $\overline{S}$ low time. After $\overline{S}$ switches high, the conversion starts on the next clock rising edge. The conversion requires 7 clock cycles thereafter.

$\overline{CC}$ (Conversion Complete) switches high at the beginning of the conversion process (when $\overline{S}$, $\overline{CS}$, and Clk are low) to indicate "busy," and switches low at the clock's rising edge corresponding to the end of the conversion. The data outputs (D7-D0) are in a high impedance (3-state) mode during the conversion, and go active (within 40 ns) after $\overline{CC}$ switches low. The outputs are also in the 3-state mode whenever $\overline{CS}$ is high.

Not shown in Figure 3 is the effects of the $\overline{R}$ ($\overline{READ}$) input. $\overline{R}$ affects the state of the outputs in that when $\overline{R}$ is low, the outputs are active (if $\overline{CS}$ is low and the MC6108 is not converting), and taking $\overline{R}$ high puts the outputs into the 3-state mode. The difference between $\overline{R}$ and $\overline{CS}$ is that $\overline{CS}$, when high, inhibits a conversion, whereas $\overline{R}$ does not affect the conversion process. Therefore, in the following examples where the MC6108 is connected directly to the microprocessor bus, $\overline{CS}$ is hard-wired low, $\overline{S}$ will initiate the conversions, and $\overline{R}$ will be controlled by the address decoder when data is to be read. Where the MC6108 is read through a port, $\overline{R}$ is hard-wired low.

ADDRESS DECODING

In order for the MC6802 microprocessor to read data from memory or memory-like devices (the MC6108 is a "read only" device), the timing requirements of Figure 5 must be satisfied. The requirements are that the data from the MC6108 must be valid while R/$\overline{W}$ is high, while VMA (Valid Memory Address) is high (which ensures the address to the decoder is valid), and while the E clock is high.

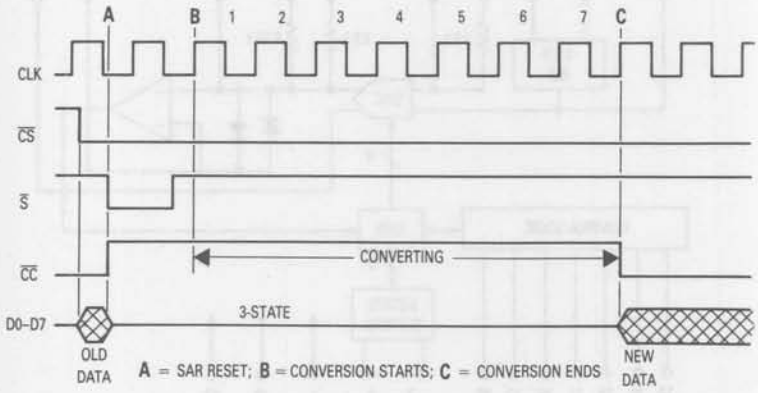

Figure 3. Timing Diagram

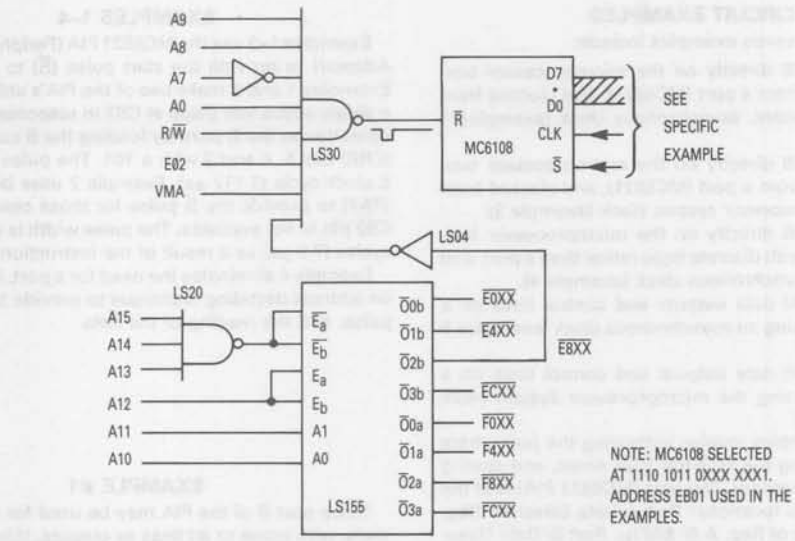

Figure 4. Address Decoder

In the microprocessor circuit used to develop the following examples, the address block $E800_H$–$EFFF_H$ was unused, and so the address $EB01_H$ was chosen for the MC6108. Since the entire block of 1K bytes was free, an incomplete decoding was possible, simplifying the decoder. Figure 4 is the schematic of the decoder, which uses three LS ICs, plus two inverters. Address lines A15 through A7, and A0, are used to activate the MC6108 at address $EB01_H$, although any address satisfying the code 1110 1011 0xxx xxx1 will work. If other addresses satisfying that code interfere with other devices in the system, then a more complete decoding involving A6–A1 is necessary.

R/$\overline{W}$, E (phase 2 clock), and VMA are also included in the decoder to satisfy the requirements of the MC6802 microprocessor. The LS155 (along with the LS20) provides a decode (active low) for each of the 1K blocks from $E000_H$ through $FFFF_H$. The LS30 provides the rest of the decoding, and provides an active low output which is connected directly to the $\overline{R}$ input on the MC6108.

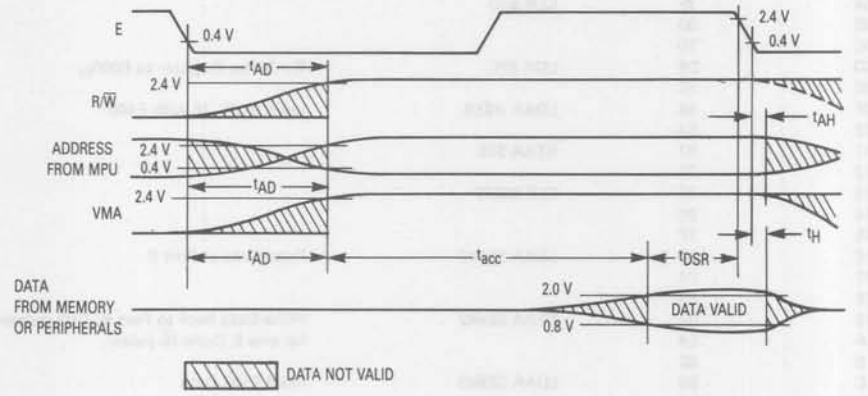

Figure 5. MC6802 Read Data From Memory

CIRCUIT EXAMPLES

The following seven examples include:

- The MC6108 directly on the microprocessor bus, controlled from a port (MC6821), and clocked from an independent, asynchronous clock (examples 1 and 2).
- The MC6108 directly on the microprocessor bus, controlled from a port (MC6821), and clocked from the microprocessor system clock (example 3).
- The MC6108 directly on the microprocessor bus, controlled with discrete logic rather than a port, and using an asynchronous clock (example 4).
- The MC6108 data outputs **and** control lines on a port, and using an asynchronous clock (examples 5 and 6).
- The MC6108 data outputs **and** control lines on a port, and using the microprocessor system clock (example 7).

All of the examples involve initializing the port where necessary, reading the MC6108 1024 times, and storing the 1K bytes in memory. The port (MC6821 PIA) is at the following address locations: Port A/Data Direction Reg. A @ $E480_H$, Control Reg. A @ $E481_H$, Port B/ Data Direction Reg. B @ $E482_H$, and Control Reg. B @ $E483_H$. The 1K bytes of data are stored at $E000_H$–$E3FF_H$, and those beginning and ending addresses are stored at $007C_H$–$007F_H$ (for use with the Index Register). The addresses used for the instructions in the listings are for reference only.

EXAMPLES 1–4

Examples 1–3 use the MC6821 PIA (Peripheral Interface Adapter) to provide the start pulse ($\overline{S}$) to the MC6108. Examples 1 and 3 make use of the PIA's ability to output a single active low pulse at CB2 in response to a "write" operation to the B port, by loading the B control register (CRB) bits 5, 4 and 3 with a 101. The pulse width is one E clock cycle (1.117 μs). Example 2 uses bit 7 of port A (PA7) to provide the $\overline{S}$ pulse for those cases where the CB2 pin is not available. The pulse width is seven E clock cycles (7.8 μs) as a result of the instructions used.

Example 4 eliminates the need for a port, instead using an address decoding technique to provide both the Start pulse, and the reading of the data.

EXAMPLE #1

Since port B of the PIA may be used for other peripherals, with some or all lines as outputs, this program sequence involves first reading port B's Peripheral Data Register, and then writing back the same information, so as to not disturb the outputs. The write operation creates the pulse at the CB2. The data from the MC6108 is read immediately thereafter. See Figure 6 for the schematic, and Figure 7 for the timing involved.

Address	OpCode	Mnemonic	Notes
			Start Initialization-
01	86	LDAA #$2C	
02	2C		
03	B7	STAA $E483	Set CB2 to Output
04	E4		
05	83		
			-Start Read/Store Program-
06	86	LDAA #$E0	Load 007C, 7D with E000
07	E0		
08	97	STAA $7C	
09	7C		
0A	7F	CLR $7D	
0B	00		
0C	7D		
0D	DE	LDX $7C	Set Index Register to $E000_H$
0E	7C		
0F	86	LDAA #$E4	Load 007E, 7F with E400
10	E4		
11	97	STAA $7E	
12	7E		
13	7F	CLR $007F	
14	00		
15	7F		
16	B6	LDAA $E482	Read Data at Port B
17	E4		
18	82		
19	B7	STAA $E482	Write Data back to Port B; CB2 pulses low
1A	E4		for one E Cycle ($\overline{S}$ pulse).
1B	82		
1C	B6	LDAA $EB01	Read 6108 Data
1D	EB		
1E	01		
1F	A7	STAA $00,X	Store 6108 Data
20	00		

Address	OpCode	Mnemonic	Notes
21	08	INX	Increment Index Register
22	9C	CPX $7E	Compare Index Reg. with 7E/7F$_H$ (E400)
23	7E		
24	2C	BGE $03	Branch if ≥ 0 to $0029
25	03		
26	7E	JMP $0016	Jump to $0016 — Read Next Byte
27	00		
28	16		
29	??	??	1K Bytes stored — Next Instruction

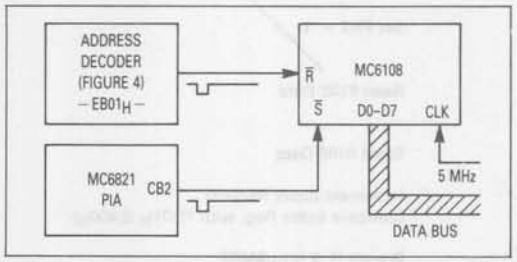

Figure 6. Reading Data Off The Bus — Example #1

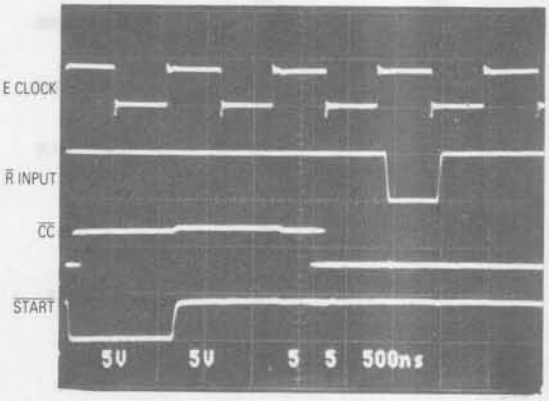

Figure 7. Example #1 Timing

EXAMPLE #2

This example involves using bit 7 of the PIA's port A (PA7) to provide the $\overline{S}$ pulse. The program sequence involves writing to the A port to bring PA7 low, then high, and then reading the data from the MC6108. See Figure 8 for the schematic, and Figure 9 for the timing involved.

Address	OpCode	Mnemonic	Notes
			-Start Initialization-
00	7F	CLR $E481	Access PIA's DDRA
01	E4		
02	81		
03	86	LDAA #$80	
04	80		
05	B7	STAA $E480	Set PA7 = Output (PA7 will provide $\overline{S}$ pulse)
06	E4		
07	80		
08	86	LDAA #$04	
09	04		
0A	B7	STAA $E481	Access Per. Data Reg. A
0B	E4		
0C	81		
0D	86	LDAA #$80	
0E	80		
0F	B7	STAA $E480	Set PA7 = 1
10	E4		
11	80		**-End Initialization-**
			-Start Read/Store Program-
12	86	LDAA #$E0	Load 007C, 7D with E000$_H$
13	E0		|
14	97	STAA $7C	|
15	7C		|
16	7F	CLR $7D	|
17	00		|
18	7D		|
19	DE	LDX $7C	Set Index Register to E000$_H$
1A	7C		

Address	OpCode	Mnemonic	Notes
1B	86	LDAA #$E4	Load 007E, 7F with $E400_H$
1C	E4		
1D	97	STAA $7E	
1E	7E		
1F	7F	CLR $007F	
20	00		
21	7F		
22	7F	CLR $E480	Set PA7 = 0
23	E4		
24	80		
25	86	LDAA #$80	$-\overline{S}$ pulse
26	80		
27	B7	STAA $E480	Set PA7 = 1
28	E4		
29	80		
2A	B6	LDAA $EB01	Read 6108 Data
2B	EB		
2C	01		
2D	A7	STAA $00,X	Store 6108 Data
2E	00		
2F	08	INX	Increment Index Register
30	9C	CPX $7E	Compare Index Reg. with $7E/7F_H$ ($E400_H$)
31	7E		
32	2C	BGE $03	Branch IF ≥ 0 to $0037
33	03		
34	7E	JMP $0022	Jump to $0022 — Read Next Byte
35	00		
36	22		
37	??	?	1K Bytes stored — Next Instruction

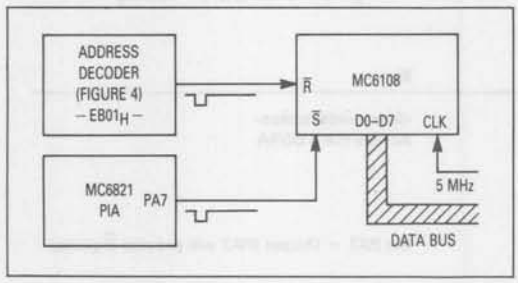

Figure 8. Reading Data Off The Bus — Example #2

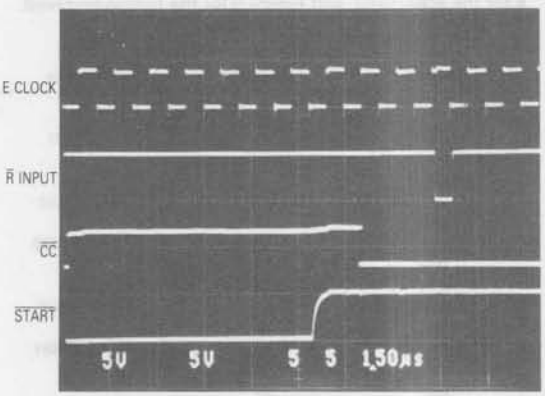

Figure 9. Example #2 Timing

3

EXAMPLE #3

This example is similar to example #1, except that the microprocessor's system clock (E) is used by the MC6108, rather than the faster 5 MHz clock. Because of the clock cycles required by the MC6108 to complete its conversion, 3 No Op instructions (6 clock cycles) are inserted between the start command ($\overline{S}$ pulse), and the reading of the data. The program sequence involves reading port B, and then writing back the same information so as to not affect any outputs. The write operation creates the $\overline{S}$ pulse at the CB2 output. The data is then read (after the 3 No Ops). See Figure 10 for the schematic, and Figure 11 for the timing involved.

Address	OpCode	Mnemonic	Notes
			-Start Initialization-
01	86	LDAA #$2C	
02	2C		
03	B7	STAA $E483	Set CB2 to Output
04	E4		
05	83		
			-Start Read/Store Program-
06	86	LDAA #$E0	Load 007C, 7D with E000
07	E0		
08	97	STAA $7C	
09	7C		
0A	7F	CLR $7D	
0B	00		
0C	7D		
0D	DE	LDX $7C	Set Index Register to $E000_H$
0E	7C		
0F	86	LDAA #$E4	Load 007E, 7F with E400
10	E4		
11	97	STAA $7E	
12	7E		
13	7F	CLR $007F	
14	00		
15	7F		
16	B6	LDAA $E482	Read Data at Port B
17	E4		
18	82		
19	B7	STAA $E482	Write Data back to Port B; CB2 pulses low
1A	E4		for one E Cycle ($\overline{S}$ pulse)
1B	82		
1C–1E	3x01	3 No Ops	MC6108 is converting
1F	B6	LDAA $EB01	Read 6108 Data
20	EB		
21	01		
22	A7	STAA $00,X	Store 6108 Data
23	00		
24	08	INX	Increment Index Register
25	9C	CPX $7E	Compare Index Reg. with $7E/7F_H$ (E400)
26	7E		
27	2C	BGE $03	Branch IF ≥ 0 to $002C
28	03		
29	7E	JMP $0016	Jump to $0016 — Read Next Byte
2A	00		
2B	16		
2C	??	??	1K Bytes stored — Next Instruction

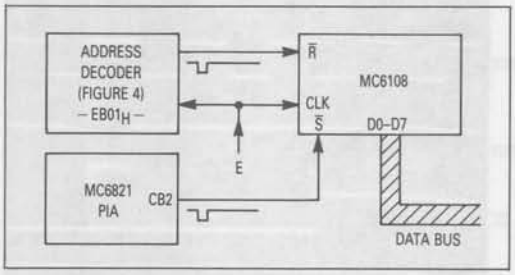

Figure 10. Reading Data Off The Bus — Example #3

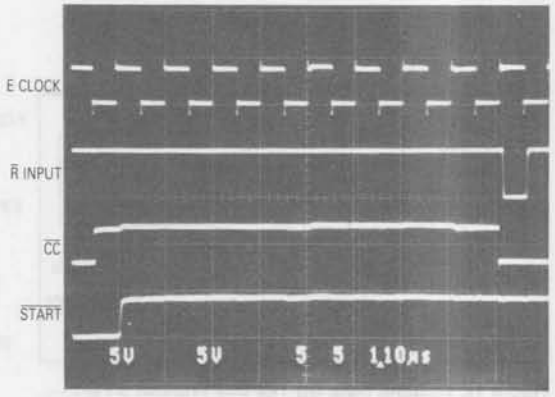

Figure 11. Example #3 Timing

EXAMPLE #4

This example does not use a PIA port for either the start ($\overline{S}$) or the Read ($\overline{R}$) operation, but instead uses some gates in addition to the address decoder of Figure 4. Address line A0 is removed from its place in Figure 4, and instead implemented as shown in Figure 12 so as to provide decoding at two addresses ($EB00_H$ and $EB01_H$). The microprocessor is made to read address $EB00_H$, creating an active low pulse at $\overline{S}$. The width of the pulse is 0.56 μs (1/2 E clock cycle), which is wide enough when using a 5 MHz clock for the MC6108. Due to the requirements of the MC6108, the minimum clock frequency usable in this configuration is 2x E clock frequency. Reading the data, by means of the $\overline{R}$ input is the same as in the previous examples. The two LS04 inverters in series with the lower OR gate provide a propagation delay to allow for the propagation delay of the address decoder block, thus preventing glitches at the $\overline{S}$ input. Figure 13 shows the timing involved.

Address	OpCode	Mnemonic	Notes
			-Start Read/Store Program-
00	86	LDAA #$E0	Load 007C, 7D with $E000_H$
01	E0		
02	97	STAA $7C	
03	7C		
04	7F	CLR $7D	
05	00		
06	7D		
07	DE	LDX $7C	Set Index Register to $E000_H$
08	7C		
09	86	LDAA #$E4	Load 007E, 7F with $E400_H$
0A	E4		
0B	97	STAA $7E	
0C	7E		
0D	7F	CLR $007F	
0E	00		
0F	7F		
10	B6	LDAA $EB00	Read $EB00 — create $\overline{S}$ pulse through
11	EB		Address Decode Logic
12	00		
13	B6	LDAA $EB01	Read 6108 Data
14	EB		
15	01		
16	A7	STAA $00,X	Store 6108 Data
17	00		
18	08	INX	Increment Index Register
19	9C	CPX $7E	Compare Index Reg. with $7E/7F_H$ ($E400_H$)
1A	7E		
1B	2C	BGE $03	Branch IF ≥ 0 to $0020
1C	03		
1D	7E	JMP $0010	Jump to $0010 — Read Next Byte
1E	00		
1F	10		
20	??	?	1K Bytes stored — Next Instruction

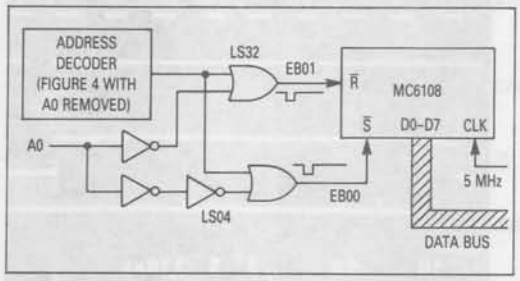

Figure 12. Reading Data Off The Bus Without a Port — Example #4

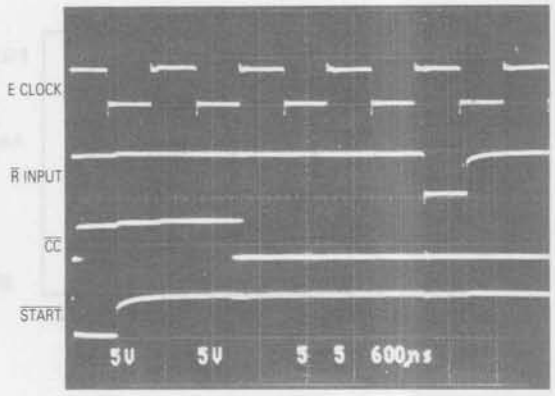

Figure 13. Example #4 Timing

EXAMPLES 5–7

Examples 5–7 use the MC6821 PIA for reading the data (through its B port) from the MC6108, as well as for the control. Examples 5 and 7 make use of the PIA's ability to output a single active low pulse at CB2 in response to a "write" operation to the B port, by loading the B control register (CRB) bits 5, 4, and 3 with a 101. The pulse width is one E clock cycle (1.117 μs). Example 6 uses bit 7 of port A (PA7) to provide the $\overline{S}$ pulse for those cases where the CB2 pin is not available. The pulse width is seven E clock cycles (7.8 μs) as a result of the instructions used.

EXAMPLE #5

The program sequence for this example is to write a 00_H to the B port to create the pulse at CB2 (writing to inputs does not affect them), and then reading the same port to obtain the MC6108's data. The conversion sequence requires one No Op before the read instruction due to the setup time required by the PIA. See Figure 14 for the schematic, and Figure 15 for the timing involved.

Address	OpCode	Mnemonic	Notes	
			-Start Initialization-	
01	7F	CLR $E483	Access PIA's DDRB	
02	E4			
03	83			
04	7F	CLR $E482	Set PB7–0 = Inputs	Initialize PIA
05	E4			
06	82			
07	86	LDAA #$2C		
08	2C			
09	B7	STAA $E483	Access Per. Data Reg. B,	
0A	E4		Set CB2 to Output	
0B	83		**-End Initialization-**	
			-Start Read/Store Program-	
10	86	LDAA #$E0	Load 007C, 7D with $E000_H$	
11	E0			
12	97	STAA $7C		
13	7C			
14	7F	CLR $7D		
15	00			
16	7D			
17	DE	LDX $7C	Set Index Register to $E000_H$	
18	7C			
19	86	LDAA #$E4	Load 007E, 7F with $E400_H$	
1A	E4			
1B	97	STAA $7E		
1C	7E			
1D	7F	CLR $007F		
1E	00			
1F	7F			
20	7F	CLR $E482	Write 00_H to Port B; CB2 pulses low for	
21	E4		one E Cycle ($\overline{S}$ pulse)	
22	82			
23	01	No Op	Required for PIA's setup time	
24	B6	LDAA $E482	Read port B (Read MC6108)	
25	E4			
26	82			
27	A7	STAA $00,X	Store Port B Data	
28	00			
29	08	INX	Increment Index Reg.	
2A	9C	CPX $7E	Compare Index Reg. with $7E/7F_H$ ($E400_H$)	
2B	7E			
2C	2C	BGE $03	Branch IF ≥ 0 to 0031_H	
2D	03			
2E	7E	JMP $0020	Jump to 0020_H — Read Next Byte	
2F	00			
30	20			
31	??	?	1K Bytes stored — Next Instruction	

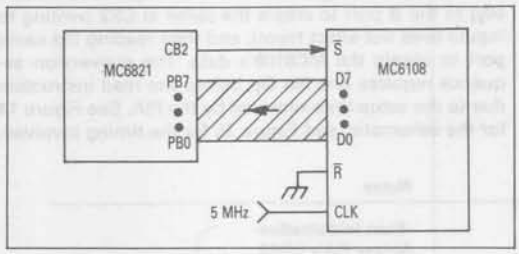

Figure 14. Reading Data Through a Port — Example #5

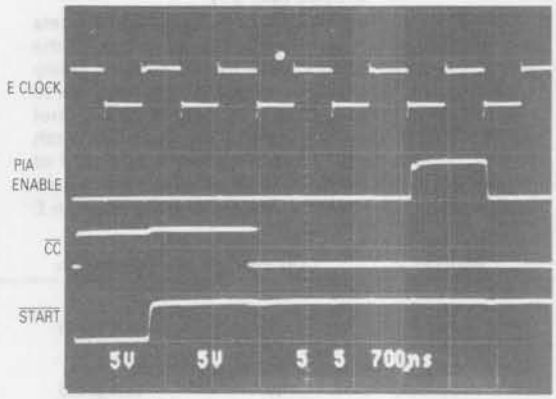

Figure 15. Example #5 Timing

EXAMPLE #6

The program sequence for the conversion is to write to the A port to bring PA7 low, and then high, and then read the B port to obtain the MC6108's data. The conversion occurs within the cycle time between PA7 switching high and reading the data, requiring no WAIT or NO-OP instructions in between. See Figure 16 for the schematic, and Figure 17 for the timing involved.

Address	OpCode	Mnemonic	Notes
			-Start Initialization-
01	7F	CLR $E481	Access PIA's DDRA
02	E4		
03	81		
04	86	LDAA #$80	
05	80		
06	B7	STAA $E480	Set PA7 = Output (PA7 will provide $\overline{S}$ pulse)
07	E4		
08	80		
09	86	LDAA #$04	
0A	04		
0B	B7	STAA $E481	Access Per. Data Reg. A
0C	E4		
0D	81		
0E	86	LDAA #$80	
0F	80		
10	B7	STAA $E480	Set PA7 = 1
11	E4		
12	80		
13	7F	CLR $E483	Access PIA's DDRB
14	E4		
15	83		
16	7F	CLR $E482	Set PB7–0 = Inputs
17	E4		
18	82		
19	86	LDAA #$04	
1A	04		
1B	B7	STAA $E483	Access Per. Data Reg. B
1C	E4		
1D	83		**-End Initialization-**
			-Start Read/Store Program-
20	86	LDAA #$E0	Load 007C, 7D with $E000_H$
21	E0		|
22	97	STAA $7C	|
23	7C		|

Address	OpCode	Mnemonic	Notes
24	7F	CLR $7D	
25	00		
26	7D		
27	DE	LDX $7C	Set Index Register to $E000_H$
28	7C		
29	86	LDAA #$E4	Load 007E, 7F with $E400_H$
2A	E4		
2B	97	STAA $7E	
2C	7E		
2D	7F	CLR $007F	
2E	00		
2F	7F		
30	7F	CLR $E480	SET PA7 = 0
31	E4		
32	80		
33	86	LDAA #$80	$-\overline{S}$ pulse
34	80		
35	B7	STAA $E480	Set PA7 = 1
36	E4		
37	80		
38	B6	LDAA $E482	Read Port B (Read MC6108)
39	E4		
3A	82		
3B	A7	STAA $00,X	Store Port B Data
3C	00		
3D	08	INX	Increment Index Reg.
3E	9C	CPX $7E	Compare Index Reg. with $7E/7F_H$ ($E400_H$)
3F	7E		
40	2C	BGE $03	Branch IF ≥ 0 to 0045_H
41	03		
42	7E	JMP $0030	Jump to 0030_H — Read Next Byte
43	00		
44	30		
45	?	?	1K Bytes stored ← Next Instruction

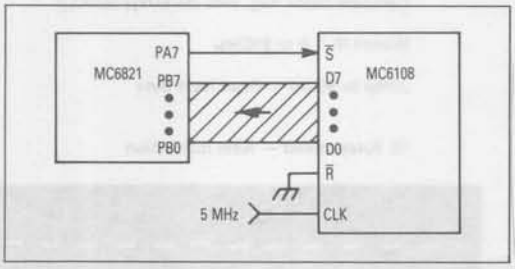

Figure 16. Reading Data Through a Port — Example #6

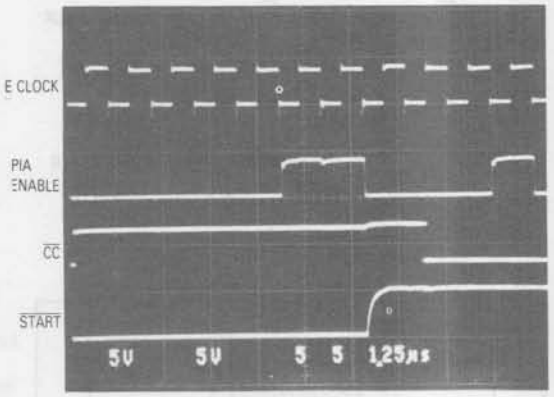

Figure 17. Example #6 Timing

EXAMPLE #7

The program sequence for this example (using the system E clock rather than a 5 MHz clock for the MC6108) is to write a 00_H to the B port to create the $\overline{S}$ pulse at CB2 (writing to inputs does not affect them), and then reading the same port to obtain the MC6108's data. Between those instruction 4 No Ops are required to give the MC6108 the necessary clock cycles to finish the conversion. See Figure 18 for the schematic, and Figure 19 for the timing involved.

Address	OpCode	Mnemonic	Notes
			-Start Initialization-
01	7F	CLR $E483	Access PIA's DDRB
02	E4		
03	83		
04	7F	CLR $E482	Set PB7–0 = Inputs
05	E4		
06	82		
07	86	LDAA #$2C	
08	2C		
09	B7	STAA $E483	Access Per. Data Reg. B,
0A	E4		Set CB2 to Output
0B	83		**-End Initialization-**
			-Start Read/Store Program-
10	86	LDAA #$E0	Load 007C, 7D with $E000_H$
11	E0		
12	97	STAA $7C	
13	7C		
14	7F	CLR $7D	
15	00		
16	7D		
17	DE	LDX $7C	Set Index Register to $E000_H$
18	7C		
19	86	LDAA #$E4	Load 007E, 7F with $E400_H$
1A	E4		
1B	97	STAA $7E	
1C	7E		
1D	7F	CLR $007F	
1E	00		
1F	7F		
20	7F	CLR $E482	Write 00_H to Port B; CB2 pulses low for
21	E4		one E Cycle ($\overline{S}$ pulse)
22	82		
23–26	4x01	4 No Ops	MC6108 is converting
27	B6	LDAA $E482	Read Port B (Read MC6108)
28	E4		
29	82		
2A	A7	STAA $00,X	Store Port B Data
2B	00		
2C	08	INX	Increment Index Reg.
2D	9C	CPX $7E	Compare Index Reg. with 007E/7F$_H$ ($E400_H$)
2E	7E		
2F	2C	BGE $03	Branch IF ≥ 0 to 0034_H
30	03		
31	7E	JMP $004B	Jump to $0020 — Read Next Byte
32	00		
33	20		
34	?	?	1K Bytes stored — Next Instruction

Initialize PIA

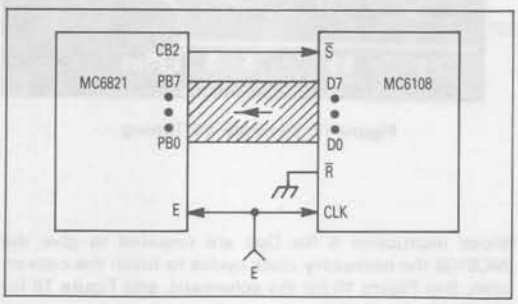

Figure 18. Reading Data Through a Port — Example #7

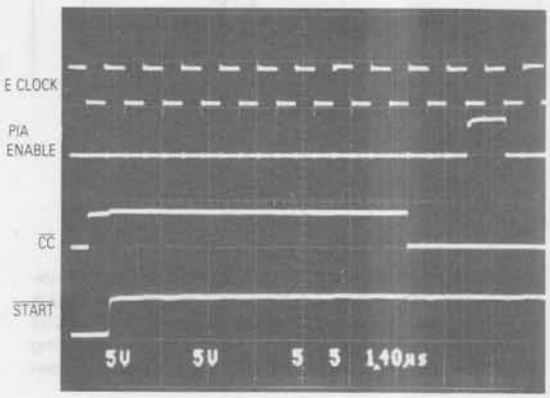

Figure 19. Example #7 Timing

OTHER EXAMPLES

Figure 20 illustrates a method for controlling several MC6108 A/D converters. The four devices are permanently enabled ($\overline{CS}$ = low) as shown in Figure 2. The PIA is set up to output a single active low pulse at the CB2 pin, as described prior to Example #1 in this application note, to initiate the conversion. The convert command ($\overline{S}$ pulse) is provided to all four converters simultaneously. The address decoder, composed of the 74LS30, LS04s, LS11, and LS155, results in one of the four converters being read by the microprocessor, depending on which address (EB00 through EB03) is selected. It should be noted that the decoder shown in this example is incomplete, as address lines A7-A2 are not included. Each individual application will determine the need for more complete decoding.

Some variations of the circuit shown are:

1) Extend the decoder to include address line A2, and use one line of the other half of the LS155 (only the "A" half is shown) to provide the $\overline{S}$ pulse to the converters, eliminating the need for the PIA.
2) Use the other half of the LS155 to provide individual $\overline{S}$ pulses to each converter.

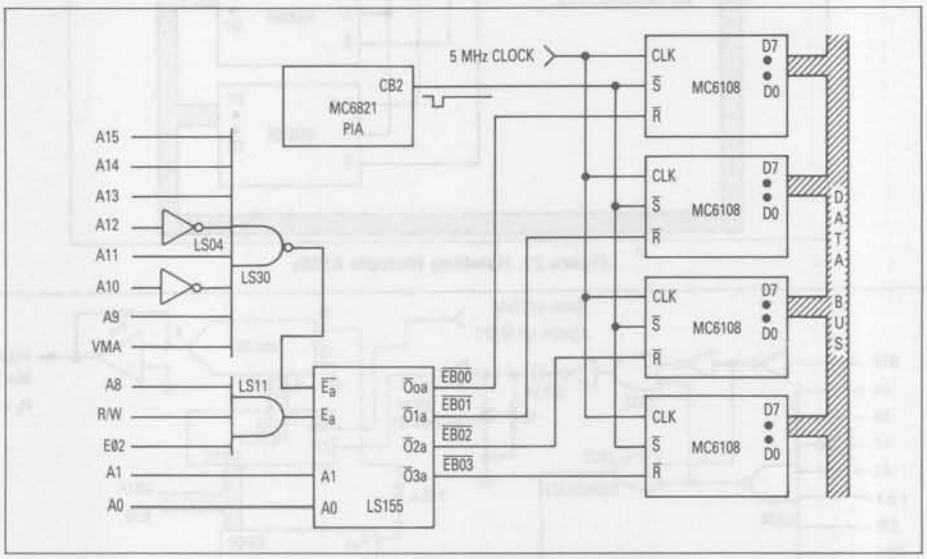

Figure 20. Handling Multiple MC6108s

Figure 21 illustrates an additional configuration for controlling several MC6108 A/D converters. In this case, the MC6821 PIA is used to both initiate the conversion, and read the data. The active low pulse at CB2 is provided to all the converters simultaneously. The selected MC6108 is then activated by bringing its $\overline{READ}$ pin low, by means of the appropriate line at the A port. The data is then read through the B port, and then the $\overline{READ}$ input is taken high. The remaining pins of each MC6108 are connected as shown in Figure 2.

Figure 22 illustrates the circuitry for reading in an analog signal, processing it according to the system requirements, and then producing an analog signal out by means of the DAC-08 D/A converter. The digital data to be converted to analog is stored in the 74LS273 octal latch when its CP input receives an active low pulse from the address decoder. In Figure 22, the latch is considered a "write only" location at address EB01. On the rising edge of the CP pulse, the data is transferred to the DAC-08 by means of the Q outputs. The output of the DAC is a current proportional to the reference current and the digital data presented to it. The op amp converts that current to an output voltage by means of the feedback resistor R_X (Max V_{out} = R_X x 2 mA).

The reference current for the DAC-08 is supplied from the MC6108's reference supply (V_{ref}). Settling time of the output voltage is approximately 1 μs with any of the currently available fast op amps, such as the MC34001 family, MC33070 family, MC34074 family, or the MC34080 family. The DAC-08 can be powered from the same +5 and −5.2 volt supplies used for the MC6108.

The MC6108 receives its Start command ($\overline{S}$ pulse) from an MC6821 PIA's CB2 output, as described in Example #1. Since the MC6108 can be considered a "Read Only" memory location, and the 74LS273 latch a "Write Only" location, they are placed at the same address (EB01 in Figure 22), but set to respond to Read and Write commands (LDAA and STAA for the MC6802 MPU). In Figure 22, the address decoder is the same as in Figure 4, except that the R/$\overline{W}$ line has been relocated. Reading the MC6108 is the same as in previous examples. When writing to the 74LS273 latch, the output pulse from the decoder (at the upper LS32 gate) is shortened to 300 ns to ensure that its rising edge occurs while data on the data bus is still valid.

CONCLUSION

The examples have shown that interfacing the MC6108 A/D converter to a microprocessor is a relatively simple process. The flexibility associated with the various control

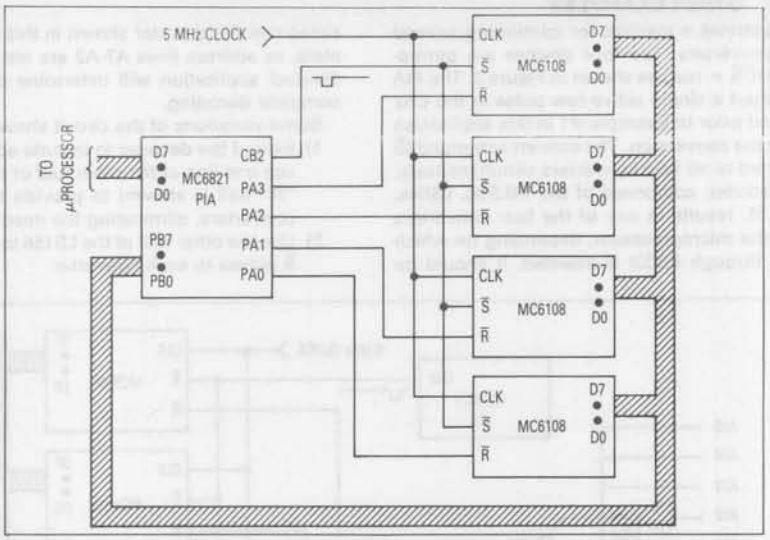

Figure 21. Handling Multiple 6108s

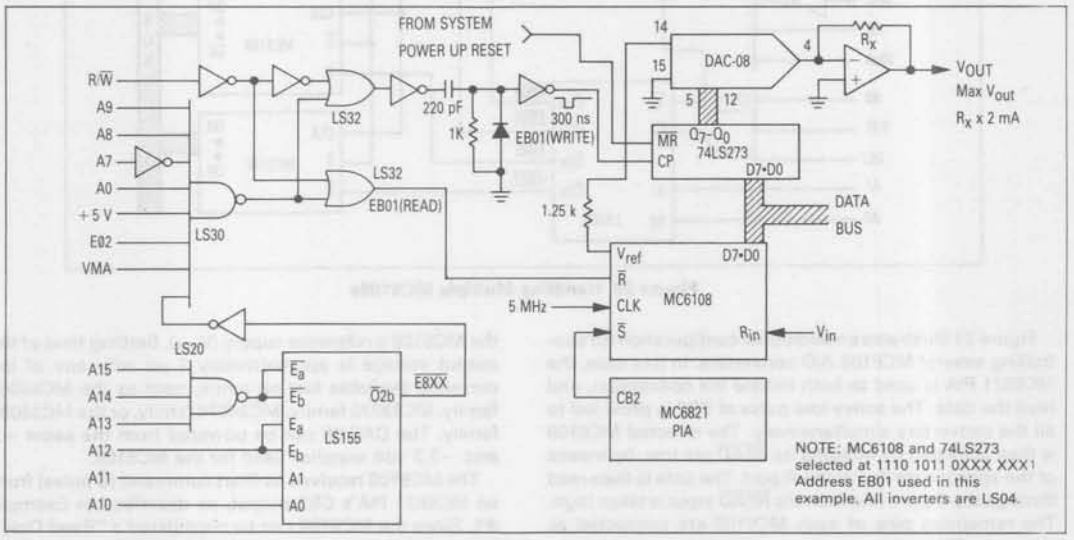

Figure 22. The MC6108 A/D and DAC-08 D/A

lines allow several combinations of a port and address decoder to be used for controlling the converter, and for reading the data.

The examples indicate there is an inverse relationship between the amount of hardware and the length of programming required. Each individual application will determine the right combination of the two.

The MC6108's high speed (1.8 μs) facilitates programming the system since interrupts and long wait states are generally not required. In most cases, the READ instruction can immediately follow the CONVERT instructions.

REFERENCES

— MC6108 Data Sheet, 1986
— MC6802 Data Sheet, 1979
— MC6821 Data Sheet, 1978
— DAC-08 Data Sheet, 1986