TEXAS INSTRUMENTS

DATA CONVERTERS

Analog Applications Journal

BRIEF

Operating multiple oversampling data converters

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1.1 Introduction

This article discusses some important considerations that should be taken into account during the design of a simultaneous sampling system using oversampling data converters. The ADS1252 ADC is used as an example.

To successfully use oversampling data converters in a simultaneous application, the modulator clock (MCLK) for each ADC must be shared. This assures that each converter is truly sampling the inputs concurrently. It has the added benefit of simplifying the digital interface since only one interrupt pin is required, regardless of the number of ADCs in the system.

However, a significant limitation is that there is a fixed amount of time—348 MCLK periods—available to read the converted data. After this fixed time, the data output register is being updated with a new data word regardless of whether the data has been read or not.

The converted data is read from the device using a shift-clock (SCLK) generated via the host system. There is no direct relationship between MCLK and SCLK, but the user should be aware that if the data is not shifted out of the ADC quickly enough T_{DOUT} time will expire and the data read back will be a meaningless mixture of old and new data. This should be carefully considered, particularly where multiple ADCs are concerned.

1.2 Oversampling catch

Oversampling data converters generally have better ac and dc specifications than Successive Approximation Register (SAR) based converters. But SARs do have one fundamental advantage, namely on command from the host, SAR converters are able to complete and deliver one measurement.

In comparison, oversampling architectures by their nature rely upon averaging repeated coarse measurements before arriving at a final value. The architecture details are beyond the scope of this paper, but it is essential to appreciate this point in order to successfully use oversampling converters.

2 Data transfer principles

The preliminary details in support of this application note are contained in the application note, Interfacing the ADS1251/52 to the MSP430, SLAA242. It is recommended that the reader should first read this application note to gain an understanding of the device's operation.

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2.1 Modulator clock (MCLK)

The modulator clock applied to the ADS1252 ADC is the principle driver used to set the characteristics of the ADC. The two properties that MCLK provide are the frequency response of the ADC and also the frequency at which the ADC indicates new data is available.

The modulator clock period (t_{MCLK}) is defined as

$$\tau_{MCLK} = \frac{1}{MCLK} \quad \text{Equation (1)}$$

2.2 Digital Interface

To briefly recap the operation of the digital interface from the datasheet, there is only one data output pin. The function of this pin is multiplexed between DOUT and DRDY. A complete conversion consumes 384 MCLK cycles. The cycle is divided into two phases (Figure 1).

The first phase of the cycle is known as DRDY mode. Following the T_{DOUT} time, the rising edge of the DOUT/DRDY signal indicates that new data will be available in 36 MCLKs. During this time, the data output register is updated. This signal is connected to an interrupt pin on the host system.

The second phase of 348 MCLKs is known as DOUT mode. During this time, the user can safely read the converted data at a clock rate determined by the shift clock (SCLK).

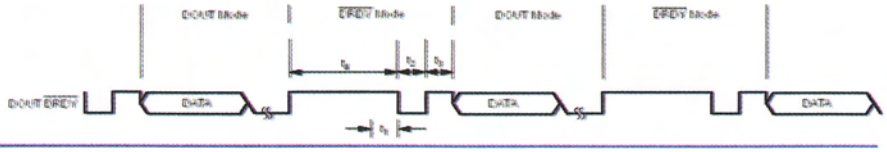

Figure 1

2.3 A tale of two clocks

Regardless of the number of ADCs, the same principle of DOUT/DRDY time must still be adhered to for the ADS1252. In general, for N data converters, the time allocated for DOUT mode can be expressed as:

$$T_{DOUT(N)} = \frac{348 * \tau_{MCLK}}{N} \text{ (s)} \quad \text{Equation (2)}$$

The maximum modulator clock (MCLK) for the ADS1252 is specified as 16MHz. Therefore t_{MCLK} is 62.5ns, and T_{DOUT} can be re-written as

$$T_{DOUT(N)} = \frac{21.75 \times 10^{-6}}{N} \text{ (s)} \quad \text{Equation (3)}$$

Figure 2 shows both SCLK signals and both DOUT/DRDY signals required to read data from two ADCs.

As the number of ADCs sharing the same modulator clock increases, the DRDY period stays the same, but the data from each ADC must be accessed faster.

To receive the complete 24 bits from each ADC requires 3 x 8-bit accesses, 24 SCLKs in total. Therefore to be able to access the data from N ADCs requires a time of N x 24 SCLKs. It is the user's responsibility to ensure that all accesses are complete prior to the next DRDY time.

An alternative approach would be to verify the maximum speed offered by the host system for SCLK, 2MHz for example, and then determine how long it would take to transfer 24 bits of data at that clock speed; this would determine the maximum modulator clock frequency that could be used. In a multiple ADC system, if the modulator clock is faster than the calculated maximum, there will not be enough time for the host to read the data before the ADC switches from DOUT mode to DRDY mode.

For example, if t_{SCLK} = 500ns then 24 x t_{SCLK} = 12µs for 24 bits of data. This indicates that it will take at least 12µs to clock the data out of any ADC (this sets T_{DOUT}), consequently if there are 5 ADCs sampling data synchronously, it will take at least 5 x 12µs (60µs) until the system can read the first ADC again.

Therefore, according to equation 2, the maximum modulator clock will be 5.8MHz.

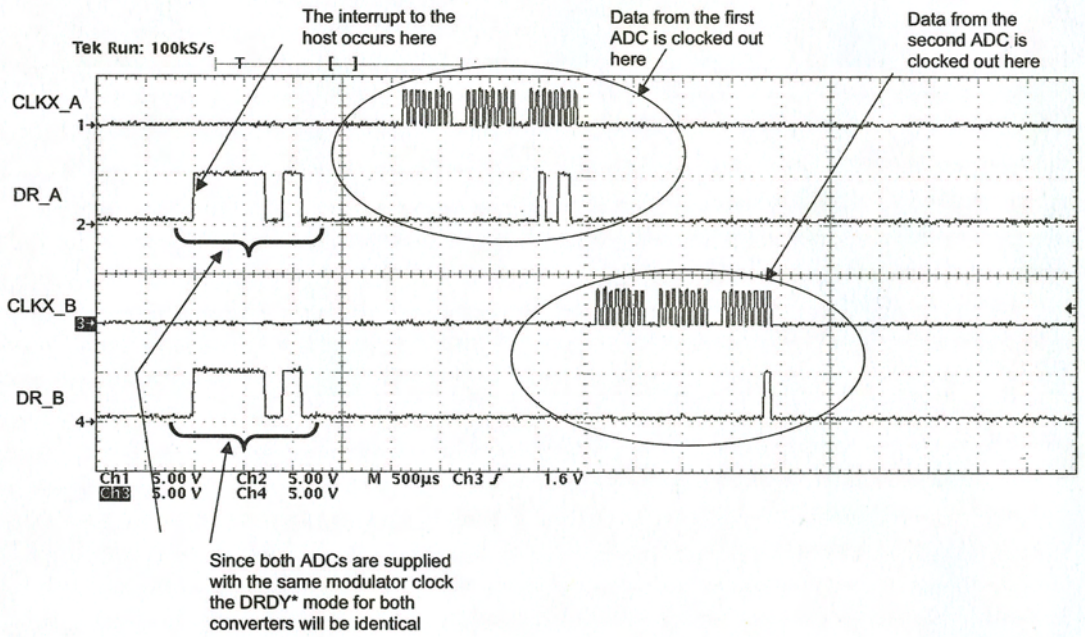

Figure 2– A composite from two adjacent screen captures showing CLKX_A, DR_A, CLKX_B and DR_B

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