RC-discharge clock makes a-d encoder logarithmic

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This analog-to-digital converter produces a 12-bit digital output that represents the natural logarithm of an input audio signal in the 1 -to- 1 ,OOO-millivolt (60-decibel) range. It is useful for monitoring slow changes in many natural processes. The circuit also may be adapted for use as a combination voice cornpander and encoder in a digital communications system.

Operation is based on the principle that the discharge rate of a voltage stored across a resistance-capacitance network is proportional to the logarithm of the ratio of the instantaneous to the initially applied voltage. When the voltage across the RC network is used to control the gating time of a counter, the counter's output is a binary-coded decimal number equal to ln Vi, where Vi is the input voltage.

The voltage across a discharging capacitor, V,, in an RC network is given by:

$$V_c = V_r e^{-t/RC}$$

where V_r is the initial voltage. This equation, when transposed, becomes:

$$t = -RC \ln(V_c/V_r)$$

Let t_i represent the time it takes the capacitor to discharge from V_r to the input voltage V_i. If during this time a down counter is gated while being clocked at frequency fc, the number of counts reached will be:

$$n_d = f_c t_i = -f_c RC \ln(V_i/V_r)$$

More generally, if the down counter is initially at a count of ni, then the net count n_n after time t_i will be:

$$n_n = n_i - n_d = n_i + f_c RC \ln(V_i/V_r)$$

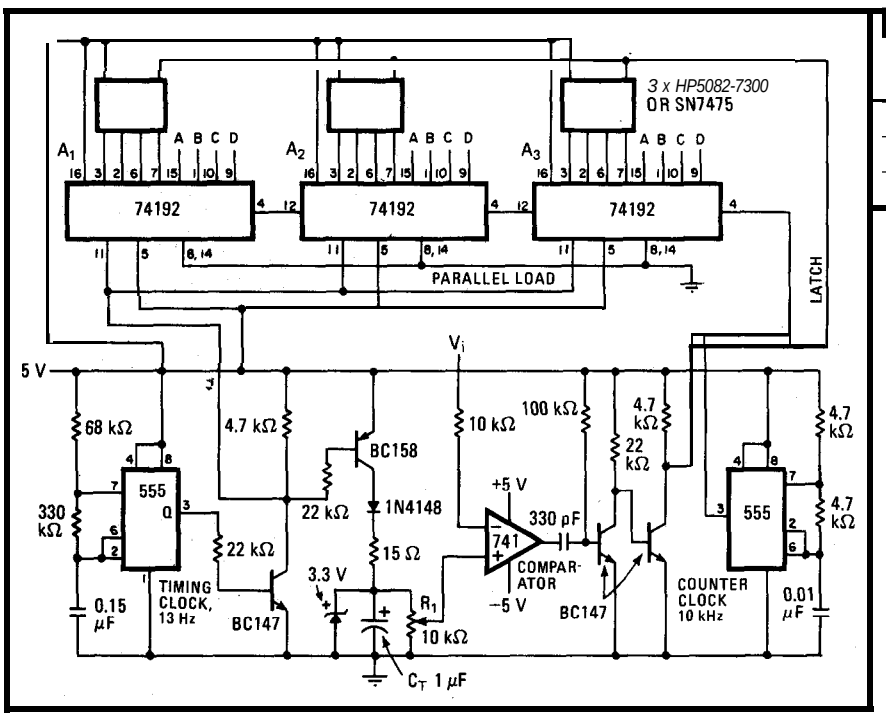
Letting V_r = 1,000 mv and n_i = 690, we arrive at:

$$n_n = 690 - 100 \ln 1000 + 100 \ln V_i = 100 \ln Vi$$

which can be reduced to $n_n = \ln Vi$ with appropriate scaling in a practical circuit.

The circuit shown in the figure implements the derived equation. When the output of the 555 timing clock is high, the 74192 up-down counter is loaded with the number 690 as shown in the table. At the same time, capacitor C_T is charged to 3.3 volts. R1 facilitates the scaling of this voltage so that the potential as seen at the noninverting input of the comparator is 1 v.

When the output of the timing clock moves low, the 74192 begins to count down at a lo-kilohertz rate and C_T begins to discharge. As the voltage at the noninverting input drops below the sample voltage, V_i, the



LOADING OF 74192 UP-DOWN COUNTER

COUNTER	NUMBER	CODING A	B	C	D
A_1	6	1	1	0	0
A_2	9	1	0	0	1
A_3	0	0	0	0	0

Natural processing. Circuit is logarithmic a-d converter and digital encoder in one. Voltage across C_T, which decays exponentially at start of each sampling cycle, controls gating time of 74192 counters, ensuring logarithmic response. Counters are preset to 690 before each encoding to eliminate constant-coefficient terms inherent in circuit's transfer function, so that output from counter is n = ln V,.

comparator output moves low and generates a latch pulse for the BCD-to-seven-segment displays, or 4-bit latches, as required. Thus the contents of the counter are stored in either the display or the latches. The sequence is then repeated. Note that a decimal point is located in the most significant display (corresponding to counter A,) so that the natural logarithm of a l,OOO-mv input signal will be correctly displayed as 6.90.

The low-frequency clock limits the input signal sampling rate to 13 hertz. However if the clock frequency is increased to 5 kHz or so, and the clock counter is replaced by one that can run at a few mega-hertz, the circuit will serve as an excellent speech encoder.