


# Precision integrator sparks current-ratio-to-frequency converter

Stefano Salvatori and Gennaro Conte,  
Università degli Studi di Roma Tre, Rome, Italy

 The Design Idea in **Figure 1** uses the  $S_1$  switch of the Texas Instruments ([www.ti.com](http://www.ti.com)) IVC102 precision integrator to select between a single input current or the superposition of two input currents. This function allows you to obtain an output signal whose characteristics directly relate to the ratio between the two input currents. The circuit achieves high accuracy independent of most of the system parameters. In addition, you can enhance accuracy if you let a digital counter control the IVC102-based circuit (**Figure 2**). In this case, the system's output is a number in the BCD (binary-coded-decimal) format proportional to the input-current ratio,

realizing a true digital conversion.

The circuit divides into two phases. The first phase begins when the output voltage of the IVC102 becomes slightly greater than the threshold voltage of the LM311 comparator. The comparator generates a falling-edge signal, and the 555 monostable starts a pulse, which closes  $S_1$ . In this case, the total input current,  $I_2 - I_1$ , generates a negative-going ramp if  $I_2$  is greater than  $I_1$ . In the delta-time period,  $\Delta T_A$ , the integrator's output voltage reaches the final voltage value. Hence,  $|V_{FIN} - V_{TH}| = (I_2 - I_1)\Delta T_A / C_{INT}$ , where  $C_{INT}$  is the value of the IVC102's integrating capacitor. When the 555 monostable's output pulse ends, the

second phase starts:  $S_1$  opens, and input current  $I_1$  discharges  $C_{INT}$ . The  $\Delta T_B$  for the output voltage to assume the threshold voltage's value is then  $C_{INT}|V_{FIN} - V_{TH}| / I_1$ , and the comparator generates a new trigger command to the monostable so that a new cycle can start. Manipulating the previous equations yields:  $I_1/I_2 = \Delta T_A f$ , where  $f = (\Delta T_A + \Delta T_B)^{-1}$ . This equation states that the generated output signal, a train of pulses, has a frequency,  $f$ , proportional to the  $I_1/I_2$  current ratio. The accuracy of the monostable directly affects the accuracy of the system. Conversely, the integrating capacitor's and threshold voltage's values do not influence the accuracy if they maintain constant values at least in the  $1/f$  time scale.

You can increase the accuracy of the circuit in **Figure 1** by modifying the section that generates the constant,  $\Delta T_A$ -wide pulse. The circuit in **Figure 2** generates a  $\Delta T_A$ -wide pulse using three

*(continued on pg 108)*

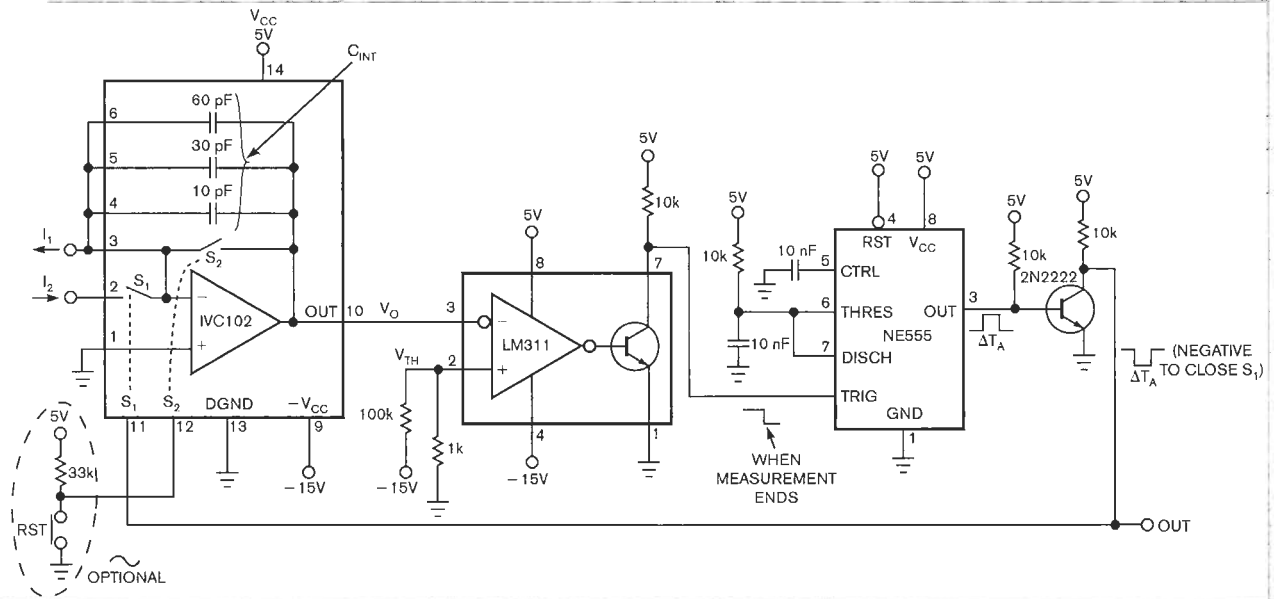


Figure 1 This circuit allows you to obtain an output-signal frequency that directly relates to the ratio between the two input currents.

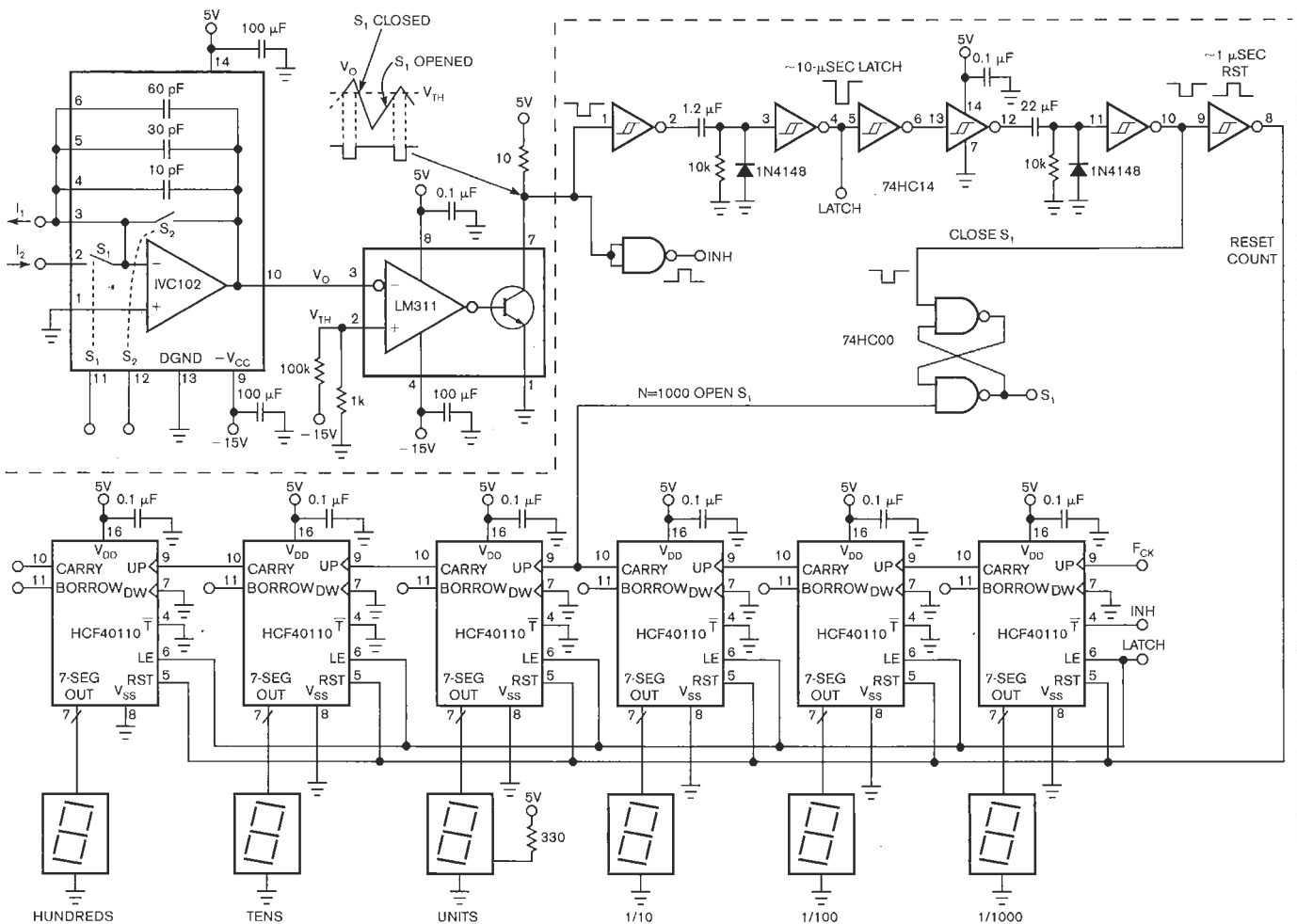


Figure 2 To the circuit in Figure 1, this design adds a BCD counter to obtain direct readouts on seven-segment LED displays.

(continued from pg 104)

HCF40110 BCD counters. When the third counter generates a carry,  $1000/f_{CK}$  seconds have elapsed. In **Figure 2**, a set/reset flip-flop controls  $S_1$ 's state, and the 74HC14 hex inverter with a Schmitt-trigger input generates the pulses that reinitialize the system. A brief description of the measurement cycle follows. When the IVC102's output voltage becomes greater than the threshold voltage, the INH (inhibit) signal connected to the toggle input of

the first HCF40110 inhibits counting. At the same time, the negative-going edge of the comparator output generates a negative-going pulse of approximately  $10 \mu\text{sec}$ , which latches the counters' values at the output to display the actual result. After this step, a negative-going pulse sets the SR flip-flop to close  $S_1$ . A corresponding positive-going pulse resets the counters. The latch-enable lines of the 40110s are tied high, so the counters' reset doesn't affect the displayed value. When the reset pulse

ends and the comparator's output goes high, the HCF40110s can count up. When the third counter generates a carry (negative-going pulse), the 1000th clock period has elapsed, and the SR flip-flop resets to open  $S_1$ . The cycle ends at the next falling edge of the comparator's output. The time period in which  $I_2 - I_1$  charges  $C_{INT}$  is  $N_A/f_{CK}$  ( $N_A = 1000$ ), and the  $I_1$  requires for discharging is  $N_B/f_{CK}$ . Manipulating the integrator-related relationships yields  $I_2/I_1 = N/N_A$ , where  $N = N_A + N_B$ . **EDN**