Some Techniques for Direct Digitization of Transducer Outputs

Jim Williams

Almost all transducers produce low level signals. Normally, high accuracy signal conditioning amplifiers are used to boost these outputs to levels which can easily drive cables, additional circuitry, or data converters. This practice raises the signal processing range well above the error floor, permitting high resolution over a wide dynamic range.

Some emerging trends in transducer-based systems are causing the use of signal conditioning amplifiers to be re-evaluated. While these amplifiers will always be useful, their utilization may not be as universal as it once was. In particular, many industrial transducer-fed systems are employing digital transmission of signals to eliminate noise-induced inaccuracies in long cable runs. Additionally, the increasing digital content of systems, along with pressures on board space and cost, make it desirable to digitize transducer outputs as far forward in the signal chain as possible. These trends point toward direct digitization of transducer outputs—a difficult task.

Classical A→D conversion techniques emphasize high level input ranges. This allows LSB step size to be as large as possible, minimizing offset and noise caused errors. For this reason, A→D LSB size is almost always above a millivolt, with 100μV–200μV per LSB available in a few 10V full-scale devices. The requirements to directly A→D convert the output of a typical strain gauge transducer are illuminating. The transducer's full-scale output is 30mV, meaning a 10-bit A→D converter must have an LSB increment of only 30μV. Performing a 10-bit conversion on a type K thermocouple monitoring a 0°C–60°C environment proves even more stringent. The type K thermocouple puts out 41.4μV/°C over the 0°C–60°C range. The LSB increment is found by:

$$\frac{60°C \times 41.4\mu V/°C}{1024} = 2.42\mu V/LSB$$

These examples furnish extraordinarily small step sizes, far below commercially available A→D units and seemingly impossible to digitize without DC preamplification. In fact, both transducers' outputs may be directly digitized to stable 10-bit resolution using circuitry specifically designed for the function.

This application note details circuit techniques which directly digitize the low level outputs of a variety of transducers. The approaches described are unique in that they do not utilize any DC gain stage. The transducer outputs receive no DC signal conditioning: A→D conversion is directly performed at low level. The circuits produce a serial data output which may be transmitted over a single wire with the characteristic noise immunity of digital systems. By eliminating the traditional DC gain stage, these circuits furnish a direct, economical way to digitize low level transducer outputs without sacrificing performance.

Figure 1 shows a simple way to convert the current output of an LM334 temperature sensor to a corresponding output frequency. The sensor pulls a temperature-dependent current (0.33%/°C) from A1's positive input node. This point, biased from the LM329-driven resistor string, responds with a varying, temperature-dependent voltage. The voltage varies the operating point of A1, configured as a self-resetting integrator. A1 integrates the LM329 referenced current into its summing point, producing a negative-going ramp at its output. When the ramp amplitude becomes large enough, the transistors turn on, resetting the feedback capacitor and forcing A1's output to zero. When the capacitor's reset current goes to zero, the transistors go off and A1 begins to integrate negatively again. The frequency of this oscillation action is dependent on A1's DC operating point, which varies with the LM334's temperature. The circuit's DC biasing values are arranged so that a 0°C to 100°C sensor temperature excursion produces 0kHz-to-1kHz at the output. Additionally, only 2V appear across the LM334, minimizing sensor power dissipation related errors. The differentiator-transistor network at A1's output provides a TTL compatible output. To calibrate this circuit, place the LM334 in a 0°C environment and trim the "0°C adjust" for 0Hz. Next, put the LM334 in a 100°C environment and set the "100°C adjust" for 1kHz output. Repeat this procedure until both points are fixed. This circuit has a stable 0.1°C resolution with ±1.0°C accuracy.

Figure 2 shows another temperature-to-frequency converter, but this circuit uses the popular type K thermocouple as a sensor. The design includes cold junction compensation for the thermocouple over a 0°C–60°C range. Accuracy is ±1°C and resolution is 0.1°C.

The thermocouple's extremely low output (41.4μV/°C) and the requirement for cold junction compensation make it one of the most difficult transducers to directly digitize. The approach used is based on the 50nV/°C input offset drift performance of the LTC1052 chopper-stabilized amplifier.

In this circuit, A1's positive input is biased by the thermocouple. A1's output drives a crude V→F converter, comprised of the 74C04 inverters and associated components. Each V→F output pulse causes a fixed quantity of charge to be dispensed into the 1μF capacitor from the 100pF capacitor via the LTC1043 switch. The larger capacitor integrates the packets of charge, producing a DC voltage at A1's negative input. A1's output forces the V→F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action

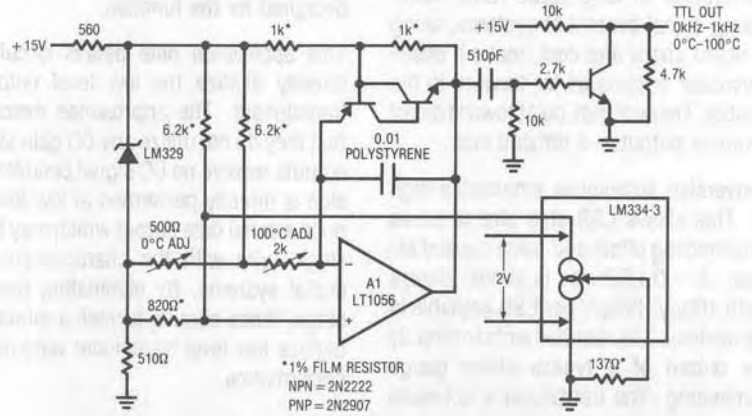

Figure 1. Temperature-to-Frequency Converter

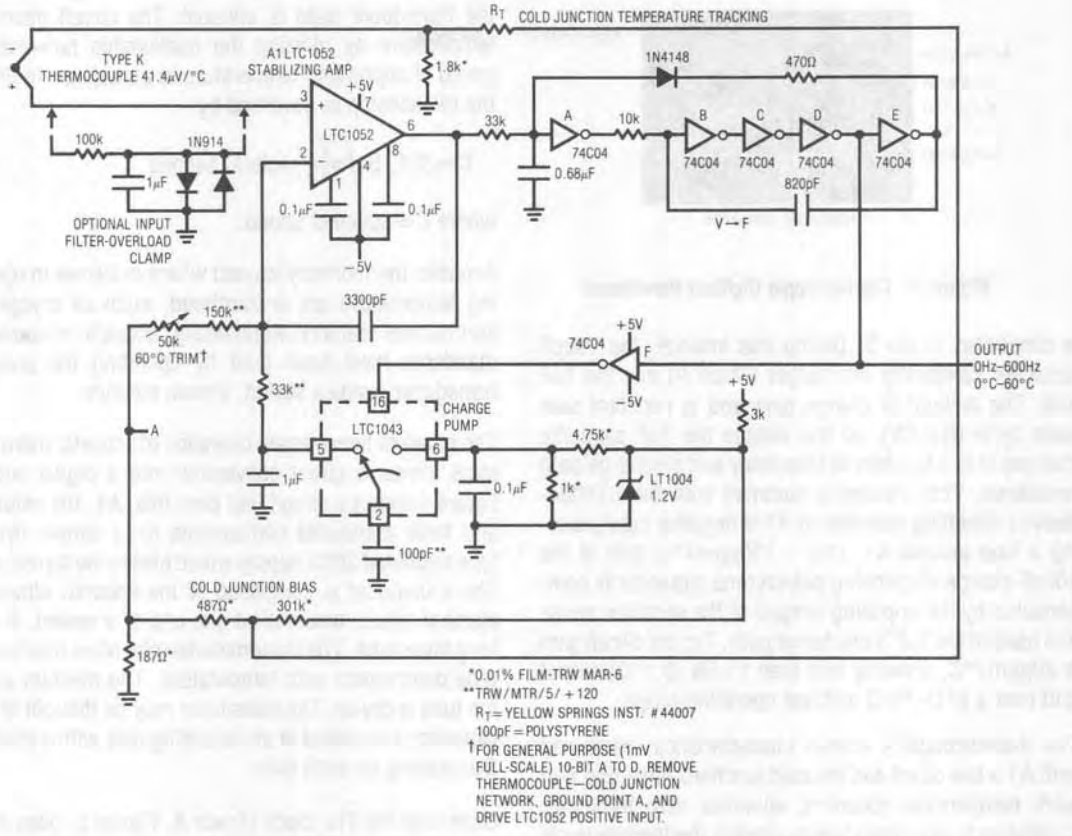

Figure 2. Thermocouple-to-Frequency Converter

eliminates drift and nonlinearities in the V→F converter as an error term and the output frequency is solely a function of the DC conditions at A1's inputs. The 3300pF capacitor forms a dominant response pole at A1, stabilizing the loop.

A1's low drift eliminates offset errors in the circuit, despite an LSB value of only 4.14μV(0.1°C)!

R_T, a thermistor, and the 1.8k, 187Ω, 487Ω and 301k values form a cold junction compensation network which is biased from the LT1004 1.2V reference. In addition to cold junction compensation, the network provides offsetting, permitting a 0°C sensor temperature to yield 0Hz at the output.

Figure 3 details circuit operation. A1's output drives the 33k-0.68μF combination, producing a ramp (Trace A, Figure 3) across the capacitor. When the ramp crosses inverter A's threshold, the cascaded inverter chain switches, producing a low output at E (Trace B). This causes the 0.68μF capacitor to discharge through the diode, resetting the capacitor to 0V. The 820pF unit provides positive AC feedback to inverter B's input (Trace C), assuring a clean reset. The frequency of this ramp-and-reset sequence varies with A1's output. Inverter F's output controls the LTC1043 switch. When the inverter output is high, pins 2 and 6 are connected, allowing the 100pF capacitor to charge to a potential derived from the LT1004 1.2V reference. When the inverter goes low, pin 2

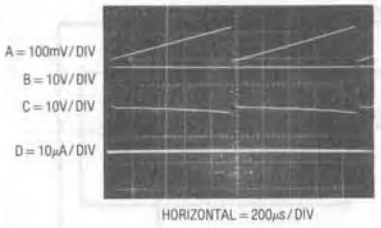

Figure 3. Thermocouple Digitizer Waveforms

is connected to pin 5. During this interval, the 100pF capacitor completely discharges (Trace D) into the 1μF unit. The amount of charge delivered is constant over each cycle (Q = CV), so the voltage the 1μF capacitor charges to is a function of frequency and discharge path resistance. This voltage is summed with the LT1004-derived offsetting potential at A1's negative input, closing a loop around A1. The −120ppm/°C drift of the 100pF charge-dispensing polystyrene capacitor is compensated by the opposing tempco of the specified resistors used in the 1μF's discharge path. Typical circuit gain is 20ppm/°C, allowing less than 1 LSB (0.1°C) output drift over a 0°C–70°C ambient operating range.

The thermocouple's known characteristics, combined with A1's low offset and the cold junction/offsetting network components specified, eliminate zero trimming. Calibration is accomplished by placing the thermocouple in a 60°C environment and adjusting the 50kΩ potentiometer for a 600Hz output. Beyond 60°C the cold junction network departs from the thermocouple's response and output error increases rapidly. Although the digital output will be a function of the thermocouple's temperature over hundreds of degrees, linearization by a monitoring processor is required.

It is worth noting that this circuit can directly convert any low level, single-ended signal. If the offsetting/cold junction network is removed and the 50kΩ potentiometer returned directly to ground, inputs may be applied to A1's positive terminal. The circuit produces a 10-bit accurate output with a full-scale range of only 1mV (1μV per LSB)! The high impedance of A1's input allows filtering or overload clamping of the input signal without introducing error.

Figure 4 is another temperature measuring circuit, but the transducer used is unusual. The circuit measures temperature by utilizing the relationship between the speed of sound and temperature in a medium. In dry air the relationship is governed by:

$$C = 331,5\sqrt{\frac{T}{273}} \text{ meters/second}$$

where C = speed of sound.

Acoustic thermometry is used where extremes in operating temperature are encountered, such as cryogenics and nuclear reactors. Additionally, acoustic temperature standards have been built by operating the acoustic transducer inside a sealed, known medium.

The inherent time domain operation of acoustic thermometers allows a direct conversion into a digital output. Figure 4 shows a circuit that does this. A1, the inductor, and their associated components for a simple flyback type regulated 200V supply which biases the transducer. The transducer is composed of the Polaroid ultrasonic element noted, mounted at one end of a sealed, 6 inch long Invar tube. The Invar material minimizes mechanical tube deformation with temperature. The medium inside the tube is dry air. The transducer may be thought of as a capacitor, composed of an insulating disc with a conductive coating on each side.

Each time the TTL clock (Trace A, Figure 5) goes high, the transducer receives AC drive via the 0.22μF capacitor. This drive causes mechanical movement of the disc and ultrasonic energy is emitted. The clock input simultaneously sets the 74C74 flip-flop output (Trace E) low and pulls the 0.01μF capacitor to ground. This cuts off drive to C1's 3kΩ output pull-up resistor (Trace C), forcing C1's output (Trace D) to zero. During the clock pulse's period, A2's output (Trace B) is saturated due to excessive signal at its input. When the clock pulse ceases, A2 comes out of bound and amplifies in its linear region. The ultrasonic transducer now acts like a capacitance microphone, with the 200V supply providing bias. Residual disc ringing is picked up and appears at A2's output. This signal cannot trigger C1, however, because the 0.01μF capacitor has not charged high enough to allow the inverter chain output to bias C1's output pull-up resistor.

The ultrasonic energy emitted by the transducer travels down the tube, bounces off the far end and heads toward the transducer. Before it returns, the 0.01μF capacitor crosses the inverter's threshold and C1's 3k resistor (Trace C) receives bias. Upon returning, the sonic energy causes a mechanical displacement of the transducer, forcing a shift in capacitance. This capacitance shift causes charge to be displaced into C2's summing point, and the output responds with an amplified version of this signal (Trace B). C1's output (Trace D) triggers, resetting the flip-flop. The flip-flop's output pulse (Trace E) represents the transit time down the tube and will vary with temperature according to the equation given. A monitoring processor can convert this pulse width into the desired temperature information.

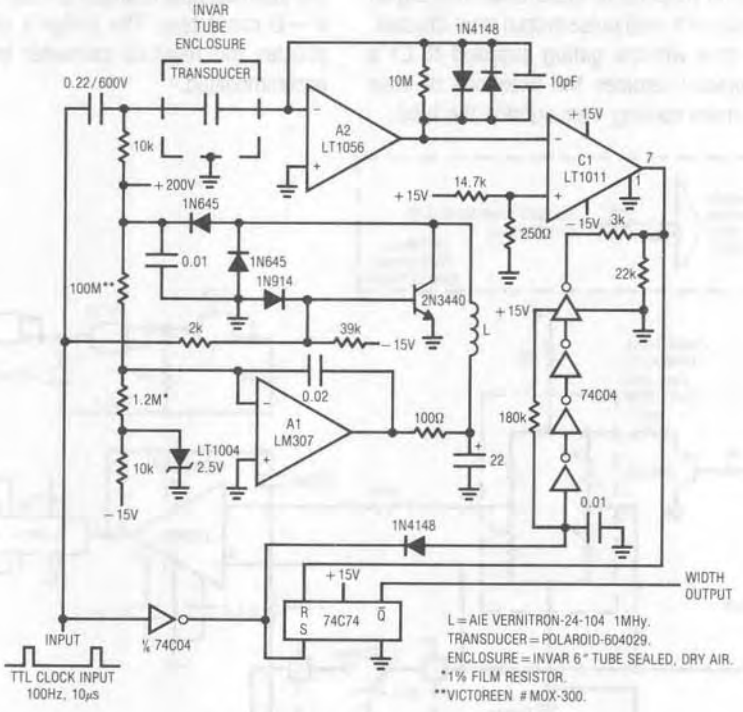

Figure 4. Acoustic Thermometer

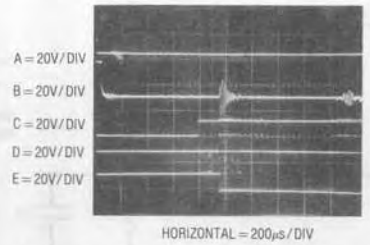

Figure 5. Acoustic Thermometer Waveforms

In the photograph another received signal, lower in amplitude, is visible at the extreme right hand side of Trace B. Its position in time identifies it as a second bounce return from the tube's far end. Also, note the increased detected noise level after the return of the first bounce. This is due to sonic energy dispersion inside the tube. The transducer picks up energy deflected from the tube walls, which is phase shifted from the desired signal. C1 is seen to respond to these unwanted signal sources, but the circuit's final pulse output is unaffected. Additionally, the time window gating supplied to C1's pull-up resistor greatly reduces the likelihood of false triggering due to noise coming from outside the tube.

Temperature sensors are not the only transducers which can be directly digitized. Strain gauge transducers account for a large class of pressure and force measurements. Typically, a strain gauge bridge-based transducer produces 3mV of full-scale output per volt of bridge drive. Figure 6 shows a way to directly digitize a strain gauge bridge's output to 10-bit accuracy. For a 7.5V bridge drive, an LSB increment is 25μV, considerably larger than the thermocouple example but still far below conventional A→D converters. The bridge's differential output complicates the required converter input structure, but is accommodated.

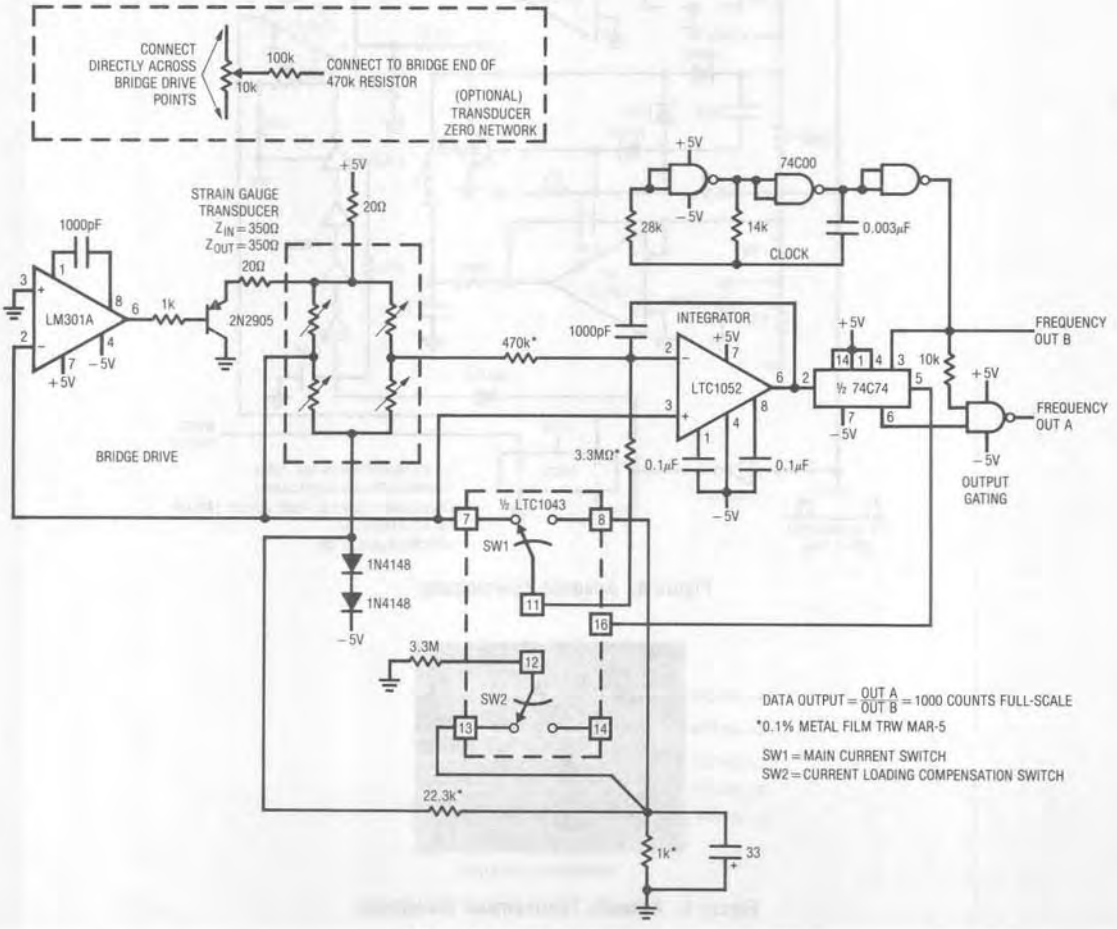

Figure 6. Strain Gauge Digitizer

A1 and the transistor provide bridge excitation. One signal output of the bridge is connected to A1's negative input. A1's positive input is at ground. A1 drives the transistor to bias the bridge at whatever voltage is required to bring its negative input to ground potential. The diode drops in the bridge's −5V return line allow the transistor to force the bridge's positive end far enough to servo A1's inputs. This arrangement allows the bridge's other output to be sensed in a single-ended, ground-referred fashion. In practice, a slight error exists due to A1's offset voltage. This error is eliminated by referring the A→D converter input to A1's negative input instead of ground.

The A→D converter is made up of A2, a flip-flop and some gates. It is based on a current balancing technique. Once again, the chopper-stabilized LTC7652's 50nV/°C input drift is required to implement the low level input A→D . Figure 7 details key A→D waveforms. Assume the flip-flop's Q output (Trace B) is low, connecting LTC1043 pins 11 and 12 to pins 7 and 13, respectively. The main current switch passes no current, as the 3.3MΩ resistor is placed across A2's inputs. The current loading compensation switch puts a 3.3MΩ value across the 1k divider resistor, lowering the voltage across it by 0.03%.

Under these conditions the only current into A2's summing point is from the bridge via the 470kΩ resistor. This positive current forces A2's output (Trace A, Figure 7) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (clock is Trace C), the flip-flop changes state (Trace B), causing the LTC1043 switch positions to reverse. Pin 12 connects to pin 14 and pin 11 to pin 8. In this case, the 3.3MΩ resistor controlled by the current loading compensation switch is disconnected from the 1k unit, but the 3.3MΩ value controlled by the main current switch replaces it. The 0.03% loading of the 3.3MΩ resistor, combined with this switching scheme, eliminate any sag or loading effects across the 1kΩ resistor during switching. The result is a quickly rising, precise current flow out of A2's summing point.

This current, scaled to be greater than the bridge's maximum output, forces A2's output movement to reverse and integrate in the positive direction. At the first clock pulse after A2's output has crossed the flip-flop's triggering threshold, switching occurs and the entire cycle repeats. Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the bridge signal current into A2's summing point. Additionally, the reference current is supplied from the 22.3k-1k divider, which is derived from the bridge drive. Thus, the A→D's reference current varies ratiometrically with the bridge output, eliminating bridge drive variations as an error source. The flip-flop's output gates the clock, producing the "frequency output A" waveform (Trace D). The 10k resistor combines with the output gate's input capacitance to slightly delay the clock signal, eliminating spurious output pulses due to flip-flop delay. The circuit's data output, the ratio of output A to the clock frequency, may be extracted with counters. Because the output is expressed as a ratio, clock frequency stability is unimportant.

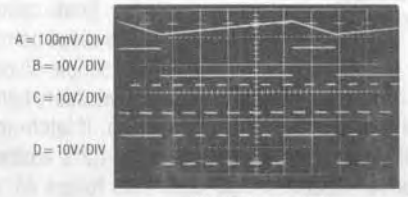

Figure 7. Strain Gauge Digitizer Waveforms

Several subtle factors are critical in setting up and using this circuit. The 470kΩ input resistor at A2 has been selected to produce less than 1 LSB loading error on the strain gauge bridge. The bridge receives only about 7.5V of drive due to the deliberate resistor and diode drops in its supply lines. At 3mV output per volt of bridge drive, full-scale signal is 22.5mV. This produces a signal current of only:

$$I = \frac{0.0225V}{470k} = 48nA.$$

To maintain 10-bit accuracy, leakage and amplifier bias current into A2's summing point must be less than 0.1% of this figure or:

$$I = \frac{48nA}{1000} = 48pA.$$

Although A2's bias current is much lower than this, board leakage can cause trouble. At a minimum, careful layout and a clean PC board are required. The best practice is to use a teflon stand-off for all summing point connections. The 470kΩ and 3.3MΩ resistors associated with A2's negative input should be placed as close as possible to the IC pin. Note also that the 3.3MΩ current summing resistor is switched to A2's positive input when it is not sourcing current to the summing point. This seemingly unnecessary connection prevents minute stray 60Hz and noise currents from being coupled to A2's summing point when the current reference is off. Failure to utilize this connection will cause jitter in the LSB. Gain trimming of this circuit may be accomplished by varying the 22.3k value. If the particular strain gauge transducer used requires zero trimming, use the optional network shown. Over a 0°C–70°C range the circuit will typically maintain its 10-bit output within 1 LSB accuracy. The tracking errors of the starred resistors are the primary contributors to this small error.

Because of their extremely wide dynamic range, photo diodes present a difficult challenge for signal conditioning circuitry. A high quality device furnishes a linear current output over a 100dB range, requiring a 17-bit A→D converter as well as a current-to-voltage input amplifier. A common approach employs a logarithmically responding current-to-voltage input amplifier to nonlinearly compress the photodiode's output, allowing a much lower resolution A→D converter to be used. Although this scheme saves the cost of the 17-bit A→D, it has the inconvenience of a nonlinear output. Also, logarithmic amplifiers respond relatively slowly, which may be detrimental in some photometric measurements. Figure 8's circuit directly converts a photodiode's current output into an output frequency with 100dB of dynamic range. Optical input power of 20nW–2mW produces a linear, calibrated 20Hz-to-2MHz output. Output response to input light steps is fast and cost is low.

The photodiode's output current feeds a highly modified, high frequency version of a Pease type charge pump I→F converter. Diode output current biases A1's negative input, causing its output (Trace A, Figure 9) to ramp in a negative direction. When A1's output crosses zero, C1's output (Trace B) goes low, causing the LT1009 diode bridge to bound at −3.7V. The 200pF-1.8k lead network at C1's positive input aids comparator high frequency response. C1's output going low also provides AC positive feedback to its positive input (Trace D). Additional AC positive feedback is supplied by output transistor Q3's collector (Trace C). During this interval, charge is pulled from A1's summing point via the 47pF-5pF capacitors (Trace E). This causes A1's output to move quickly positive, switching C1 after the positive feedback around it has decayed. The LT1009 diode bridge now bounds at +3.7V. The 47pF-5pF pair receives charge, A2's summing junction recovers and the entire cycle repeats at a frequency linearly related to photodiode output current. D1 and D2 compensate the bridge diodes. Diode connected Q1 compensates steering diode Q2. The diode connected transistors provide lower leakage than simple diodes. C2 provides circuit latch-up protection, necessary because of the circuit's AC coupled feedback loop. If latch-up occurs, A1's output saturates low, causing C2's emitter-follower connected output to go high. This forces A1's output positive, initiating normal circuit action.

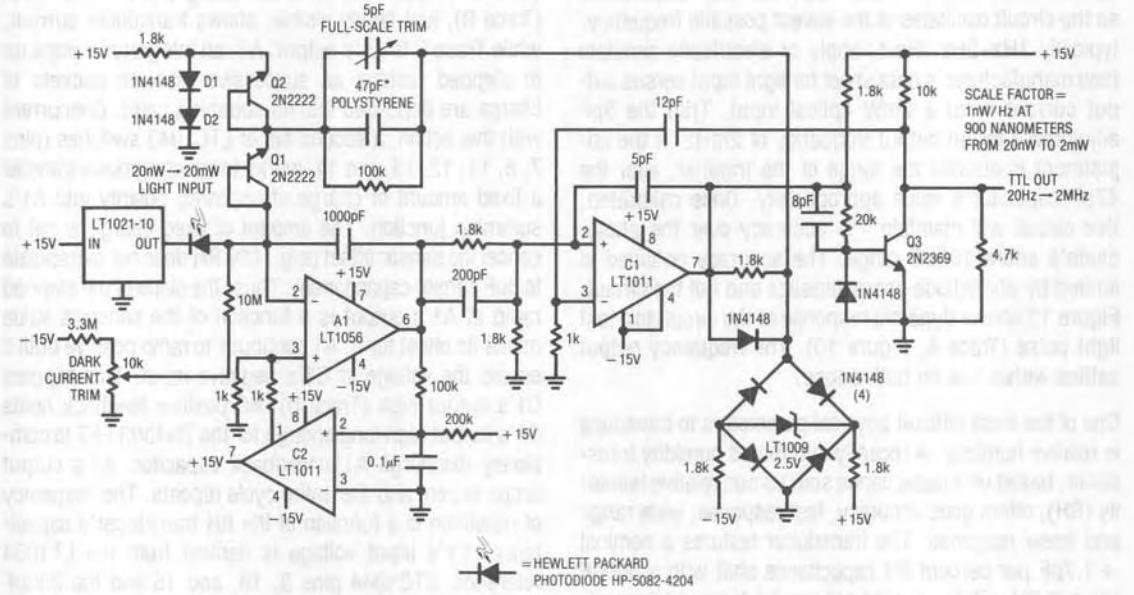

Figure 8. Photodiode Digitizer

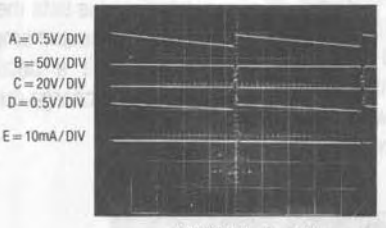

Figure 9. Photodiode Digitizer Waveforms

The LT1021-10 reference biases the photodiode, providing optimum optical current response characteristics. To trim this circuit, place the photodiode in a *completely* dark environment. Trim the "dark current" adjustment so the circuit oscillates at the lowest possible frequency, typically 1Hz–2Hz. Next, apply or electrically simulate (see manufacturer's data sheet for light input versus output current data) a 2mW optical input. Trim the 5pF adjustment for an output frequency of 2MHz. If the adjustment is outside the range of the trimmer, alter the 47pF capacitor's value appropriately. Once calibrated, this circuit will maintain 1% accuracy over the photodiode's entire 100dB range. The accuracy obtained is limited by photodiode characteristics and not the circuit. Figure 10 shows dynamic response of the circuit to a fast light pulse (Trace A, Figure 10). The frequency output settles within 1μs on both edges.

One of the most difficult physical parameters to transduce is relative humidity. A recently introduced humidity transducer, based on a capacitance shift versus relative humidity (RH), offers good accuracy, fast response, wide range and linear response. The transducer features a nominal +1.7pF per percent RH capacitance shift with a 500pF value at RH = 76%. It does not require temperature compensation. A significant consideration in signal conditioning this transducer is that the average voltage across the device must be zero. No net DC may pass through the transducer. Figure 11's circuit converts the RH transducer's capacitive shifts directly into a calibrated frequency output. The LTC1043 switched-capacitor instrumentation building block IC free runs at 150kHz. Pin 2 (Figure 12, Trace A) is alternately connected between the LT1004 negative reference and A1's summing junction. The 1μF-22MΩ combination associated with the RH transducer ensures the device's required pure AC biasing.

When pin 2 is connected to pin 6, the transducer receives a negative charge. When the LTC1043's internal clock switches, pin 2 is tied to pin 5, depositing all of the transducer's charge into A1's summing point. A1's input (Trace B), just faintly visible, shows transducer current, while Trace C is A1's output. A1, an integrator, ramps up in stepped fashion as successive discrete packets of charge are deposited into its summing point. Concurrent with this action, a second set of LTC1043 switches (pins 7, 8, 11, 12, 13, and 14) works to synchronously transfer a fixed amount of charge of opposing polarity into A1's summing junction. The amount of fixed charge is set to cancel the sensor offset (e.g., 0% RH does not extrapolate to 0pF sensor capacitance). Thus, the slope of the stepped ramp at A1's output is a function of the sensor's value minus its offset term. A1 continues to ramp positive until it equals the voltage at C1's negative input. This triggers C1's output high (Trace D). AC positive feedback holds C1's output high long enough for the 2N4393 FET to completely discharge A1's feedback capacitor. A1's output drops to zero and the entire cycle repeats. The frequency of repetition is a function of the RH transducer's capacitance. C1's input voltage is derived from the LT1004 reference. LTC1044 pins 3, 18, and 15 and the 330pF value form a simple charge pump which biases A2's summing point. A2's output assumes whatever value is required to maintain its summing point at zero. The 0.22μF capacitor integrates A2's response to DC, while the feedback resistors establish the operating point. Because A2's output voltage determines ramp height, its feedback resistor's value sets the circuit's gain slope. Traces E, F, and G and time and amplitude expansions of Traces A, B, and C permit a detailed look at the effects of the transducer's charge dumping on A1's output ramp.

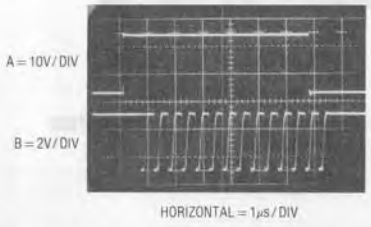

Figure 10. Step Response of Photodiode Digitizer

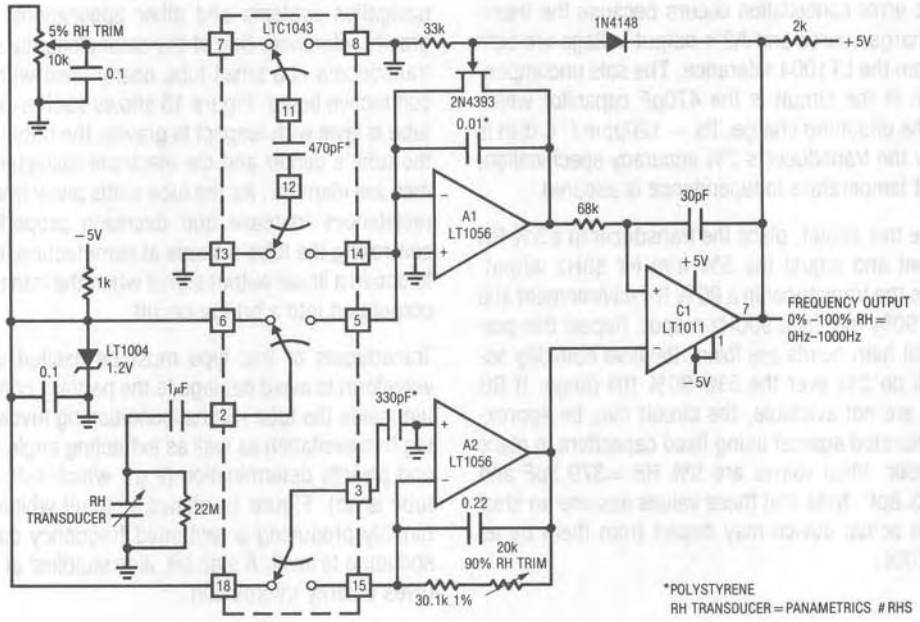

Figure 11. Humidity-to-Frequency Converter

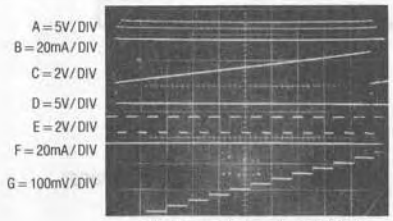

Figure 12. Humidity → Frequency Converter Waveforms

Circuit temperature dependence is low because the 330pF and 0.01μF polystyrene capacitors' (both gain terms) −120ppm drifts ratiometrically cancel. Further ratiometric error cancellation occurs because the transducer's charge source and A2's output voltage are both derived from the LT1004 reference. The sole uncompensated term in the circuit is the 470pF capacitor which supplies the offsetting charge. Its −120ppm/°C drift is well below the transducer's 2% accuracy specification, and circuit temperature independence is assured.

To calibrate this circuit, place the transducer in a 5% RH environment and adjust the 5% trim for 50Hz output. Next, place the transducer in a 90% RH environment and adjust the 90% trim for a 900Hz output. Repeat this procedure until both points are fixed. Relative humidity accuracy will be 2% over the 5%–90% RH range. If RH standards are not available, the circuit may be approximately calibrated against using fixed capacitors in place of the sensor. Ideal values are 5% RH = 379.3pF and 90% = 523.8pF. Note that these values assume an ideal sensor. An actual device may depart from them by as much as 10%.

Another frequently required physical parameter is level. Level transducers which measure angle from ideal level are employed in road construction, machine tools, inertial navigation systems and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. Figure 13 shows such a device. If the tube is level with respect to gravity, the bubble resides in the tube's center and the electrode resistances to common are identical. As the tube shifts away from level, the resistances increase and decrease proportionally. By controlling the tube's shape at manufacture it is possible to obtain a linear output signal when the transducer is incorporated into a bridge circuit.

Transducers of this type must be excited with an AC waveform to avoid damage to the partially conductive liquid inside the tube. Signal conditioning involves generat ing this excitation as well as extracting angle information and polarity determination (e.g., which side of level the tube is on). Figure 14 shows a circuit which does this, directly producing a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

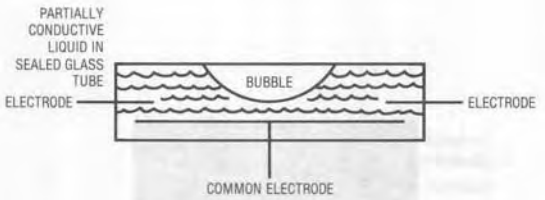

Figure 13. Bubble Based Level Transducer

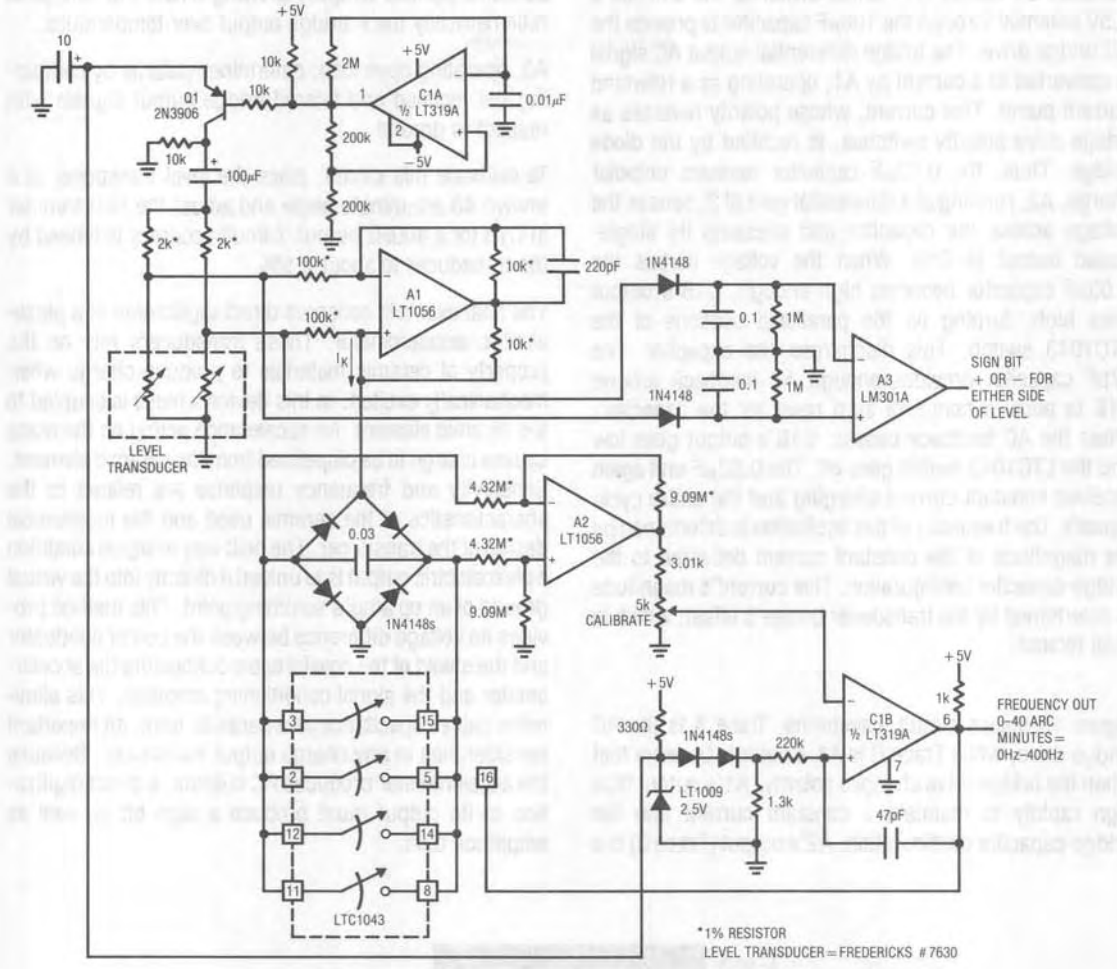

Figure 14. Level Transducer Digitizer

The level transducer is configured with a pair of 2kΩ resistors to form a bridge. The required AC bridge excitation is developed at C1A, which is configured as a multivibrator. C1 biases Q1, which switches the LT1009's 2.5V potential through the 100μF capacitor to provide the AC bridge drive. The bridge differential output AC signal is converted to a current by A1, operating as a Howland current pump. This current, whose polarity reverses as bridge drive polarity switches, is rectified by the diode bridge. Thus, the 0.03μF capacitor receives unipolar charge. A2, running at a differential gain of 2, senses the voltage across the capacitor and presents its single-ended output to C1B. When the voltage across the 0.03μF capacitor becomes high enough, C1B's output goes high, turning on the paralleled sections of the LTC1043 switch. This discharges the capacitor. The 47pF capacitor provides enough AC feedback around C1B to allow a complete zero reset for the capacitor. When the AC feedback ceases, C1B's output goes low and the LTC1043 switch goes off. The 0.03μF unit again receives constant current charging and the entire cycle repeats. The frequency of this oscillation is determined by the magnitude of the constant current delivered to the bridge-capacitor configuration. This current's magnitude is determined by the transducer bridge's offset, which is level related.

Figure 15 shows circuit waveforms. Trace A is the AC bridge drive, while Trace B is A1's output. Observe that when the bridge drive changes polarity, A1's output flips sign rapidly to maintain a constant current into the bridge-capacitor configuration. A2's output (Trace C) is a unipolar, ground-referred ramp. Trace D is C1B's output pulse and the circuit's output. The diodes at C1B's positive input provide temperature compensation for the sensor's positive tempco, allowing C1B's trip voltage to ratiometrically track bridge output over temperature.

A3, operating open loop, determines polarity by comparing the rectified and filtered bridge output signals with respect to ground.

To calibrate this circuit, place the level transducer at a known 40 arc-minute angle and adjust the 5kΩ trimmer at C1B for a 400Hz output. Circuit accuracy is limited by the transducer to about 2.5%.

The final example concerns direct digitization of a piezoelectric accelerometer. These transducers rely on the property of ceramic materials to produce charge when mechanically excited. In this device a mass is coupled to the ceramic element. An acceleration acting on the mass causes charge to be dispensed from the ceramic element. Sensitivity and frequency response are related to the characteristics of the ceramic used and the mechanical design of the transducer. The best way to signal condition a piezoelectric output is to unload it directly into the virtual ground of an op amp's summing point. This method provides no voltage difference between the center conductor and the shield of the coaxial cable connecting the accelerometer and the signal conditioning amplifier. This eliminates cable capacitance as a parasitic term, an important consideration in any charge output transducer. Because the accelerometer produces AC outputs, a direct digitization of its output must produce a sign bit as well as amplitude data.

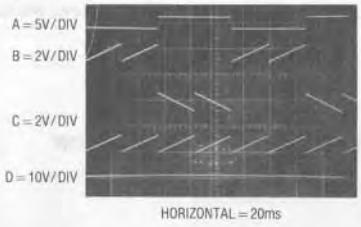

Figure 15. Level Transducer Digitizer Waveforms

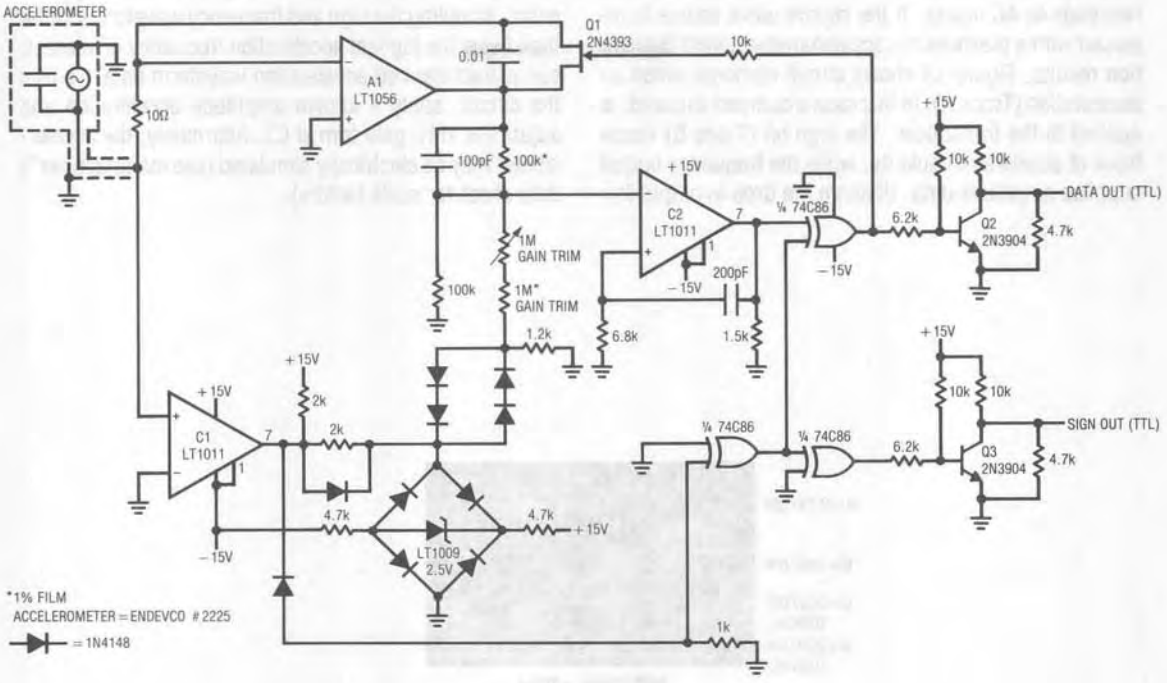

Figure 16. Accelerometer Digitizer

Figure 16's circuit accomplishes a complete, direct A→D conversion on the piezoelectric accelerometer noted and is generally applicable to other devices in this class. To understand the circuit it is convenient to replace the accelerometer with a square wave source coming through a resistor. When the square wave is positive, the A1 integrator responds with a negative-going ramp output (Trace A, Figure 17). C1, detecting the square wave polarity, goes high and the LT1009 diode bridge (Trace B) limits at +3.7V. A1's ramp output is summed with the bridge's output at C2's negative input. The series diodes temperature-compensate the bridge diodes. When A1's output goes far enough negative, C2's (Trace C) output goes high. The output gating is arranged so that with C1's output low and C2 high, Q1's gate (Trace D) receives turn-on bias. Q1 comes on, discharging A1's feedback capacitor and resetting A1's output to zero. Local AC positive feedback at C2 ensures adequate time for a complete zero reset of A1's feedback capacitor. The 100pF capacitor at C2's input aids high frequency response. When the AC feedback decays away, Q1 goes off, A1 begins to ramp negative again and the cycle repeats as long as the input square wave is positive. The frequency of oscillation is directly proportional to the current into A1's summing point. When the input square wave goes negative, A1 abruptly begins to ramp in the positive direction. Simultaneously, the C1 input polarity detector output goes negative, forcing the LT1009 bridge output negative. C2's output now switches when A2's output exceeds a positive limit. The output gating, directed by C1's polarity signal, inverts C2's output to supply proper drive to Q1's gate. Q1 turns on and resetting occurs. Thus, the loop maintains oscillation, but with all signs reversed. The Q2 and Q3 level shifters supply TTL data outputs for data and sign.

This circuit constitutes an I→F converter which responds to AC inputs. If the square wave source is replaced with a piezoelectric accelerometer, direct digitization results. Figure 18 shows circuit response when an acceleration (Trace A), in this case a damped sinusoid, is applied to the transducer. The sign bit (Trace B) keeps track of acceleration polarity, while the frequency output supplies amplitude data. Observe the drop in output frequency as the input waveform damps. A monitoring processor, sampling the sign and frequency waveforms faster than twice the highest acceleration frequency of interest, can extract desired acceleration waveform data. To trim the circuit, apply a known amplitude acceleration and adjust the 1MΩ gain trim at C2. Alternately, the accelerometer may be electrically simulated (see manufacturer's data sheet for scale factors).

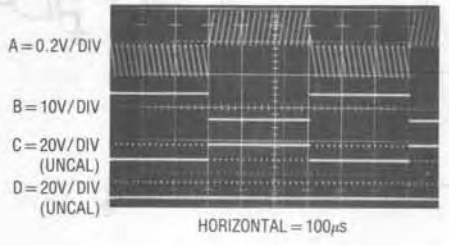

Figure 17. Accelerometer Digitizer Waveforms with Square Wave Test Drive

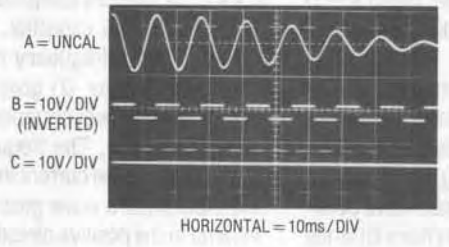

Figure 18. Accelerometer Digitizer Response