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External components improve SAR-ADC accuracy

DIRECTLY DRIVING THE INPUT OF A CAPACITIVE SAR ADC WITH AN OP-AMP OUTPUT CAN PRODUCE TRANSIENTS THAT DEGRADE THE CONVERTER'S PERFORMANCE. INTERPOSING AN RC NETWORK CAN SOLVE THE PROBLEM—PROVIDED THAT YOU KNOW WHAT VALUES TO USE.

It is tempting to use an op amp to directly drive the input of a SAR (successive-approximation-register) ADC. Unfortunately, this configuration can limit circuit performance. An external RC (resistor-capacitor) network better isolates the converter from the driver amplifier and allows greater flexibility in op-amp selection. Getting the best performance from a SAR ADC may be more important than you think. Even if you convert signals that are well below the frequency limitations of the converter and amplifier, you can't ignore the dynamic characteristics of the SAR ADC's input structure.

Figure 1 shows a single-supply combination SAR-ADC/op-amp circuit. This circuit places the op amp in an inverting-gain configuration. IC_1 is a unity-gain-stable, single-supply CMOS op amp with a gain-bandwidth product of 5 MHz. The single-supply configuration avoids the effect of the amplifier-input limitations, such as a limited input range and input common-mode-crossover distortion. The designer of this circuit uses the ADC-reference output to bias the amplifier's noninverting input as well as the negative input of the ADC, thus keeping the op-amp operation between the supply rails. IC_2 is a 12-bit, 500k-sample/sec SAR ADC.

In **Figure 1**, the circuit appears to be functional; the op amp's low-impedance output drives the SAR ADC. **Figure 2** shows the FFT-test results for this circuit, with a 15-kHz op-amp-input signal. In **Figure 2a**, the SAR ADC's acquisition time equals 265 nsec. In **Figure 2b**, the acquisition time is 560 nsec. These acquisition times extend neither the op amp nor the ADC beyond its specified performance limits.

The measurement results show that the length of the acquisition time affects the performance; increasing the acquisition time from 250 to 560 nsec improves the performance, although increasing the acquisition time also slightly increases the total throughput time. With the longer acquisition time, the SNR (signal-to-noise ratio) increases from 70.8 to 71.5 dB and the THD (total harmonic distortion) decreases from −71.4 to −78.6 dB (**Reference 1**).

STANDARD SAR-ADC MODEL

A capacitive SAR ADC's input stage contains a capacitive-charge-redistribution network (**Figure 3** and **references 2** and **3**). In **Figure 3**, V_{SH0} is the initial voltage across the sampling capacitor, C_{SH}. Depending on the converter's input structure, this voltage can equal the input during the previous conversion, ground, or V_{REF}. Opening S_2 and closing S_1 cause signal acquisition. When S_1 closes, the voltage across the sampling capacitor, C_{SH}, changes to V_{IN}. Charge from the voltage source, V_{IN}, passes through the sampling-switch path of S_1 and R_{S1} onto C_{SH}. As the charge redistributes itself, the charge previously on C_{SH} changes so that V_{CSH} equals V_{IN} (**Figure 4**).

TABLE 1 WORST-CASE SETTLING TIME OF SAR ADC

ADC resolution (bits)	k_1 (time-constant multiplier to 1-LSB accuracy, $½^N$)	k_2 (time-constant multiplier to ½-LSB accuracy, $½^{N+1}$)
8	5.5	6.24
10	6.9	7.62
12	8.3	9.01
14	9.7	10.4
16	11.1	11.78
18	12.5	13.17

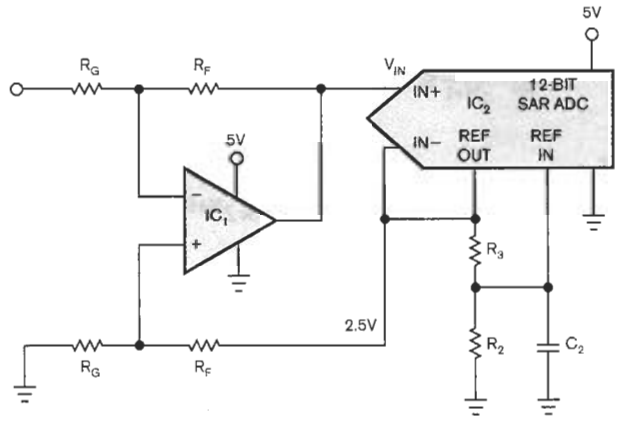

Figure 1 In this sample application circuit for a SAR-ADC system, if $R_F = R_G$, the noise gain for amplifier IC_1 is 2V/V.

If you consider only the ADC input, the ADC's bandwidth depends on the internal sampling capacitor, C_{SH}, and the switch resistance, R_{SI}. From the time constant, $\tau = R_{SI} \times C_{SH}$, you can derive the settling time of this one-pole system. The minimum acquisition time for the SAR converter is the time required for the sampling mechanism to capture the input voltage. The acquisition time begins after the issuance of the sample command and the charging of the hold capacitor, C_{SH}.

You can use the following **equations** to determine the settling time for the network in **Figure 3**.

$$V_{CSH}(t) = V_{CSH}(t_0) + (V_{IN} - V_{CSH}(t_0)) \times \left(1 - e^{\frac{-t}{\tau}}\right), \quad (1)$$

where $V_{CSH}(t)$ is voltage versus time across the sampling capacitor, C_{SH}; $V_{CSH}(t_0)$ is voltage across the sampling capacitor, C_{SH}, at the start of the acquisition time; V_{IN} is the ADC's input voltage; τ is the acquisition-time constant, equal to $R_{SI} \times C_{SH}$; and t is a time variable in seconds.

If you want the error not to exceed ½ LSB, the time at which the voltage on the sampling capacitor, C_{SH}, approaches within ½ LSB of the input voltage establishes the acquisition time.

$$V_{IN} - V_{CSH}(t_{AQ}) \le \frac{1}{2}\ \text{LSB}, \quad (2)$$

or

$$V_{CSH}(t_{AQ}) \ge V_{IN} - \frac{1}{2}\ \text{LSB}, \quad (3)$$

where $V_{CSH}(t_{AQ})$ is voltage across the sampling capacitor, C_{SH}, at the end of the sampling period, and t_{AQ} is the acquisition time, or the amount of time from the beginning of the sampling period (t_0) to the end of the sampling period. Further,

$$\frac{1}{2}\ \text{LSB} = \frac{\text{FSR}}{2^{N+1}}, \quad (4)$$

where FSR is the input full-scale range of the N-bit converter.

If you change $V_{CSH}(t)$ to $V_{CSH}(t_{AQ})$ and $V_{CSH}(t_0)$ to V_{SH0} and make **equations 1** and **3** equal, you can derive the following **equations:**

$$V_{IN} - \frac{\text{FSR}}{2^{N+1}} \le V_{SH0} + (V_{IN} - V_{SH0}) \times \left(1 - e^{\frac{-t_{AQ}}{\tau}}\right), \quad (5)$$

or

$$t_{AQ} \ge \tau \times \ln\left(\frac{V_{IN} - V_{SH0}}{\text{FSR}} \times 2^{N+1}\right). \quad (6)$$

If

$$k = \ln\left(\frac{V_{IN} - V_{SH0}}{\text{FSR}} \times 2^{N+1}\right), \quad \text{then} \quad (7)$$

$$t_{AQ} \ge k \times \tau. \quad (8)$$

You can calculate settling time as a function of the input-stage time constant and the time-constant multiplier, k, for a variety of ADC resolutions. **Table 1** summarizes these cal-

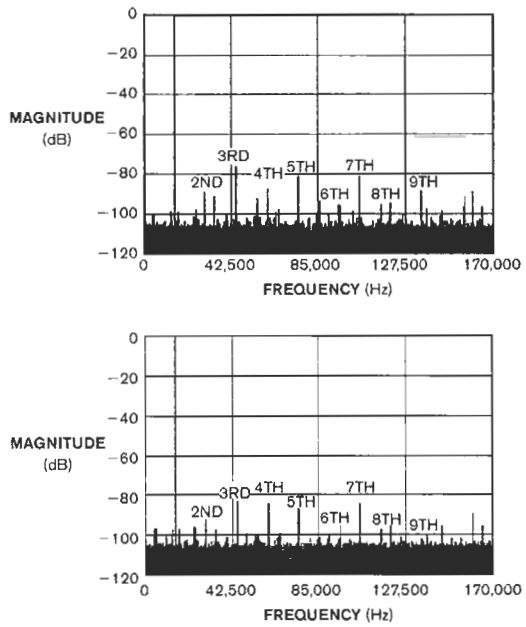

Figure 2 The measured FFT results of Figure 1's 500k-sample/sec, 12-bit SAR ADC show that an acquisition time of 265 nsec produces significant harmonic distortion (a), whereas an acquisition time of 560 nsec decreases harmonic distortion (b).

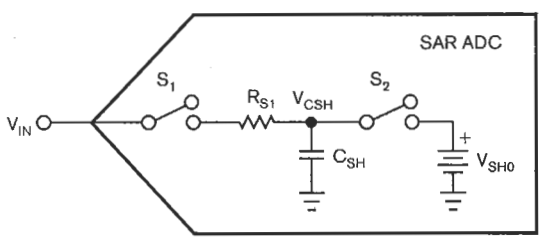

Figure 3 The equivalent input elements for the SAR ADC include an internal input RC pair, R_{S1} and C_{SH}; two switches, S_1 and S_2; and a voltage, V_{SH0}.

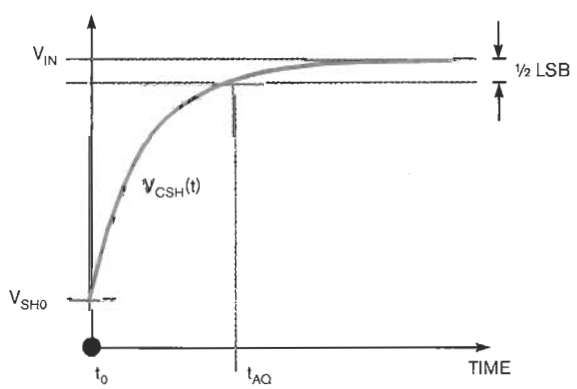

Figure 4 The voltage across the sampling capacitor changes with a single-pole response during the SAR-ADC acquisition period.

culations. You can use these calculations to evaluate the acquisition time of any SAR ADC. For the worst-case analysis (**Equation 5** and **Table 1**), assume that V_{SH0} equals 0V. **Figure 5** shows the change of the initial charge of the Texas Instruments ADS8361, a 16-bit, 500k-sample/sec SAR ADC, as a function of the input-signal amplitude.

With the ADS8361, S_1's closed-switch resistance, R_{S1}, is 20Ω. The ADS8361's internal sampling capacitor, C_{SH}, is equal to 25 pF. From **Figure 5**, you can see that the sinusoidal input voltage frequency is much lower than the converter's sampling frequency. If you measure lower input frequency signals, $f_{IN} \leq f_S/10$, the calculation uses an initial voltage on V_{SH0} equal to half of the full-scale range. On the other hand, if there is a front-end multiplexer, V_{SH0} is 0V. For a 16-bit SAR ADC, the time-constant multiplier, k_1, for 1-LSB error equals 11.09. If you need ½-LSB error, $k_2=11.78$. The detailed discussion in **Reference 4** explains how to determine the initial charge of the sampling capacitor in a capacitive SAR ADC.

A CHARGE BANK AT THE SAR-ADC INPUT

Figure 6 illustrates a driving amplifier, followed by an RC pair that connects to the input of a SAR ADC. The capacitor, C_{IN}, acts as a charge bank that supplies ample charge to the SAR ADC's internal capacitor array. Using the previous calculation for a 16-bit SAR ADC, the time constant, τ ($\tau=R_{IN}\times C_{IN}$), of the external RC filter in which $k_2=t_{AQ}/\tau$ is between 11 and 12. A k value of 11 or 12 does not degrade the performance of the signal chain. However, by fine-tuning the formulas, you can achieve optimum performance with lower k values.

EVALUATING THE CHARGE-BANK CIRCUITRY

In the circuit of **Figure 6**, the charge on C_{IN} follows the input voltage before and after the internal ADC sampling switch, S_1, closes. With this condition in mind, the timing evaluation ignores the influence of R_{IN}. **Figure 7** shows the model of a new SAR-ADC system. In this system, capacitors C_{IN} and C_{SH} have different initial voltages. At the start of a conversion, the charge quickly redistributes between C_{IN} and C_{SH} through R_{S1}.

Figure 8 shows a simplified circuit for the capacitive input stage of the circuit in **Figure 7**. Before the input-signal acquisition, S_1 is open (**Figure 8a**). The input capacitor, C_{IN}, has

TABLE 2 CHANGES IN K AS A FUNCTION OF C_{IN}

ADC resolution (bits)	C_{IN} (pF)	α	k_3 (time-constant multiplier to ½-LSB accuracy)	R_{IN} (Ω)
16	200	8	9.59	1576
16	400	16	8.95	894
16	1000	40	8.07	411
16	4000	160	6.7	126

Notes:
Using worst-case values, V_{IN} is the full-scale voltage, or 2^N, and V_{SH0} is 0V.
$\alpha=C_{IN}/C_{SH}$.

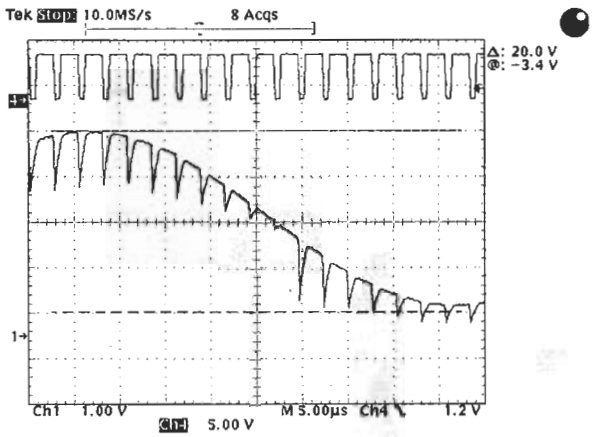

Figure 5 After an acquisition command, the ADS8361 requires a surge of current to charge its sampling capacitor, C_{SH}, for different initial voltages of V_{SH0}.

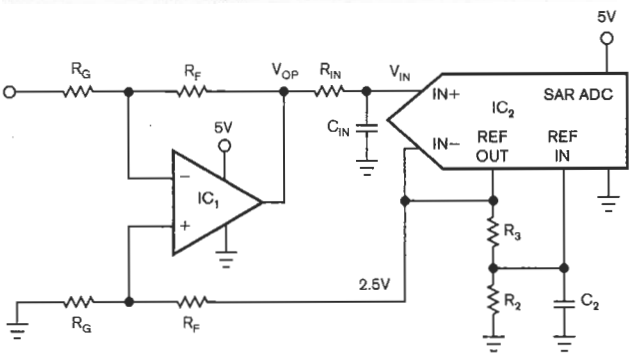

Figure 6 The correct configuration for the external input circuits of the SAR ADC is a driving amplifier followed by an RC network comprising R_{IN} and C_{IN}.

an initial voltage of V_{IN}, and the voltage across the sampling capacitor, C_{SH}, equals V_{SH0}. S_1 closes at the start of signal acquisition (**Figure 8b**). The capacitor voltages, V_{IN} and V_{CSH}, become equal (**Figure 8c**) as the charge quickly redistributes between C_{IN} and C_{SH}.

The following **equations** calculate the charge on capacitors C_{IN} and C_{SH}:

$$Q_{IN}=C_{IN}\times V_{IN}, \quad (9)$$

and

$$Q_{SH}=C_{SH}\times V_{SH0}. \quad (10)$$

After S_1 closes, the charge on C_{IN} and C_{SH} distributes between the capacitors. C_{IN} and C_{SH} combine into an equivalent capacitance, C_{TOT} (**Figure 8b** and **8c**). The effective capacitance and charge distribution are:

$$C_{TOT}=C_{IN}+C_{SH}, \quad (11)$$

and

$$Q_{TOT}=Q_{IN}+Q_{SH}. \quad (12)$$

Using **equations 9** through **12**, you can calculate a new equivalent voltage on capacitors C_{IN} and C_{SH}:

$$V_{TOT} = \frac{C_{IN}}{C_{IN}+C_{SH}} \times V_{IN} + \frac{C_{SH}}{C_{IN}+C_{SH}} \times V_{SH0}. \quad (13)$$

Introducing the ratio $C_{IN}/C_{SH}=\alpha$, **Equation 13** transforms into:

$$V_{TOT} = \frac{\alpha}{\alpha+1} \times V_{IN} + \frac{1}{\alpha+1} \times V_{SH0}. \quad (14)$$

Now, you can calculate the required time constant of the input RC for the circuit in **Figure 6**.

$$V_{TOT}(t) = V_{TOT}(t_0) + (V_{IN} - V_{TOT}(t_0)) \times \left(1 - e^{\frac{-t}{\tau}}\right), \quad (15)$$

where $V_{TOT}(t)$ is the voltage versus time across capacitor C_{TOT} and $V_{TOT}(t_0)$ is the voltage across C_{TOT} at the start of the acquisition time, using **Equation 14**.

Again, to limit the error to ½ LSB, you must make the acquisition time long enough for the voltage on C_{TOT} to approach the input voltage within ½ LSB.

$$V_{IN} - V_{TOT}(t_{AQ}) \le \frac{1}{2} \text{ LSB}, \quad (16)$$

or

$$V_{TOT}(t_{AQ}) \ge V_{IN} - \frac{1}{2} \text{ LSB}, \quad (17)$$

where $V_{TOT}(t_0)$ is the voltage across the capacitor, C_{TOT}, at the end of the sampling period. By changing $V_{TOT}(t)$ to $V_{TOT}(t_0)$ and making **equations 15** and **17** equal, you obtain:

$$V_{IN} - \frac{FSR}{2^{N+1}} \le V_{TOT}(t_0) + (V_{IN} - V_{TOT}(t_0)) \times \left(1 - e^{\frac{-t_{AQ}}{\tau}}\right), \quad (18)$$

and

$$t_{AQ} \ge \tau \times \ln\left(\frac{V_{IN} - V_{TOT}(t_0)}{FSR} \times 2^{N+1}\right). \quad (19)$$

Now, you can define a new way of calculating the time-constant multiplier, k_3, using **equations 14** and **19**.

$$k = \ln\left[\frac{\left(1 - \frac{\alpha}{\alpha+1}\right) \times V_{IN} - \frac{1}{\alpha+1} \times V_{SH0}}{FSR} \times 2^{N+1}\right]. \quad (20)$$

Equation 20 shows that k_3 is a function of not only the initial charge, V_{SH0}, but also the external capacitor, C_{IN}. In the ADS8361, a 16-bit SAR ADC with a lower input-frequency signal of $f_{IN} \le f_S/10$, C_{SH}'s calculated initial charge, V_{SH0}, is half of the full-scale range. On the other hand, with the multiplexed signal at the input to the converter, you must use $V_{SH0}=0V$. With these assumptions, **Equation 20** becomes:

$$k = \ln\left(\frac{1}{\alpha+1} \times 2^{N+1}\right). \quad (21)$$

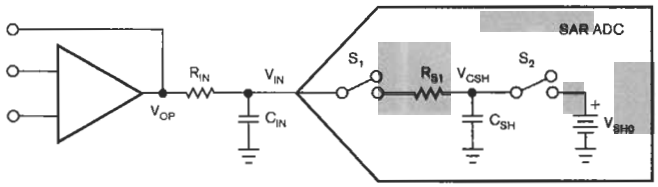

Figure 7 C_{IN}, at the SAR-ADC input, provides a charge reservoir during sampling.

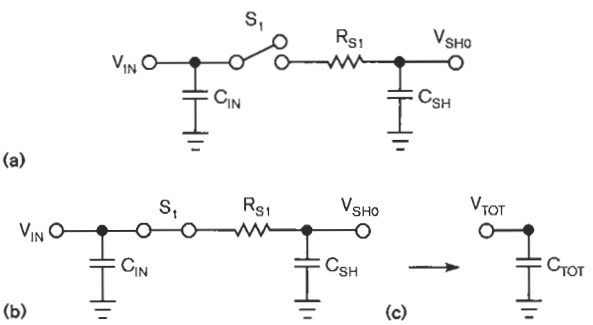

Figure 8 These simplified models describe the external and internal ADC capacitors.

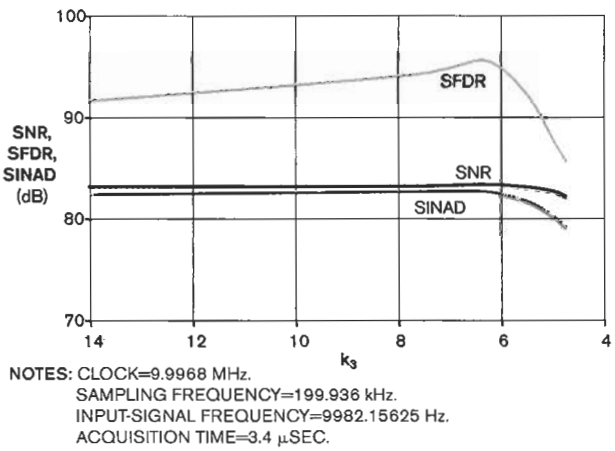

Figure 9 Results measured from the circuit of Figure 6 show that acquisition time has little effect on SNR and SINAD until you reduce the time-constant multiplier, k, to less than 6. SFDR reaches a maximum when k is slightly greater than 6. The circuit's active devices are Texas Instruments' 16-bit ADS8361 ADC and OPA350 single-supply CMOS amplifier.

Table 2 shows how k_3 changes as a function of C_{IN} and shows lower valued time-constant multipliers, k_3, for **Figure 6**'s 16-bit SAR ADC.

TEST RESULTS

Figure 9 shows the results for the ADS8361, a 16-bit converter, tested in the configuration in **Figure 6**. The results show that the ADS8361 maintains good performance with

SNR, SFDR (spurious-free dynamic range), and SINAD (signal, noise, and distortion) until k_3 becomes smaller than six. This result differs from the k_1-multiplier values of 11.1 and 11.78 that **Table 1** generates. In **Figure 9**, the 16-bit ADS8361 SAR ADC operates at 200k samples/sec (t_{AQ}=3.4 µsec). The frequency of the input signal is 10 kHz. In **Equation 20**, the initial voltage on V_{SH0} is equal to half the full-scale range. The value of the sampling capacitor, C_{SH}, is 25 pF, and the value of C_{IN} is 2.2 nF. With these assumptions, **Equation 20** becomes:

$$\alpha = \frac{C_{IN}}{C_{SH}} = \frac{2.2\ nF}{25\ pF} = 88, \tag{22}$$

$$k_4 = \ln\left[\frac{\left(1-\frac{\alpha}{\alpha+1}\right)\times V_{IN} - \frac{1}{\alpha+1}\times V_{SH0}}{FSR}\times 2^{N+1}\right] \tag{23}$$

$$= \ln\left[\frac{\left(1-\frac{88}{88+1}\right)\times 5V - \frac{1}{88+1}\times 2.5V}{5V}\times 2^{16+1}\right] =$$

and

$$R_{IN} = \frac{t_{AQ}}{k_4\times(C_{IN}+C_{SH})} = \frac{3.4\ \mu SEC}{6.6\times(2.2\ nF+25\ pF)} = 231.5\Omega. \tag{24}$$

Note that, in **Figure 9**, the improvement in SFDR is approximately 5 dB.

A LITTLE RC FINESSE HELPS

The following **equations** illustrate the key design guidelines for the SAR-ADC input circuits in **Figure 6.**

$$\tau = R_{IN}\times(C_{IN}+C_{SH}) \le \frac{t_{AQ}}{k}. \tag{25}$$

For multiplexed signals, this **equation** is:

$$k = \ln\left(\frac{1}{\alpha+1}\times 2^{N+1}\right). \tag{26}$$

And, for lower-input-frequency signals,

$$k = \ln\left[\frac{\left(1-\frac{\alpha}{\alpha+1}\right)\times V_{IN} - \frac{1}{\alpha+1}\times V_{SH0}}{FSR}\times 2^{N+1}\right], \tag{27}$$

where $\alpha = C_{IN}/C_{SH}$.

To maximize the system's SNR, the value of C_{IN} should be as large as possible with the op amp's driving capability in mind. For preservation of the ADC's THD, C_{IN} should be either a ceramic device with a chip-on-glass dielectric or a silver-mica

unit with ≤5% tolerance. The value of R_{IN} depends primarily on the acquisition time, the value of C_{IN}, and the op amp's driving capability. R_{IN} isolates amplifier IC_1 from load capacitor C_{IN}, which, for low-noise performance, should be a metal-film device with ≤1% tolerance. The RC filter between the op amp and the SAR ADC may compromise the amplifier's stability. **Reference 5** provides more details on op-amp selection and stability. EDN

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