Table of Contents

Driving a SAR ADC directly without a front-end buffer circuit (low-power, low-sampling-speed DAQ)

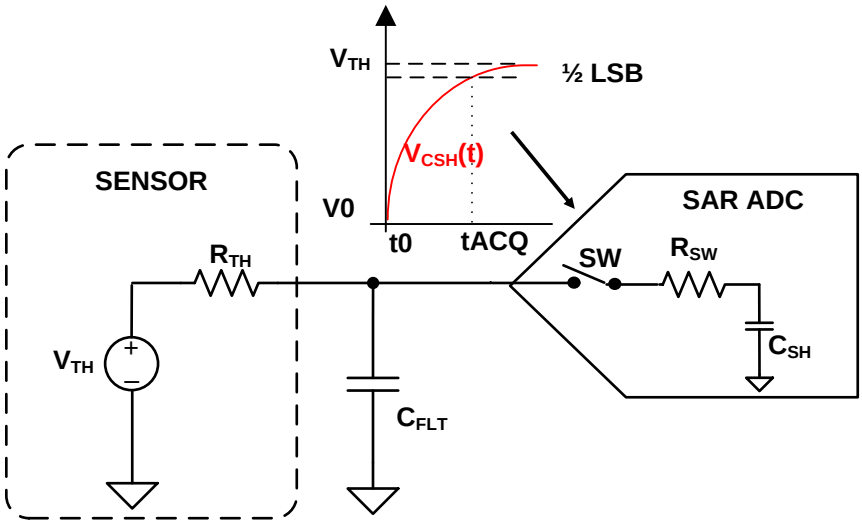
Abhijeet Godbole

Design Description

This design explains how sensor outputs can be directly interfaced with a SAR ADC input. In applications such as *Environmental Sensors*, *Gas Detectors*, and *Smoke or Fire Detectors*, the input is very slow-moving and the sensor output voltage is sampled at fairly slower speeds (10ksps or so). In such or similar systems, the sensor output can be directly interfaced with the SAR ADC input without the need for a driver amplifier to achieve a small form-factor, low-cost design.

Interfacing Sensor Output Directly to a SAR ADC

The following figure shows a typical application diagram for interfacing a sensor directly to a SAR ADC input without the use of a driver amplifier. The sensor block highlights the Thevenin equivalent of a sensor output. Voltage source, V_{TH}, is the Thevenin-equivalent voltage and source resistance R_{TH} is the Thevenin-equivalent impedance. Most sensor data sheets provide the Thevenin model of the sensor from which the value of the series impedance can be easily calculated.



Specifications

Parameter	Calculated	Simulated	Measured
Transient ADC Input Settling Error	< 0.5LSB < 100.5µV	36.24µV	N/A
Step Input Full Scale Range	3.15V	3.15V	3.14978
Input Source Impedance (R_{TH})	10kΩ	10kΩ	10.01kΩ
Filter Capacitor Value (C_{FLT})	680pF	680pF	N/A
ADC Sampling Speed	10ksps	10ksps	10ksps

Design Note

1. Determine source impedance of input signal. Calculate the RC time constant of the input source impedance and filter capacitor (known value).
2. Determine the minimum acquisition time required for the input signal to settle for a given source impedance and the filter capacitor combination.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.

Component Selection for ADC Input Settling

SAR ADCs can be directly interfaced with sensors when the analog input source is capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal to within ½ of an LSB within the acquisition time of the SAR ADC. To achieve this, the external RC filter (R_{TH} and C_{FLT}) must settle within the acquisition time (t_{ACQ}) of the ADC. The relationship between the ADC acquisition time and RC time constant of the external filter is:

$$t_{ACQ} \geq k \cdot \tau_{FLT}$$

where

- $\tau_{FLT} = R_{TH} \cdot C_{FLT}$
- k is the single pole time constant for N bit ADC

The following design example values are given in the table on page 1:

R_{TH} = 10kΩ

C_{FLT} = 680pF

K = 11 (Single pole time constant multiplier for 14-bit ADC) – More information is found on page 96 and page 97 of the *Analog Engineer's Pocket Reference*.

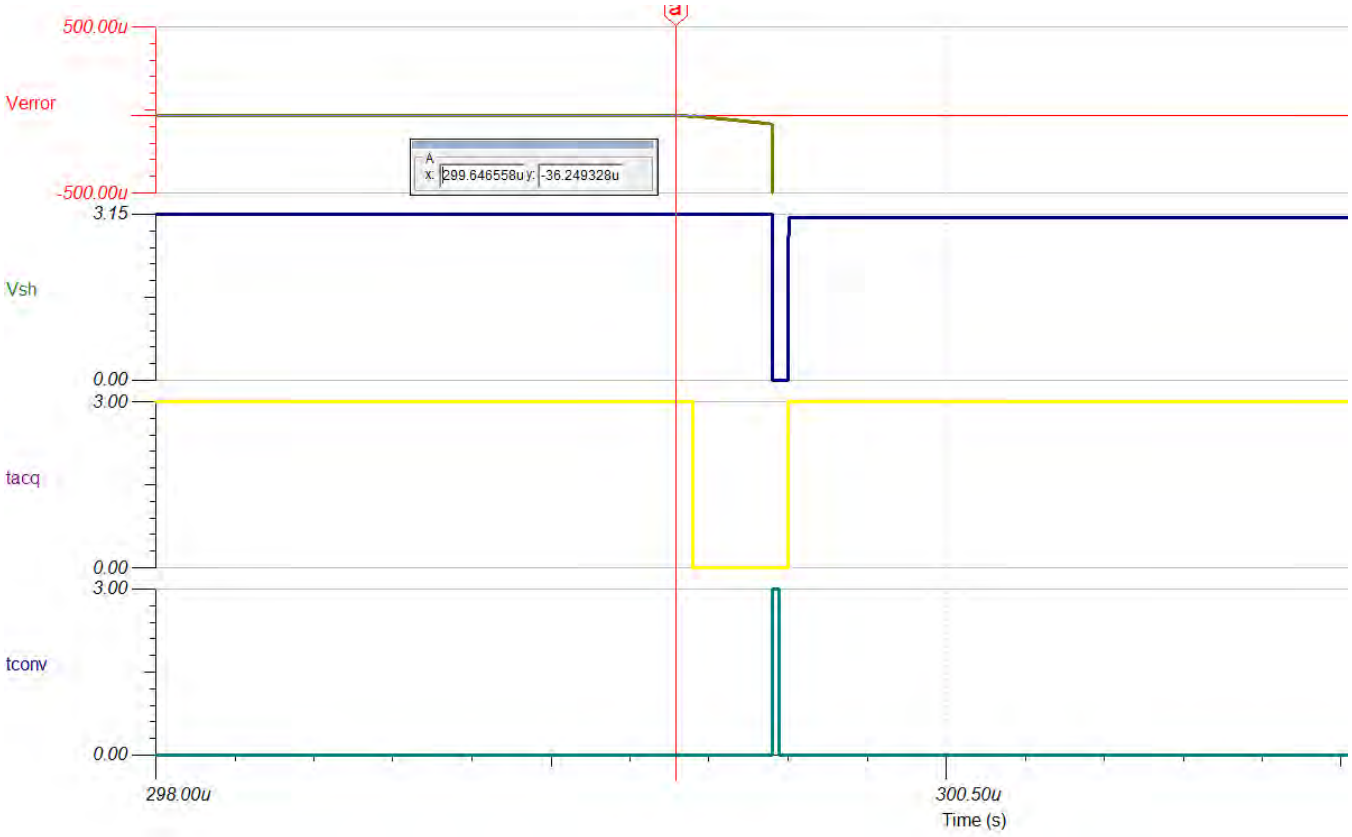
Minimum acquisition time required for proper settling is calculated using this equation:

$$t_{ACQ} \geq 11 \cdot 10k\Omega \cdot 680pF = 74.80\mu s$$

For more information on SAR ADCs and front end design for SAR ADCs, refer to *Introduction to SAR ADC Front-End Component Selection*.

Transient Input Settling Simulation using TI-TINA

The following figure shows the settling of an *ADS7056* ADC given a 3.15-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* in the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Increasing Acquisition Time of SAR ADC for Input Signal Settling

The acquisition time of a SAR ADC can be increased by reducing the throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput.
2. Keeping the SCLK fixed at the highest permissible value and increasing the CS high time.

The following table lists the acquisition time for the previous two cases for the *ADS7056* SAR ADC operating at 10ksps throughput (tcycle = 100µs). Case 2 provides a longer acquisition time for the input signal to settle because of the increased frequency of the SCLK given a fixed conversion and cycle time.

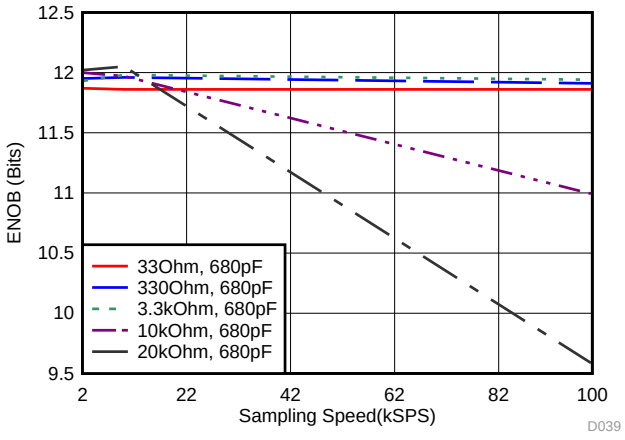
Case	SCLK	t_{cycle}	Conversion Time ($18 \cdot t_{SCLK}$)	Acquisition Time ($t_{cycle} - t_{conv}$)
1	0.24MHz	100µs	74.988µs	25.01µs
2	60MHz	100µs	0.3µs	99.70µs

The following table shows a performance comparison between an 8-, 10-, 12-, and 14-bit ADC with respect to sampling speed and effective number of bits (ENOB) when a sensor output with an output impedance of 10kΩ is directly interfaced with the ADC input. As expected, the ENOB degrades with higher sampling rates because the acquisition time decreases.

Sampling Speed (ksps)	ADS7040 (8-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7041 (10-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7042 (12-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 1.5nF)	ADS7056 (14-bit ADC) ENOB (R_{TH} = 10kΩ, C_{FLT} = 680pF)
10	7.93	9.87	10	12.05
100	7.92	9.85	9.97	10.99
500	7.88	9.68	9.95	8.00

Performance Achieved at Different Throughput Rates with Different Source impedance

The following figure provides the ENOB achieved from the ADS7056 at different throughout with different input impedances. Note that all the results for the following graph were taken with a 100-Hz analog input signal and without an ADC driver amplifier.



Design Featured Devices:

Device	Key Features	Link	Similar Devices
ADS7040	8-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7040	www.ti.com/adcs
ADS7041	10-bit resolution, SPI, 1Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7041	www.ti.com/adcs
ADS7042	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7042	www.ti.com/adcs
ADS7056	14-bit resolution, SPI, 2.5-Msps sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	www.ti.com/product/ADS7056	www.ti.com/adcs

NOTE: The ADS7042 and ADS7056 use the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key file

Source files for interfacing sensor output directly with SAR ADCs – http://www.ti.com/lit/zip/sbac178.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters. Added link to circuit cookbook landing page.

Low-power sensor measurements: 3.3-V, 1-ksps, 12-bit, single-ended, dual-supply circuit

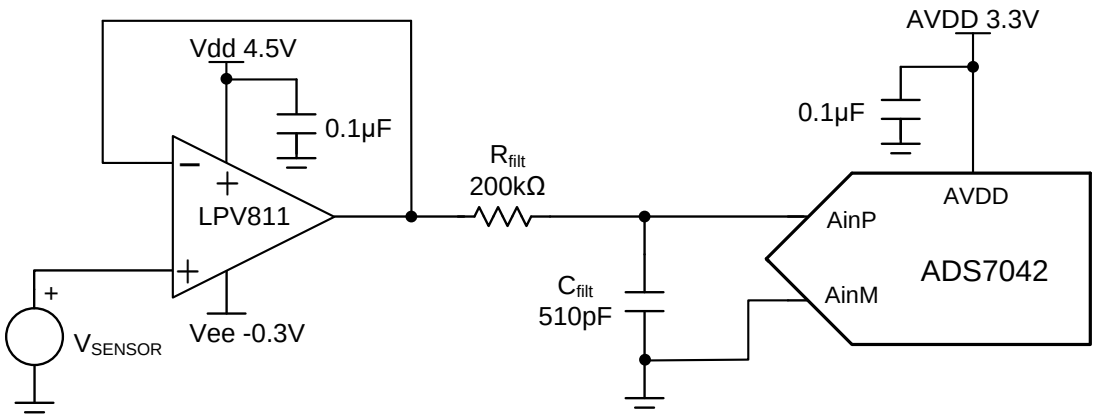
Reed Kaczmarek

Input	ADC Input	Digital Output ADS7042
V_{inMin} = 0V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
V_{inMax} = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies		
AVDD	**V_{ee}**	**V_{dd}**
3.3V	–0.3V	4.5V

Design Description

This design shows an low-power amplifier being used to drive a SAR ADC that consumes only nW of power during operation. This design is intended for systems collecting sensor data and require a low-power signal chain which only burns single-digit µW of power. *PIR sensors*, *gas sensors*, and *glucose monitors* are a few examples of power-sensitive systems that benefit from this SAR ADC design. The values in the component selection section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3 V, 1 ksps, 12-bit Single-Ended, Single Supply* shows a simplified version of this circuit where the negative supply is grounded. The –0.3-V negative supply in this example is used to achieve the best possible linear input signal range. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5 × LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

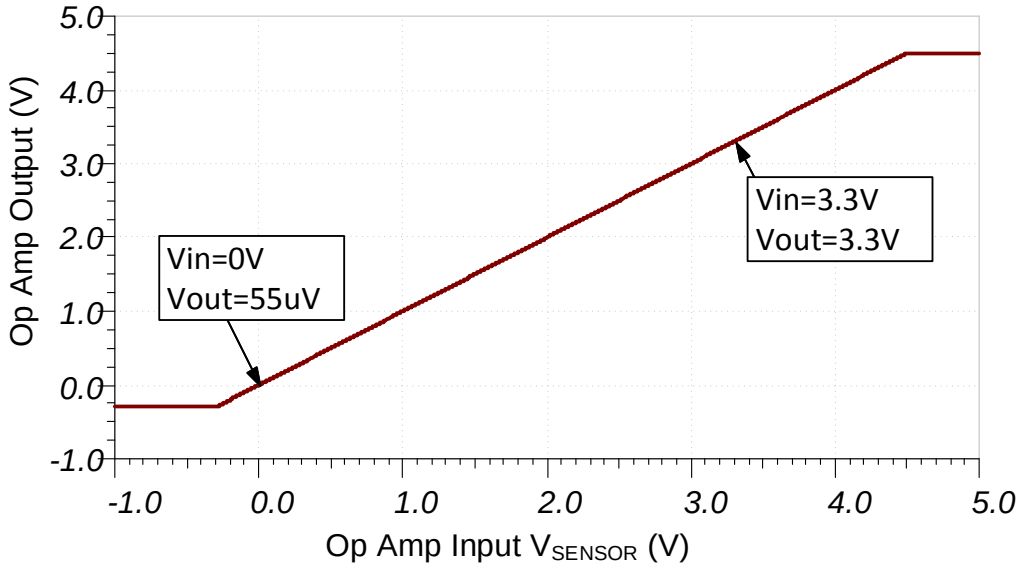
1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the component selection section.
2. Select a COG (NPO) capacitor for Cfilt to minimize distortion.
3. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt (see *Introduction to SAR ADC Front-End Component Selection*). These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify the design you will need to select a different RC filter.

Component Selection

1. Select a low-power op amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - LPV811 – 450-nA supply current, 8-kHz gain bandwidth product, unity gain stable
2. Find op amp maximum and minimum output for linear operation:
   $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 V_{cm} specification
   $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 Vout swing specification
   $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification
3. Typical power calculations (at 1ksps) with expected values. See *SAR ADC Power Scaling* for a detailed description of trade-offs in low-power SAR design:
   $P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 230nA \times 3.3V = 759nW$
   $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 450nA \times (4.5V - (-0.3V)) = 2.16\mu W$
   $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.16\mu W = 2.919\mu W$
4. Typical power calculations (at 1ksps) with measured values:
   $P_{AVDD} = I_{AVDD\_AVG} \times AVDD = 214.8nA \times 3.3V = 708.8nW$
   $P_{LPV811} = I_{LPV811} \times (V_{dd} - V_{ee}) = 431.6nA \times (4.5V - (-0.3V)) = 2.071\mu W$
   $P_{total} = P_{AVDD} + P_{LPV811} = 708.8nW + 2.071\mu W = 2.780\mu W$
5. Find Rfilt and Cfilt to allow for settling at 1ksps. Refer to *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) for the algorithm to select Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

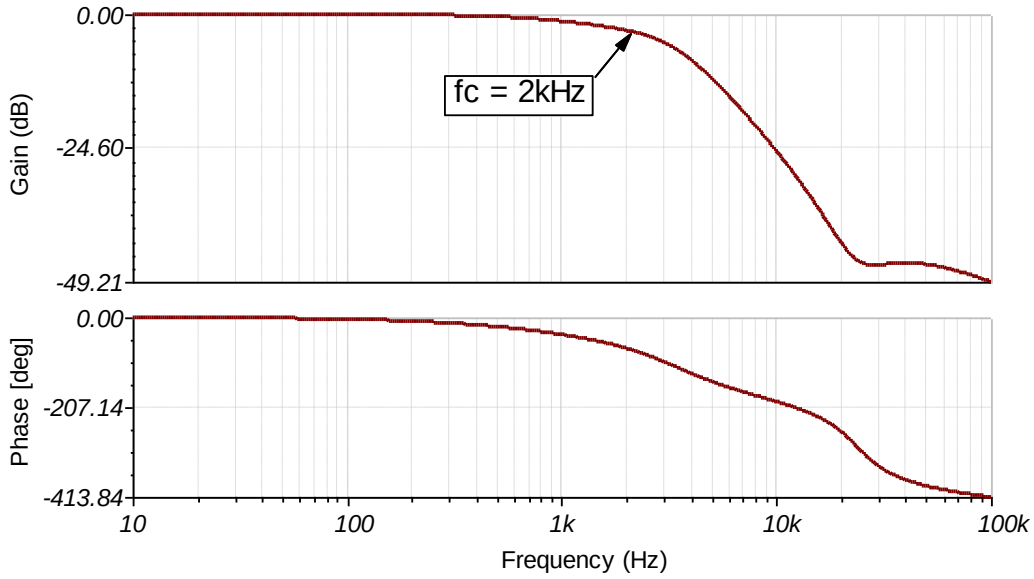
The following graph shows a linear output response for inputs from 0 to 3.3V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



AC Transfer Characteristics

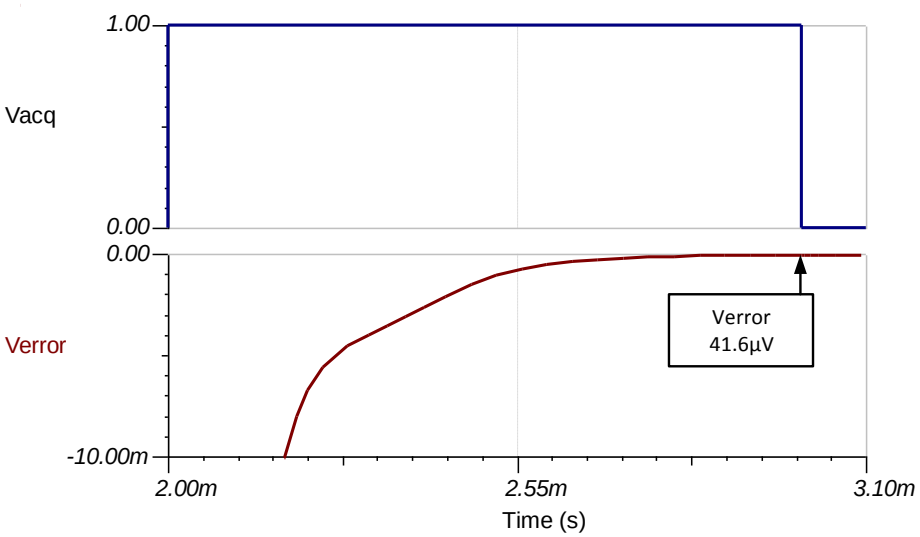
The bandwidth simulation includes the effects of the amplifier output impedance and the RC charge bucket circuit (R_{filt} and C_{filt}).The bandwidth of the RC circuit is shown in the following equation to be 1.56kHz. The simulated bandwidth of 2kHz includes effects from the output impedance interacting with the impedance of the load. See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times (200k\Omega) \times (510pF)} = 1.56kHz$$



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of an LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



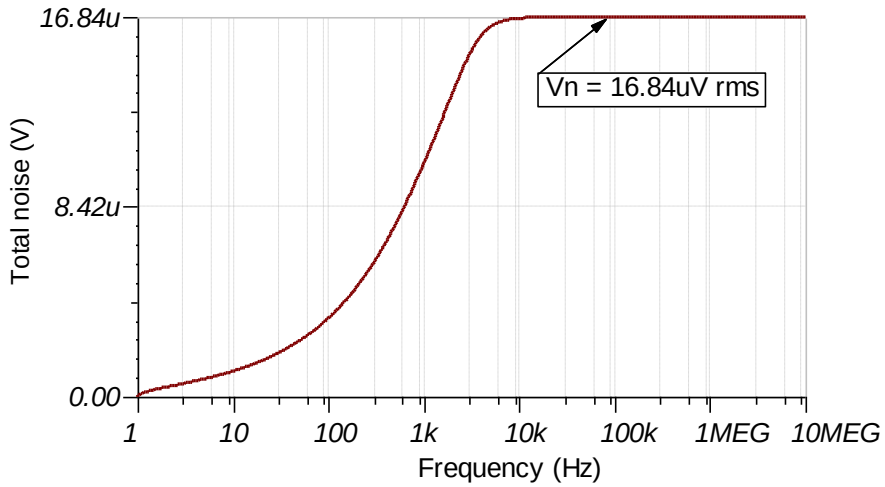
Noise Simulation

This section walks through a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times 200k\Omega \times 510pF} = 1560Hz$$

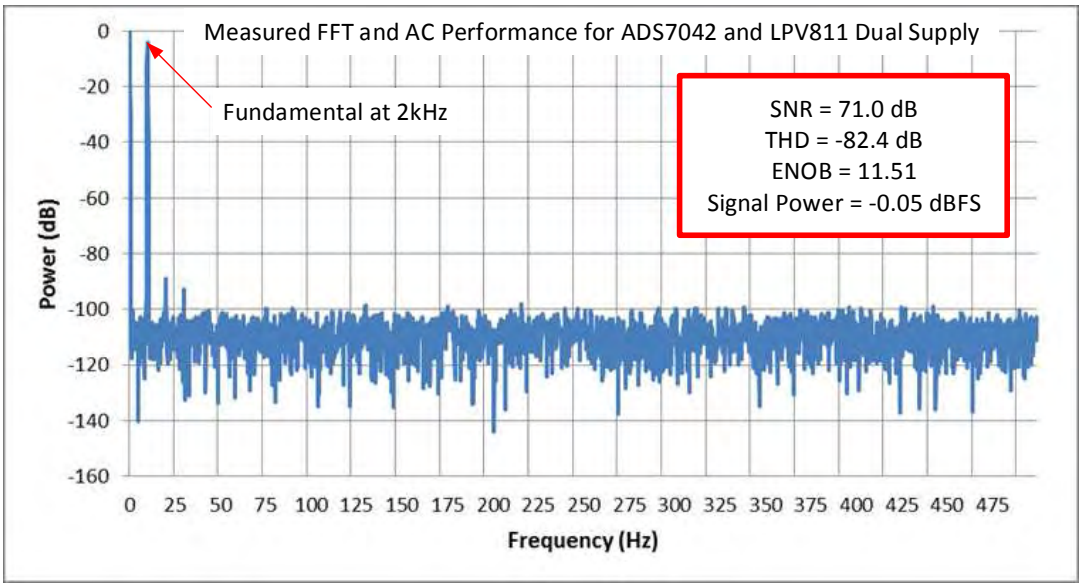
$$E_n = e_{n811} \times \sqrt{K_n \times f_c} = \frac{340nV}{\sqrt{Hz}} \times \sqrt{1.57 \times 1560Hz} = 16.8\mu V$$

Note that the calculated and simulated values match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM with a 10-Hz input sine wave. The AC performance indicates SNR = 71.0dB, THD = –82.4dB, and ENOB (effective number of bits) = 11.51, which matches well with the specified performance of the ADC, SNR = 70dB and THD = –80dB. This test was performed at room temperature. See *Introduction to Frequency Domain* for more details on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042 (1)	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD reference input range 1.6 V to 3.6 V.	www.ti.com/product/ADS7042	www.ti.com/adcs
LPV811 (2)	8-kHz bandwidth, rail-to-rail output, 450-nA supply current, unity gain stable	www.ti.com/product/LPV811	www.ti.com/opamp

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

(2) The LPV811 is also commonly used in low-speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across the entire ADC input range.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files (TINA)

Design files for this circuit – http://www.ti.com/lit/zip/sbam342.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Low-power sensor measurements: 3.3-V, 1-ksps, 12-bit, single-ended, single-supply circuit

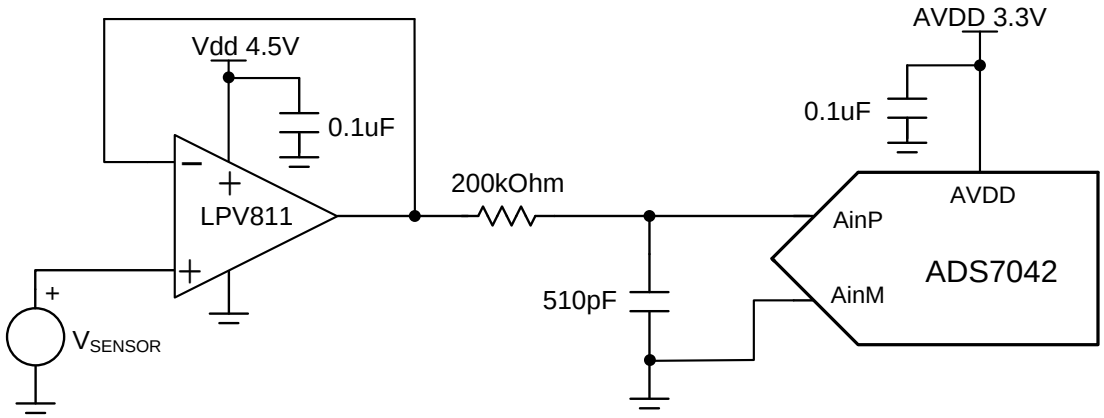
Reed Kaczmarek

Input	ADC Input	Digital Output ADS7042
VinMin = 0 V	AIN_P = 0V, AIN_M = 0V	000_H or 0_{10}
VinMax = 3.3V	AIN_P = 3.3V, AIN_M = 0V	FFF_H or 4096_{10}

Power Supplies		
AVDD	**Vee**	**Vdd**
3.3V	0V	4.5V

Design Description

This design shows an ultra-low power amplifier being used to drive a SAR ADC that consumes only nanoWatts of power during operation. This design is intended for collecting sensor data by providing overall system-level power consumption on the order of single-digit microWatts. *PIR sensors*, *gas sensors*, and *glucose monitors* are a few examples of possible implementations of this SAR ADC design. The values in the *component selection* section can be adjusted to allow for different data throughput rates and different bandwidth amplifiers. *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows a more sophisticated version of this circuit where the negative supply is connected to a small negative voltage (–0.3V). The single-supply version has degraded performance when the amplifier output is near zero volts. However, in most cases the single-supply configuration is preferred for its simplicity.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling (1ksps)	< 0.5·LSB = 402µV	41.6µV	N/A
AVDD Supply Current (1ksps)	230nA	N/A	214.8nA
AVDD Supply Power (1ksps)	759nW	N/A	709nW
VDD OPAMP Supply Current	450nA	N/A	431.6nA
VDD OPAMP Supply Power	2.025µW	N/A	1.942µW
AVDD + VDD System Power (1ksps)	2.784µW	N/A	2.651µW

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open loop gain specification. This is covered in the *component selection* section.
2. Select COG capacitors to minimize distortion.
3. Use 0.1% 20ppm/°C film resistors or better to minimize distortion.
4. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. Refer to the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select a low-power operational amp:
   - Supply current < 0.5µA
   - Gain bandwidth product > 5kHz (5 times the sampling rate)
   - Unity gain stable
   - For this cookbook, the LPV811 was selected. It has a 450-nA supply current, 8-kHz gain bandwidth product, and is unity gain stable.
2. Find op amp maximum and minimum output for linear operation

   $V_{ee} + 0V < V_{out} < V_{dd} - 0.9V$ from LPV811 Vcm specification

   $V_{ee} + 10mV < V_{out} < V_{dd} - 10mV$ from LPV811 Vout swing specification

   $V_{ee} + 0.3V < V_{out} < V_{dd} - 0.3V$ from LPV811 Aol linear region specification

   $0.3V < V_{in} < 3.4V$ Combined worst case

   NOTE: The linear range of the LPV811 is 300mV above ground. This means to design a system to guarantee a full linear range from 0V to 3.3V (full-scale range (FSR) of ADS7042), then a negative supply is required. This design shows that full-measured SNR and THD specifications of the ADS7042 are met without using a negative supply voltage. This testing was only at room temperature and for a more robust system; *Low-Power Sensor Measurements: 3.3V, 1ksps, 12-bit Single-Ended, Dual Supply* shows this design using a negative supply instead of ground.
3. Typical power calculations (at 1ksps) with expected values:

   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 230nA \cdot 3.3V = 759nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 450nA \cdot (4.5V - 0V) = 2.025\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 759nW + 2.025\mu W = 2.794\mu W$
4. Typical power calculations (at 1ksps) with measured values:

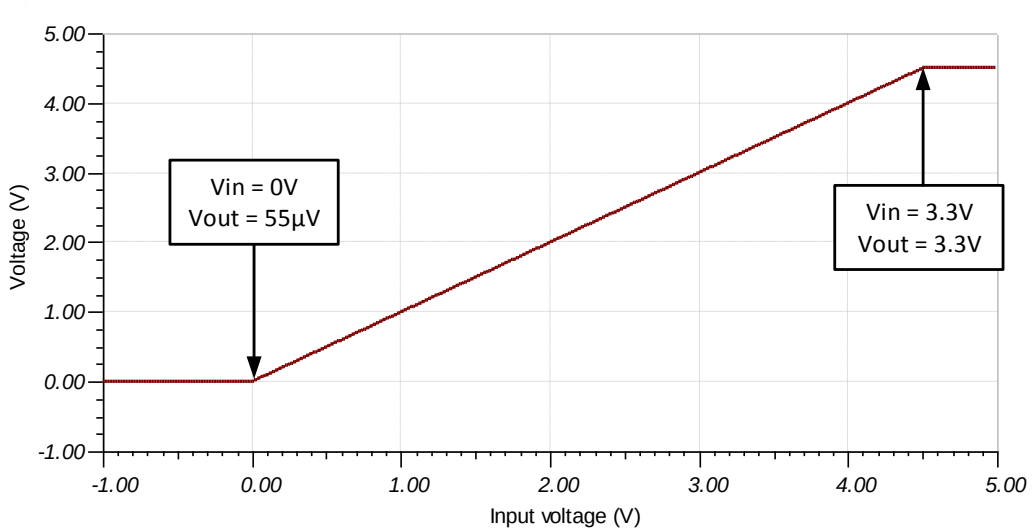
   $P_{AVDD} = I_{AVDD\_Avg} \cdot AVDD = 214nA \cdot 3.3V = 709nW$

   $P_{LPV811} = I_{LPV811} \cdot (V_{dd} - V_{ee}) = 431.6nA \cdot (4.5V - 0V) = 1.942\mu W$

   $P_{total} = P_{AVDD} + P_{LPV811} = 709nW + 1.942\mu W = 2.651\mu W$
5. Find Rfilt and Cfilt to allow for settling at 1ksps. *Refine the Rfilt and Cfilt Values* (a *Precision Labs* video) showing the algorithm for selecting Rfilt and Cfilt. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

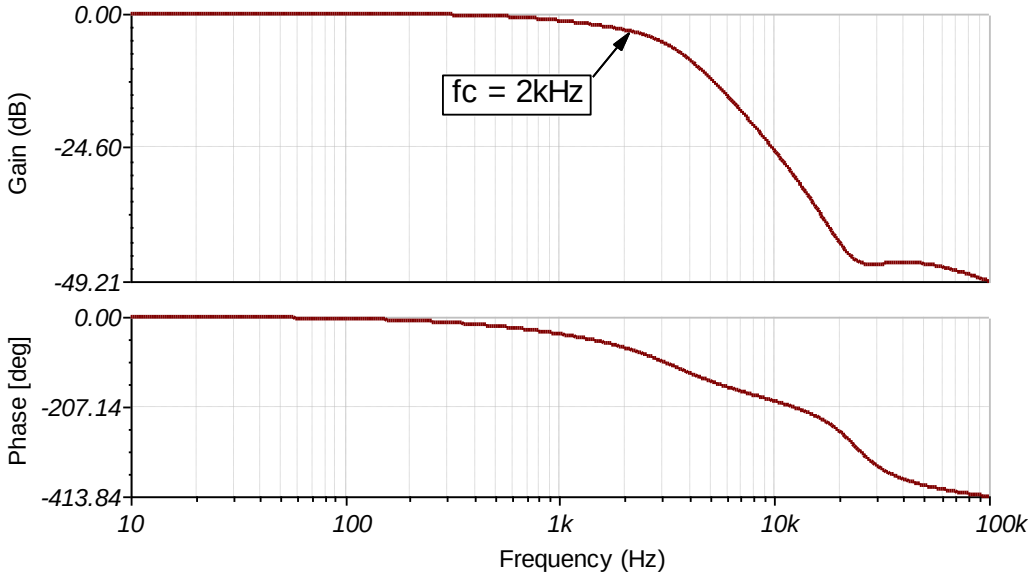
DC Transfer Characteristics

The following graph shows a linear output response for inputs from 0 to 3.3V. The FSR of the ADC falls within the linear range of the op amp.



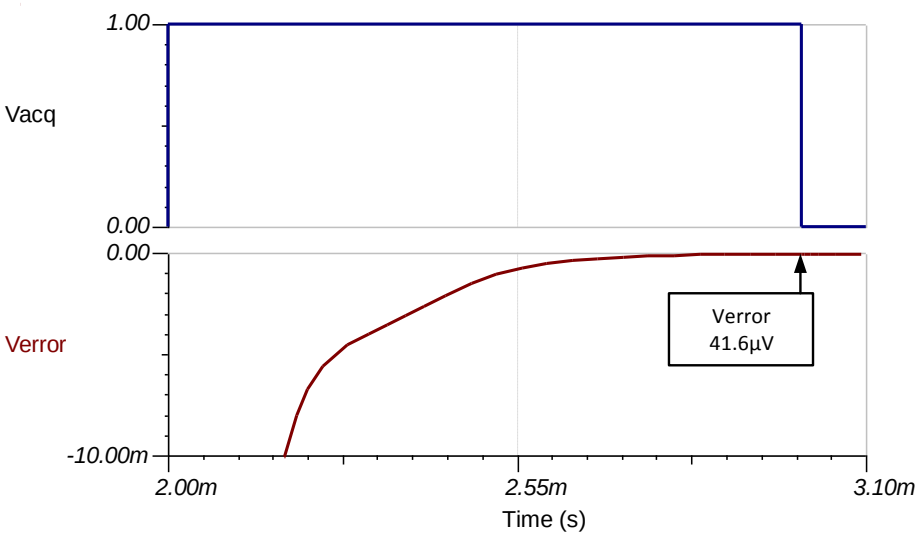
AC Transfer Characteristics

The bandwidth is simulated to be 7.02kHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow for settling at 1ksps.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 3-V DC input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (402µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



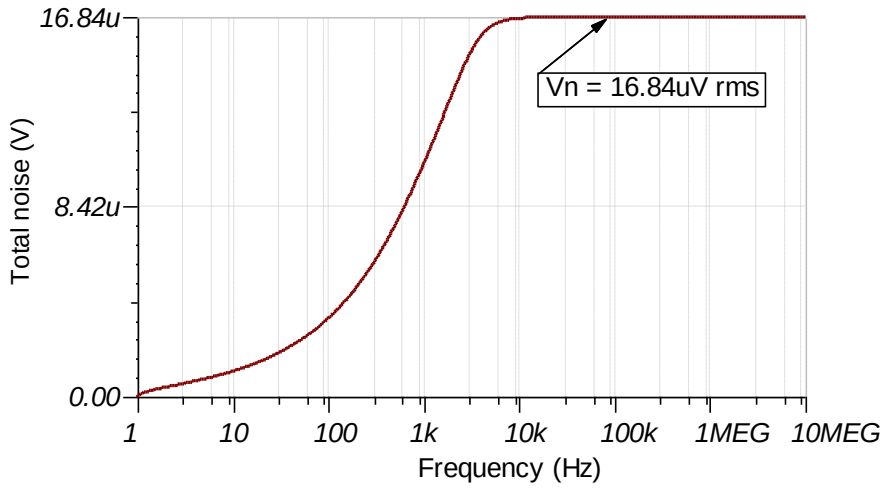
Noise Simulation

This section details a simplified noise calculation for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (200k\Omega) \cdot (510pF)} = 1560.3Hz$$

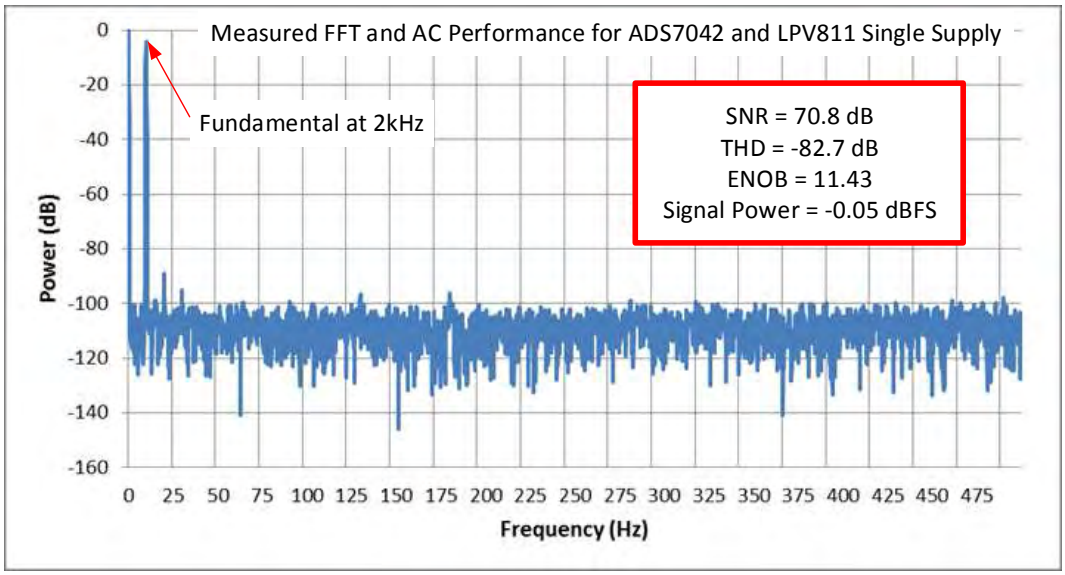
$$E_n = e_{n811} \cdot \sqrt{2 \cdot K_n \cdot f_c} = (340nV / \sqrt{Hz}) \cdot \sqrt{1.57 \cdot (1560Hz)} = 16.8\mu V$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS7042EVM-PDK. The AC performance indicates SNR = 70.8dB, THD = –82.7dB, and ENOB (effective number of bits) = 11.43, which matches well with the specified performance of the ADC of SNR = 70dB.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7042[1]	12-bit resolution, SPI, 1-Msps sample rate, single-ended input, AVDD, Vref input range 1.6 V to 3.6 V.	www.ti.com/product/ADS7042	www.ti.com/adcs
LPV811[2]	8 kHz bandwidth, Rail-to-Rail output, 450 nA supply current, unity gain stable	www.ti.com/product/LPV811	www.ti.com/opamp

(1) The ADS7042 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.
(2) The LPV811 is also commonly used in low speed applications for sensors. Furthermore, the rail-to-rail output allows for linear swing across all of the ADC input range.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Tina files for low-power sensor measurements - http://www.ti.com/lit/zip/sbam341.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.