Pushing the State of the Art with Multichannel A/D Converters

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INTRODUCTION

Like the rabbit decoy at dog races, the most demanding data-acquisition system requirements inherently stay ahead of commercial integrated-circuit analog-to-digital converter (ADC) performance. These extreme requirements have led to development—by both users and manufacturers—of many innovative "performance-enhancement" approaches that fulfill high-end data acquisition system needs while waiting for the next performance breakthrough.

One approach is to substantially increase sampling rate, reduce noise, or extend dynamic range by filling a converter "slot" with a design that uses more than one A/D conversion channel. This approach becomes increasingly practical as individual converter cost, size, and power requirements decrease for a given bandwidth and resolution, and as multiple converters are used (often packaged together) in a growing number of applications.

This article will discuss multichannel approaches using *signal averaging*, for increased resolution without loss of speed—and *time interleaving*, to increase sampling rates without loss of resolution. These approaches have resulted in products with improved specifications that embody these principles, such as the AD10678[1] 16-bit, 80-MSPS ADC—and the AD12500[2] 12-bit, 500-MSPS ADC.

Averaging

Signal-to-noise ratio (SNR), in dB, is a key performance metric for applications such as ultrasound and radar. The ADCs used in these systems can be affected by many external noise sources, including clock noise, power supply noise, and layout-induced digital noise coupling. As long as the square root of the sum of the squares (*root-sum-square*, or RSS) of noncorrelated noise sources is less than the inherent quantization noise of the ADC, output averaging can effectively lower the overall noise floor.

Systems requiring higher SNR often use digital post processors to sum the outputs of multiple ADC channels. The signals add directly, while noise from the individual ADCs—assumed to be uncorrelated—sums as the RSS, so summing improves the overall SNR. Summing the outputs of four ADCs improves the SNR by 6 dB, or 1 LSB. The AD6645[3] 14-bit, 80-MSPS ADC specifies an *effective number of bits* (ENOB) of 12. Figure 1 shows how four AD6645s can be summed to achieve two extra bits of resolution, and one extra bit of performance.

The input to each ADC consists of a signal term (V_S) and a noise term (V_N). Summing four noisy voltage sources results in a total voltage, V_T, which is the linear sum of the four signal voltages plus the RSS of the four noise voltages, i.e.,

$$V_T = V_{S1} + V_{S2} + V_{S3} + V_{S4} + \sqrt{V_{N1}^{\,2} + V_{N2}^{\,2} + V_{N3}^{\,2} + V_{N4}^{\,2}} \quad (1)$$

Since $V_{S1} = V_{S2} = V_{S3} = V_{S4}$, the signal has effectively been multiplied by four, while the converter noise—with equal rms values—has been multiplied by only two, thereby increasing the signal-to-noise ratio by a factor of two, or 6.02 dB. Thus, the 6.02-dB increase (ΔSNR) that results from summing four like signals gives rise to one additional bit of effective resolution. Since $SNR(\text{dB}) = 6.02N + 1.76$, where N is the number of bits,

$$N + \Delta N = \left[\frac{SNR(dB)}{6.02} - \frac{1.76}{6.02}\right] + \frac{6.02\,dB}{6.02} = N + 1 \quad (2)$$

Table I shows the increased SNR that results from summing the outputs of multiple ADCs. From the standpoint of simplicity, summing four ADCs is an obvious choice. Larger numbers may also be of interest in critical cases, but that would depend on other system specifications (including cost) and the amount of board space available.

Table I. Increase in SNR vs. Number of ADCs

Number of ADCs	Increase in SNR (dB)
2	3
4	6
8	9
16	12
32	15

The ideal SNR for a 14-bit ADC is (6.02 × 14) + 1.76 = 86.04 dB. The AD6645 data sheet specifies a typical SNR of only 74 dB, however, yielding an ENOB of 12 bits.

$$ENOB = \frac{(74 - 1.76)}{6.02} = 12\ bits \quad (3)$$

Thus, summing the outputs of four converters together recoups one extra bit, pushing the system-level ENOB to 13 bits (80 dB).

Systems like this require design effort, of course, in addition to system prototyping, qualification, and test development. The AD10678, however, integrates four AD6645s, a clock distribution system, and a complex programmable logic device (CPLD) that has been configured to provide a high-speed addition algorithm.

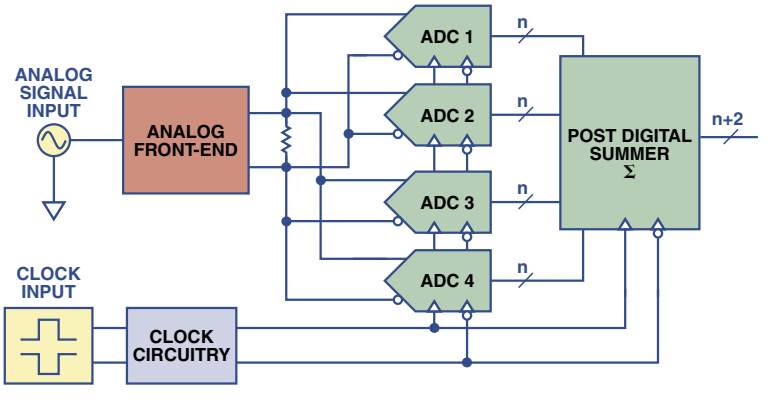

Figure 1. Summing four ADCs in parallel.

Fully tested and specified, the AD10678 is available—at a low cost—in a 2.2 × 2.8-inch PCB package. The FFT (fast Fourier-transform) plot shown in Figure 2 demonstrates the converter's excellent performance, providing 80.22-dB SNR with an 80-MSPS clock and 10-MHz analog input.

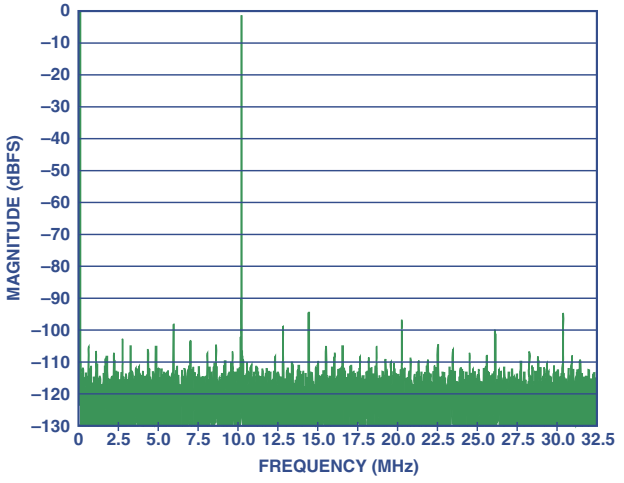

Figure 2. AD10678 FFT plot at an 80-MSPS encode rate and V_S = 10 MHz. SNR = 80.22 dBFS @ –1.33 dBFS.

In addition to the increased SNR, this architecture also provides improved dc accuracy. The offset and gain errors of the four devices are not correlated, so lower system offset and gain errors are achieved in the same way that noise is reduced. There is no improvement in linearity, however, and the *spurious-free dynamic range* (SFDR) of the system is actually dominated by the *worst* ADC.

The hardware for this implementation takes up more space on the PCB and dissipates four times the power, but it may still be advantageous to use this technique, compared to averaging the output of a single ADC that operates at four times the speed. Nevertheless, the increased number of signal samples at the higher speed will also serve to reduce normal-mode noise that arrives with the input signal. As processes improve, newer designs continue to push down the core power of the ADCs. Also, available quad and octal ADCs make multiple-ADC systems easier to implement and less space-intensive. The AD9229[4] quad 12-bit, 50-MSPS/65-MSPS ADC, for example, is available in a 48-LFCSP (7 mm × 7 mm) package. It dissipates only 300 mW per channel.

While it is feasible to improve specified SNR by standardizing on higher-level input voltages, this puts more stress on the design of the drive amplifier, and will degrade the *system-level* SNR, as both signal and noise will be amplified. A subtle benefit of the summing architecture is that the full-scale analog input doesn't have to be any larger than it would be with a single ADC.

Comparing hardware and software costs, the averaging approach may offer some benefits over digital filtering per se, but it can often make the job easier even when filtering is called for by overall system considerations that provide for cost-effective processing hardware and software.

Time Interleaving

Time interleaving of M ADCs allows the sample rate to be increased by the factor, M. By properly phasing each ADC's clock signal, the maximum sample rate of any standard integrated-circuit ADC type can be multiplied by the number of ADCs in the system. The proper clock phase required for each ADC can be calculated using the following relationship:

$$\phi_m = 2\pi\left(\frac{m-1}{M}\right), \text{where} \quad (4)$$

M = the number of ADCs

m is the specific ADC, i.e., $1 \le m \le M$

For example, a 4-channel system that employs the AD9444[5] 14-bit, 80-MSPS ADC, will create a 14-bit, 320-MSPS function when the individual clocks are properly sequenced in 90° (π/2) increments. Figure 3 captures the basic block diagram for this type of system. Time interleaving has already been leveraged for 12-bit integrated solutions in the AD12400[6]/AD12500 product family. Figure 4 displays the AD12500 block diagram, which includes all of the necessary ADCs, clock management, power supply, and digital post-processing functions.

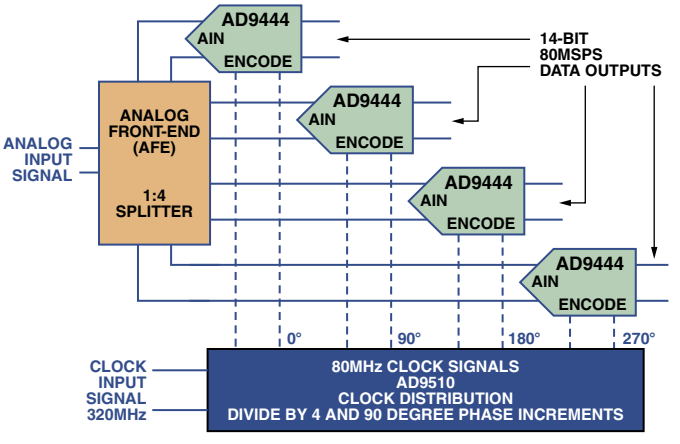

Figure 3. 4-channel time-interleaved ADC.

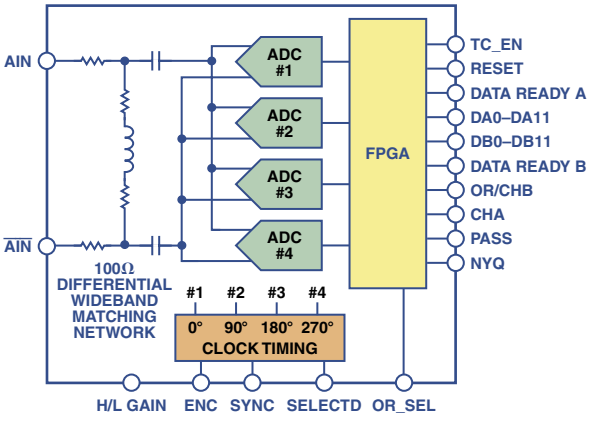

Figure 4. AD12500 block diagram.

The most obvious advantage of increasing the sample rate of an ADC system is the resulting increase in the analog sampling bandwidth, also known as the *Nyquist zone*. Increased Nyquist zones in digitizer systems offer numerous benefits: digital oscilloscopes achieve greater analog input bandwidth; software-defined radio systems increase the number of channels; and radar systems achieve greater spatial resolution. Figure 5 displays a simulated FFT plot for a 22-MHz tone on a 14-bit, 320-MSPS ADC system.

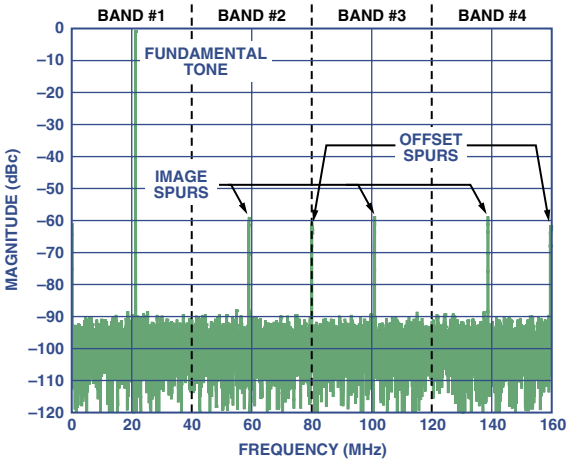

Figure 5. 4-channel time-interleaving FFT.

The FFT spectrum of this ADC system has a Nyquist zone of 160 MHz. For discussion purposes, the 160-MHz Nyquist zone can be split into four separate 40-MHz bands, each of which represents the Nyquist zone of a single AD9444 sampling at a rate of 80 MSPS. The fundamental tone of 22 MHz is in band #1. In addition to the fundamental tone, two types of nonharmonic distortion products can be observed in Figure 5—*offset spurs* and *image spurs*. The locations of these distortion products can be predicted for single-tone input signals with the following relationships:

$$f_{O1} = \frac{f_S}{4} \qquad f_{O2} = \frac{f_S}{2} \tag{5}$$

$$f_{X1} = \frac{f_S}{2} - f_{AIN} \qquad f_{X2,3} = \frac{f_S}{4} \pm f_{AIN} \tag{6}$$

These distortion products present a primary challenge associated with time interleaving. They are a direct result of channel-to-channel gain-, phase-, and offset-matching errors. In fact, the magnitude of these spurs is directly proportional to the magnitude of the errors.[7,8] For example, a 1% gain error in one channel would result in an image spur magnitude of 52 dBc. These spurs become problematic when a system's frequency plan involves the frequency bands in which the distortion resides. In such cases, the channel-to-channel matching behavior must be carefully managed in the development process.

If the system performance goal is 10-bit ENOB and the image spurs are the dominant factor, then the gain matching must be better than 0.1% and the phase matching must be better than 0.07 degrees (2 ps at 100 MHz)! From an implementation standpoint, many different error sources need to be reduced or eliminated to achieve this performance level.

The geometry of the traces from the analog and clock inputs of each ADC needs to be matched to ensure that the propagation delays are within their budgeted levels. While the clock function is relatively simple, it can also introduce errors that threaten these performance levels. Advanced technologies, such as silicon-germanium RSECL (*reduced-swing ECL*), can offer orders-of-magnitude improvement in rise-, fall-, and propagation-delay times when compared with those of their contemporary ECL counterparts. Depending on the input frequency, manual length trims may be used to overcome aperture delay errors as well.

Differences in power-supply-level behavior can create the need to use tight-tolerance supplies, such as linear regulators mounted in close proximity to the ADCs. Also, temperature-related behavior creates the need to manage the mechanical design to ensure tight temperature matching of the ADCs. The ADCs themselves may need to be screened for one or all of the following: gain, offset, aperture delay, and input-capacitance matching. Obviously screening four individual ADCs for tight tolerances in all their key parameters would be very difficult and costly! Such added complexity and increased risk must be weighed against the development and component cost goals of a system design.

For a narrow set of operating conditions, *an analog trim* process can be used to match ADC channels in time-interleaving ADC systems. But *digital post-processing* offers another approach to achieving tight channel-matching over a wider set of operating conditions. High-speed, configurable digital platforms, such as *field-programmable gate arrays* (FPGAs), have provided convenient vehicles for integrating advanced post-processing techniques—such as *Advanced Filter Bank* (AFB™).[9]

The AD12400 12-bit, 400-MSPS ADC comprises two high-speed ADCs, and leverages time interleaving and AFB to attain a level of performance that has not been achieved with individual commercial ADCs as of this writing. Figure 6 captures wide-bandwidth dynamic-range performance data, and compares analog and digital matching techniques. 14-bit matching (86 dBc) was achieved by "hand-tuning" the gain and phase for each channel at 128 MHz, but the performance degrades very quickly: 12-bit (74 dBc) performance is achieved for a bandwidth of only 20 MHz. On the other hand, when the digital matching is enabled, better than 12-bit performance is maintained over the entire 170-MHz test range—outstanding performance resulting from a well-designed digital post-processing technique.

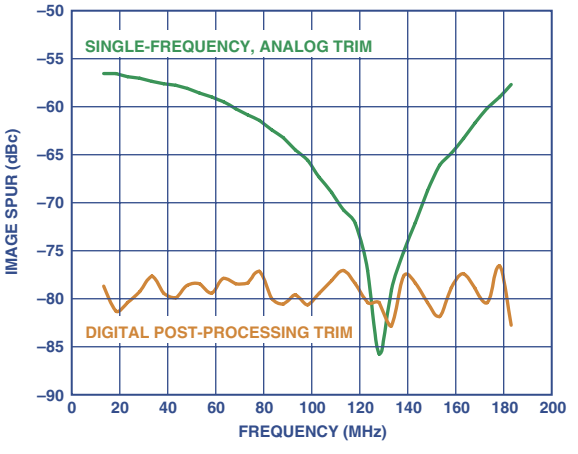

Figure 6. AD12400 wide-band image-spur performance.

Thus, when system designs require sample rates that are higher than commercially-available individual ADCs can handle, time interleaving is worth considering. If 10- to 12-bit performance is required over the entire Nyquist band, integrated solutions such as the AD12400 and AD12500 provide the benefits of time interleaving by successfully managing the difficulties associated with very tight channel-matching requirements.

Averaging vs. Time Interleaving

We have summarized here two techniques for achieving performance beyond the capability of currently available single ADCs. We've also shown examples of available high-performance multichip products achieved by using these techniques. The fact that such standard products are available—with design problems solved and standard specifications provided—may be sufficient for many readers. However, the following comments are for the benefit of users who may wish to further investigate the possibilities of these areas of performance using available standard single or multichannel uncommitted ADCs.

A common metric that can be used to compare topologies is SNR. If the AD9444 is the ADC of choice, and the system design calls for 40-MHz bandwidth and 79-dB typical SNR, one could consider both averaging and time interleaving. Both approaches would require the use of four AD9444 channels to achieve 5-to-6 dB of noise improvement over the AD9444's inherent SNR. Since both approaches can yield similar noise improvement, it's worth considering the secondary trade-offs to illustrate a typical design "trade-space."

First, the averaging approach will be less complex to implement than time interleaving. The clocks for the four ADCs in the averaging circuit can be derived from a resistive splitter, a magnetic splitter, or a simple 1:4 "fan-out" distribution IC. The time-interleaving approach requires the use of at least two D-type flip-flops to achieve the required division by 4 and 90° sequencing functions. In some cases, four additional flip-flops might be used to buffer the timing signal so as to maintain tight timing. In order to achieve the desired 6 dB SNR improvement, the time-interleaving approach is likely to employ a digital filter that requires real-time multipliers and adders (or a portion of processing time if available in the system design). The averaging approach only requires a real-time adder, resulting in a substantial reduction in digital logic.

The effectiveness of each noise-reduction technique must be carefully considered as well. In particular, the level of noise correlation and bandwidth in each channel must be understood. As the channel-to-channel noise correlation increases, the averaging approach becomes less effective. In systems for which the dominant noise source is jitter or phase noise, the noise-correlation risk can degrade the SNR improvement.

Time interleaving essentially spreads the noise over four times the bandwidth, then filters out the unused 120 MHz. In this case, the wideband characteristics of the noise spectrum must be studied and understood. If the spectral content of each channel's noise is uniformly distributed over the 160-MHz Nyquist band, this technique should yield a 6-dB SNR improvement. However, if the noise-energy distribution is more prominent within the 40-MHz band of interest, the SNR improvement goal of 6 dB might not be attainable.

Another important factor to consider when comparing these topologies is frequency planning. If a single-tone system is used, and the input frequency is above one-quarter of a single ADC's sample rate (20 MHz in the example), the 2nd, 3rd, 4th, 5th, and 6th harmonics fall outside of the 40-MHz band of interest. Therefore, they are reduced or removed altogether by the digital noise filter. In addition, the image spurs discussed above also fall outside of the band of interest and are thus filtered. In multitone systems, some of the components also fall out of the band of interest, lowering the total harmonic distortion of the system.

In conclusion, averaging offers a simpler approach to achieving 6 dB of noise improvement, but time interleaving offers several benefits that may warrant consideration when developing system architectures.

Uses of Multichannel Analog-to-Digital Converter Systems

Multichannel ADCs have played a substantial role in advancing data acquisition system performance. Ultrasound systems seeking higher definition sum up to 128 ADC channels for better signature. Digital oscilloscope manufacturers have developed ways to time interleave ADCs to accommodate their high sample rate requirements.[10,11] Other receiver systems have been able to use *frequency-division multiple access* (FDMA), employing multiple ADC channels to segment their frequency bands—reducing the input bandwidth requirements on each ADC and further increasing the dynamic range. As ADCs become increasingly available in multichannel integrated-circuit quad- and octal-type packages to save power and space, multiple-channel system architectures are being developed using them to provide functions or performance not previously available.

FOR FURTHER READING

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This article can be found at http://www.analog.com/library/analogdialogue/archives/39-05/multichannel.html, with a link to a PDF.