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Flexible Hopfield neural-network ADCs quash noise

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 A Hopfield network can convert analog signals into digital format and can perform associative recalling, signal estimation, and combinatorial optimization similar to the way a human retina performs first-level signal processing. This Design Idea explores the Hopfield-neural-network paradigm for ADCs.

Simple converters comprise one-layer neurons that accept analog inputs and generate digital-bit outputs; such neurons make up one form of adaptive- and distributive-processing networks. These neurons comprise voltage comparators driving either analog inverters or followers and fully connected feedback resistors from the analog outputs of the inverters or followers to the comparators (figures 1 and 2). Reference and analog-input voltages drive the neural networks, and digital outputs come from the comparators in the networks. Hopfield networks have learning capabilities; the circuit in this Design Idea can apply different adap-

tive-learning rules by using alternative comparator-inverter/comparator-follower schemes, conductance-node-layout schemes—reciprocals of the feedback resistances—between the input comparators, and bit-order readouts.

As the analog-input voltage increases, the circuit can produce either monotonically increasing (from a comparator-inverter scheme) or decreasing (from a comparator-follower scheme) bit-word outputs. Decreasing outputs are the complements of increasing outputs and suggest subtractive-bit operations. Further, you can shape the digital responses of the converters to analog-input voltages in varying degrees using different conductance-node layouts as part of rule adaptation. For further flexibility, reversing bit order for digital readouts allows for reflection of circuit responses about analog-input/digital-output characteristics.

You can simply state a few symbols and their meanings to construct the two converters. For energy functions,

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the resistive network conductances—synapse weightings (S) in the form of reciprocal resistances (R)—have the designations $S_{ij} = 1/R_{ij}$, where I is the I th input comparator, J is the J th feedback path to the I th comparator, and I does not equal J —that is, there is no self-feedback path of the comparator to itself. The conductance between the input terminal of the I th comparator and the reference voltage, V_R , has the designation $S_{IR} = 1/R_{IR}$. The conductance between the input terminal of the I th comparator and the analog-input-signal voltage, V_S , has the designation $S_{IS} = 1/R_{IS}$.

For graphical curve fittings, Y is the normalized output-bit variable, and X is the normalized input analog voltage from a nonzero average value (less than one) to one. A , B , and C are curve-fitting constants in the curve equation $Y = 1 - A \times (1 - X)^C$ and the complementary-curve equation $Y = A \times (1 - X)^C$, where A is a coefficient, B is the lower limit for X and is less than one, and C is a power con-

TABLE 1 INPUT VOLTAGE VERSUS OUTPUT WORD

Input analog voltage (V)			Output binary word	
Raw range	Normalized range	Average normalized range	Raw	Normalized
0 to 0.189	0 to 0.2855	0.1427	0	0
0.189 to 0.265	0.2855 to 0.4003	0.3429	1000	0.5333
0.265 to 0.378	0.4003 to 0.571	0.4856	1100	0.8
0.378 to 0.662	0.571 to 1	0.7855	1110	0.933
More than 0.662	1	1	1111	1

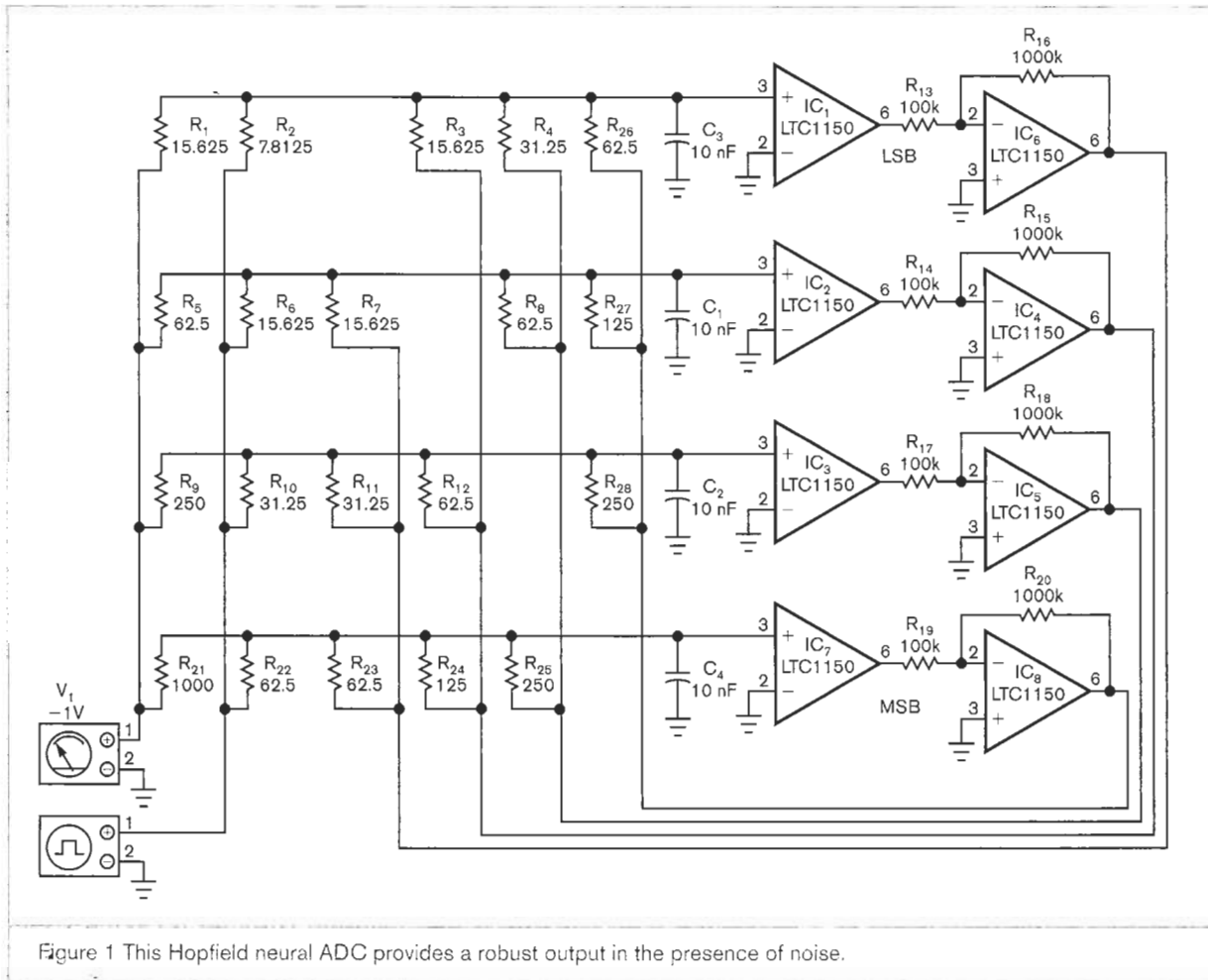


Figure 1 This Hopfield neural ADC provides a robust output in the presence of noise.

stant. For bit-pattern readout reversals, you can have the curve equation $Y=A \times (X-B)^C$ and the complementary-curve equation $Y=1-A \times (X-B)^C$.

Figure 1 shows a 4-bit neural ADC employing voltage inverters that comparators feed. The comparators connect with their positive terminals joined to input nodes and with their negative terminals grounded. The bases of this network are inverse factors of one-half—that is, reciprocal factors of two—input-node conductances $S_{ij} = -1 \times 2^{(2-i-j)}$, where the -1 factor comes from negative feedback through the related resistor; $S_{iR} = 2^{(1-2 \times i)}$; and $S_{iS} = 2^{(1-i)}$. To determine node resistances, choose a maximum node resistance of 1000Ω corresponding to a minimum conductance of 0.0078125 , and a minimum node resistance of 7.8125Ω corresponding to a maximum conductance of one. Calculate all oth-

er resistances from the ratios between the extremes of conductances. Using these values, you can construct Table 1. The table lists bits ranging from the most significant bit to the least significant. The table shows that the digitization process is inaccurate in that it is not linear with input voltage and with many intermediate bit words missing. But the process is precise because it is repeatable over sizable input-voltage ranges. From the table, you can derive the following curve-fitting equation: $Y=1-1.6243 \times (1-X)^{3.1508}$. When X is over the normalized range of 0.1427 to 1 , $A=1.6243$, $B=0.1427$, and $C=3.1508$. The Y equation is essentially cubic, and it quantitatively shows the highly nonlinear nature of the digitization process. You can obtain a “flipped” mirror—that is, not a true mirror, or pseudoscopic—version of the curve of the straight line on a

normalized graph by reversing the bit-order readout from the circuit so that the resulting curve equation would be: $Y=1.6243 \times (X-0.1427)^{3.1508}$.

Without analog-input-voltage transformation, such as the use of look-up tables or logarithmic amplifiers to process the input voltage, or digital corrective logic, digital responses from simple Hopfield neural converters are nonlinear and crude. However, these responses are still possibly useful for such applications as associative memory and pattern classification because of robustness in output precision.

Indeed, because of output digital stability, the Hopfield neural converter can allow for unwanted analog-input-signal noisiness or variations. This scenario is in strong contrast to conventional interface circuits between analog-transmission media and digital-

computing machines. This Design Idea shows that flexible circuit adaptability can exist in producing various forms of stable digital outputs from neural

ADCs depending on a designer's needs for neural-network-signal processing. This adaptability can be in the forms of various input-node-conductance

layouts; comparator/inverter and comparator/follower combinations; and the selected order of bit-readout patterns from the comparators. **EDN**

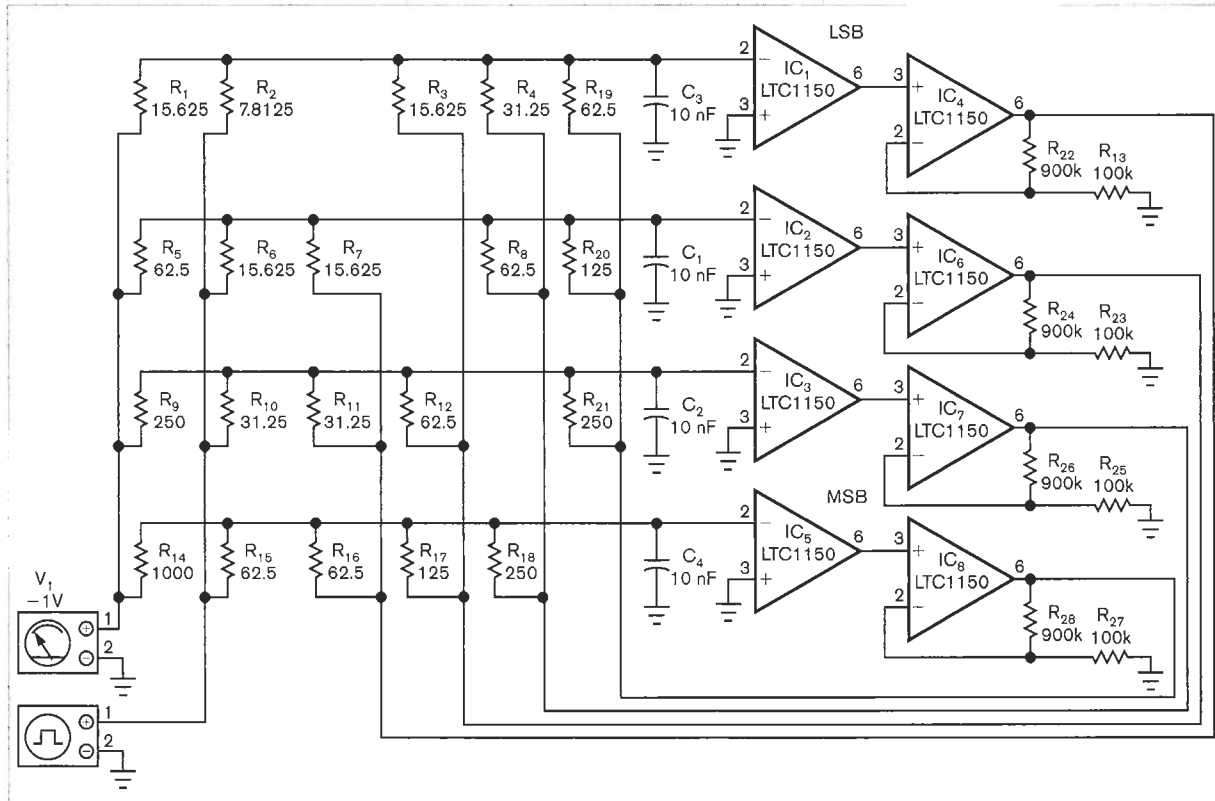


Figure 2 This version of the Hopfield neural ADC features inverted bit outputs.