Oversampling ADCs for 16-Bit Resolution

2.5-MHz AD9260 (>1-MHz inputs)
1.2-MHz AD7723 (≤460-kHz input)

Analog Devices has introduced two new CMOS high-speed 16-bit oversampling A/D converters for handling wideband signals with wide dynamic range in applications where low power, small footprint, and low-cost monolithic solutions are essential.

The **AD9260**, using a 20-MSPS clock in an 8× oversampling mode (Figure 1), can output 16-bit signals at a 2.5-MHz word rate, providing a 1.01-MHz signal passband with 0.004-dB ripple and 100-dB SFDR (spurious-free dynamic range). The **AD7723**, with a 19.2-MHz clock, and using 16× oversampling, can provide 16-bit performance for 460-kHz inputs, at a 1.2-MHz output word rate. In less-demanding applications, to conserve battery capacity, the AD9260's power requirement can be reduced from 585 mW to 150 mW; and the AD7723's 500-mW can be halved. The AD7723 also has a 200-µW standby mode. The table provides a few additional points of comparison.

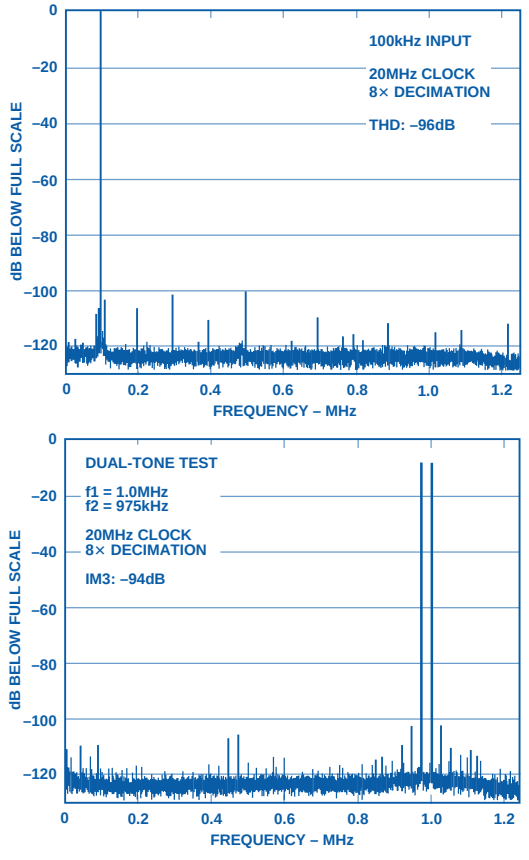

Figure 1. AD9260 SFDR: single (100-dB) and dual-tone (95-dB) performance.

Both devices have internal references; the AD7723 provides 2.5 V, and the AD9260's reference has both 1.0 and 2.5-V modes. They are housed in 44-pin QFP packages, the AD9260 in MQFP, and the AD7723 in PQFP. Both will operate with +5-V analog and digital supplies, but the AD9260's digital supplies are specified in +3 V operation for power economy and minimum noise. Evaluation boards are available for each type.

Characteristic	**AD9260**	**AD7723**
Resolution, bits	16	16
Sample rate, MSPS	20	19.2
Output data rate, MSPS @ OSR	2.5 @ 8×	1.2 @ 16×
Oversampling ratio selection	1×, 2×, 4×, 8×	16×, 32×
Filtering characteristic	LP	LP, BP
Power dissipation, mW (max)	630	500
Dissipation reduction, mW	to 150	50%, 200 µW
Internal reference, V	1,2.5	2.5
SFDR, dB (low-frequency signals)	100	90
SNR, dB, 1.2 MHz thruput	88.5 typ	83 min
44-pin package	MQFP	PQFP
Faxcode,* **or circle** (reply card)	2155, **6**	2103, **7**
Price, USD (1000s)	$39.90	$23

Typical applications: 16-bit performance at wide bandwidths and high sampling rates is especially useful in communications equipment. A key example is in echo cancellation in modems for full-duplex communications, where the same channel is shared for simultaneously transmitted and received signals (Figure 2). In such equipment, a strong transmitted signal (and its echoes) and a weak received signal may be in close proximity in time or frequency. In order to sort them out using DSP techniques, the signal must first be converted to digital without losing small components in noise and without generating spurious components (spurs) by distorting large components. This calls for a wide-dynamic-range device that has high SFDR with low distortion (both harmonic and intermodulation) and low quantization noise.

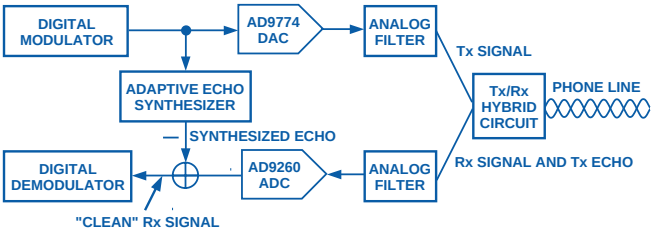

Figure 2. Full-duplex digital error-cancelling modem.

The AD9260 has been successfully evaluated for wire-line and wireless communication applications, such as wideband cellular base stations, echo cancelling ADSL modems, single-pair HDSL modems, navigational systems, and broadband CDMA base stations. The high speed, dynamic range, low power, high-level integration, and low price of both devices make them useful in sonar, radios, instrumentation, test equipment, and in other signal-capture and -analysis applications. When its throughput is suitable, the AD7723's low cost and special properties are useful in bandpass applications, where a standby condition is necessary, where choice of serial or parallel operation is required, and/or where an oversampling ratio of 16 or more is desirable.

ARCHITECTURAL CONSIDERATIONS

Sigma-delta A/D converters traditionally offer high resolution at low cost for industrial, audio and low-frequency communication applications, but the tradeoffs between resolution and speed have generally limited bandwidths to below 200 kHz. Second-order single-bit modulators can meet the high resolution requirements of the industrial market, but at the cost of large oversampling ratios (OSR) and inherent unsuitability for high output-data-rate (ODR) applications.

*For data, consult our Web site, **www.analog.com** ("Product Center"), AnalogFax line **800-446-6212** (with Faxcode), or use the reply card.

Increased bandwidth is typically pursued with single-loop modulators by increasing the order of integration in the loop. For example the AD7722, which uses a 7th-order modulator, has 90-dB SNR at a 195-kHz output data rate, while being clocked at 12.5 MHz. To improve bandwidth by increasing the ODR rate of such converters would be difficult because it would require a more costly manufacturing process and power-hungry integrating amplifiers capable of settling to the required accuracy. Thus practical considerations limit the single-loop single-bit architecture to output data rates of 100-200 kHz.

To extend the resolution/bandwidth frontier, new architectures are required. Though the details are beyond the scope of this brief discussion, it is worth noting that the AD9260 ventures into new ground to achieve a state-of-the-art *tour de force* solution; and AD7723 successfully implements an advanced cascade design approach. The single-bit DACs used in most of our sigma-delta ADCs, although guaranteeing excellent distortion, generate large amounts of quantization noise that degrades SNR. By using multi-bit DACs within the modulator and employing shuffling techniques to randomize the non-linearity of the DACs, both high resolution and good distortion are realized in the AD9260. To reduce the effect of quantization noise further, in both the AD9260 and AD7723, the quantization noise added by the DACs is first measured and then subtracted digitally.

FEATURES AND PERFORMANCE

The **AD9260** (Figure 3) achieves both high dynamic range and very wide input signal bandwidth at a modest 8× oversampling ratio by combining sigma-delta techniques with a high-speed pipelined A/D converter. The differential analog input is fed into a 2nd-order sigma-delta modulator employing a 5-bit flash quantizer and 5-bit feedback. At the same time, a 12-bit pipelined A/D converter quantizes the input to the flash converter with greater accuracy. The loop architecture provides the equivalent of a stable second-order loop with 12-bit quantizer and 12-bit feedback, free from idle tones and other idiosyncrasies sometimes associated with higher-order single-bit ∑-Δ modulators.

The modulator output is fed into a three-stage decimation filter, and a MODE control allows the output to bypass any or all stages,

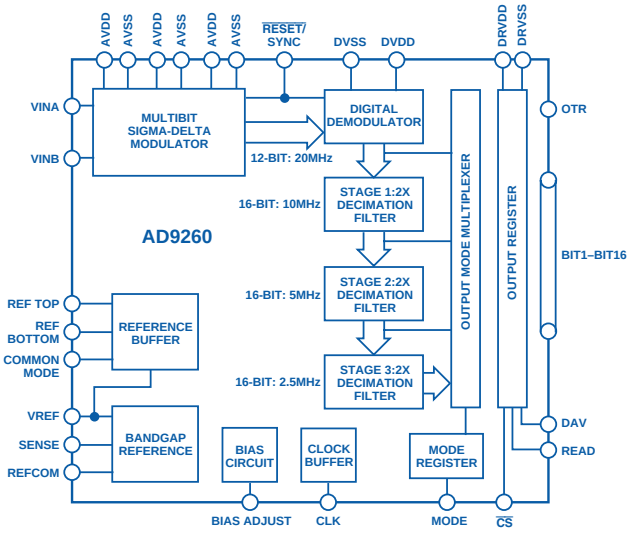

Figure 3. AD9260 block diagram.

providing the choice of output at the clock rate (1×), or decimated by 2×, 4×, or 8×. The decimation filter's stopband rejects frequencies between 1.25 and 18.75 MHz, substantially easing antialiasing requirements on the analog input. A reference, with buffer, is provided on-chip. In the 2.5-V mode (optimum noise & distortion), 4-V p-p full-scale differential inputs can be handled. In the 1-V mode, the range is 1.6 V p-p. Arbitrarily programmable values are also available via an external resistive divider. A bias adjustment scales the power proportionally to the clock rate, permitting reduced dissipation (and performance) over clock rate reduction from 20 to 5 MSPS and 585 to 150 mW.

The **AD7723** (Figure 4) uses a number of cascaded first and second-order sigma-delta modulators, each comprising one or more integrators, a comparator, and a 1-bit DAC. The first modulator performs the actual analog-to-digital conversion, and the modulators that follow, with their correction logic, successively remove the quantization noise contributed by the preceding modulators and at the same time lower their own noise floor by shifting their own quantization noise upward in frequency. To meet the performance requirements of the AD7723, 5th order noise shaping was employed, resulting in an output that contains only the input signal and 5th-order shaped quantization noise from Modulator 4.

The AD7723 can be clocked at up to 19.2 MHz. A 5-stage FIR decimation filter is used to both reduce the output data rate and remove the out-of-band quantization noise. The ADC output can be taken from either the 4th or the 5th filter. Data from the fourth filter has an output data rate (ODR) of 1.2 MHz and a SINAD of 85 dB, while data from the 5th filter has an ODR of 600 kHz but a higher SINAD of 88 dB. The 5th filter can also be configured as a high-pass filter, allowing the AD7723 to be used as a band-pass ADC.

The AD7723 provides flexible serial or parallel interfacing, high oversampling rate (OSR) to minimize anti-alias filter complexity, and accepts unipolar or bipolar inputs for simple interfacing to input drive circuits. Operating temperature range is –40 to +85°C.

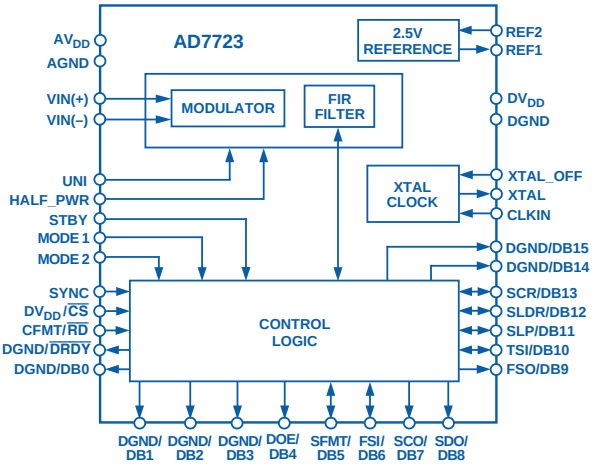

Figure 4. AD7723 block diagram.

The AD9260 was designed by a team comprising members of our high-speed converter group, in Wilmington, MA, led by Todd Brooks. The AD7723 was designed by Peter Hurrell (who also furnished much of the above text) and Colin McIntosh, of our design group in Newbury, England.