Power Digital-to-Analog Conversion Using Sigma-Delta and Pulse Width Modulations

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***Abstract* - Practical Digital-to-Analog converters with more than 18-bit resolution (SNR>110dB), reduced analog complexity and alternatively capable of directly driving a power amplifier achieving an outstanding overall power efficiency greater than 80% are reported. This paper overviews the emerging importance of power D/A converters while introducing the basic concepts of class-D amplification and presenting four different approaches to realize such a conversion based on enhanced PWM mapping and Sigma-Delta modulation.**

I. INTRODUCTION

The concept of power digital-to-analog conversion was introduced in the early 1990's [1] and was originally developed from research completed on achieving high efficiency digital audio amplification. Digital audio components are now commonly found in everyday life, for example in the form of compact discs (CDs), digital video discs (DVD), MP3 portable players, personal digital assistants (PDA), wireless telephones, and others. Conventionally, reproduction of the sound requires conversion from digital form to analog followed by inefficient analog linear amplification (class A and/or B). Several attempts have been made to implement an efficient power amplifier able to directly couple to a digital input signal [2, 3, 4 & 5], removing the need to convert to analog first. Because of its digital input and analog output such an amplifier is also referred to as a power D/A converter and its applications can go well beyond the audio signals.

Along this paper the reader will find how high quality D/A conversion with high resolution and linearity can be obtained based on power digital amplifiers. The fundamentals and historical development of power digital-to-analog conversion are presented in section II. From there, section III introduces some of the best performance modern archi-

tectures while section IV describes one of the latest and most promising approaches. Finally, limitations and predicted research on the topic is discussed in section V.

II. Basic Concepts

A digital power amplifier is to be understood as a power amplifier operating in class-D mode. The class-D mode of operation was invented by Baxandall in 1959 [6] and consists of a simple two-level signal driving a power switch. The two level signal is a high frequency PWM signal containing the modulator signal in the low frequency portion of the spectra, the control signal is recovered through linear, passive low pass filtering which removes the carrier frequency. When an ideal switching characteristic is assumed, this discontinuous mode of operation results in an outstanding power efficiency of 100%.

While in a traditional class AB amplifier the transistors operate in the linear region acting as variable resistor network between the supply and the load, and the voltage that is dropped across the transistors is lost as heat, the output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between.

Early attempts to develop switching amplifiers were limited by the vacuum tubes' large voltage drops and low current capabilities, which reduced the amplifiers' efficiencies and limited their output power. In the late 1960's, bipolar transistors became a practical alternative to vacuum tubes and allowed the implementation of switching amplifiers with very high efficiencies at low frequencies. However, using bipolar transistors at the required frequency to capture the spectra of a control signal with a larger bandwidth (for example, 20KHz audio signals bandwidth requires at least 100KHz switching frequency) results in excessive switching losses that eliminate the class-D amplifier's efficiency advantages [7]. In the 1980's MOSFET became available that could meet both the switching speed and conduction-loss requirements to effectively implement class-D amplifiers. This and others advances in semiconductor technology made possible the first commercially available integrated analog class-D amplifiers [8],[9],[10].

The basic class-D system schematic is illustrated in figure 1. An incoming signal is applied to one output of a comparator, and a triangle (modulating) waveform is applied to the other comparator input. The output of the comparator is a pulse width modulated,

PWM, signal that controls a power switch comprising a MOSFET bridge which reconstructs the control signal at a higher voltage level. The resulting waveform is passed into an analog passive low pass filter which recovers the original analog input signal and filters the high frequency carrier.

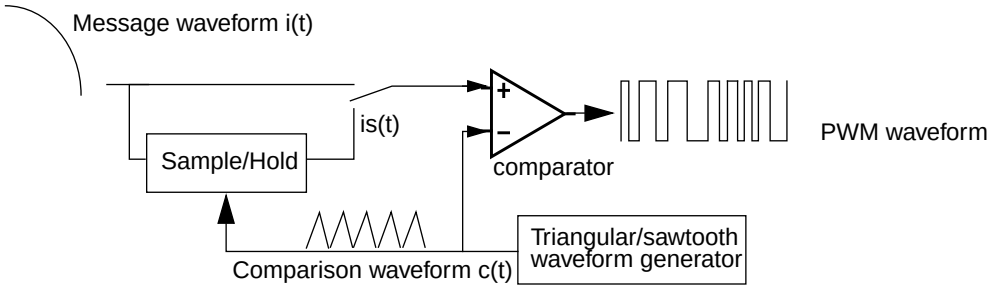

Fig. 1. Analog PWM/Class-D amplifier schematic.

Figure 2 shows an example of PWM waveforms from a matlab simulation.

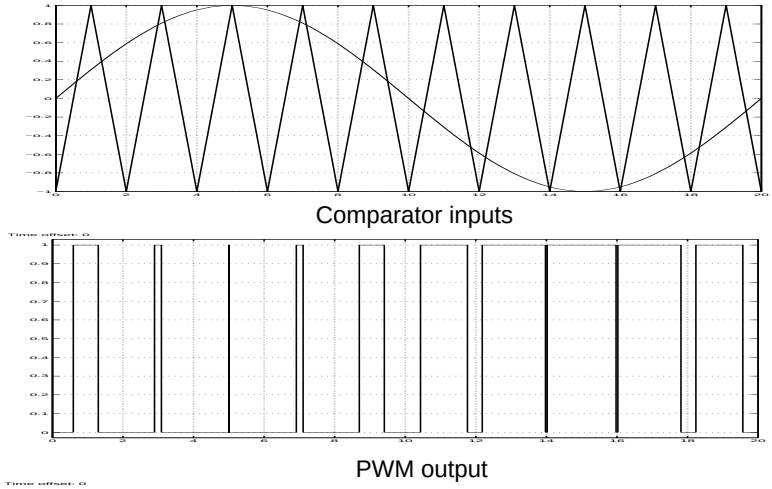

Fig. 2. Pulse width modulation with natural sampling. Signal=5KHz, triangle comparison waveform= 100KHz (from Matlab simulations).

Most of the discussion up to this point has been regarding class-D amplifiers because it is a necessary background to introduce the power D/A concept.

Since today audio is increasingly derived from digital sources, the motivation to find a digital alternative to analog power amplification has gained more and more attention and along the way a new technique for digital-to-analog conversion (D/A) has been developed based on class-D power amplifiers. Because of their switching behavior, class-D stages are driven with a binary signal and thus can be conceived as being digital

themselves from a signal theoretical point of view.

The challenge now arises in how to generate the binary high frequency switching waveform from the digital code to replicate the original analog signal. The straightforward approach is to apply direct PCM-to-PWM conversion (applying uniform sampling) together with a LPF as demodulator which actually serves as D/A converter. This is an analogy to the classical analog concept of class-D amplification. However, the analysis of the spectral properties of uniformly sampled PWM reveals that this process introduces harmonic and non-harmonic distortion terms (PWM is inherently noisy [11]) as it is proven in figure 3.

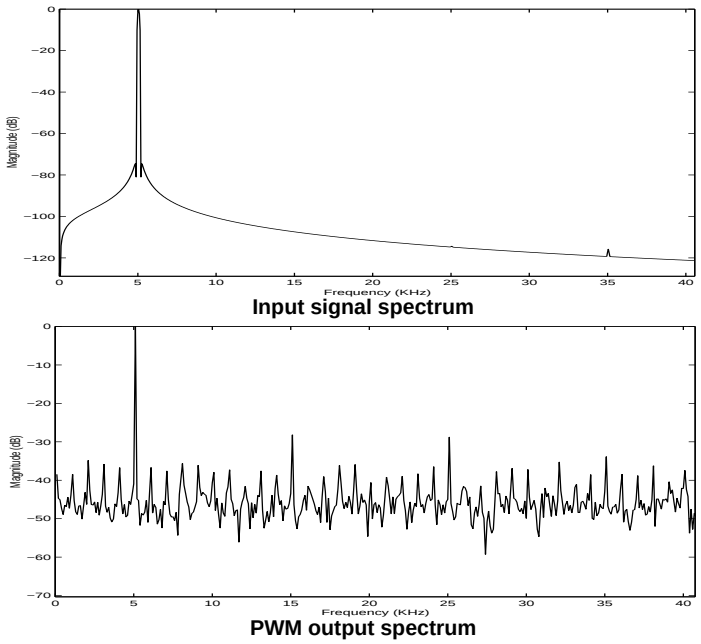

Fig. 3. Spectra from the uniform PWM process shown in figure 2 (Matlab simulation).

Therefore, to obtain an overall linear transfer characteristic (i.e. a wideband amplifier/converter) it is a requirement that within the baseband of the switching signal there must not be any other signal content than that of the original input signal. The properties of the binary switching signal (intermediate signal) depend on the process chosen for modulation and demodulation. The resulting generalized structure of a digital amplifier is shown in figure 4.

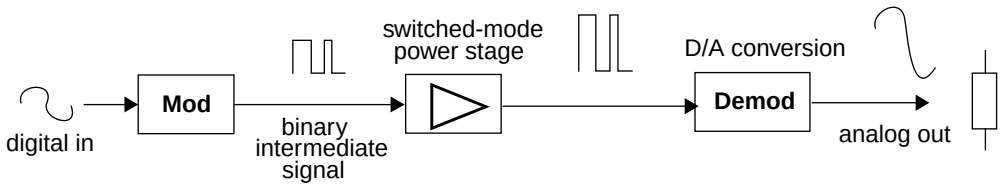

Fig. 4. Generalized structure of the digital power amplifier (power D/A conversion).

Since a minimal power loss must be accomplished by the demodulator, a passive L-C type low pass filter (LPF) is well suited. The modulator process must be such that the low pass filter serves as exact demodulator of the intermediate signal, this in turn must have a baseband being exactly free of any distortion terms (harmonic and no-harmonic).

A lot of effort has been taken to overcome the deficiencies of direct PCM-to-PWM in order to minimize distortion terms in the baseband. The early publications [12] presented conceptual system architectures which were clearly impractical, relying on modulator clock speeds of tens of GHz. The classical approach here is to considerably increase the ratio of the carrier to signal frequency. The incorporation of Noise Shaping techniques brought this down to several tens of MHz but distortions due to the underlying modulation process were still there. More appealing is the approach to modify or to preprocess the input signal and then apply it to a pulse width modulator. This approach is called enhanced concept of the D/A power amplifier as shown in figure 5 and explained in section II.

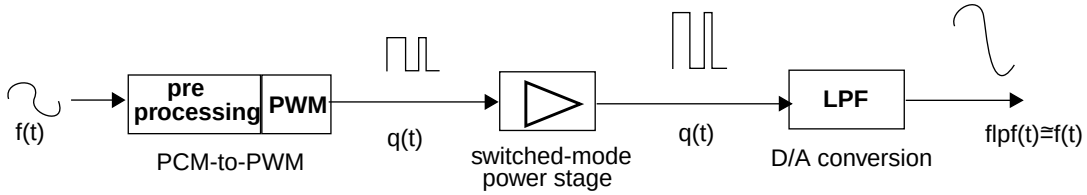

Fig. 5. Enhanced concept of the D/A power amplifier.

A further approach, as suggested in [1], applies SDM (Sigma Delta Modulation) within a digital power amplifier strategy. A power DAC based on this concept is described in section II.

In the last the last three years, some companies have launched digital power amplifiers based on these techniques (most notably [13], [14]) with extraordinary performance.

III. MODERN ARCHITECTURES

3.1 The enhanced concept Power DAC

Experimental results based on this technique proposed in [1] & [11],demonstrate superior performance when comparing spectral characteristics to equivalent resolution (16-bit) existing PAM D/A converters. High SNR (>98dB) and high linearity (second harmonic at -108dB) have been achieved, and in listening tests additional noise was not found to be noticeable.

The overall scheme in which the core conversion process is PWM is shown in figure 6. This figure also shows the additional components needed to turn the PWM DAC into a power amplifier.

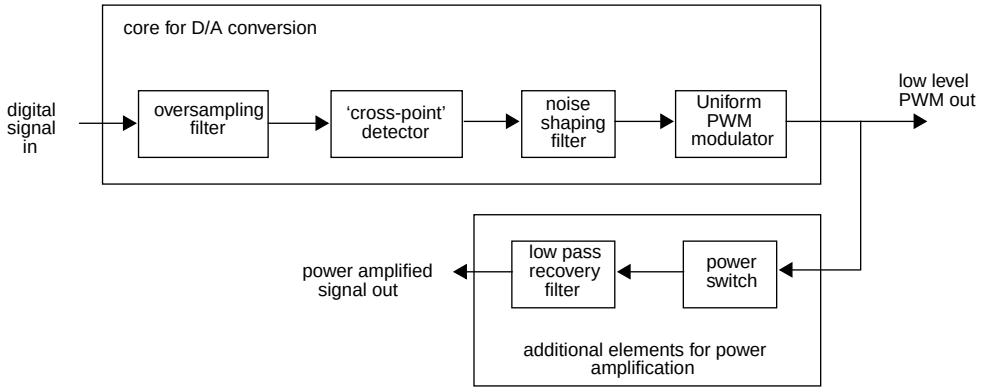

Fig. 6. Complete scheme for high-resolution power DAC using enhanced PWM concept.

First, the digital input is processed by an oversampling filter which effectively increases the sampling rate (e.g. from 44.1KHz to 325.8KHz). The primary purpose of this stage is to help to reduce distortion. The 'cross-point detector' is a linearizer which improves the distortion performance of the system. When the original analog input is compared to a triangular or sawtooth waveform to generate the PWM signal, the process is called NPWM (Natural-PWM). However, in this case the original analog waveform is not available but only its samples (taken from the PCM input), thus only UPWM (Uniformly-sampled-PWM) can be done. Figure 7 shows the difference between NPWM and UPWM. It is clear from figure 7 that the NPWM and UPWM 'cross-points' are different introducing some distortion to the resulting UPWM signal. What the 'cross-point detector' block does is to approximate the UPWM to a NPWM process by calculating the time

instant at which the continuous waveform would cross the comparison waveform. The calculation is done interpolating the data from the PCM samples using some numerical method. This process has been known as Pseudo-NPWM and really helps to improve final SNR.

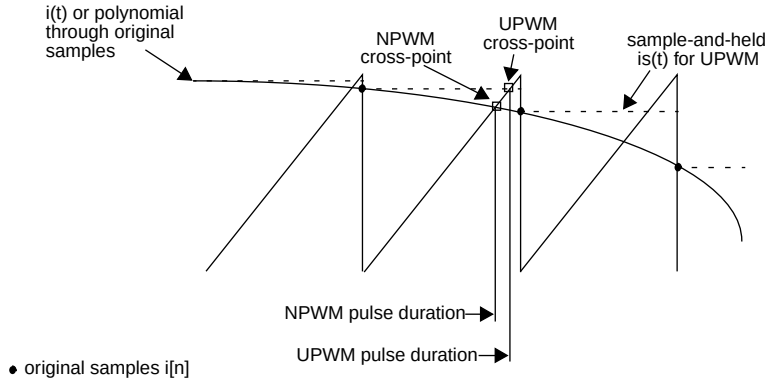

Fig. 7. Principles of Pseudo-NPWM.

The need to increase the signal's sampling rate (oversampling) in order to reduce distortion has been already mentioned. But a practical problem now arises. Assuming that an 8-times oversampling will give an acceptable level of performance for 16-bit signals, if the audio sampling frequency is 44.1KHz, this is going to be raised to 8 X 44KHz = 352.8KHz. There are 2^{16} (= 65536) different possible pulse lengths, so the clock controlling the modulator must operate at 352.8KHz x 65536 = 23GHz, which is certainly impractical. The solution to this problem can be achieved by using Sigma-Delta modulation (noise shaping). The oversampled 16-bit data is truncated by a quantizer Q after it has been added to the feedback error from previous truncations which has been passed through a shaping filter H(z). The operation of such a nonlinear system has been much investigated over recent years, as described in references [15], [16].

Thus, if 8 bits remain after truncation, the 'extra noise' level introduced will be about 50dB below peak signal level. The aim is to noise-shape the 'extra noise' out of the band of interest. The extra noise is squeezed out of the wanted band (low frequencies) and appears (amplified) at higher frequencies not occupied by signal. The noise transfer function of the filter used (1-H(z)) is a cascade of differentiators. In the simplest form, H= Z^{-1}, i.e. (1-H(z)) is a first order differentiator. If noise shaping is applied to reduce the wordlength to 8 bits, the frequency of the clock needed to drive the modulator is now just

352.8KHZ x 2^8 = 90.3MHz.

Finally the PWM block can be implemented by using counters to determine the position and width of the pulses. The order of the noise shaping filter may be two or four depending on the quality of the interpolation in the cross-point detector block. Now the low-level PWM output can be used just like the output of any other DAC (after suitable filtering) or alternatively, it can be used to control a class-D power switching stage as shown in figure 6.

3.2 Sigma-Delta Power DAC

A next major development was in ways to use Sigma-Delta Modulation to convert an oversampled PCM input signal into a 1-bit code suitable for controlling a power switch. Sigma-Delta modulation systems are widely used in analog-to-digital (A/D) and digital-to-analog (D/A) converters to generate a single bit (two level) code which represents the input signal in the low frequency portion of the spectrum. This form of modulation is also suitable for power D/A conversion using the methodology of figure 8.

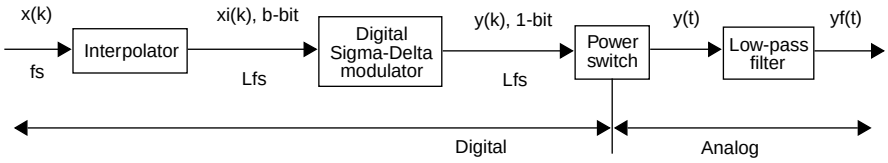

Fig. 8. Sigma-Delta Power DAC.

The modulator employs feedback around a 1-bit quantizer to redistribute the quantization noise at high frequencies outside the input signal spectrum. For power D/A conversion the essential features are that the SDM should generate a 1-bit code with high resolution in the baseband (> 16-bits for audio) and a low average pulse repetition frequency (PRF) to reduce power dissipation in the output stage.

Since SDM produces an output code with a PRF which is too high for efficient conversion and furthermore the PRF is signal dependent increasing distortion and noise in the presence of a non-ideal output stage, a new technique called ‘bit flipping’ [2] (or SDPIM in [17]) is introduced to reduce and regulate the PRF.

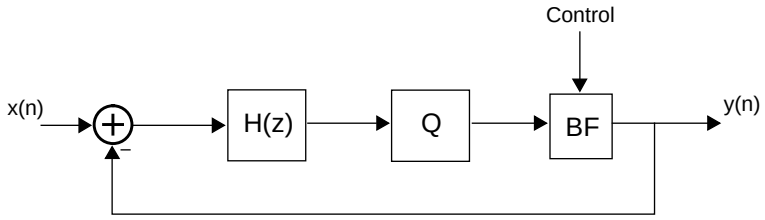

Fig. 9. Block diagram of bit-flipping SDM.

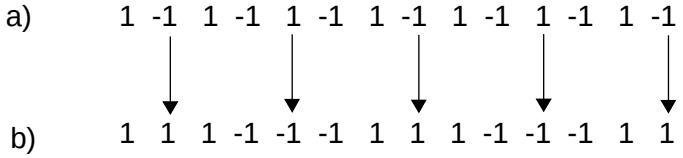

Fig. 10. Bit-flipping technique.

The concept of bit-flipping is illustrated in figures 9 and 10. The principle is to selectively invert the state of the quantizer output so that, for example, the bit pattern of fig. 10a is converted to the grouped pattern of fig. 10b. Every bit inversion introduces an additional error equal in magnitude to the quantizer interval but occurring within the feed-back loop so that it is spectrally shaped together with the quantizer error. The inversion error also helps to decorrelate the quantizer error from its input. Bit-flipping occurs when the PRF exceeds a predetermined target. The control can be implemented as a counter which counts down on every sample and counts up N steps if a transition occurs between the current and previous output bits. A counter value grater than zero indicates the target rate is exceeded and a bit-flipping should occur. For oversampling ratio L and sampling rate F_s, the value of N is given by: $N = \frac{LF_s}{2F_t}$ (1)

A target PRF of around F_t = 350KHz is required to yield low power dissipation in the output stage, leading a value N = 4 for parameters L = 64 and F_s = 44.1KHz.

The noise transfer function (NTF) defines the spectral shaping of the error intro-duced by the1-bit quantizer and the bit-flipper. For the prototype design presented in [2], a seventh order modulator was used as a cascade of resonator filter structure (figure 11). This structure has low sensitivity to coefficient quantization and requires minimal number of coefficients.

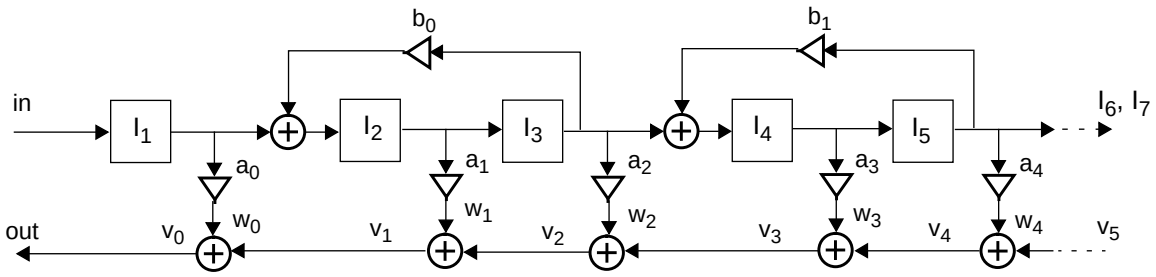

Fig. 11. Loop filter structure. I = integrator.

In [13] it is shown that the noise transfer function of the filter is given by:

$$NTF(z) = \frac{(z-1)N_1N_2N_3}{(a_0-1+z)N_1N_2N_3 + D_1N_2N_3 + D_2N_3 + D_3} \quad (2)$$

where:

$$N_i(z) = (z-1)^2 + b_i \quad (3)$$

$$D_k(z) = a_{2k-1}(z-1) + a_{2k} \quad (4)$$

Optimal set of coefficients a_k and b_i were determined through simulations choosing coefficients values to be a power of two.

The reported simulations results reveal that the modulator achieves over 18-bit resolution at an average PRF of 352.8KHz within the whole audio band. An extraordinary low clock rate of only 5.64MHz is used.

IV. Novel State-of-the-art Approaches

4.1 Click Modulation approach

An interesting recent research development is the proposal to use Logan's click modulation [5], which offers some advantages in that it is inherently linear in the signal band. Logan's theory is based on the complex theory of functions. In the modulation scheme, analytic signals that do not have a negative frequency content are used. Owing to this fact, a Hilbert transform will be incorporated. In the following, the resulting steps necessary to transform a given input signal f(t) into a binary signal q(t) having a separated baseband are summarized in fig. 12. For detailed derivation refer to [5].

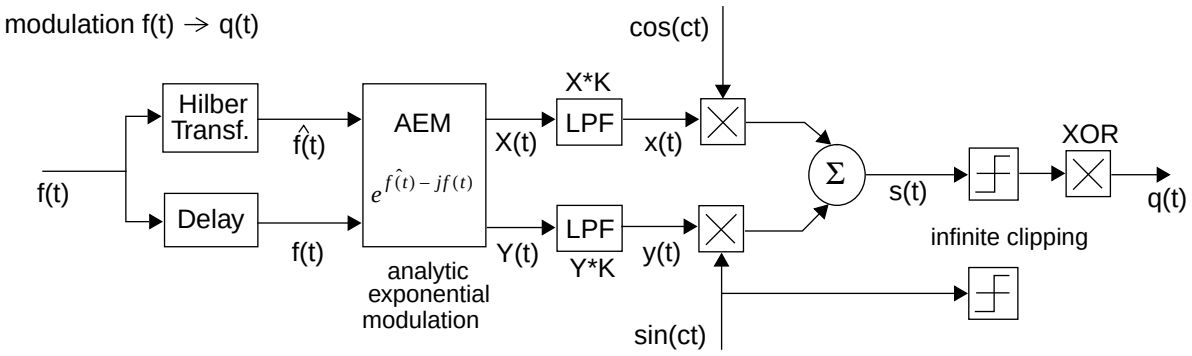

Fig. 12. Novel click modulation based scheme for power DACs.

As can be found from (5), s(t) is a single sideband (SSB) signal with carrier because x(t) has a mean value of one while y(t) is a pure AC signal.

$$s(t) = Re\{z(t)e^{-jct}\} = x(t)\cos(ct) + y(t)\sin(ct) \tag{5}$$

What is left now is to find a square wave representation q(t) such that holds the fundamental demand of having a separate baseband. According to click modulation theory, all the necessary information is contained within the zeros of s(t). These zeros interleave with the equally spaced zeros of the SSB carrier sin(ct). By combining these zeros in form of infinitely clipping the signals they belong to a square -waved signal that can be constructed as:

$$q(t) = -\frac{\pi}{2}\{\operatorname{sgn} s(t))\} \cdot \{\operatorname{sgn} \sin(ct)\} \tag{6}$$

From (6), q(t) has the appearance of being one-sided pulse width modulated, but the fact that q(t) has an exactly separated baseband has been proven by Logan.

Due to the heavy DSP computation required, an excessively high clock frequency of 3GHz would be required for a resolution of 16 bits. However a practical implementation with reduced bandwidth is reported in [5]. The resulting switching rate of 24KHz almost equals the original sampling rate. The trade-off is that a higher order low-pass filter is required to contain the distortion terms which lie beyond the switching frequency. Despite the reduced bandwidth of 4.8KHz mainly because of lacking DSP performance, 12-bit PCM-to-PWM conversion at 24KHz switching rate was achieved in the prototype described in [5] proving that the click modulation idea works.

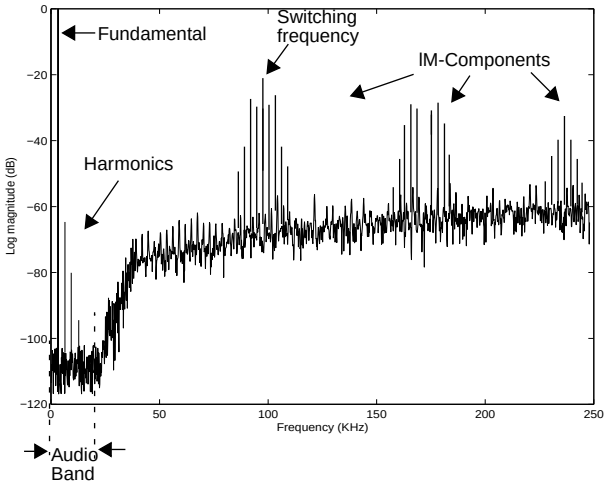

Fig. 13. Approximate Power DAC output spectrum.

V. Future Of Power D/A Conversion

As it has been shown, power D/A converters with high resolution, linearity and efficiency are already available for signals within the audio frequency band. As the signal processing algorithms become optimized, signals with wider bandwidth will be able to be processed by the converter, extending even more the practical applications.

Power DACs are to be the dominant technology in the digital future of the sound. It is not new that the audio industry is moving or has already moved to digital technologies (Digital or Dolby Surround, THX, MP3, digital FM, DATs, CDs, DVDs, are just some examples) but traditional linear power amplifiers, well known for being inefficient, are still used for reproduction. Because of their compact size, low heat dissipation and paltry power consumption, future generations of power DACs (as class-D audio amplifiers) will play an important role in digital sound systems (like [13], [14]).

A motivating factor driving research on power digital-to-analog converters is its perfect suitability for wireless applications. In this field, the research is directed towards low-power digital-audio portable applications such as cellular phones, handheld computers, personal digital assistants (PDAs) and hearing aids. Their increased efficiency provides one main advantage over class-AB amplifiers: reduced power supply requirements which translates to longer run-times on batteries, lower cost/smaller power supply designs and elimination of heat sinks. One of the most challenging requirements in this case, will be to compensate for power supply noise as the supply voltage levels become

smaller in wireless systems.

Applications are not restricted to audio signals, but also arise in medical, space, and defence engineering, since precise motor control by microprocessor has similar demands (i.e. high quality amplification over a limited bandwidth).

VI. CONCLUSION

PWM DACs differ from conventional converters as there is no analog process and the conversion is performed by a counting procedure. There is no longer the possibility of missing codes (since the process doesn't rely on analog matching or accuracy) and a complete converter may be constructed from digital standard logic components alone, save for a final passive low-pass filter. These characteristics yield to implementations which require very little area on a chip and very low power consumption.

The basic concepts, historical development and a comparison of different modern power DACs architectures were presented in this paper. Practical implementations and performance figures (18-bit resolution) demonstrate the capabilities of the power DAC concept. Finally, its main limitation (reduced bandwidth) and predicted research in the field was discussed in section V.

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