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CHAPTER 7: DATA CONVERTER SUPPORT CIRCUITS

SECTION 7.1: VOLTAGE REFERENCES

Reference circuits and linear regulators actually have much in common. In fact, the latter could be functionally described as a reference circuit, but with greater current (or power) output. Accordingly, almost all of the specifications of the two circuit types have great commonality (even though the performance of references is usually tighter with regard to drift, accuracy, etc.). In many cases today the support circuitry is included in the converter package. This is advantageous to the designer since it simplifies the design process and guarantees performance of the system.

Precision Voltage References

Voltage references have a major impact on the performance and accuracy of analog systems. A ±5 mV tolerance on a 5 V reference corresponds to ±0.1% absolute accuracy which is only 10-bit accuracy. For a 12-bit system, choosing a reference that has a ±1 mV tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. Note that many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not as important, although noise and short-term stability may be.

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen for temperature coefficient and aging characteristics which preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. Noise is an instantaneous change in the reference voltage. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up, and their behavior with transient loads. With regard to the first, always bear in mind that voltage references *do not power up instantly* (this is true of references inside ADCs and DACs as well as discrete designs). Thus it is rarely possible to turn on an ADC and reference, whether internal or external, make a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving.

Regarding the second point, a given reference IC may or may not be well suited for pulse-loading conditions, dependent upon the specific architecture. Many references use low power, and therefore low bandwidth, output buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs (especially successive approximation and flash ADCs). Suitable decoupling can ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer amplifier may be used to drive the node where the transients occur.

Types of Voltage References

In terms of the functionality of their circuit connection, standard reference ICs are often only available in *series*, or *three-terminal* form (V_{IN}, Common, V_{OUT}), and also in positive polarity only. The series types have the potential advantages of lower and more stable quiescent current, standard pretrimmed output voltages, and relatively high output current without accuracy loss. *Shunt*, or *two-terminal* (i.e., diode-like) references are more flexible regarding operating polarity, but they are also more restrictive as to loading. They can in fact eat up excessive power with widely varying resistor-fed voltage inputs. Also, they sometimes come in nonstandard voltages. All of these various factors tend to govern when one functional type is preferred over the other.

Some simple diode-based references are shown in Figure 7.1. In the first of these, a current driven forward biased diode (or diode-connected transistor) produces a voltage, $V_f = V_{REF}$. While the junction drop is somewhat decoupled from the raw supply, it has numerous deficiencies as a reference. Among them are a strong TC of about –0.3%/°C, some sensitivity to loading, and a rather inflexible output voltage, it is only available in 600 mV jumps.

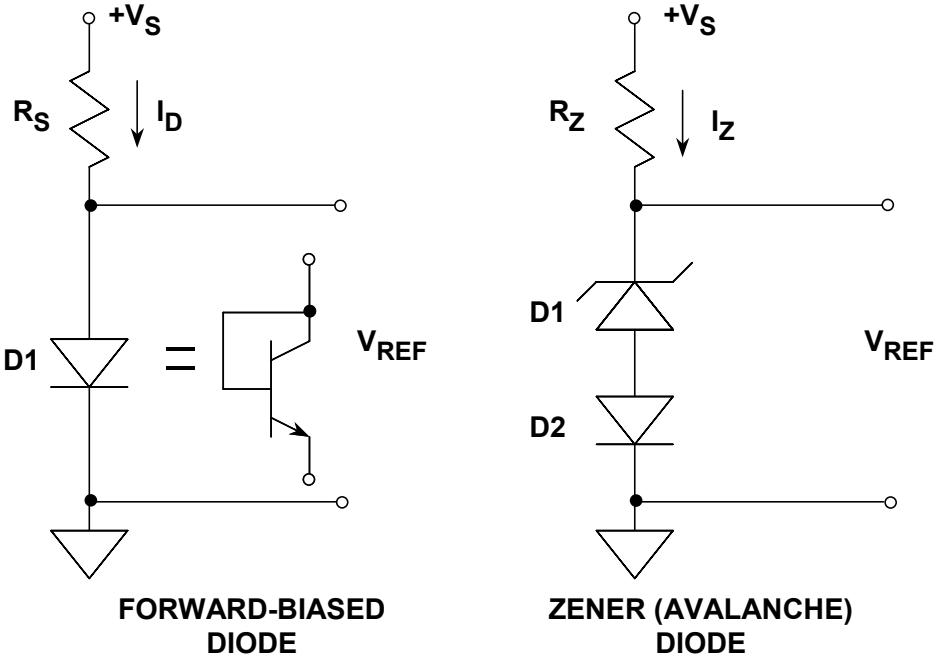

Figure 7.1: *Simple Diode Reference Circuits*

By contrast, these most simple references (as well as all other shunt-type regulators) have a basic advantage, which is the fact that the polarity is readily reversible by flipping connections and reversing the drive current. However, a basic limitation of all shunt regulators is that load current must always be less (usually appreciably less) than the driving current, I_D.

In the second circuit of Figure 7.1, a zener or avalanche diode is used, and an appreciably higher output voltage realized. While true *zener* breakdown occurs below 5 V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. Note that diode reverse breakdown is referred to almost universally today as *zener*, even though it is usually avalanche breakdown. With a D1 breakdown voltage in the 5 V to 8 V range, the net positive TC is such that it equals the negative TC of forward-biased diode D2, yielding a net TC of 100 ppm/°C or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package "temperature-compensated zener" references, such as the 1N821-1N829 series.

The temperature-compensated zener reference is limited in terms of initial accuracy, since the best TC combinations fall at odd voltages, such as the 1N829's 6.2 V. And, the scheme is also limited for loading, since for best TC the diode current must be carefully controlled. Unlike a fundamentally lower voltage (<2 V) reference, zener diode based references must of necessity be driven from voltage sources appreciably higher than 6 V levels, so this precludes operation of zener references from 5 V system supplies. References based on low TC zener (avalanche) diodes also tend to be noisy, due to the basic noise of the breakdown mechanism. This has been improved greatly with *monolithic* zener types, as is described further below.

Band Gap References

The development of low voltage (<5 V) references based on the band gap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first of these was the LM109 (Reference 1), and a basic band gap reference cell is shown in Figure 7.2.

This circuit is also called a "ΔV_{BE}" reference because the differing current densities between matched transistors Q1 - Q2 produces a ΔV_{BE} across R3. It works by summing the V_{BE} of Q3 with the amplified ΔV_{BE} of Q1 - Q2, developed across R2. The ΔV_{BE} and V_{BE} components have opposite polarity TCs; ΔV_{BE} is proportional to absolute temperature (PTAT), while V_{BE} is complementary to absolute temperature (CTAT). The summed output is V_R, and when it is equal to 1.205 V (silicon band gap voltage), the TC is a minimum.

The band gap reference technique is attractive in IC designs because of several reasons; among these are the relative simplicity, and the avoidance of zeners and their noise. However, very important in these days of ever decreasing system supplies is the fundamental fact that band gap devices operate at low voltages, i.e., <5 V. Not only are they used for standalone IC references, but they are also used within the designs of many other linear ICs such as ADCs and DACs.

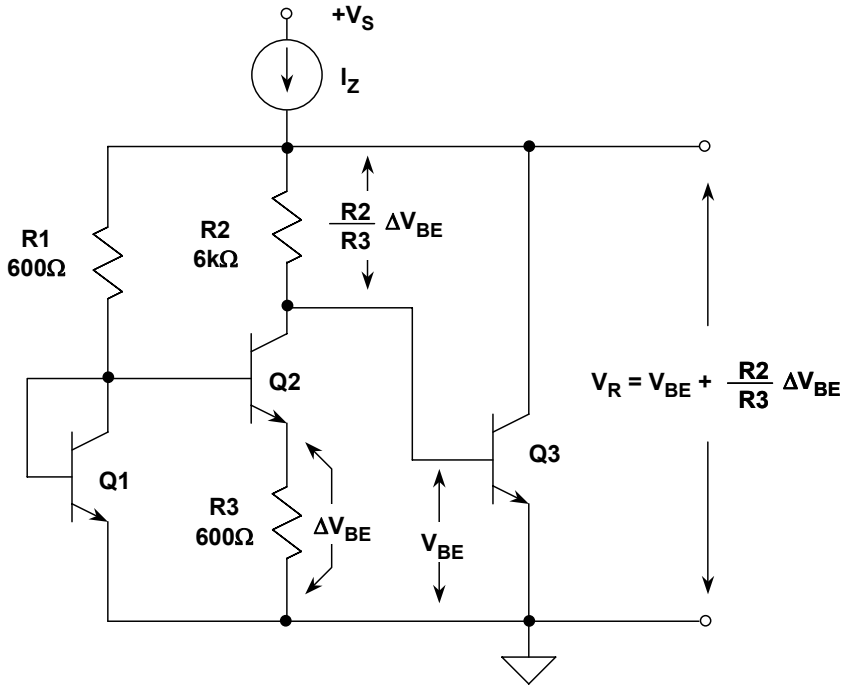

Figure 7.2: *Basic Band Gap Reference*

However, the basic designs of Figure 7.2 suffer from load and current drive sensitivity, plus the fact that the output needs accurate scaling to more useful levels, i.e., 2.5 V, 5 V, etc. The load drive issue is best addressed with the use of a buffer amplifier, which also provides convenient voltage scaling to standard levels.

An improved three-terminal band gap reference, the AD580 (introduced in 1974) is shown in Figure 7.3. Popularly called the "Brokaw Cell" (see References 2 and 3), this circuit provides on-chip output buffering, which allows good drive capability and standard output voltage scaling. The AD580 was the first precision band gap based IC reference, and variants of the topology have influenced further generations of both industry standard references such as the REF01, REF02, and REF03 series, as well as more recent ADI band gap parts such as the REF19x series, the AD680, AD780, the AD1582-85 series, the ADR38x series, the ADR39x series, and recent SC-70 and SOT-23 offerings of improved versions of the REF01, REF02, and REF03 (designated ADR01, ADR02, and ADR03).

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), by virtue of equal load resistors and a closed loop around the buffer op amp. Due to the resultant smaller V_{BE} of the 8 × area Q2, R2 in series with Q2 drops the ΔV_{BE} voltage, while R1 (due to the current relationships) drops a PTAT voltage V1:

$$V_1 = 2 \times \frac{R1}{R2} \times \Delta V_{BE} \quad . \qquad \text{Eq. 7-1}$$

The band gap cell reference voltage V_Z appears at the base of Q1, and is the sum of V_{BE} (Q1) and V_1, or 1.205 V, the band gap voltage:

$$V_Z = V_{BE(Q1)} + V_1 \qquad \text{Eq. 7-2}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \Delta V_{BE} \qquad \text{Eq. 7-3}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln \frac{J1}{J2} \qquad \text{Eq. 7-4}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln 8 \qquad \text{Eq. 7-5}$$

$$= 1.205\text{V} .$$

Note that J1 = current density in Q1, J2 = current density in Q2, and J1/J2 = 8.

However, because of the presence of the R4/R5 (laser trimmed) thin film divider and the op amp, the actual voltage appearing at V_{OUT} can be scaled higher, in the AD580 case 2.5 V. Following this general principle, V_{OUT} can be raised to other practical levels, such as for example in the AD584, with taps for precise 2.5 V, 5 V, 7.5 V, and 10 V operation. The AD580 provides up to 10-mA output current while operating from supplies between 4.5 V and 30 V. It is available in tolerances as low as 0.4%, with TCs as low as 10 ppm/°C.

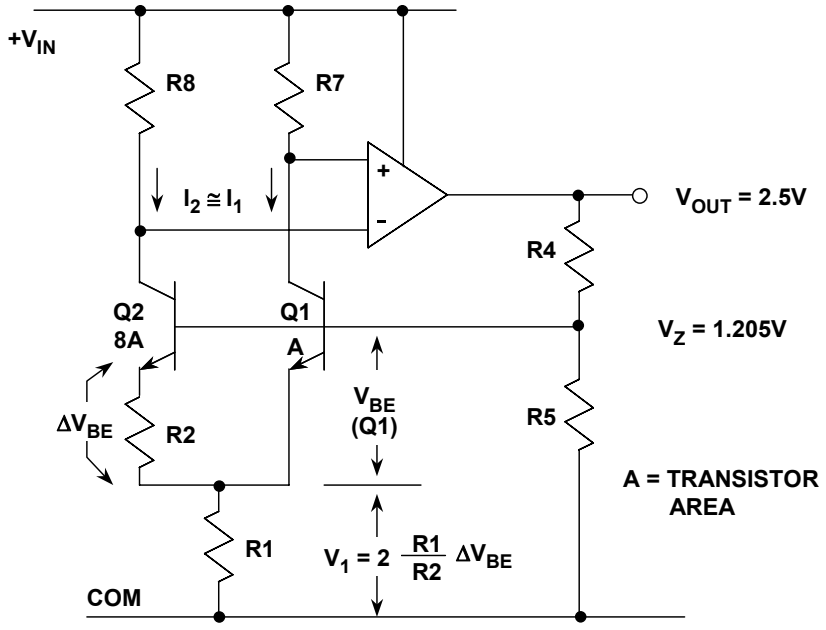

Figure 7.3: *AD580 Precision Band gap Reference Uses Brokaw Cell (1974)*

Many of the recent developments in band gap references have focused on smaller package size and cost reduction, to address system needs for smaller, more power efficient and less costly reference ICs. Among these are several recent band gap-based IC references.

The AD1580 (introduced in 1996) is a shunt mode IC reference which is functionally quite similar to the classic shunt IC reference, the AD589 (introduced in 1980) mentioned above. A key difference is the fact that the AD1580 uses a newer, small geometry process, enabling its availability within the tiny SOT-23 package. The very small size of this package allows use in a wide variety of space limited applications, and the low operating current lends itself to portable battery-powered uses. The AD1580 circuit is shown in simplified form in Figure 7.4.

In this circuit, like transistors Q1 and Q2 form the band gap core, and are operated at a current ratio of 5 times, determined by the ratio of R7 to R2. An op amp is formed by the differential pair Q3 - Q4, current mirror Q5, and driver/output stage Q8 - Q9. In closed loop equilibrium, this amplifier maintains the bottom ends of R2 - R7 at the same potential.

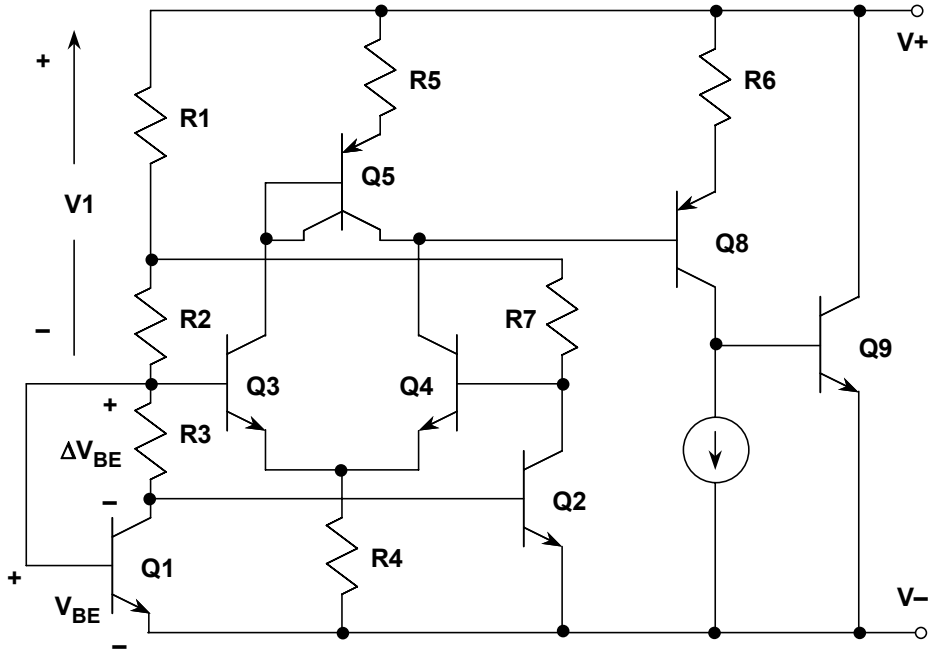

Figure 7.4: *AD1580 1.2 V Shunt Type Band Gap Reference has Tiny Size in SOT-23 Footprint*

As a result of the closed-loop control described, a basic ΔV_{BE} voltage is dropped across R3, and a scaled PTAT voltage also appears as V1, which is effectively in series with V_{BE}. The nominal band gap reference voltage of 1.225 V is then the sum of Q1's V_{BE} and V1. The AD1580 is designed to operate at currents as low as 50 µA, also handling maximum currents as high as 10 mA. It is available in grades with voltage tolerances of ±1 or ±10 mV, and with corresponding TCs of 50 or 100 ppm/°C.

The circuit diagram for the series, shown in Figure 7.5, may be recognized as a variant of the basic Brokaw band gap cell, as described under Figure 7.3. In this case Q1 - Q2 form the core, and the overall loop operates to produce the stable reference voltage V_{BG} at the base of Q1. A notable difference here is that the op amp's output stage is designed with

push-pull common-emitter stages. This has the effect of requiring an output capacitor for stability, but it also provides the IC with relatively low dropout operation.

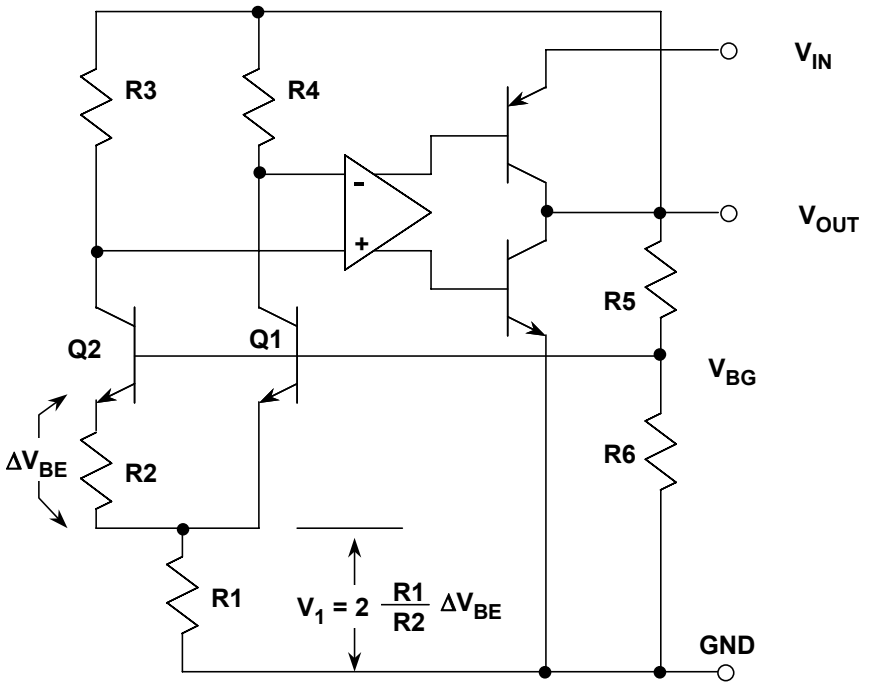

Figure 7.5: *AD1582 to AD1585 2.5-5 V Series Type Band Gap References*

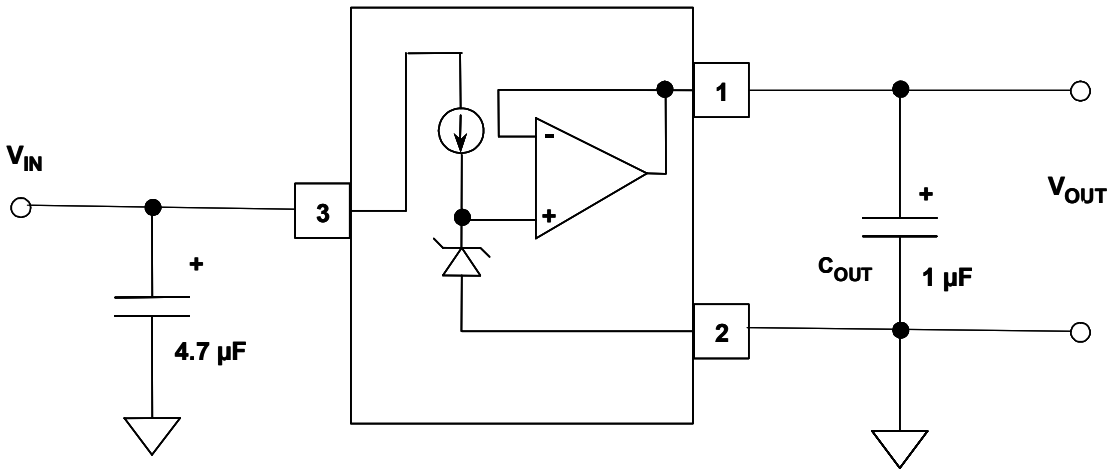

Figure 7.6: *AD1582 to AD1585 Series Connection Diagram*

The low dropout feature means essentially that V_{IN} can be lowered to as close as several hundred mV above the V_{OUT} level without disturbing operation. The push-pull operation also means that this device series can actually both sink and source currents at the output,

as opposed to the classic reference operation of sourcing current (only). For the various output voltage ratings, the divider R5-R6 is adjusted for the respective levels.

The AD1582-series is designed to operate with quiescent currents of only 65 μA (maximum), which allows good power efficiency when used in low power systems with varying voltage inputs. The rated output current for the series is 5 mA, and they are available in grades with voltage tolerances of ±0.1 or ±1% of V_{OUT}, with corresponding TCs of 50 or 100 ppm/°C.

Because of stability requirements, devices of the AD1582 series must be used with both an output and input bypass capacitor. Recommended worst case values for these are shown in the hookup diagram of Figure 7.6. For the electrical values noted, it is likely that tantalum chip capacitors will be the smallest in size.

Buried Zener References

In terms of the design approaches used within the reference core, the two most popular basic types of IC references consist of the band gap and buried zener units. Band gaps have been discussed, but zener based references warrant some further discussion.

In an IC chip, surface operated diode junction breakdown is prone to crystal imperfections and other contamination, thus zener diodes formed at the surface are more noisy and less stable than are *buried* (or sub-surface) ones. ADI zener based IC references employ the much preferred buried zener. This improves substantially upon the noise and drift of surface-mode operated zeners (see Reference 4). Buried zener references offer very low temperature drift, down to the 1 ppm/°C to 2 ppm/°C (AD588 and AD586), and the lowest noise as a percent of full-scale, i.e., 100 nV/√Hz or less. On the downside, the operating current of zener type references is usually relatively high, typically on the order of several mA. The zener voltage is also relatively high, typically on the order of 5 V. This limits its application in low voltage circuits.

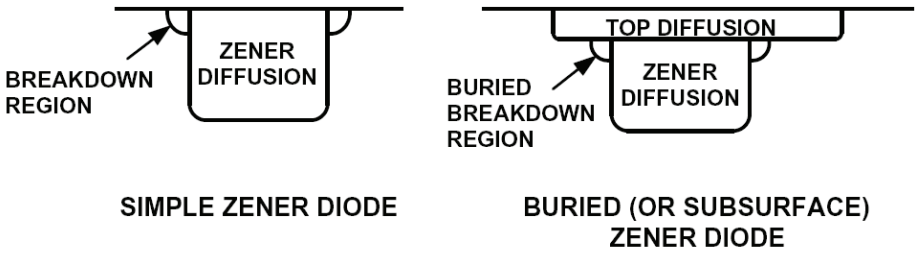

Figure 7.7: *Simple Surface Zener vs. a Buried Zener*

An important general point arises when comparing noise performance of different references. The best way to do this is to compare the ratio of the noise (within a given bandwidth) to the dc output voltage. For example, a 10 V reference with a 100 nV/√Hz noise density is 6 dB more quiet in relative terms than is a 5 V reference with the same noise level.

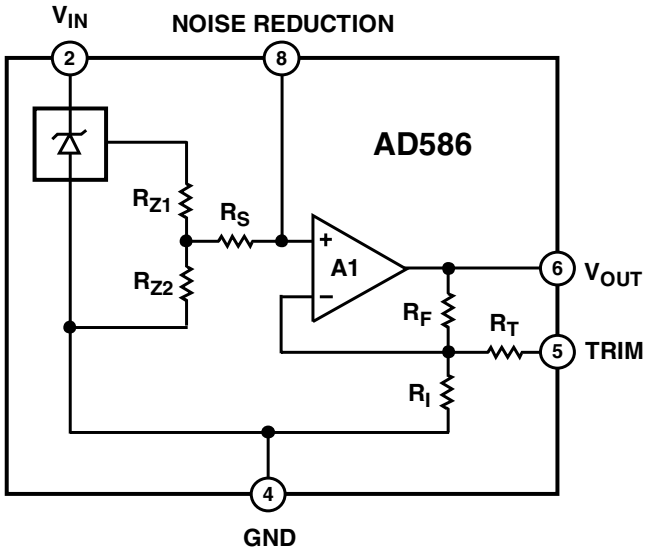

Figure 7.8: *Typical Buried Zener Reference (AD586)*

XFET® References

A third and relatively new category of IC reference core design is based on the properties of junction field effect (JFET) transistors. Somewhat analogous to the band gap reference for bipolar transistors, the JFET based reference operates a pair of junction field effect transistors with different pinchoff voltages, and amplifies the differential output to produce a stable reference voltage. One of the two JFETs uses an extra ion implantation, giving rise to the name XFET (eXtra implantation junction Field Effect Transistor) for the reference core design.

The basic topology for the XFET reference circuit is shown in Figure 7.9. J1 and J2 are the two JFET transistors, which form the core of the reference. J1 and J2 are driven at the same current level from matched current sources, I1 and I2. To the right, J1 is the JFET with the extra implantation, which causes the difference in the J1 - J2 pinchoff voltages to differ by 500 mV. With the pinchoff voltage of two such FETs purposely skewed, a differential voltage will appear between the gates for identical current drive conditions and equal source voltages. This voltage, ΔV_P, is:

$$\Delta V_P = V_{P1} - V_{P2} , \qquad \text{Eq. 7-6}$$

where V_{P1} and V_{P2} are the pinchoff voltages of FETs J1 and J2, respectively.

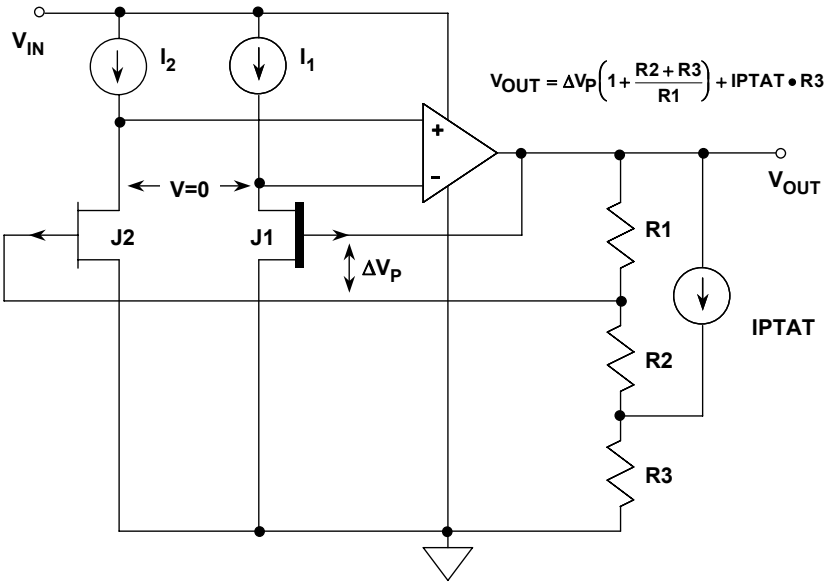

Figure 7.9: *XFET Reference Simplified Schematic*

Note that, within this circuit, the voltage ΔV_P exists between the *gates* of the two FETs. We also know that, with the overall feedback loop closed, the op amp axiom of zero input differential voltage will hold the sources of the two JFET at same potential. These source voltages are applied as inputs to the op amp, the output of which drives feedback divider R1 - R3. As this loop is configured, it stabilizes at an output voltage from the R1 - R2 tap which does in fact produce the required ΔV_P between the J1 - J2 gates. In essence, the op amp amplifies ΔV_P to produce V_{OUT}, where

$$V_{OUT} = \Delta V_P\left(1 + \frac{R2 + R3}{R1}\right) + (I_{PTAT})(R3). \qquad \text{Eq. 7-7}$$

As can be noted, this expression includes the basic output scaling (leftmost portion of the right terms), plus a rightmost temperature dependent term including I_{PTAT}. The I_{PTAT} portion of the expression compensates for a basic negative temperature coefficient of the XFET core, such that the overall net temperature drift of the reference is typically in a range of 3 ppm/°C to 8 ppm/°C.

The XFET architecture offers performance improvements over band gap and buried zener references, particularly for systems where operating current is critical, yet drift and noise performance must still be excellent. XFET noise levels are lower than band gap based bipolar references operating at an equivalent current, the temperature drift is low and linear at 3 ppm/°C to 8 ppm/°C (allowing easier compensation when required), and the series has lower hysteresis than band gaps. Thermal hysteresis is a low 50 ppm over a −40°C to +125°C range, less that half that of a typical band gap device. Finally, the long-term stability is excellent, typically only 50 ppm/1000 hours.

Figure 7.10 summarizes the pro and con characteristics of the three reference architectures; band gap, buried zener, and XFET.

BANDGAP	BURIED ZENER	XFET®
< 5V Supplies	> 5V Supplies	< 5V Supplies
High Noise @ High Power	Low Noise @ High Power	Low Noise @ Low Power
Fair Drift and Long Term Stability	Good Drift and Long Term Stability	Excellent Drift and Long Term Stability
Fair Hysteresis	Fair Hysteresis	Low Hysteresis

Figure 7.10: *Characteristics of Reference Architectures*

Though modern IC references come in a variety of styles, series operating, fixed output positive types do tend to dominate. They may or may not be low power, low noise, and/or low dropout, or available within a certain package. Of course, in a given application, any single one of these differentiating factors can drive a choice, thus it behooves the designer to be aware of all the different devices available.

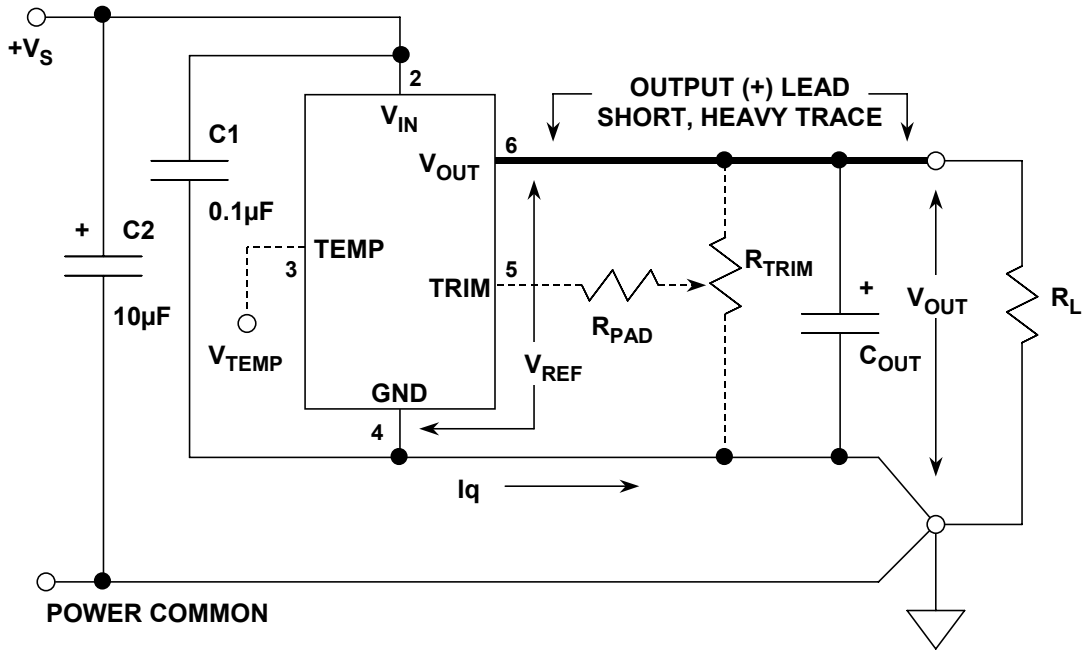

Figure 7.11: *Standard Positive Output Three Terminal Reference Hookup (8-pin DIP Pinout)*

Figure 7.11 shows the typical schematic for a series type IC positive reference (in an 8 pin package. Note that (x) numbers refer to the standard pin for that function). There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin (5). Some band gap references also have a high impedance PTAT output (V_{TEMP}) for temperature sensing (pin 3). The intent here is that no appreciable current be drawn from this pin, but it can be useful for such nonloading types of connections as comparator inputs, to sense temperature thresholds, etc.

Some references have a pin labeled “noise reduction.” This may cause some confusion. A capacitor connected to this pin will reduce the noise of the reference cell itself, this cell is typically followed by an internal buffer. The noise of this buffer will not be affected.

All references should use decoupling capacitors on the input pin (2), but the amount of decoupling (if any) placed on the output (pin 6) depends upon the stability of the reference's output op amp with capacitive load. Simply put, there is no hard and fast rule for capacitive loads here. For example, some three terminal types *require* the output capacitor for stability (i.e., REF19x and AD1582 to AD1585 series), while with others it is optional for performance improvement (AD780, REF43, ADR29x, ADR43x, AD38x, AD39x, ADR01, ADR02, ADR03). Even if the output capacitor is optional, it may still be required to supply the energy for transient load currents, as presented by some ADC reference input circuits. The safest rule then is that you should use the data sheet to verify what are the specific capacitive loading ground rules for the reference you intend to use, for the load conditions your circuit presents.

Voltage Reference Specifications

Tolerance

It is usually better to select a reference with the required value and accuracy, and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as approximately 0.04% can be achieved with the AD586, AD780, REF195, and ADR43x-series, while the AD588 is 0.01%. If and when trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. When/if additional external scaling is required, a precision op amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

Drift

The XFET and buried zener reference families have the best long term drift and TC performance. The XFET ADR43x-series have TCs as low as 3 ppm/°C. TCs as low as 1 ppm/°C to 2 ppm/°C are available with the AD586 and AD588 buried zener references, and the AD780 band gap reference is almost as good at 3 ppm/°C.

The XFET series achieves long terms drifts of 50 ppm/1000 hours, while the buried zener types come in at 25 ppm/1000 hours. Note that where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift—this is not correct, and can in fact be quite pessimistic. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about $\sqrt{8.766} \approx$ 3 times the 1000 hour figure, and the ten year value will be roughly 9 times the 1000 hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects full-scale accuracy as shown in Figure 7.12. This table shows system resolution and the TC required to maintain ½ LSB error over an operating temperature range of 100°C. For example, a TC of about 1 ppm/°C is required to maintain ½ LSB error at 12 bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of ½ LSB for popular full-scale ranges.

Supply Range

IC reference supply voltages range from about 3 V (or less) above rated output, to as high as 30 V (or more) above rated output. Exceptions are devices designed for low dropout, such as the REF19X, AD1582 to AD1585, ADR38X, ADR39X series. At low currents,

the REF195 can deliver 5 V with an input as low as 5.1 V (100 mV dropout). Note that due to process limits, some references may have more restrictive maximum voltage input ranges, such as the AD1582 to AD1585 series (12 V), the ADR29x series (15 V), and the ADR43x series (18 V).

		½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	REQUIRED DRIFT (ppm/ºC)	10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 7.12: *Reference Temperature Drift Requirements for Various System Accuracies (1/2 LSB Criteria, 100°C Span)*

Load Sensitivity

Load sensitivity (or output impedance) is usually specified in µV/mA of load current, or mΩ, or ppm/mA. While figures of 70 ppm/mA or less are quite good (AD780, REF43, REF195, ADR29X, ADR43X), it should be noted that external wiring drops can produce comparable errors at high currents, without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return. For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588, AD688, ADR39x) are used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore the source impedance is a function of frequency. Typical reference output impedance rises at 6 dB/octave from the dc value, and is nominally about 10 Ω at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op amp within the reference remains stable for such loading.

Line Sensitivity

Line sensitivity (or regulation) is usually specified in µV/V, (or ppm/V) of input change, and is typically 25 ppm/V (–92 dB) in the REF43, REF195, AD680, AD780, ADR29X,

ADR39X, and ADR43X. For dc and very low frequencies, such errors are easily masked by noise.

As with op amps, the line sensitivity (or power supply rejection) of references degrades with increasing frequency, typically 30 dB to 50 dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a low dropout pre-regulator, such as one of the ADP3300-series parts.

Noise

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1 Hz to 10 Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op amps) is a plot of noise voltage spectral density (nV/√Hz) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a Gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of 6.6 × rms is used to define a practical peak value—statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than ½ LSB in order to maintain required accuracy. If peak-to-peak noise is assumed to be 6 times the rms value, then for an N-bit system, reference voltage full-scale V_{REF}, reference noise bandwidth (BW), the required noise voltage spectral density E_n (V/√Hz) is given by:

$$E_n \leq \frac{V_{REF}}{12 \cdot 2^N \cdot \sqrt{BW}}. \qquad \text{Eq. 7-8}$$

For a 10 V, 12-bit, 100 kHz system, the noise requirement is a modest 643 nV/√Hz. Figure 7.13 shows that increasing resolution and/or lower full-scale references make noise requirements more stringent. The 100 kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC references have noise spectral densities around 100 nV/√Hz, so additional filtering is obviously required in most high resolution systems, especially those with low values of V_{REF}.

Some references, for example, the AD587 buried zener type, have a pin designated as the *noise reduction pin* (see data sheet). This pin is connected to a high impedance node preceding the on-chip buffer amplifier. Thus an externally connected capacitor C_N will form a low-pass filter with an internal resistor, to limits the effective noise bandwidth seen at the output. A 1 µF capacitor gives a 3 dB bandwidth of 40 Hz. Note that this method of noise reduction is by no means universal, and other devices may implement

noise reduction differently, if at all. Also note that it does not affect the noise of the buffer amplifier.

There are also general purpose methods of noise reduction, which can be used to reduce the noise of any reference IC, at any standard voltage level. Note that the DC characteristics of the reference filter will affect the accuracy of the reference.

	NOISE DENSITY (nV/√Hz) FOR 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

Figure 7.13: *Reference Noise Requirements for Various System Accuracies (1/2 LSB / 100 kHz Criteria)*

Scaled References

A useful approach when a nonstandard reference voltage is required is to simply buffer and scale a basic low voltage reference diode. With this approach, a potential difficulty is getting an amplifier to work well at such low voltages as 3 V. A workhorse solution is the low power reference and scaling buffer shown in Figure 7.14. Here a low current 1.2 V two terminal reference diode is used for D1, which can be either a 1.200 V ADR512, 1.235 V AD589, or the 1.225 V AD1580. Resistor R1 sets the diode current in either case, and is chosen for the diode minimum current requirement at a minimum supply of 2.7 V. Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

The amplifier U1 both buffers and optionally scales up the nominal 1.0 V or 1.2 V reference, allowing much higher source/sink output currents. Of course, a higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach.

In Figure 7.14, without gain scaling resistors R2 - R3, V_{OUT} is simply equal to V_{REF}. With the use of the scaling resistors, V_{OUT} can be set anywhere between a lower limit of V_{REF}, and an upper limit of the positive rail, due to the op amp's rail-to-rail output swing. Also, note that this buffered reference is inherently low dropout, allowing a +4.5 V (or more) reference output on a +5 V supply, for example. The general expression for V_{OUT} is shown in the figure, where V_{REF} is the reference voltage.

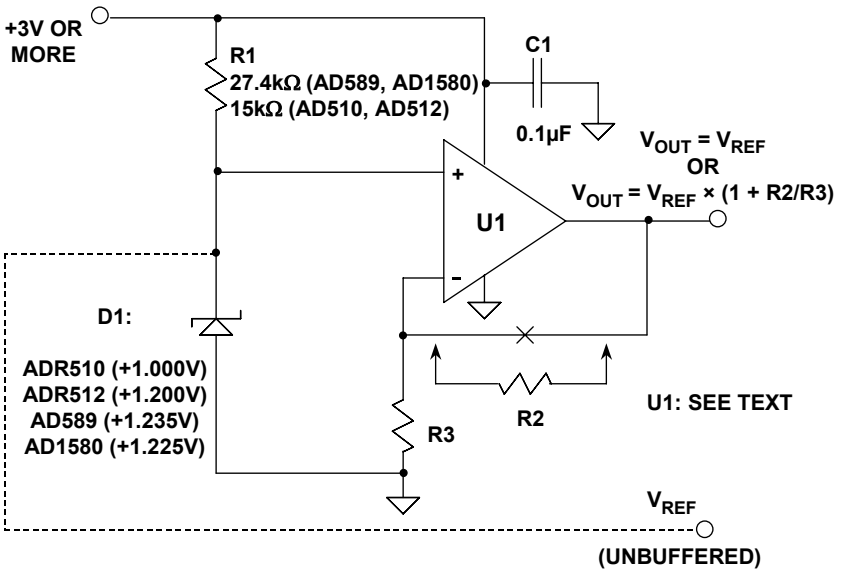

Figure 7.14: *Rail-to-Rail Output Op Amps Allow Greatest Flexibility in Low Dropout References*

Voltage Reference Pulse Current Response

The response of references to dynamic loads is often a concern, especially in applications such as driving ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-delta ADC may be the switched capacitor circuit shown in Figure 7.15. The dynamic load causes current spikes in the reference as the capacitor C_{IN} is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. Thus it is important to maintain a low noise, transient free potential at the ADC's reference input. Be aware that if the reference source impedance is too high, dynamic loading can cause the reference input to shift by more than 5 mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads. Therefore it is quite important to verify that the device chosen will satisfactorily drive the output capacitance required. In any case, the converter reference inputs should always be decoupled—with at least 0.1 µF, and with an additional 5 µF to 50 µF if there is any low frequency ripple on its supply.

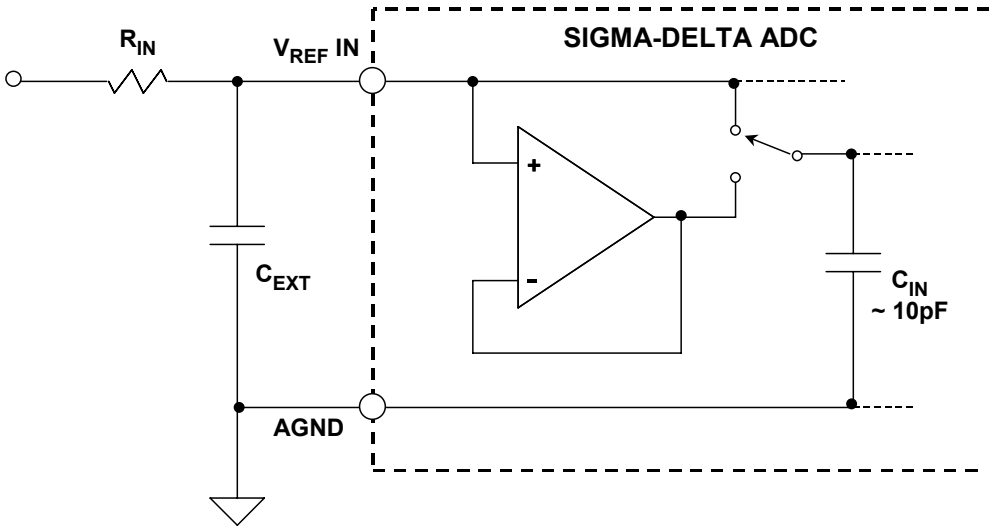

Figure 7.15: *Switched Capacitor Input of Sigma-Delta ADC Presents a Dynamic Load to the Voltage Reference*

Since some references misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 7.16. In a typical voltage reference, a step change of 1 mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a 0.01 µF capacitor is connected to the reference output.

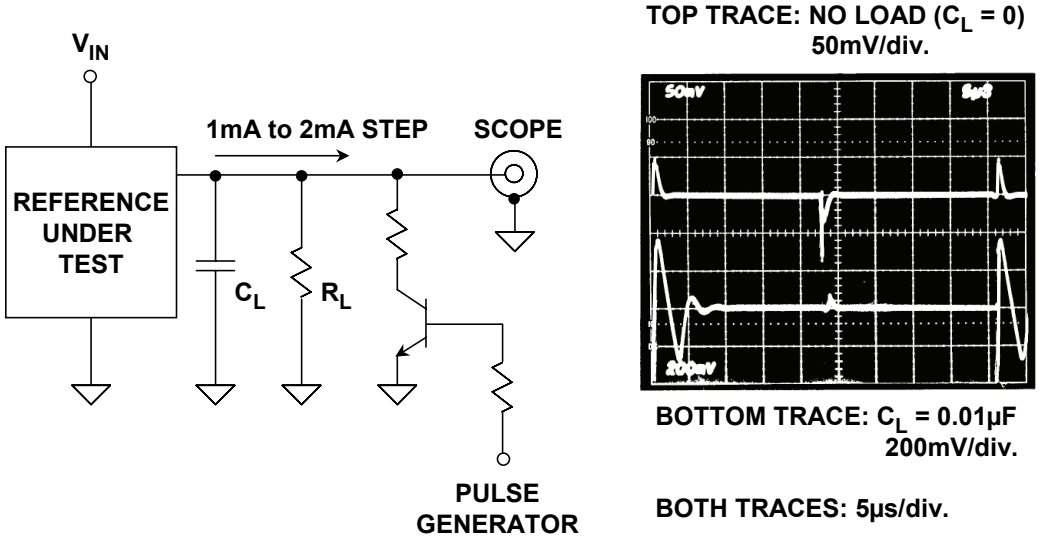

Figure 7.16: *Make Sure Reference is Stable with Large Capacitive Loads*

As noted above, reference bypass capacitors are useful when driving the reference inputs of successive-approximation ADCs. Figure 7.17 illustrates reference voltage settling behavior immediately following the "Start Convert" command. A small capacitor (0.01 µF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. As shown by the bottom trace, decoupling with a ≥ 1 µF capacitor maintains the reference stability during conversion.

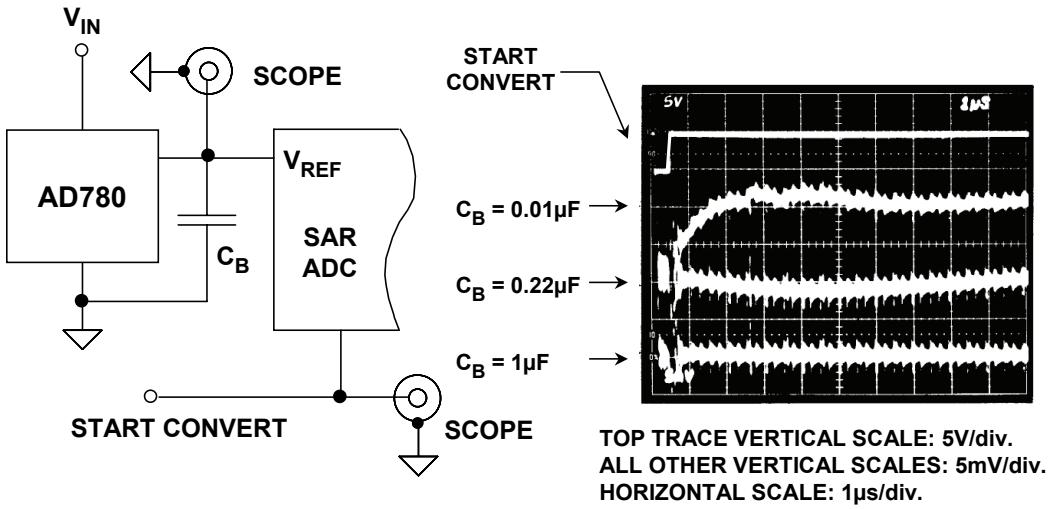

Figure 7.17: *Successive Approximation ADCs Can Present a Dynamic Transient Load to the Reference*

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

Low Noise References for High Resolution Converters

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5 V internal reference with a 0.1 Hz to 10 Hz noise of 8.3 µV rms (2600 nV/√Hz), while the AD780 reference noise is only 0.67 µV rms (200 nV/√Hz). The internal noise of the AD7710-series in this bandwidth is about 1.7 µV rms. The use of the AD780 increases the effective resolution of the AD7710 from about 20.5 bits to 21.5 bits.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! For example, the early AD574 had a guaranteed uncalibrated gain accuracy of 0.125% when using an internal 10 V reference (which itself had a specified accuracy of only ±1%). It is obvious that if such a device, having an internal reference which is at one end of the specified range, is used with an external reference of exactly 10 V, then its gain will be about 1% in error.

REFERENCES:
VOLTAGE REFERENCES

1. Bob Widlar, "New Developments in IC Voltage Regulators," **IEEE Journal of Solid State Circuits**, Vol. SC-6, February, 1971.

2. Paul Brokaw, "A Simple Three-Terminal IC Band gap Voltage Reference," **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

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4. Dan Sheingold, Section 20.2 within **Analog-Digital Conversion Handbook, 3d. Edition**, Prentice-Hall, 1986.

5. Walt Jung, "Build an Ultra-Low-Noise Voltage Reference," **Electronic Design Analog Applications Issue**, June 24, 1993.

6. Walt Jung, "Getting the Most from IC Voltage References," **Analog Dialogue**, 28-1, 1994, pp. 13-21.

Notes:

SECTION 7.2: ANALOG SWITCHES AND MULTIPLEXERS

Introduction

Solid state analog switches and multiplexers have become an essential component in the design of electronic systems which require the ability to control and select a specified transmission path for an analog signal. These devices are used in a wide variety of applications including multichannel data acquisition systems, process control, instrumentation, video systems, etc.

Early CMOS switches and multiplexers were typically designed to handle signal levels up to ±10 V while operating on ±15 V supplies. In 1979, Analog Devices introduced the popular ADG200-series of switches and multiplexers, and in 1988 the ADG201-series was introduced which were fabricated on a proprietary linear-compatible CMOS process (L^2CMOS). These devices allowed input signals to ±15 V when operating on ±15 V supplies.

A large number of switches and multiplexers were introduced in the 1980s and 1990s, with the trend toward lower on resistance, faster switching, lower supply voltages, lower cost, lower power, and smaller surface-mount packages.

Today, analog switches and multiplexers are available in a wide variety of configurations, options, etc., to suit nearly all applications. On resistances less than 0.5 Ω, picoampere leakage currents, signal bandwidths greater than 1 GHz, and single 1.8 V supply operation are now possible with modern CMOS technology.

Although CMOS is by far the most popular IC process today for switches and multiplexers, bipolar processes (with JFETs) and complementary bipolar processes (also with JFET capability) are often used for special applications such as video switching and multiplexing where the high performance characteristics required are not attainable with CMOS. Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time is generally not fast enough, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch on resistance with signal level (R_{ON} modulation) can introduce unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer better solutions at video frequencies—with obvious power and cost increases above CMOS devices.

CMOS Switch Basics

The ideal analog switch has no on resistance, infinite off impedance and zero time delay, and can handle large signal and common-mode voltages. Real CMOS analog switches meet none of these criteria. It can be more correctly thought of as a variable resistor which changes from very high to very low resistance. But if we understand the limitations of analog switches, most of these limitations can be overcome.

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the "on" state, its resistance can be less than 1 Ω, while in the "off" state, the resistance increases to several hundreds of megohms, with picoampere leakage currents. CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease. A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 7.18.

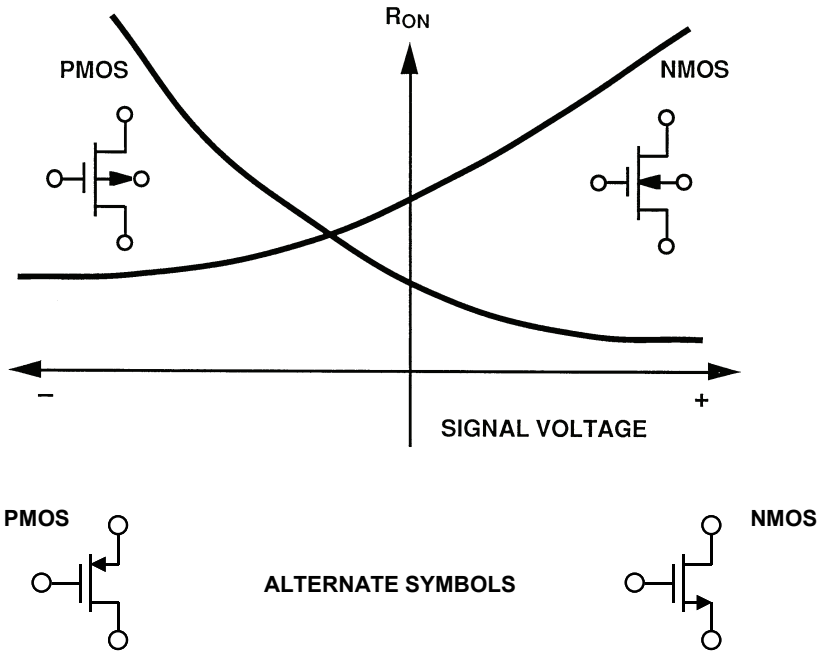


Figure 7.18: *MOSFET Switch ON Resistance vs. Signal Voltage*

The complementary-MOS process (CMOS) yields good P-channel and N-channel MOSFETs. Connecting the PMOS and NMOS devices in parallel forms the basic bilateral CMOS switch of Figure 7.19. This combination reduces the on resistance, and also produces a resistance which varies much less with signal voltage.

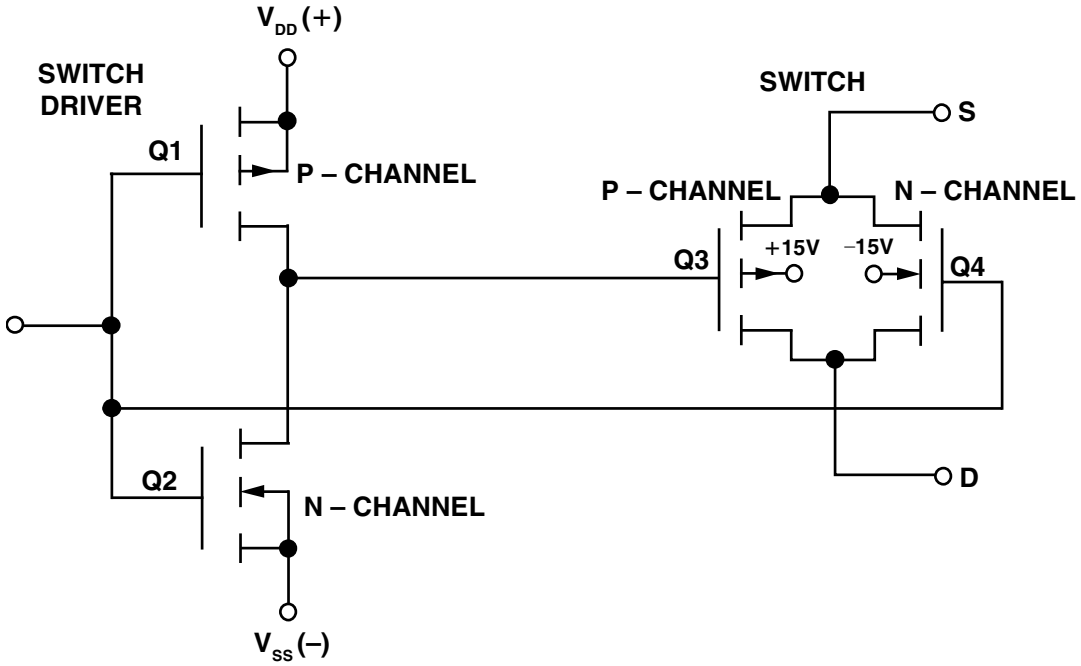


Figure 7.19: *Basic CMOS Switch Uses Complementary Pair to Minimize R_{ON} Variation due to Signal Swings*

Figure 7.20 shows the on resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can causes errors in dc accuracy as well as ac distortion. The bilateral CMOS switch solves this problem. On resistance is minimized, and linearity is also improved. The bottom curve of Figure 7.20 shows the improved flatness of the on resistance characteristic of the switch.

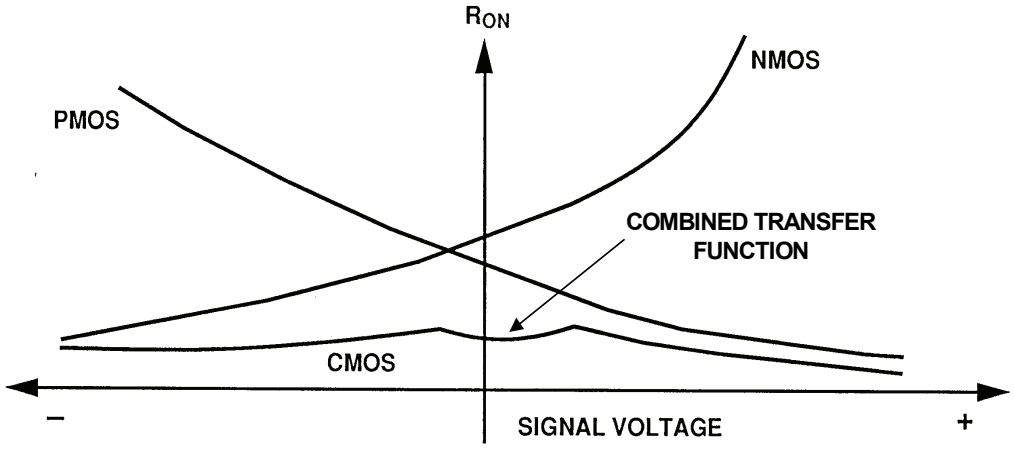


Figure 7.20: *CMOS Switch ON Resistance vs. Signal Voltage*

The ADG8xx-series of CMOS switches are specifically designed for less than 0.5 Ω on resistance and are fabricated on a sub-micron process. These devices can carry currents up to 400 mA, operate on a single 1.8 V to 5.5 V supply, and are rated over an extended temperature range of –40°C to +125°C. On resistance over temperature and input signal level is shown in Figure 7.21.

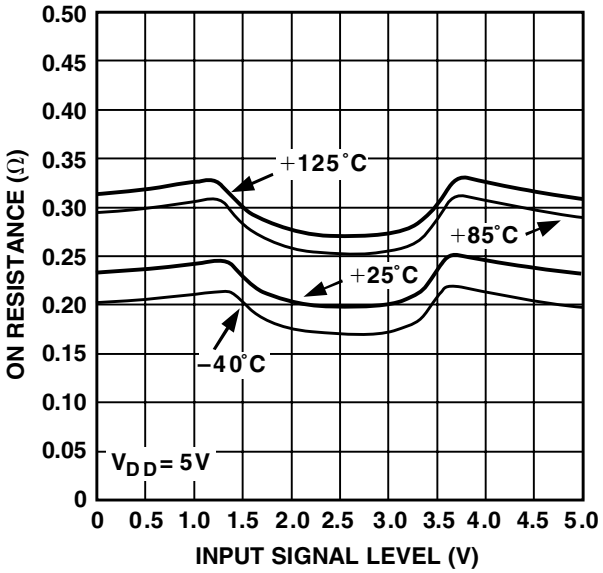


Figure 7.21: *ON Resistance vs. Input Signal for ADG801/ADG802 CMOS Switch, V_{DD} = +5 V*

Error Sources in the CMOS Switch

It is important to understand the error sources in an analog switch. Many affect ac and dc performance, while others only affect ac. Figure 7.22 shows the equivalent circuit of two adjacent CMOS switches. The model includes leakage currents and junction capacitances.

DC errors associated with a single CMOS switch in the on state are shown in Figure 7.23. When the switch is on, dc performance is affected mainly by the switch on resistance (R_{ON}) and leakage current (I_{LKG}). A resistive attenuator is created by the R_G-R_{ON}-R_{LOAD} combination which produces a gain error. The leakage current, I_{LKG}, flows through the equivalent resistance of R_{LOAD} in parallel with the sum of R_G and R_{ON}. Not only can R_{ON} cause gain errors—which can be calibrated using a system gain trim—but its variation with applied signal voltage (R_{ON} modulation) can introduce distortion—for which there is no calibration. Low resistance circuits are more subject to errors due to R_{ON}, while high resistance circuits are affected by leakage currents. Figure 7.23 also gives equations that show how these parameters affect dc performance.

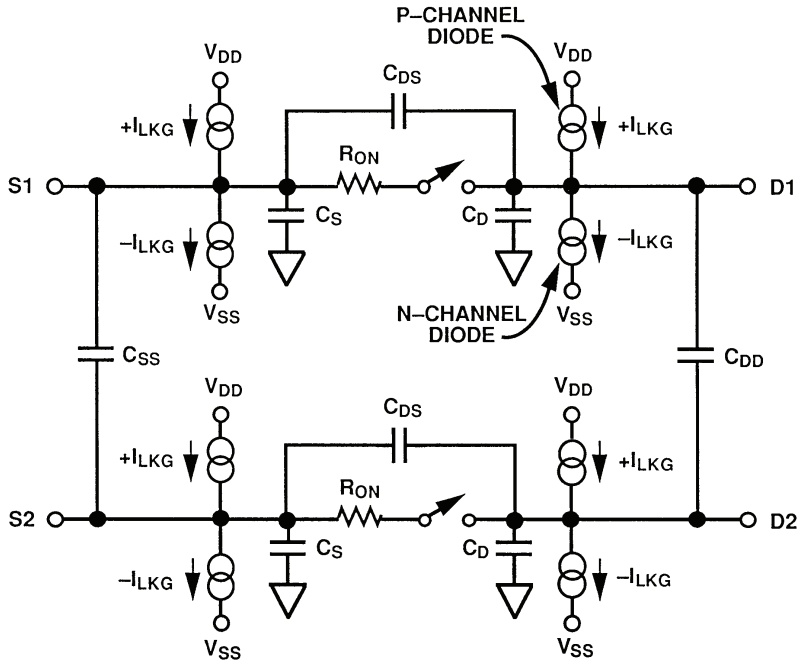
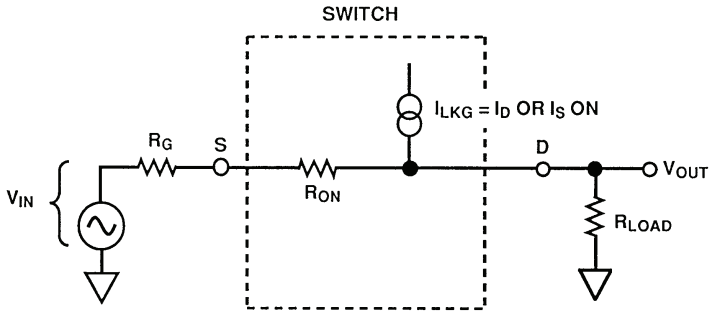


Figure 7.22: *Equivalent Circuit of Two Adjacent CMOS Switches*



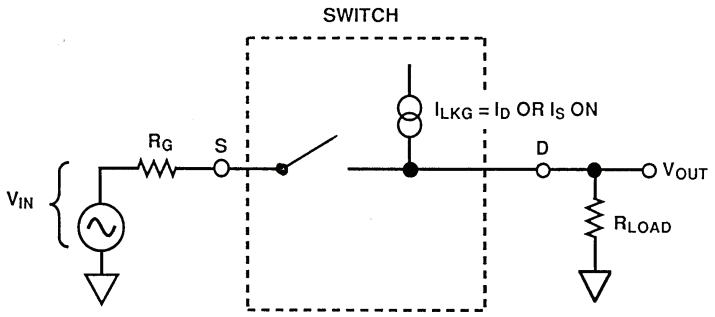
$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

IF $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}}\right]$$

Figure 7.23: *Factors Affecting DC Performance for ON Switch Condition: R_{ON}, R_{LOAD}, and I_{LKG}*

When the switch is OFF, leakage current can introduce errors as shown in Figure 7.24. The leakage current flowing through the load resistance develops a corresponding voltage error at the output.

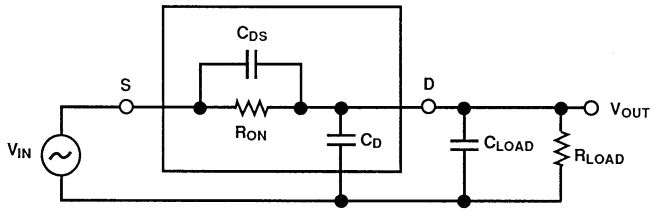


Leakage current creates error voltage at V_{OUT} equal to:

$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 7.24: *Factors Affecting DC Performance for OFF Switch Condition: I_{LKG} and R_{LOAD}*

Figure 7.25 illustrates the parasitic components that affect the ac performance of CMOS switches. Additional external capacitances will further degrade performance. These capacitances affect feedthrough, crosstalk, and system bandwidth. C_{DS} (drain-to-source capacitance), C_D (drain-to-ground capacitance), and C_{LOAD} all work in conjunction with R_{ON} and R_{LOAD} to form the overall transfer function.



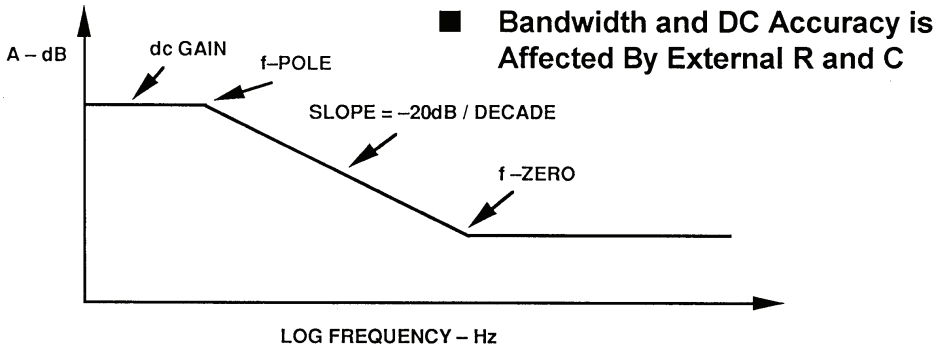
$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right]\left[\frac{sR_{ON}C_{DS} + 1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

$$A(dB) = 20\log\left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right] + 10\log\left[\omega^2(R_{ON}C_{DS})^2 + 1\right] - 10\log\omega^2\left[\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)^2(C_{LOAD} + C_D + C_{DS})^2 + 1\right]$$

Figure 7.25: *Dynamic Performance Considerations: Transfer Accuracy vs. Frequency*

In the equivalent circuit, C_{DS} creates a frequency zero in the numerator of the transfer function A(s). This zero usually occurs at high frequencies because the switch on resistance is small. The bandwidth is also a function of the switch output capacitance in combination with C_{DS} and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in the in Figure 7.26 which shows the overall Bode plot for the switch in the on state. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance C_D. Thus, to maximize bandwidth, a switch should have low input and output capacitance and low on resistance.

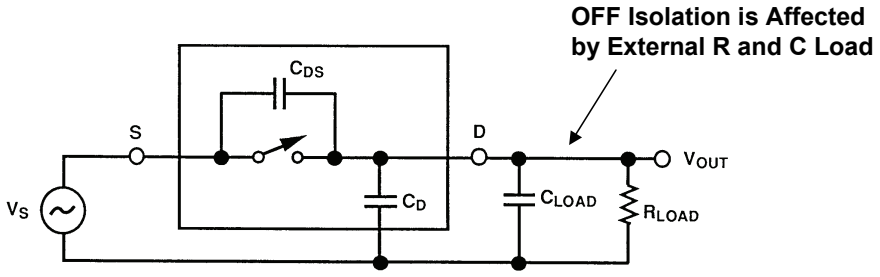


$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right]\left[sR_{ON}C_{DS} + 1\right]\left[\frac{1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

$$\text{DC GAIN} = \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}, \quad f_{ZERO} = \frac{0.159}{R_{ON}C_{DS}}, \quad f_{POLE} = \frac{0.159}{\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS})}$$

Figure 7.26: *Bode Plot of CMOS Switch Transfer Function in the ON State*

The series-pass capacitance, C_{DS}, not only creates a zero in the response in the ON state, it degrades the feedthrough performance of the switch during its OFF state. When the switch is off, C_{DS} couples the input signal to the output load as shown in Figure 7.27.



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 7.27: *Dynamic Performance Considerations: Off Isolation*

Large values of C_{DS} will produce large values of feedthrough, proportional to the input frequency. Figure 7.28 illustrates the drop in OFF isolation as a function of frequency. The simplest way to maximize the OFF isolation is to choose a switch that has as small a C_{DS} as possible.

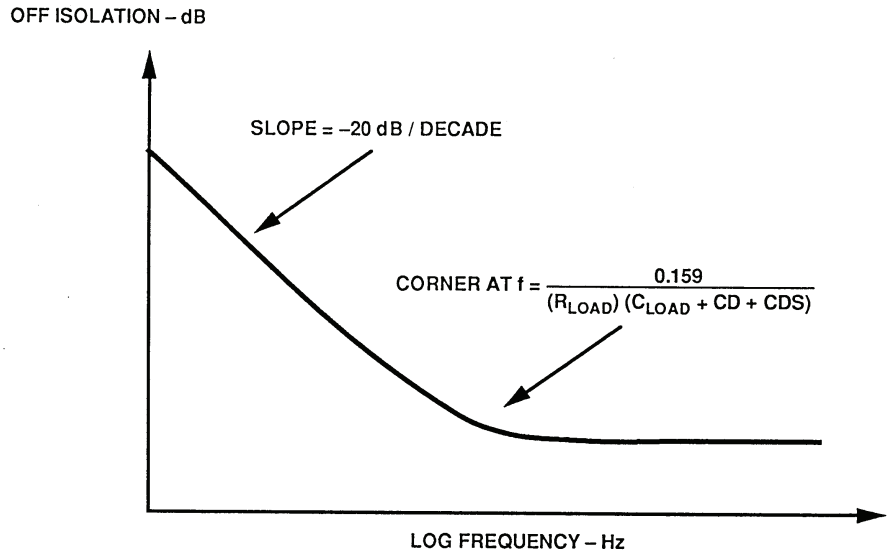


Figure 7.28: *Off Isolation vs. Frequency*

Figure 7.29 shows typical CMOS analog switch OFF isolation as a function of frequency for the ADG708 8-channel multiplexer. From dc to several kilohertz, the multiplexer has nearly 90 dB isolation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 10 MHz, the switch shown still has nearly 60 dB of isolation.

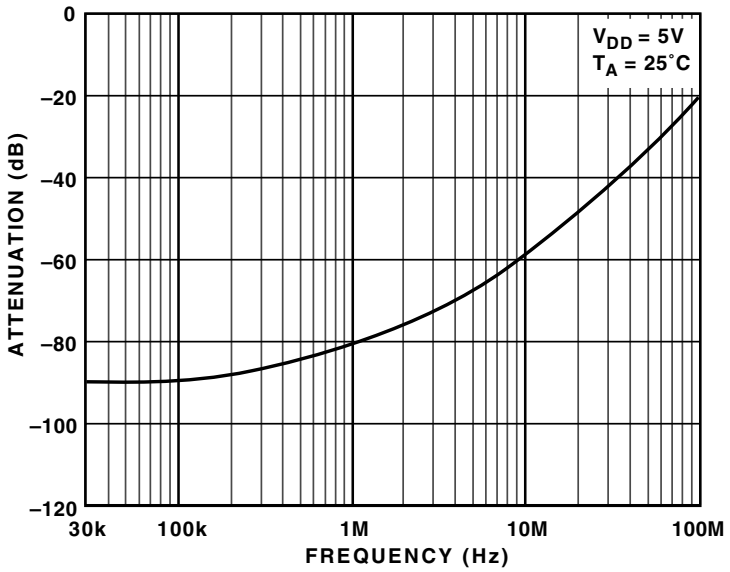


Figure 7.29: *OFF Isolation vs. Frequency for ADG708 8-Channel Multiplexer*

Another ac parameter that affects system performance is the charge injection that takes place during switching. Figure 7.30 shows the equivalent circuit of the charge injection mechanism.

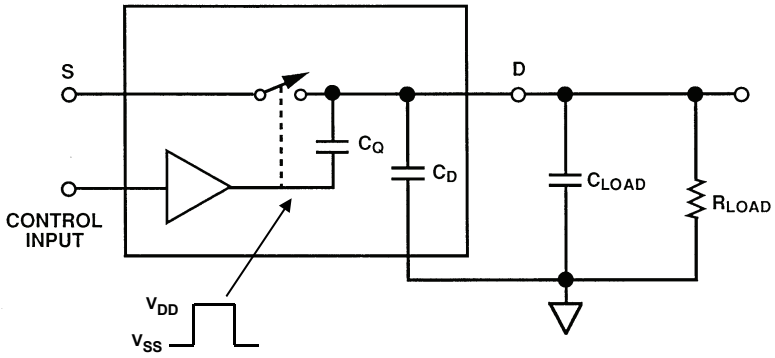


Figure 7.30: *Dynamic Performance Considerations: Charge Injection Model*

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS}, or vice versa) at the gate of the CMOS switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance C_Q. The amount of charge coupled depends on the magnitude of the gate-drain capacitance.

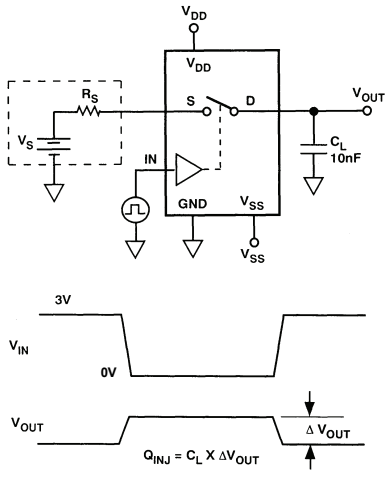


Figure 7.31: *Effects of Charge Injection on Output*

The charge injection introduces a step change in output voltage when switching as shown in Figure 7.31. The change in output voltage, ΔV_{OUT}, is a function of the amount of charge injected, Q_{INJ} (which is in turn a function of the gate-drain capacitance, C_Q) and the load capacitance, C_L.

Another problem caused by switch capacitance is the retained charge when switching channels. This charge can cause transients in the switch output, and Figure 7.32 illustrates the phenomenon.

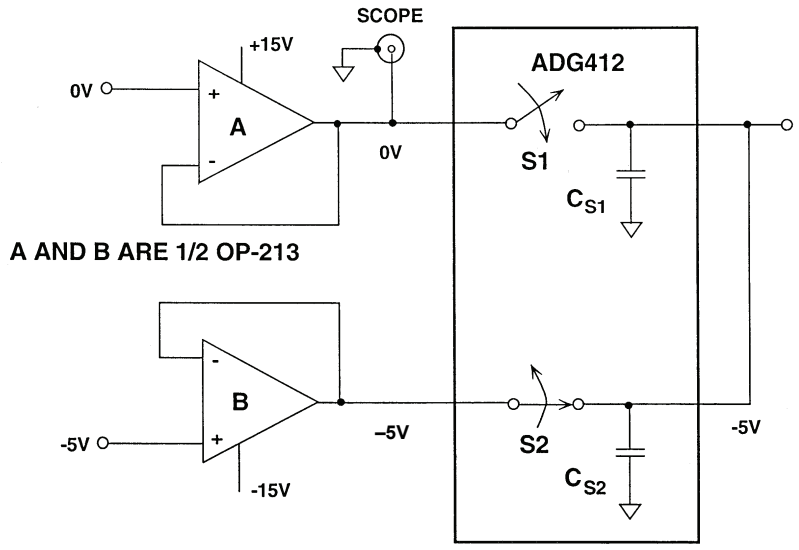


Figure 7.32: *Charge Coupling Causes Dynamic Settling Time Transient When Multiplexing Signals*

Assume that initially S2 is closed and S1 open. C_{S1} and C_{S2} are charged to –5 V. As S2 opens, the –5 V remains on C_{S1} and C_{S2}, as S1 closes. Thus, the output of Amplifier A sees a –5 V transient. The output will not stabilize until Amplifier A's output fully discharges C_{S1} and C_{S2} and settles to 0 V. The scope photo in Figure 7.33 depicts this transient. The amplifier's transient load settling characteristics will therefore be an important consideration when choosing the right input buffer.

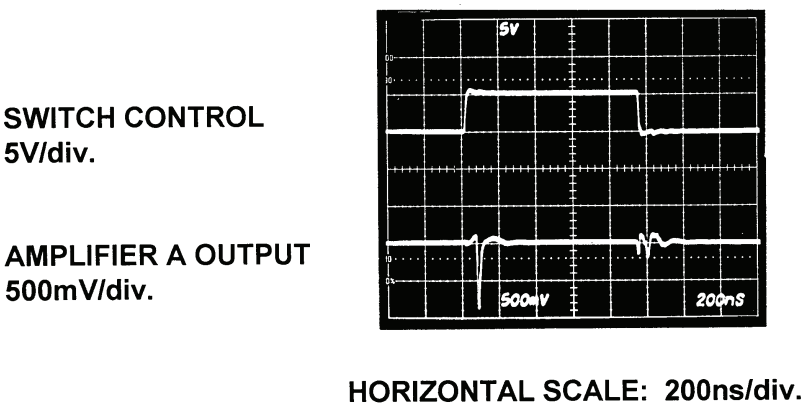


Figure 7.33: *Output of Amplifier Shows Dynamic Settling Time Transient Due to Charge Coupling*

Crosstalk is related to the capacitances between two switches. This is modeled as the C_{SS} capacitance shown in Figure 7.34.

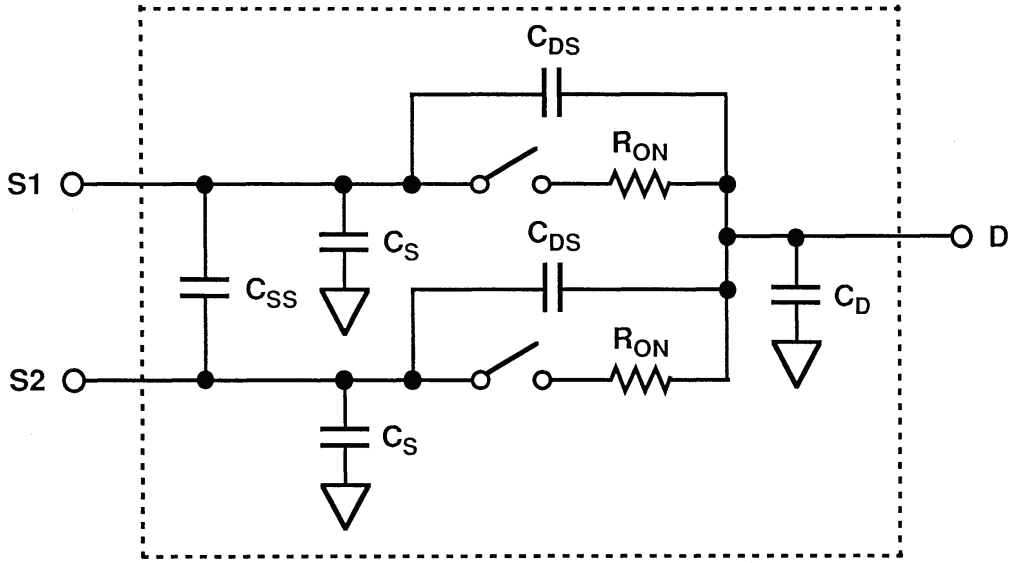


Figure 7.34: *Channel-to-Channel Crosstalk Equivalent Circuit for Adjacent Switches*

Figure 7.35 shows typical crosstalk performance of the ADG708 8-channel CMOS multiplexer.

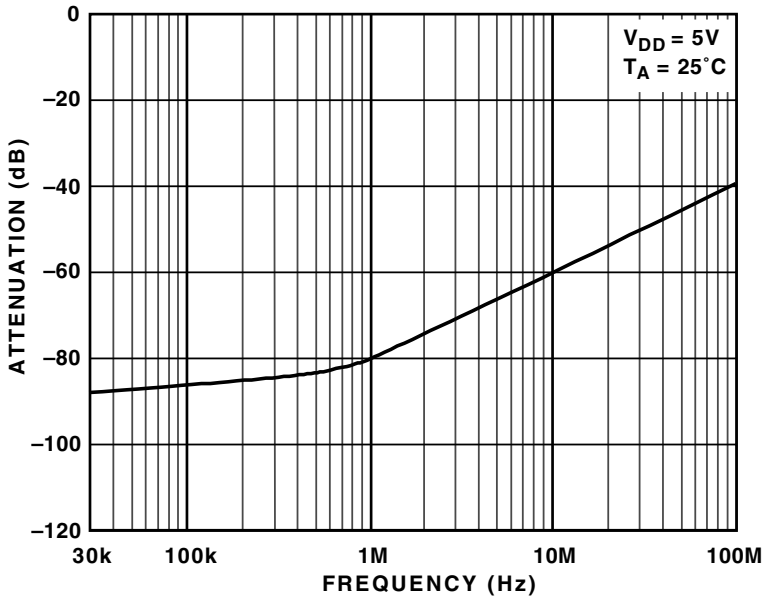
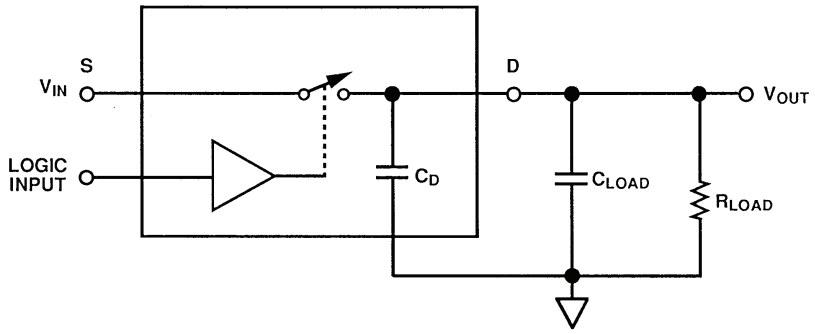


Figure 7.35: *Crosstalk vs. Frequency for ADG708 8-Channel Multiplexer*

Finally, the switch itself has a settling time that must be considered. Figure 7.36 shows the dynamic transfer function. The settling time can be calculated, because the response is a function of the switch and circuit resistances and capacitances. One can assume that this is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy as shown in Figure 7.37.



$$\text{OFF-TO-ON:}\quad t_{SETT} = t_{ON} + \left(\frac{R_{ON}R_{LOAD}}{R_{ON}+R_{LOAD}}\right)(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

$$\text{ON-TO-OFF:}\quad t_{SETT} = t_{OFF} + (R_{LOAD})(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

Settling time is the time required for the switch output to settle within a given error band of the final value.

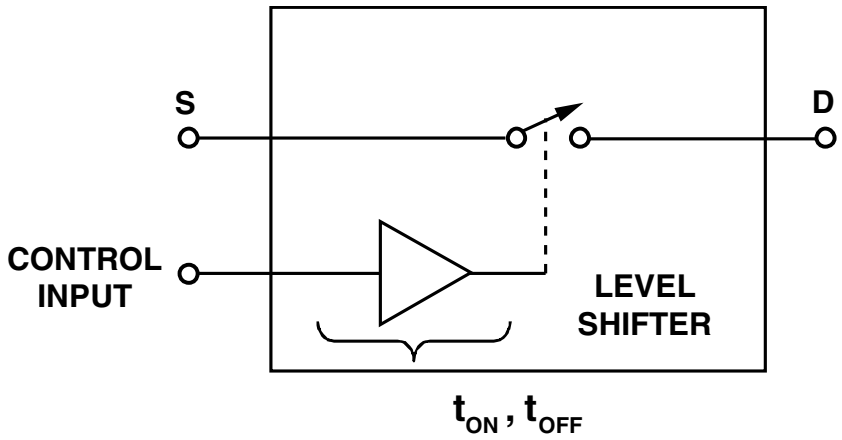
Figure 7.36: *Multiplexer Settling Time*

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Figure 7.37: *Number of Time Constants Required to Settle to 1 LSB Accuracy for a Single-Pole System*

Applying the Analog Switch

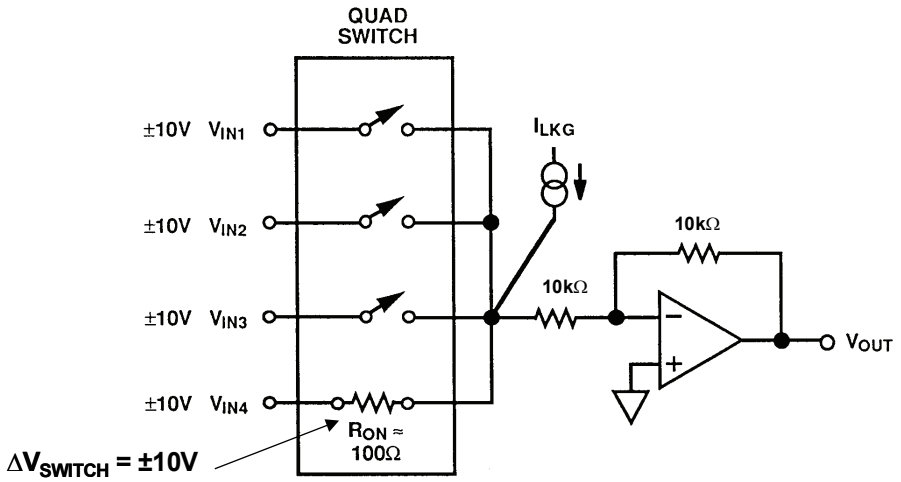
Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propagation delay from the control input to the toggling of the switch, and are largely caused by time delays in the drive and level-shift circuits (see Figure 7.38). The t_{ON} and t_{OFF} values are generally measured from the 50% point of the control input leading edge to the 90% point of the output signal level.



- **t_{ON} and t_{OFF} should not be confused with settling time.**
- **t_{ON} and t_{OFF} are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.**
- **t_{ON} and t_{OFF} are measured from the 50% point of the control input to the 90% point of the output signal level.**

Figure 7.38: *Applying the Analog Switch: Dynamic Performance Considerations*

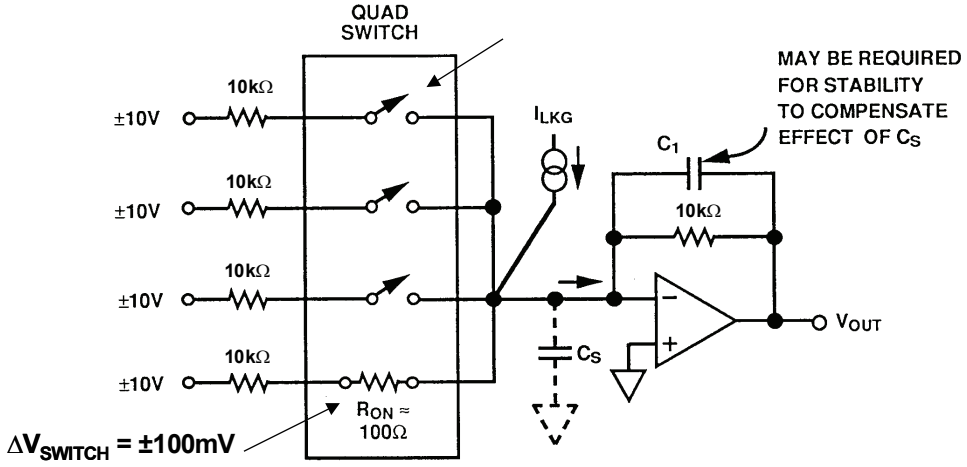
We will next consider the issues involved in buffering a CMOS switch or multiplexer output using an op amp. When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the on-resistance, and its nonlinear change as a function of input voltage, will cause gain and distortion errors as shown in Figure 7.39. If the resistors are large, the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of R_{ON}.



- **ΔR_{ON} caused by ΔV_{IN} , degrades linearity of V_{OUT} relative to V_{IN}.**
- **ΔR_{ON} causes overall gain error in V_{OUT} relative to V_{IN} .**

Figure 7.39: *Applying the Analog Switch: Unity Gain Inverter with Switched Input*

To minimize the effect of R_{ON} change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 7.76. This ensures the switches are only modulated with about ±100 mV rather than the full ±10 V—but a separate resistor is required for each input leg.

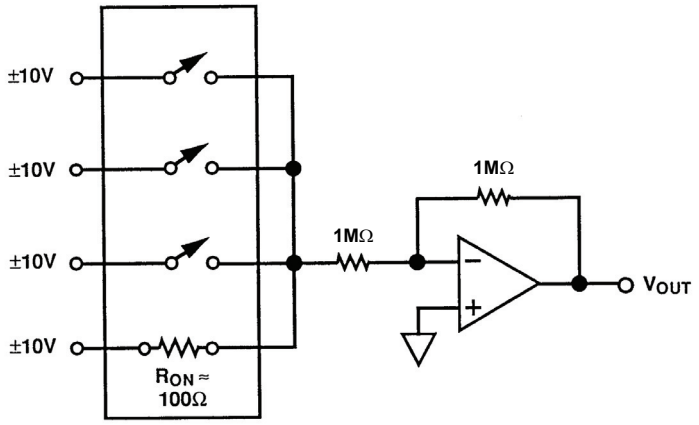


- **Switch drives a virtual ground.**
- **Switch sees only ±100mV, not ±10V, minimizes ΔR_{ON} .**

Figure 7.40: *Applying the Analog Switch: Minimizing the Influence of ΔR_{ON}*

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer, because any capacitance added to that node introduces phase shift to the amplifier closed-loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance, C_1, across the feedback resistor may be required to stabilize the circuit.

The finite value of R_{ON} can be a significant error source in the circuit shown in Figure 7.41. The gain-setting resistors should be at least 1,000 times larger than the switch on-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy but lower bandwidth and greater sensitivity to leakage and bias current.



- **ΔR_{ON} is small compared to 1MΩ switch load.**
- **Effect on transfer accuracy is minimized.**
- **Bias current and leakage current effects are now very important.**
- **Circuit bandwidth degrades.**

Figure 7.41: *Applying the Analog Switch: Minimizing Effects of ΔR_{ON} Using Large Resistor Values*

A better method of compensating for R_{ON} is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 7.42. It is a safe assumption that the multiple switches, fabricated on a single chip, are well-matched in absolute characteristics and tracking over temperature. Therefore, the amplifier is closed-loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.

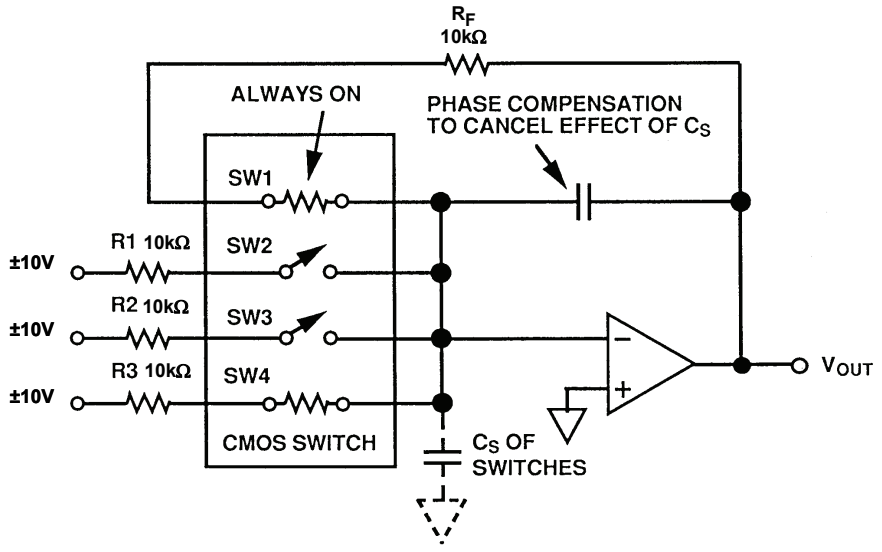


Figure 7.42: *Applying the Analog Switch: Using "Dummy" Switch in Feedback to Minimize Gain Error Due to ΔR_{ON}*

The best multiplexer design drives the noninverting input of the amplifier as shown in Figure 7.43. The high input impedance of the noninverting input eliminates the errors due to R_{ON}.

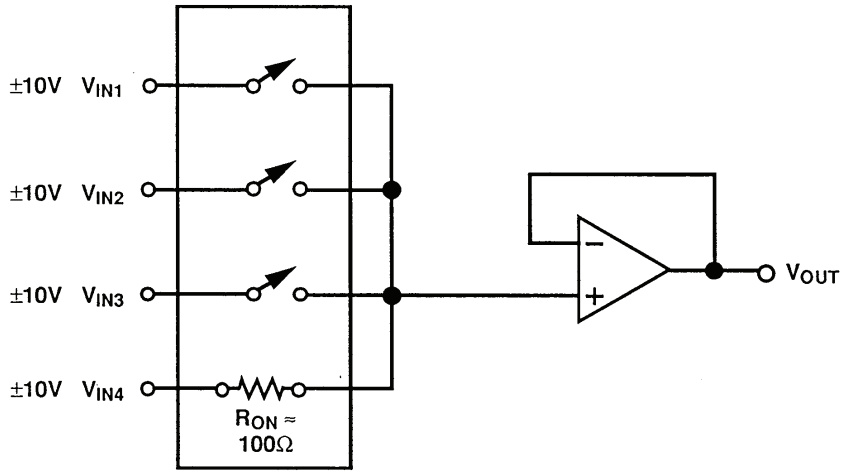
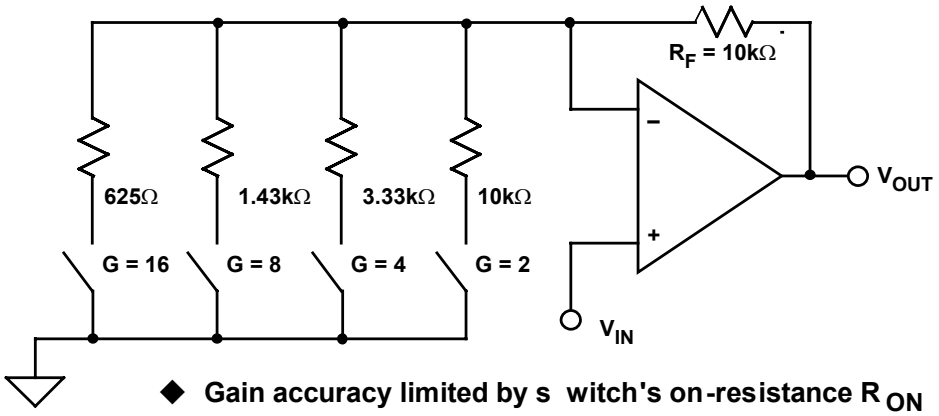


Figure 7.43: *Applying the Analog Switch: Minimizing the Influence of ΔR_{ON} Using Noninverting Configuration*

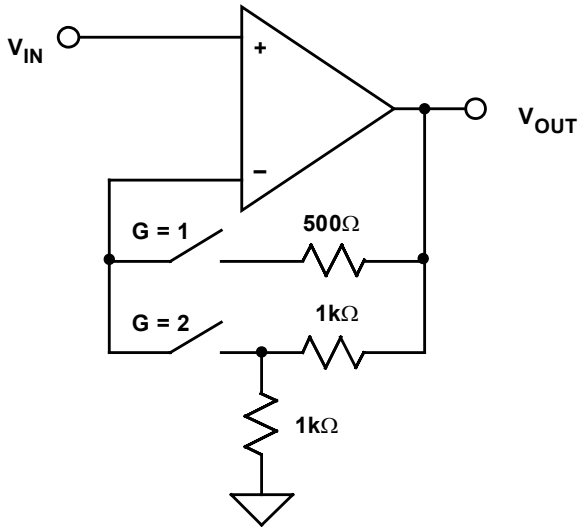
CMOS switches and multiplexers are often used with op amps to make programmable gain amplifiers (PGAs). To understand R_{ON}'s effect on their performance, consider Figure 7.44, a poor PGA design. A noninverting op amp has 4 different gain-set resistors, each grounded by a switch, with an R_{ON} of 100 Ω to 500 Ω. Even with R_{ON} as low as 25 Ω, the gain of 16 error would be 2.4%, worse than 8-bit accuracy! R_{ON} also changes over temperature, and switch-switch.



- Gain accuracy limited by s witch's on-resistance R_{ON} and R_{ON} modulation
- R_{ON} typically 1 - 500Ω for CMOS or JFET switch
- For R_{ON} = 25Ω, there is a 2 .4% gain error for G = 16
- R_{ON} drift over temperature limits accuracy
- Must use very low R_{ON} switches

Figure 7.44: *A Poorly Designed PGA Using CMOS Switches*

To attempt "fixing" this design, the resistors might be increased, but noise and offset could then be a problem. The only way to accuracy with this circuit is to use relays, with virtually no R_{ON}. Only then will the few mΩ of relay R_{ON} be a small error vis-à-vis 625 Ω.



- R_{ON} is not in series with gain setting resistors
- R_{ON} is small compared to input impedance
- Only slight offset errors occur due to bias current flowing through the switches

Figure 7.45: *Alternate PGA Configuration Minimizes the Effects of R_{ON}*

It is much better to use a circuit insensitive to R_{ON}! In Figure 7.45, the switch is placed in series with the inverting input of an op amp. Since the op amp input impedance is very large, the switch R_{ON} is now irrelevant, and gain is now determined solely by the external resistors. Note—R_{ON} may add a small offset error if op amp bias current is high. If this is the case, it can readily be compensated with an equivalent resistance at V_{IN}.

1 GHz CMOS Switches

The ADG918/ADG919 are the first switches using a CMOS process to provide high isolation and low insertion loss up to and exceeding 1 GHz. The switches exhibit low insertion loss (0.8 dB) and high off isolation (37 dB) when transmitting a 1 GHz signal. In high frequency applications with throughput power of +18 dBm or less at 25°C, they are a cost-effective alternative to gallium arsenide (GaAs) switches. A block diagram of the devices is shown in Figure 7.82 along with isolation and loss versus frequency plots given in Figure 7.46.

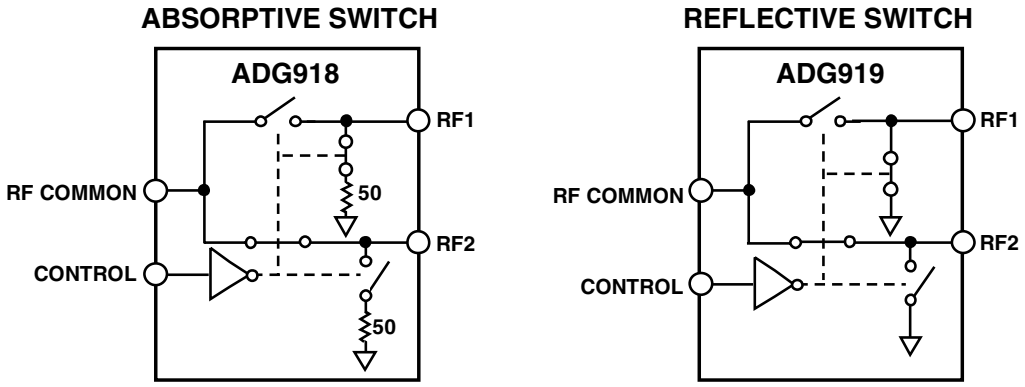


Figure 7.46: *1-GHz CMOS 1.65-V to 2.75-V 2:1 Mux/SPDT Switches*

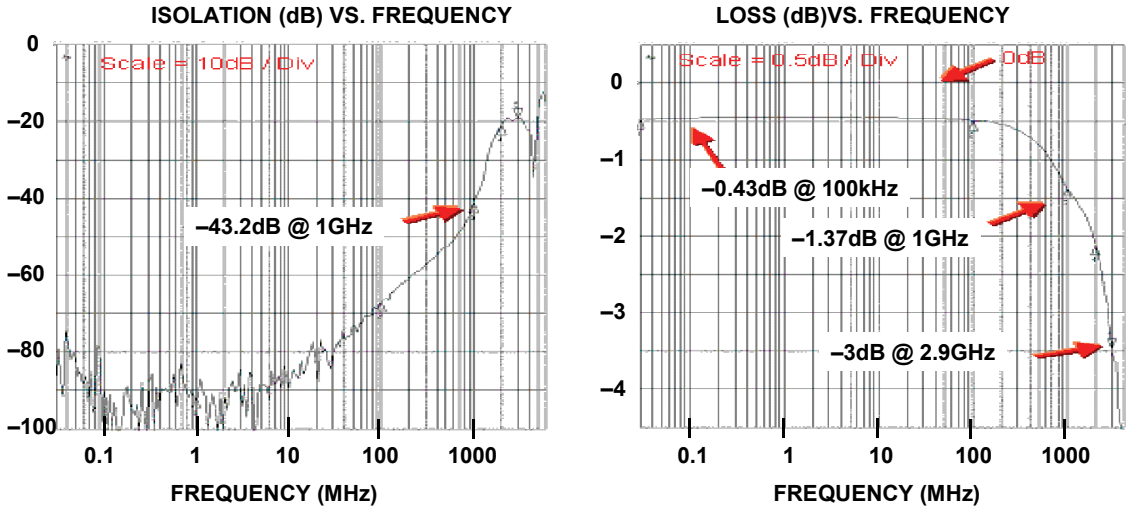


Figure 7.47: *Isolation and Frequency Response of ADG918/ADG919 1 GHz Switch*

The ADG918 is an absorptive switch with 50 Ω terminated shunt legs that allow impedance matching with the application circuit, while the ADG919 is a reflective switch designed for use where the terminations are external to the chip. Both offer low power consumption (<1 μA), tiny packages (8-lead MSOP and 3 mm × 3 mm lead frame chip scale package), single-pin control voltage levels that are CMOS/LVTTL compatible, making the switches ideal for wireless applications and general-purpose RF switching.

Video Switches and Multiplexers

In order to meet stringent specifications of bandwidth flatness, differential gain and phase, and 75 Ω drive capability, high speed complementary bipolar processes are more suitable than CMOS processes for video switches and multiplexers. Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 50 ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch on-resistance with signal level (R_{on} *modulation*) introduces unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies. The tradeoffs, of course, are higher power and cost.

Functional block diagrams of the AD8170/AD8174/AD8180/AD8182 bipolar video multiplexers are shown in Figure 7.48. The AD8183/AD8185 video multiplexer is shown in Figure 7.49. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10 ns to 0.1%. The AD8186/AD8187 are single-supply versions of the AD8183/AD8185.

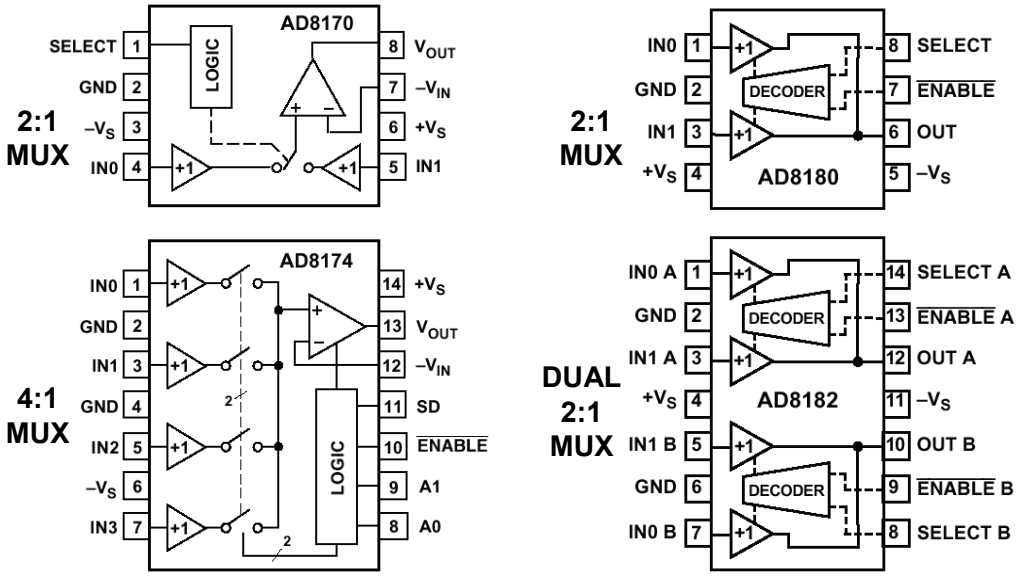


Figure 7.48: *AD8170/AD8174/AD8180/AD8182 Bipolar Video Multiplexers*

The AD8170/8174 series of muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80 dB for the entire family.

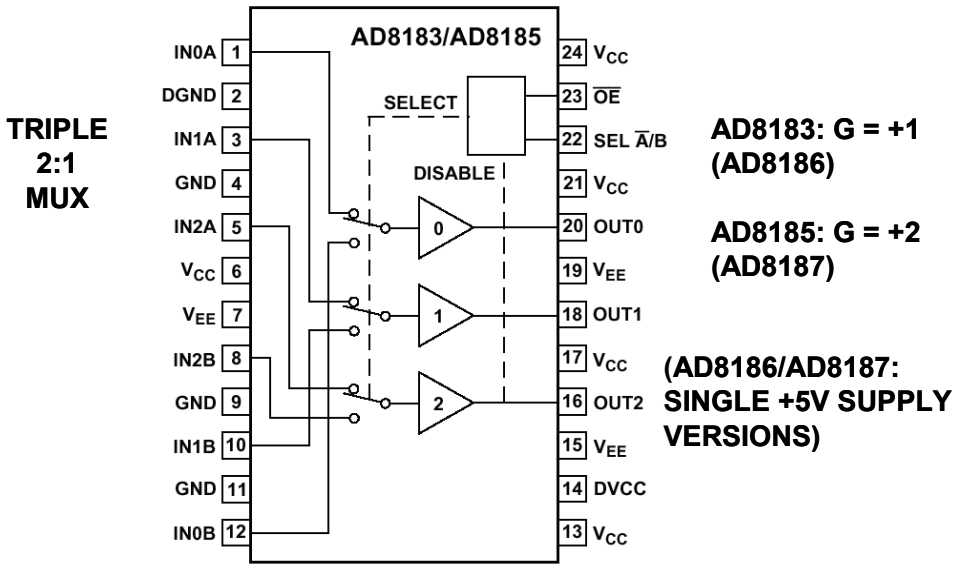


Figure 7.49: *AD8183/AD8185 Video Multiplexers*

Figure 7.50 shows an application circuit for three AD8170 2:1 muxes, where a single RGB monitor is switched between two RGB computer video sources.

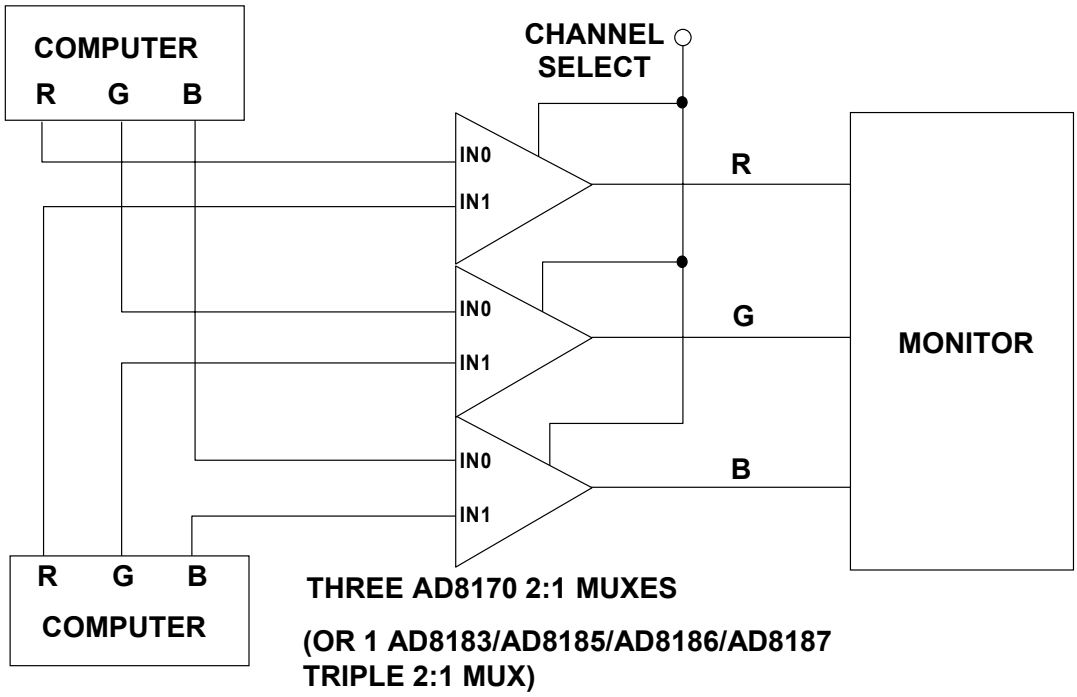


Figure 7.50: *Dual Source RGB Multiplexer Using Three 2:1 Muxes*

In this setup, the overall effect is that of a three-pole, double-throw switch. The three video sources constitute the three poles, and either the upper or lower of the video sources constitute the two switch states. Note that the circuit can be simplified by using a single AD8183, AD8185, AD8186, or AD8187 triple dual input multiplexer.

The AD8174 or AD8184 4:1 mux is used in Figure 7.51, to allow a single high speed ADC to digitize the RGB outputs of a scanner.

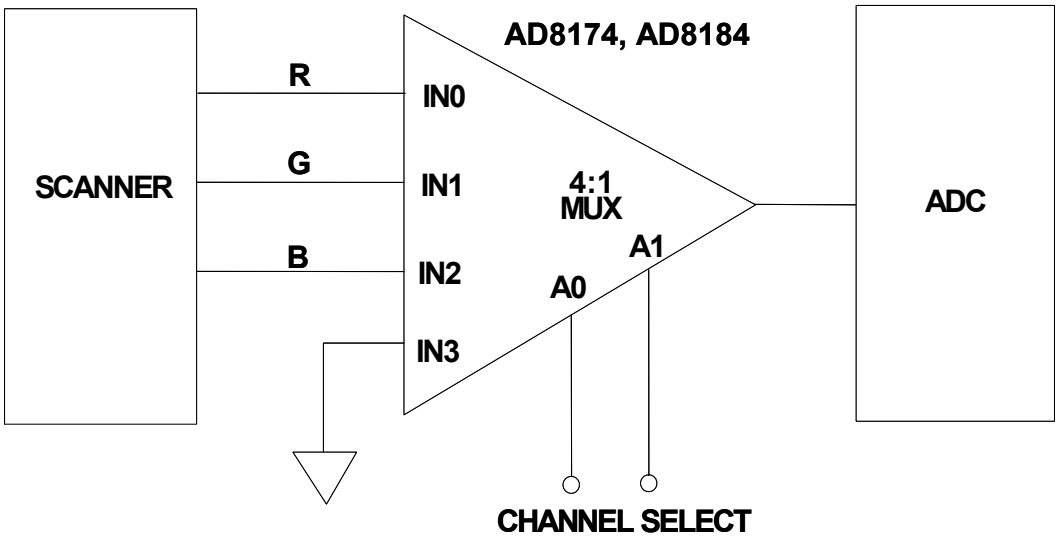


Figure 7.51: *Digitizing RGB Signals with One ADC and A 4:1 Mux*

The RGB video signals from the scanner are fed in sequence to the ADC, and digitized in sequence, making efficient use of the scanner data with one ADC.

Video Crosspoint Switches

The AD8116 extends the multiplexer concepts to a fully integrated, 16 × 16 buffered video crosspoint switch matrix (Figure 7.52). A crosspoint switch allows any input to be connected to any output, or combination of outputs. The only limitation is that any output can have no more than one input connected to it.

The 3 dB bandwidth is of the AD8116 is greater than 200 MHz, and the 0.1 dB gain flatness extends to 60 MHz. Channel switching time is less than 30 ns to 0.1%. Channel-to-channel crosstalk is −70 dB measured at 5 MHz. Differential gain and phase is 0.01% and 0.01° for a 150 Ω load. Total power dissipation is 900 mW on ±5 V.

The AD8116 includes output buffers that can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control that can accommodate daisy-chaining of several devices. The AD8116 package is a 128-pin 14 mm × 14 mm LQFP.
Other members of the crosspoint switch family include the AD8108/AD9109 8 × 8 crosspoint switch, the AD8110/AD8111 260 MHz 16 × 8 buffered crosspoint switch, the AD8113 audio/video 60 MHz 16 × 16 crosspoint switch, and the AD8114/AD8115 low cost 225 MHz 16 × 16 crosspoint switch.

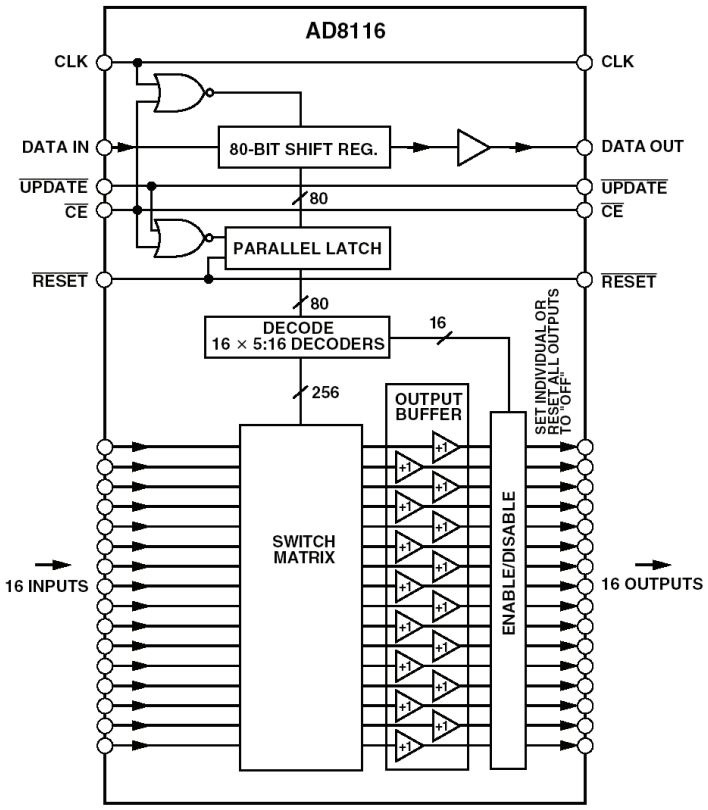


Figure 7.52: *AD8116 16×16 200-MHz Buffered Video Crosspoint Switch*

Digital Crosspoint Switches

The AD8152 is a 3.2 Gbps 34 × 34 asynchronous digital crosspoint switch designed for high speed networking (see Figure 7.53). The device operates at data rates up to 3.2 Gbps per port, making it suitable for Sonet/SDH OC-48 with Forward Error Correction (FEC). The AD8152 has digitally programmable current mode outputs that can drive a variety of termination schemes and impedances while maintaining the correct voltage level and minimizing power consumption. The part operates with a supply voltage as low as +2.5 V, with excellent input sensitivity. The control interface is compatible with LVTTL or CMOS/TTL.

As the lowest power solution of any comparable crosspoint switch, the AD8152 dissipates less than 2 W at 2.5 V supply with all I/Os active and does not require external heat sinks. The low jitter specification of less than 45 ps make the AD8152 ideal for high speed networking systems. The AD8152's fully differential signal path reduces jitter and crosstalk while allowing the use of smaller single-ended voltage swings. It is offered in a 256-ball SBGA package that operates over the industrial temperature range of 0°C to +85°C.

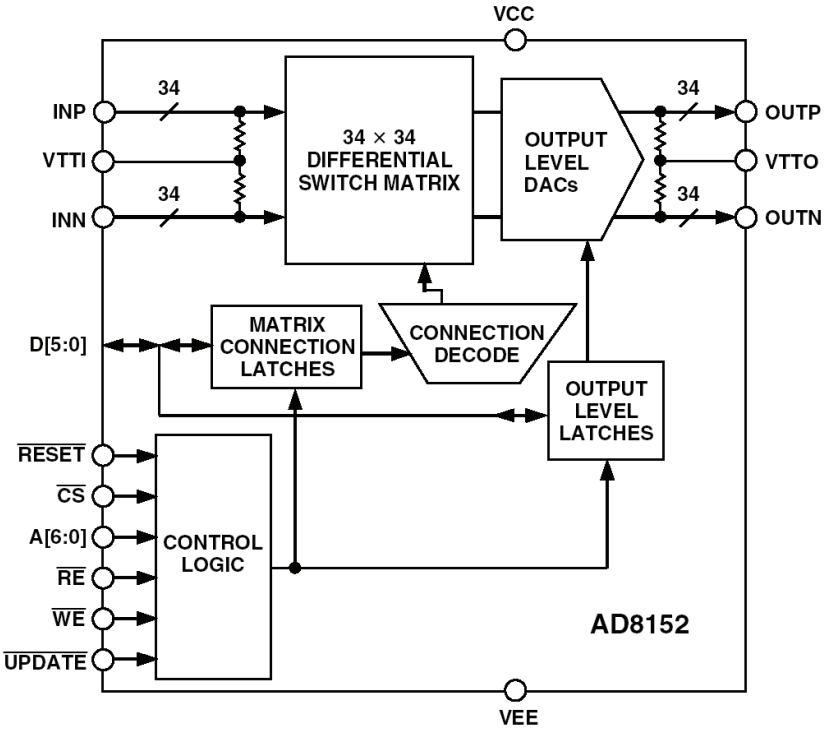


Figure 7.53: *AD8152 3.2-Gbps Asynchronous Digital Crosspoint Switch*

Parasitic Latch-Up in CMOS Switches and Muxes

Because multiplexers are often at the front-end of a data acquisition system, their inputs generally come from remote locations—hence, they are often subjected to overvoltage conditions. Although this topic is treated in more detail in Chapter 11, an understanding of the problem as it relates to CMOS devices is particularly important. Although this discussion centers around multiplexers, it is germane to nearly all types of CMOS parts.

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 7.54. Parasitic SCR (silicon controlled rectifier) latch-up can occur if the analog switch terminal has voltages more positive than V_{DD} or more negative than V_{SS}. Even a transient situation, such as power-on with an input voltage present, can trigger a parasitic latch-up. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

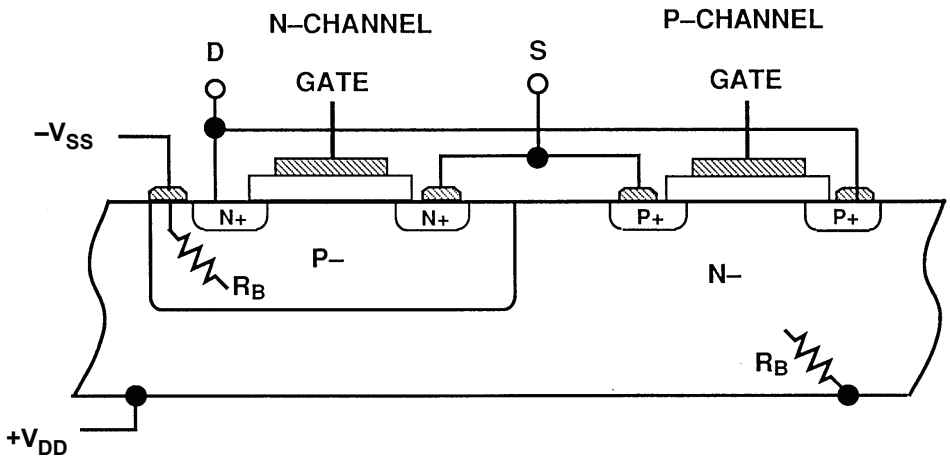


Figure 7.54: *Cross-Section of a Junction-Isolation CMOS Switch*

The parasitic SCR mechanism is shown in Figure 7.55. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than V_{DD} or one diode drop more negative than V_{SS}. In the former case, the V_{DD} terminal becomes the SCR gate input and provides the current to trigger SCR action. In the case where the voltage is more negative than V_{SS}, the V_{SS} terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

In general, to prevent the latch-up condition, the inputs to CMOS devices should never be allowed to be more than 0.3 V above the positive supply or 0.3 V below the negative supply. Note that this restriction also applies when the power supplies are off ($V_{DD} = V_{SS} = 0$ V), and therefore devices can latch up if power is applied to a part when signals are present on the inputs. Manufacturers of CMOS devices invariably place this restriction in the data sheet table of absolute maximum ratings. In addition, the input current under overvoltage conditions should be restricted to 5 mA to 30 mA, depending upon the particular device.

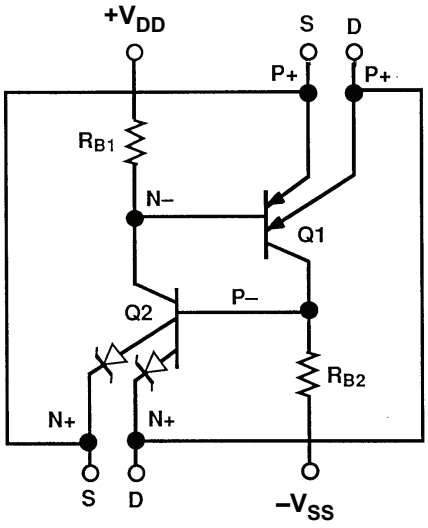
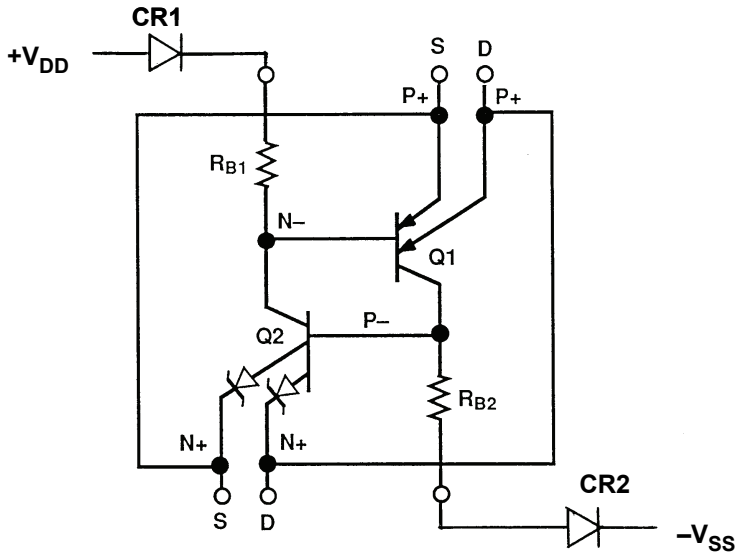


Figure 7.55: *Bipolar Transistor Equivalent Circuit for CMOS Switch Shows Parasitic SCR Latch*

In order to prevent this type of SCR latch up, a series diode can be inserted into the V_{DD} and V_{SS} terminals as shown in Figure 7.56. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.



Diodes CR1 and CR2 block base current drive to Q1 and Q2 in the event of overvoltage at S or D.

Figure 7.56: *Diode Protection Scheme for CMOS Switch*

If diode protection is used, the analog voltage range of the switch will be reduced by one V_{BE} drop at each rail, and this can be inconvenient when using low supply voltages.

As noted, CMOS switches and multiplexers must also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level as shown in Figure 7.57, generally less than 5 mA to 30 mA. Because of the resistive attenuator formed by R_{LOAD} and R_{LIMIT}, this method works only if the switch drives a relatively high impedance load.

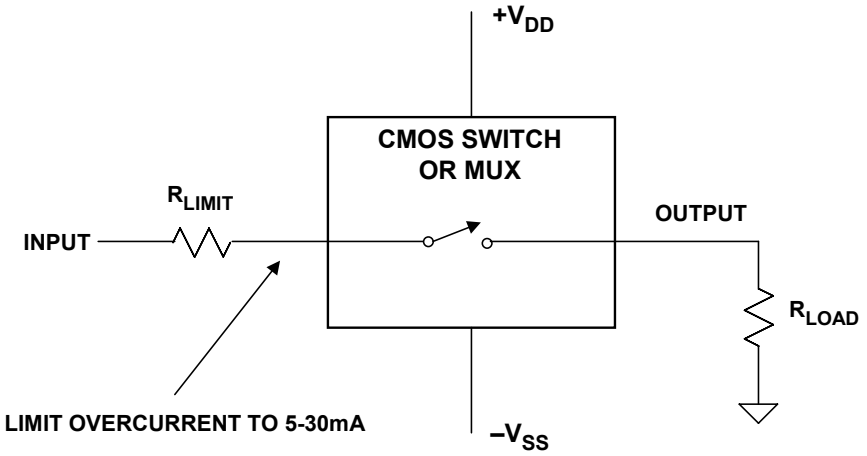


Figure 7.57: *Overcurrent Protection Using External Resistor*

A common method for input protection is shown in Figure 7.58 where Schottky diodes are connected from the input terminal to each supply voltage as shown. The diodes effectively prevent the inputs from exceeding the supply voltage by more than 0.3 V to 0.4 V, thereby preventing latch-up conditions. In addition, if the input voltage exceeds the supply voltage, the input current flows through the external diodes to the supplies, not the device. Schottky diodes can easily handle 50 mA to 100 mA of transient current, therefore the R_{LIMIT} resistor can be quite low. It must be remembered that the Schottky diodes will have some capacitance and leakage current.

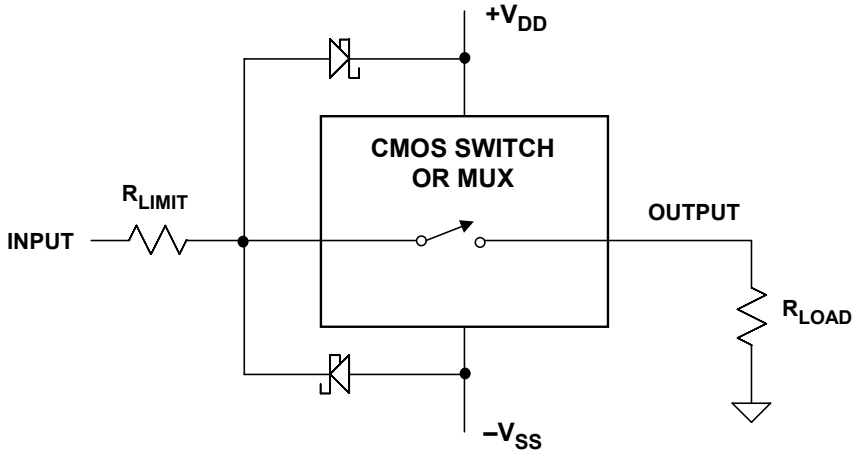


Figure 7.58: *Input Protection Using External Schottky Diodes*

Most CMOS devices have internal ESD-protection diodes connected from the inputs to the supply rails, making the devices less susceptible to latch-up. However, the internal diodes begin conduction at 0.6 V, and have limited current-handling capability, thus adding the external Schottky diodes offers an added degree of protection.

Note that latch-up protection does not provide overcurrent protection, and vice versa. If both fault conditions can exist in a system, then both protective diodes and resistors should be used.

Analog Devices uses trench-isolation technology to produce its LC^{2}MOS analog switches. The process reduces the latch-up susceptibility of the device, the junction capacitances, increases switching time, and leakage current, and extends the analog voltage range to the supply rails.

Figure 7.59 shows the cross-sectional view of the trench-isolated CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction. Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latch-up are greatly reduced.

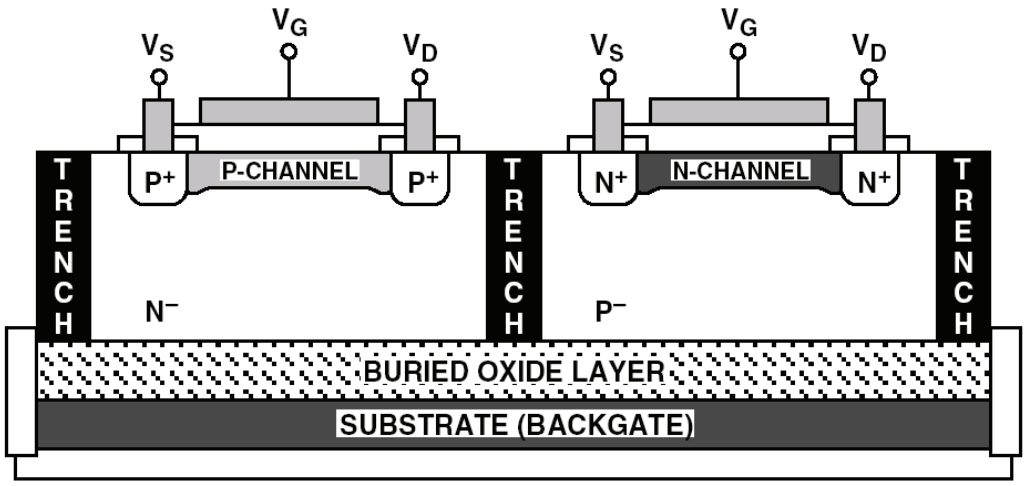


Figure 7.59: *Trench-Isolation L^{2}CMOS Structure*

The ADG508F, ADG509F, ADG528F, ADG438F, and ADG439F are ±15 V trench-isolated L^{2}CMOS multiplexers which offer fault protection for input and output overvoltages between –40 V and + 55 V. These devices use a series structure of three MOSFETS in the signal path: an N-channel, followed by a P-channel, followed by an N-channel. In addition, the signal patch becomes a high impedance when the power supplies are turned off. This structure offers a high degree of latch up and overvoltage protection—at the expense of higher R_{ON} (~300 Ω), and more R_{ON} variation with signal level. For more details of this protection method, refer to the individual product data sheets.

SECTION 7.3: SAMPLE-AND-HOLD CIRCUITS

Introduction and Historical Perspective

The *sample-and-hold amplifier*, or SHA, is a critical part of most data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

Although today the SHA function has become an integral part of the *sampling* ADC, which is the vast majority of ADCs made today, understanding the fundamental concepts governing its operation is essential to understanding ADC dynamic performance.

When the sample-and-hold is in the sample (or track) mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period (such as the AD684, AD781, and AD783). These will not be considered here. Strictly speaking, a sample-and-hold with good tracking performance should be referred to as a *track-and-hold* circuit, but in practice the terms are used interchangeably.

The most common application of a SHA is to maintain the input to an ADC at a constant value during conversion. With many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted—this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion. See the section in Chapter 6 on successive approximation ADCs.

Integration of the SHA function was made possible by new process developments including high speed complementary bipolar processes and advanced CMOS processes. In fact, the proliferation and popularity of sampling ADCs has been so great that today (2006), one rarely has the need for a separate SHA.

The advantage of a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall dc and ac performance is fully specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA. This is especially important when one considers dynamic specifications such as SFDR and SNR.

Although the largest applications of SHAs are with ADCs, they are also occasionally used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

Basic SHA Operation

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 7.60.

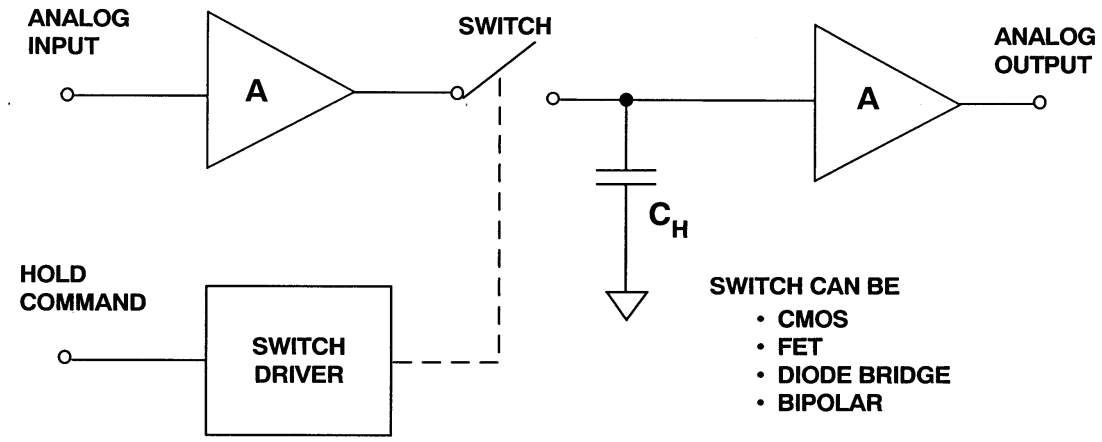


Figure 7.60: *Basic Sample-and-Hold Circuit*

The energy storage device, the heart of the SHA, is almost always a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the *track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 7.61, and some of the SHA error sources are shown graphically in Figure 7.62. Because there are both dc and ac performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Pedestal Nonlinearity	STATIC: ◆ Droop ◆ Dielectric ◆ Absorption	
DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise	DYNAMIC: ◆ Acquisition Time ◆ Switching Transient

Figure 7.61: *Sample-and-Hold Specifications*

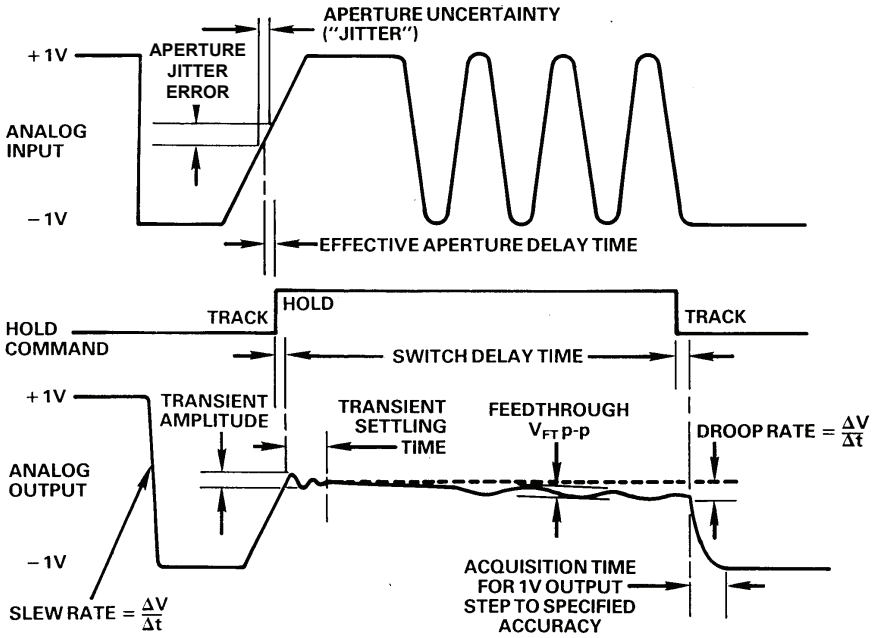


Figure 7.62: *Some Sources of Sample-and-Hold Errors*

Specifications

While the specifications of the sample and hold part of a sampling converter are not broken out separately, their effect is included in the overall specifications of the converter.

Track Mode Specifications

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold

mode.) The principal track mode specifications are *offset*, *gain*, *nonlinearity*, *bandwidth*, *slew rate*, *settling time*, *distortion*, and *noise*. However, distortion and noise in the track mode are often of less interest than in the hold mode.

Track-to-Hold Mode Specifications

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of nonideal switches. This results in a hold mode dc offset voltage which is called *pedestal* error as shown in Figure 7.63. If the SHA is driving an ADC, the pedestal error appears as a dc offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold-mode distortion.

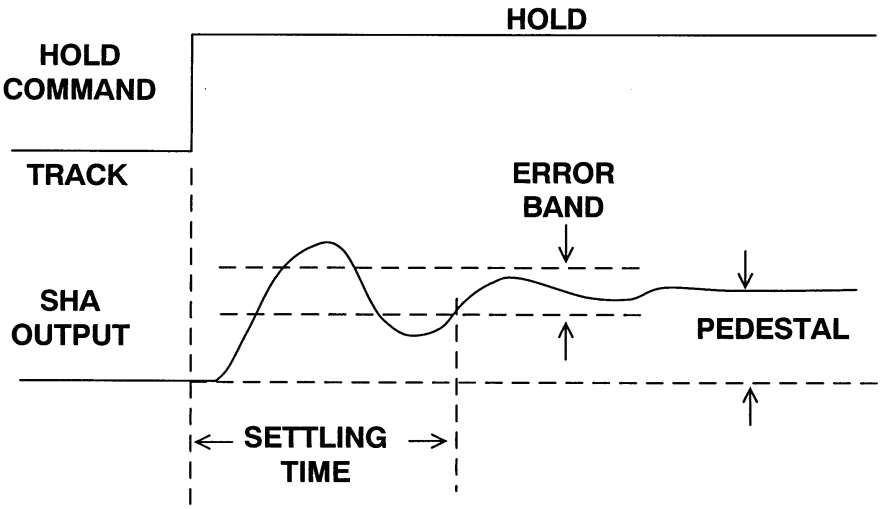


Figure 7.63: *Track-to-Hold Mode Pedestal, Transient, and Settling Time Errors*

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but nonzero) interval required for this action is called *aperture time*. The various quantities associated with the internal SHA timing are shown in the Figure 7.64.

The actual value of the voltage that is held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself. Figure 7.65

shows what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold pedestal and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch as shown in Figure 7.65. The first order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (t_a).

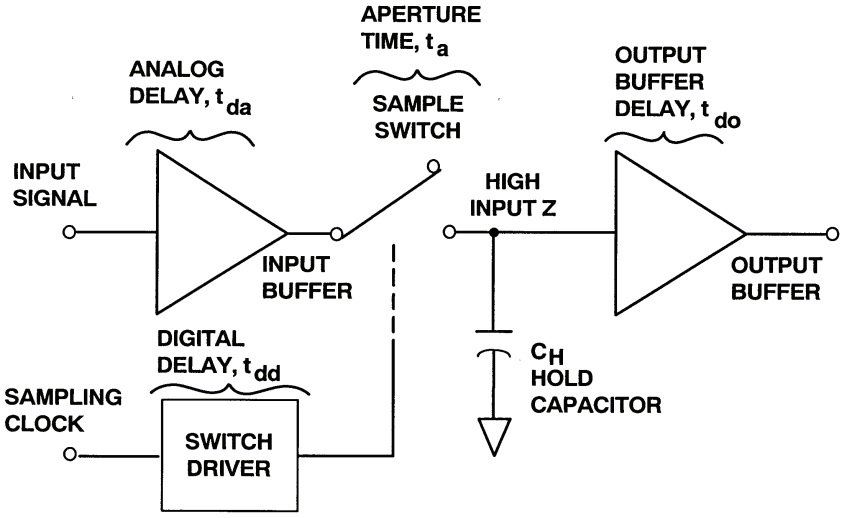


Figure 7.64: *SHA Circuit Showing Internal Timing*

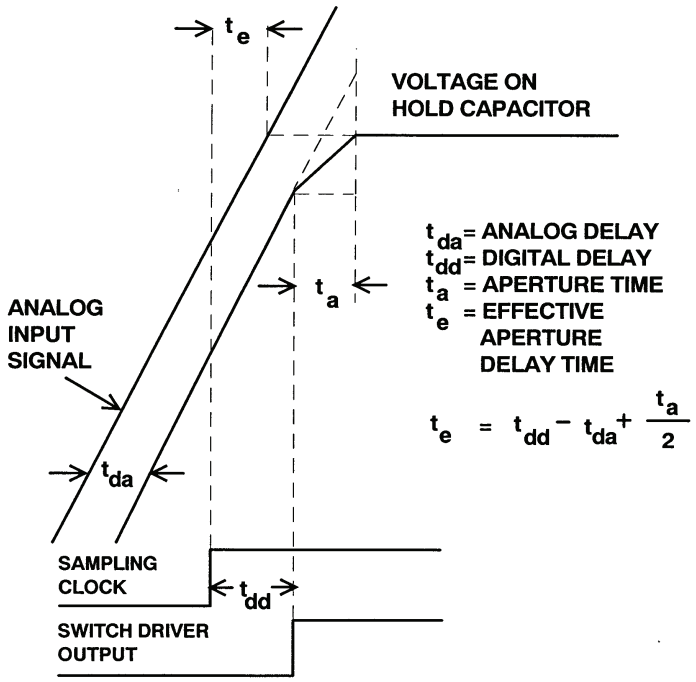


Figure 7.65: *SHA Waveforms*

The model shows that the finite time required for the switch to open (t_a) is equivalent to introducing a small delay in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. It is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, (t_e) and is defined as the time difference between the analog propagation delay of the front-end buffer (t_{da}) and the switch digital delay (t_{dd}) plus one-half the aperture time ($t_a/2$). The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time ($t_a/2$) and the switch digital delay (t_{dd}) is less than the propagation delay through the input buffer (t_{da}). The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero-crossing of the input sine wave is the aperture delay time as shown in Figure 7.66.

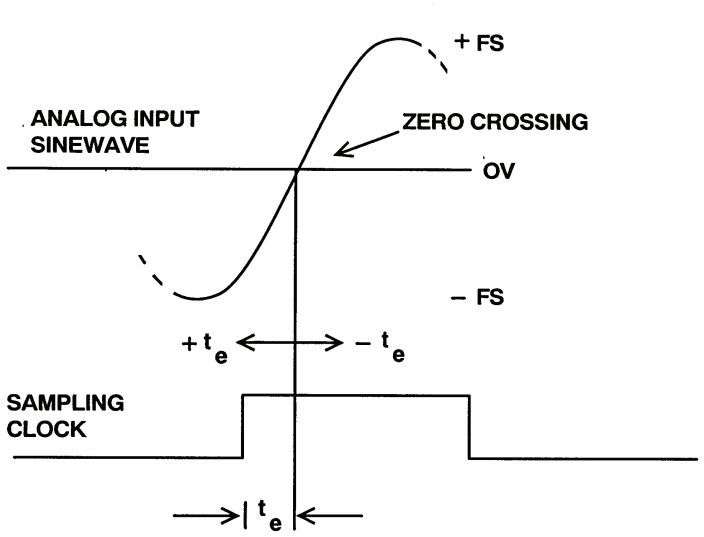


Figure 7.66: *Effective Aperture Delay Time*

Aperture delay produces no errors, but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). If there is sample-to-sample variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 7.67. This sample-to-sample variation in the instant the switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in picoseconds rms. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input dv/dt increases.

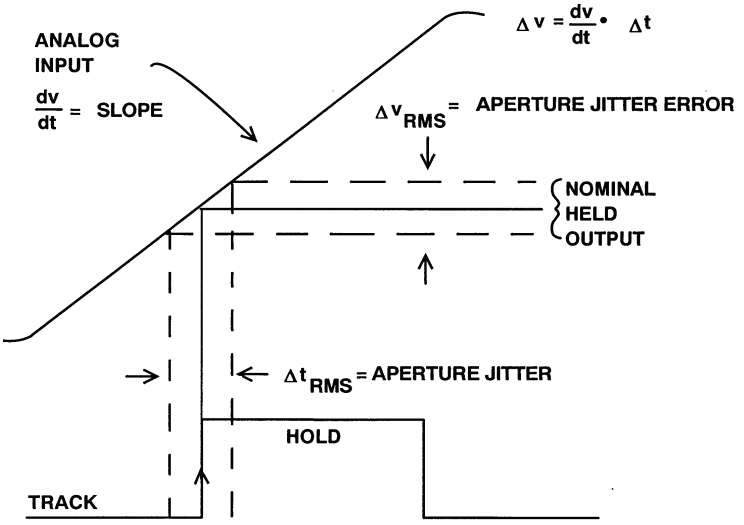


Figure 7.67: *Effects of Aperture or Sampling Clock Jitter on SHA Output*

Figure 7.68 shows the effects of total sampling clock jitter on the signal-to-noise ratio (SNR) of a sampled data system. The total rms jitter will be composed of a number of components, the actual SHA aperture jitter often being the least of them.

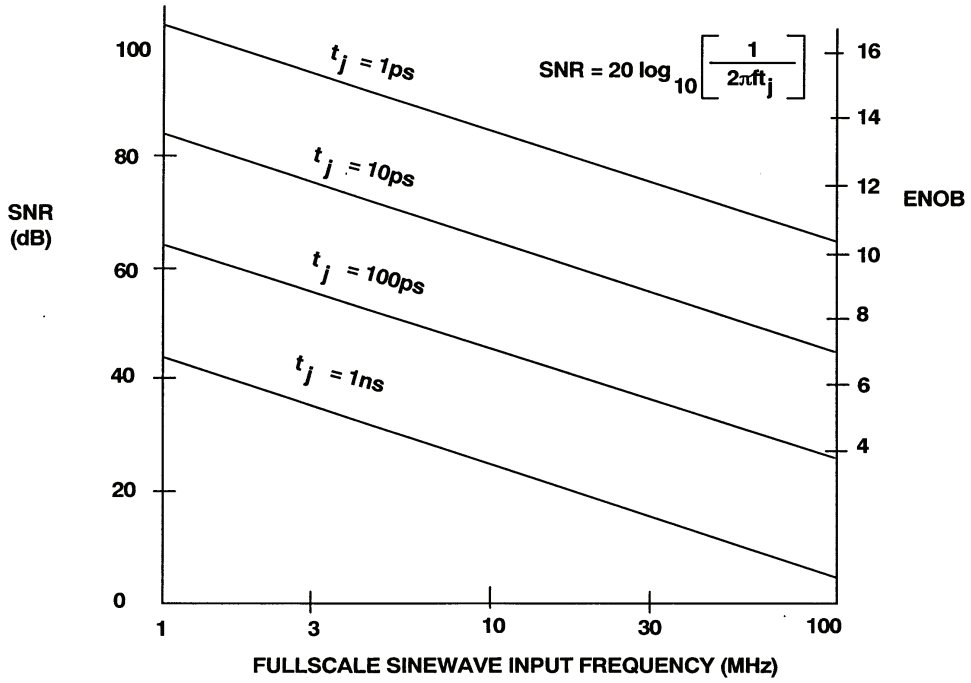


Figure 7.68: *Effects of Sampling Clock Jitter on SNR*

Hold Mode Specifications

During the hold mode there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows in or out of the hold capacitor, it will slowly charge or discharge, and its voltage will change. This effect is known as *droop* in the SHA output and is expressed in V/µs. Droop can be caused by leakage across a dirty PC board if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of the output buffer amplifier. An acceptable value of droop is where the output of a SHA does not change by more than ½ LSB during the conversion time of the ADC it is driving, although this value is highly dependent on the ADC architecture. Where droop is due to leakage current in reversed biased junctions (CMOS switches or FET amplifier gates), it will double for every 10°C increase in chip temperature—which means that it will increase a thousand fold between +25°C and +125°C. Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode. Differential techniques are often used to reduce the effects of droop in modern IC sample-and-hold circuits that are part of the ADC.

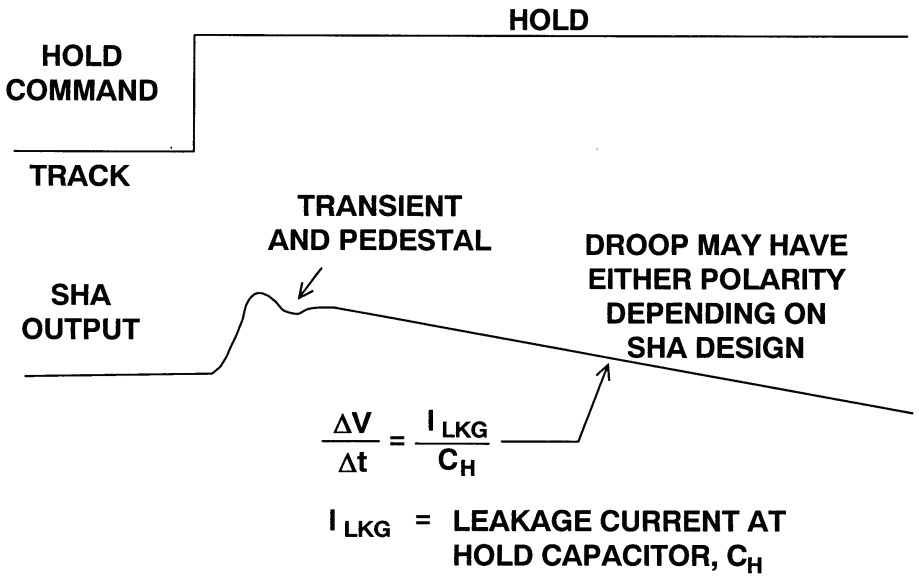


Figure 7.69: *Hold Mode Droop*

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit, it will recover some of its charge as shown in Figure 7.70. The phenomenon is known as *dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

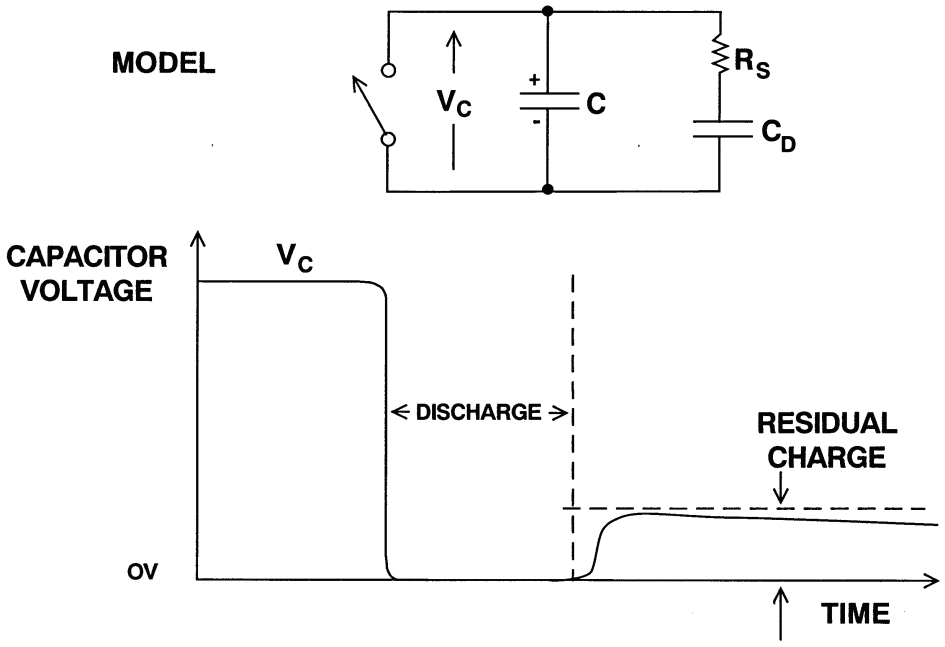


Figure 7.70: *Dielectric Absorption*

Hold-to-Track Transition Specifications

When the SHA switches from hold to track, it must reacquire the input signal (which may have made a full scale transition during the hold mode). *Acquisition time* is the interval of time required for the SHA to reacquire the signal to the desired accuracy when switching from hold to track. The interval starts at the 50% point of the sampling clock edge, and ends when the SHA output voltage falls within the specified error band (usually 0.1% and 0.01% times are given). Some SHAs also specify acquisition time with respect to the voltage on the hold capacitor, neglecting the delay and settling time of the output buffer. The hold capacitor acquisition time specification is applicable in high speed applications, where the maximum possible time must be allocated for the hold mode. The output buffer settling time must of course be significantly smaller than the hold time.

Acquisition time can be measured directly using modern digital sampling scopes (DSOs) or digital phosphor scopes (DPOs) which are insensitive to large overdrives.

Internal SHA Circuits for IC ADCs

CMOS ADCs are quite popular because of their low power and low cost. The equivalent input circuit of a typical CMOS ADC using a differential sample-and-hold is shown in Figure 7.71. While the switches are shown in the *track* mode, note that they open/close at the sampling frequency. The 16 pF capacitors represent the effective capacitance of switches S1 and S2, plus the stray input capacitance. The C_S capacitors (4 pF) are the sampling capacitors, and the C_H capacitors are the hold capacitors. Although the input circuit is completely differential, this ADC structure can be driven either single-ended or

differentially. Optimum performance, however, is generally obtained using a differential transformer or differential op amp drive.

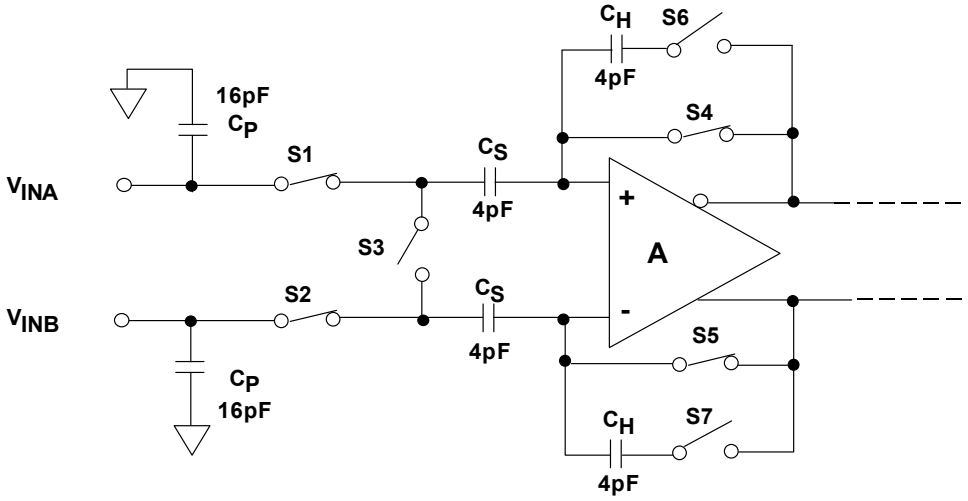


Figure 7.71: *Simplified Input Circuit for a Typical Switched Capacitor CMOS Sample-and-Hold*

In the *track* mode, the differential input voltage is applied to the C_S capacitors. When the circuit enters the *hold* mode, the voltage across the sampling capacitors is transferred to the C_H hold capacitors and buffered by the amplifier A (the switches are controlled by the appropriate sampling clock phases). When the SHA returns to the *track* mode, the input source must charge or discharge the voltage stored on C_S to a new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency f_S, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_S$), the input impedance is dynamic, and certain input drive source precautions should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a resistor equal to $1/(C_S f_S)$ connected between the inputs. Since C_S is only a few picofarads, this resistive component is typically greater than several kΩ for an f_S = 10 MSPS.

Figure 7.72 shows a simplified circuit of the input SHA used in the AD9042 12-bit, 41-MSPS ADC introduced in 1995 (Reference 7). The AD9042 is fabricated on a high speed complementary bipolar process, XFCB. The circuit comprises two independent SHAs in parallel for fully differential operation—only one-half the circuit is shown in the figure. Fully differential operation reduces the error due to droop rate and also reduces second-order distortion. In the track mode, transistors Q1 and Q2 provide unity-gain buffering. When the circuit is placed in the hold mode, the base voltage of Q2 is pulled negative until it is clamped by the diode, D1. The on-chip hold capacitor, C_H, is

nominally 6 pF. Q3 along with C_F provide output current bootstrapping and reduce the V_{BE} variations of Q2. This reduces third-order signal distortion. Track mode THD is typically –93 dB at 20 MHz. In the time domain, full-scale acquisition time to 12-bit accuracy is 8 ns. In the hold mode, signal-dependent pedestal variations are minimized by the voltage bootstrapping action of Q3 and the A = 1 buffer along with the low feedthrough parasitics of Q2. Hold mode settling time is 5 ns to 12-bit accuracy. Hold-mode THD at a clock rate of 50 MSPS and a 20 MHz input signal is –90 dB.

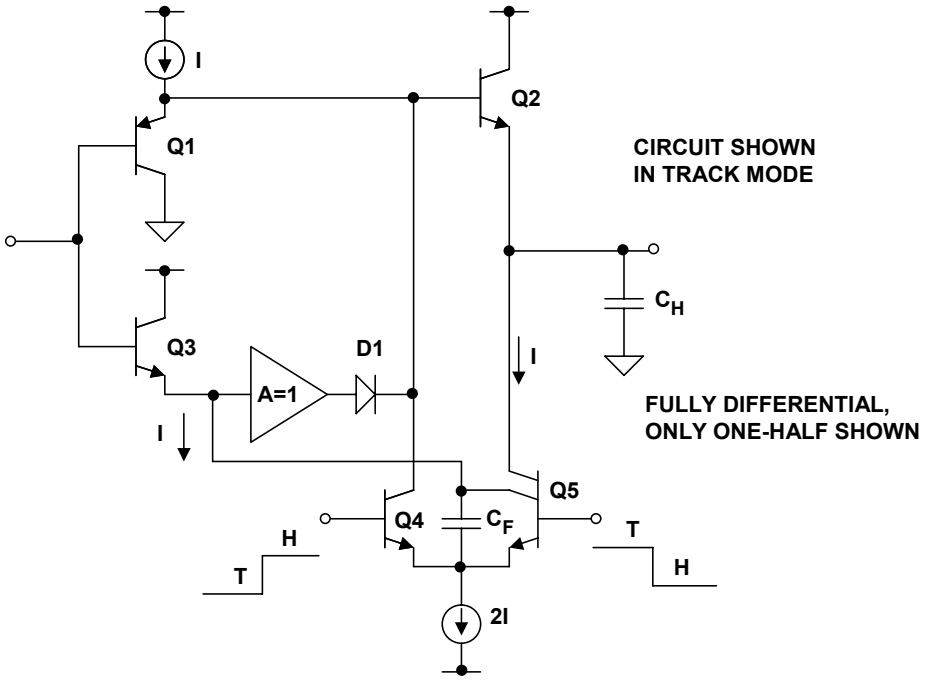


Figure 7.72: *SHA Used in AD9042 12-Bit, 41 MSPS ADC Introduced in 1995*

Figure 7.73 shows a simplified schematic of one-half of the differential SHA used in the AD6645 14-bit, 105-MSPS ADC recently introduced (Reference 9 gives a complete description of the ADC including the SHA). In the track mode, Q1, Q2, Q3, and Q4 form a complementary emitter follower buffer which drives the hold capacitor, C_H. In the hold mode, the polarity of the bases of Q3 and Q4 is reversed and clamped to a low impedance. This turns off Q1, Q2, Q3, and Q4, and results in double isolation between the signal at the input and the hold capacitor. As previously discussed, the clamping voltages are bootstrapped by the held output voltage, thereby minimizing nonlinear effects.

Track mode linearity is largely determined by the V_{BE} modulation of Q3 and Q4 when charging C_H. Hold mode linearity depends on track mode linearity plus nonlinear errors in the track-to-hold transitions caused by imbalances in the switching of the base voltages of Q3 and Q4 and the resulting imbalance in charge injection through their base-emitter junctions as they turn off.

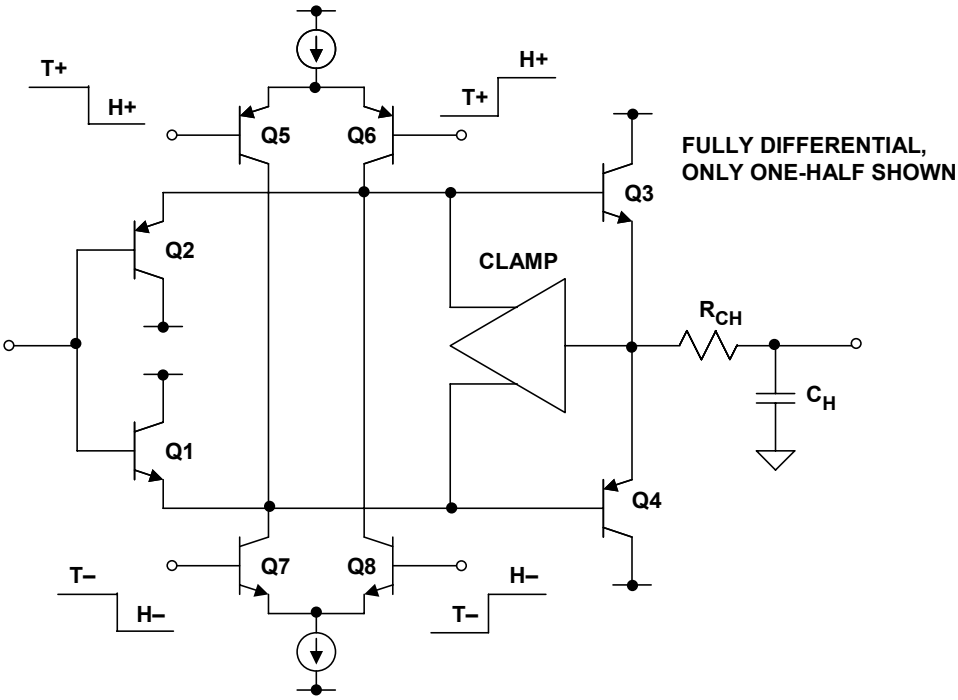


Figure 7.73: *SHA Used in AD6645 14-Bit, 105 MSPS ADC*

REFERENCES: SAMPLE-AND-HOLD CIRCUITS

1. Alec Harley Reeves, "Electric Signaling System," **U.S. Patent 2,272,070**, filed November 22, 1939, issued February 3, 1942. Also **French Patent 852,183** issued 1938, and **British Patent 538,860** issued 1939. *(The classic patents on PCM including descriptions of a 5-bit, 6-kSPS vacuum tube ADC and DAC).*

2. L. A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," **Bell System Technical Journal**, Vol 27, No. 1, January 1948, pp. 1-43. *(Describes the culmination of much work leading to this 24-channel experimental PCM system. In addition, the article describes a 50-kSPS vacuum tube sample-and-hold based on a pulse transformer driver).*

3. J. R. Gray and S. C. Kitsopoulos, "A Precision Sample-and-Hold Circuit with Subnanosecond Switching," **IEEE Transactions on Circuit Theory**, CT11, September 1964, pp. 389-396. *(an excellent description of a solid-state transformer-driven diode bridge SHA, along with a detailed mathematical analysis of the circuit and associated errors).*

4. J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," **Bell System Technical Journal**, Vol. 44, pp. 1887-1940, Nov. 1965. *(summarizes experiments on ADCs based on the electron tube coder as well as a bit-per-stage Gray code 9-bit solid state ADC. The electron beam coder was 9-bits at 12MSPS, and represented the fastest of its type).*

5. D. J. Kinniment, D. Aspinall, and D.B.G. Edwards, "High-Speed Analogue-Digital Converter," **IEE Proceedings**, Vol. 113, pp. 2061-2069, Dec. 1966. *(a 7-bit 9MSPS three-stage pipelined error corrected converter is described based on recircuilating through a 3-bit stage three times. Tunnel (Esaki) diodes are used for the individual comparators. The article also shows a proposed faster pipelined 7-bit architecture using three individual 3-bit stages with error correction. The article also describes a fast bootstrapped transformer-driven diode-bridge sample-and-hold circuit).*

6. O. A. Horna, "A 150 Mbps A/D and D/A Conversion System," **Comsat Technical Review**, Vol. 2, No. 1, pp. 39-72, 1972. *(a description of a subranging ADC including a detailed analysis of the sample-and-hold circuit).*

7. Roy Gosser and Frank Murden, "A 12-bit 50 MSPS Two-Stage A/D Converter," **1995 ISSCC Digest of Technical Papers**, p. 278. *(a description of the AD9042 error corrected subranging ADC using MagAMP stages for the internal ADCs).*

8. Carl Moreland, "An 8-bit 150 MSPS Serial ADC," **1995 ISSCC Digest of Technical Papers**, Vol. 38, p. 272. *(a description of an 8-bit ADC with 5 folding stages followed by a 3-bit flash converter, including a discussion of the sample-and-hold circuit).*

9. Carl Moreland, Frank Murden, Michael Elliott, Joe Young, Mike Hensley, and Russell Stop, "A 14-bit 100-Msample/s Subranging ADC," **IEEE Journal of Solid State Circuits**, Vol. 35, No. 12, December 2000, pp. 1791-1798. *(describes the architecture used in the 14-bit, 105MSPS AD6645 ADC and also the sample-and-hold circuit).*

Notes:

SECTION 7.4: CLOCK GENERATION AND DISTRIBUTION CIRCUITS

Developing a high frequency, high resolution system is a nontrivial task. Any high speed analog-to-digital converter (ADC) is extremely sensitive to the quality of the sampling clock provided by the user. Since an ADC can be thought of as a sampling mixer; any noise, distortion, or timing jitter on the clock is combined with the desired signal at the ADC output. Clock integrity requirements scale with the analog input frequency and resolution. The higher analog input frequency applications at 14-bit (or higher) resolution are the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution where the step size and quantization error can be ignored, the available SNR can be expressed approximately by:

$$SNR = 20 \times \log_{10}\left(\frac{1}{2\pi f t_j}\right) \qquad \text{Eq. 7-9}$$

where f is the highest analog frequency being digitized, and t_j is the rms jitter on the sampling clock. Fig. XX shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB)

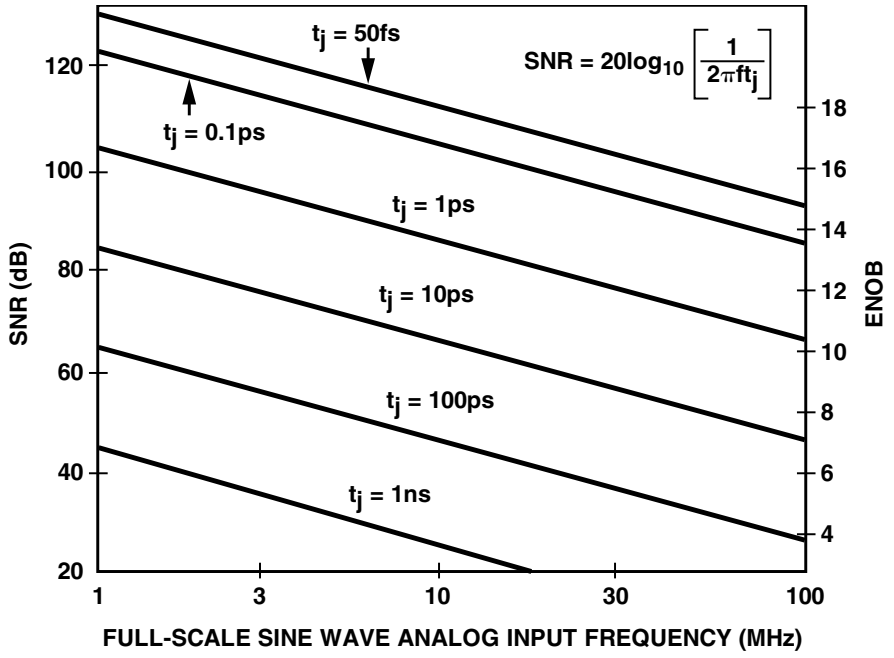


Figure 7.74: *ENOB and SNR vs. Analog Input Frequency*

Contribution to Overall System Performance

In IF sampling converters, clock purity is of extreme importance. As with the mixing process, the input signal is multiplied by a local oscillator, or in this case, a sampling clock. Since multiplication in the time domain is convolution in the frequency domain, the spectrum of the sample clock is convolved with the spectrum of the input signal. Since aperture uncertainty is equivalent to wideband noise on the clock, it shows up as wideband noise in the sampled spectrum as well. And since an ADC is a sampling system, the spectrum is periodic and repeated around the sample rate.

This wideband noise therefore raises the noise floor of the ADC. The theoretical SNR for an ADC, as limited by aperture uncertainty, is determined by the following equation.

$$\text{SNR} = -20 \times \log_{10}\left[(2\pi f_{\text{ANALOG}} t_{\text{JITTER}} \text{ rms})\right] \qquad \text{Eq. 7-10}$$

If Equation 7-10 is evaluated for an analog input of 201 MHz and 0.7 ps rms jitter, the theoretical SNR is limited to 61 dB. Therefore, systems that require very high dynamic range and very high analog input frequencies also require a very low jitter encode source. With care PLLs using VCXOs can achieve less than 1 ps rms jitter, but jitter less than 0.1 ps rms requires a dedicated low noise crystal oscillator, as discussed in the previous chapter. It should be noted that the jitter of a typical TTL/CMOS gate to about 1 ps to 4 ps. Low voltage SiGe reduced swing ECL gate can have about 0.2 ps rms.

When considering overall system performance, a more generalized equation may be used. This equation builds on the previous equation but includes the effects of thermal noise and differential nonlinearity.

$$\text{SNR} = -20\log_{10}\left[\overbrace{(2\pi \times f_a \times t_{j\,\text{rms}})^2}^{\text{SAMPLING CLOCK JITTER}} + \overbrace{\frac{2}{3}\left(\frac{1+\varepsilon}{2^N}\right)^2}^{\text{QUANTIZATION NOISE, DNL}} + \overbrace{\left(\frac{2 \times \sqrt{2} \times V_{\text{NOISErms}}}{2^N}\right)^2}^{\text{EFFECTIVE INPUT NOISE}}\right]^{\frac{1}{2}} \qquad \text{Eq. 7-11}$$

where:

F_a = analog input frequency
$T_{j\,rms}$ = aperture jitter of ADC and external clock
ε = average DNL of converter (~ 0.4 LSB)
$V_{NOISE\,rms}$ = effective ADC input noise in LSBs
N = number of bits

Although this is a simple equation, it provides much insight into the noise performance that can be expected from a data converter.

CLOCK GENERATION CIRCUITS

Analog Devices has designed dedicated clocking product specifically designed to support the extremely stringent clocking requirements of the highest performance data converters. The first of these is the AD9540. This device features high performance PLL circuitry, including a flexible 200 MHz phase frequency detector and a digitally controlled charge pump. The device also provides a low jitter, 655 MHz CML-mode, PECL-compliant output driver with programmable slew rates. External VCO rates up to 2.7 GHz are supported. Extremely fine tuning resolution (steps less than 2.33 μHz) is another feature supported by this device. Information is loaded into the AD9540 via a serial I/O port that has a device write-speed of 25 Mb/s. The AD9540 frequency divider can also be programmed to support a spread spectrum mode of operation.

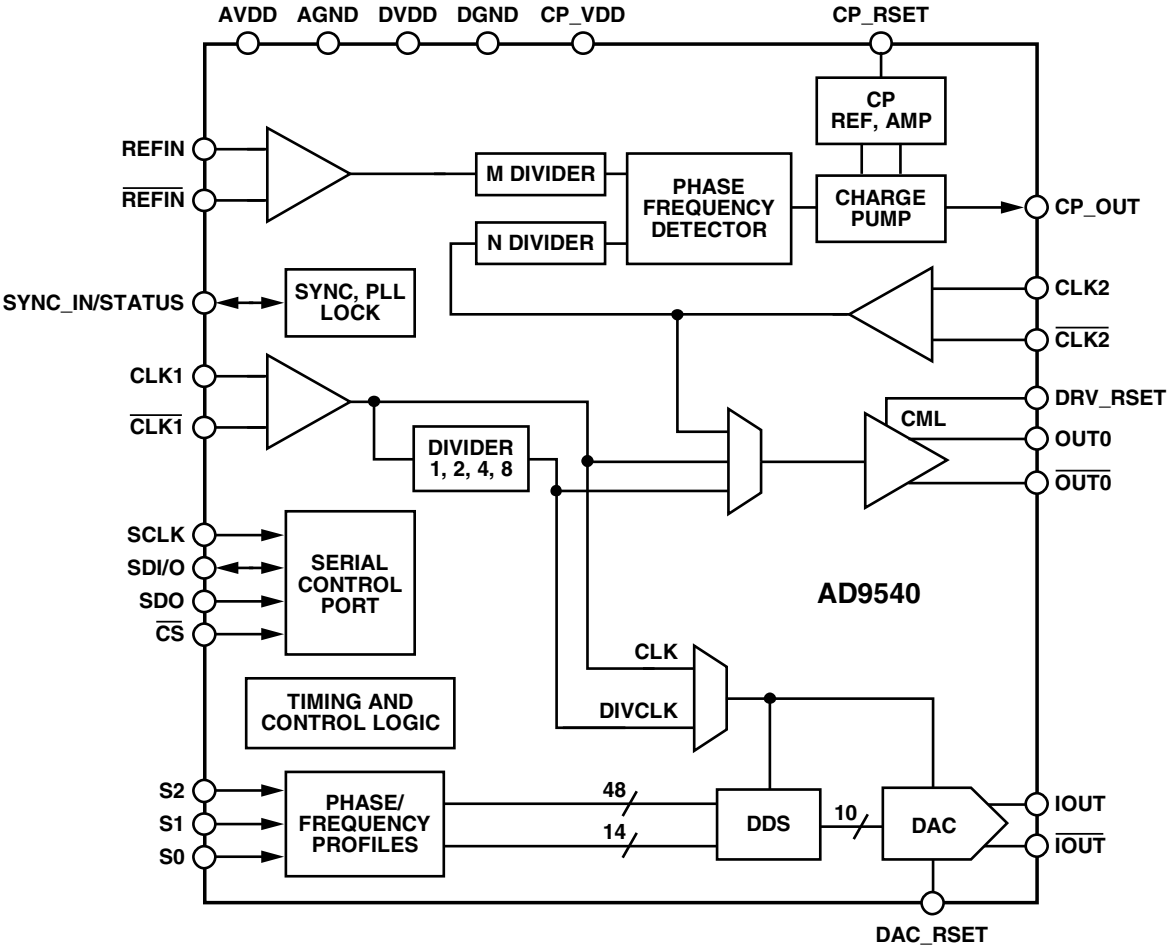


Figure 7.75: *AD9540 Block Diagram*

The block diagram of the AD9540 is shown in Figure 7.75. An overview shows that all the necessary component blocks are present for generating both of the needed clocks. In generating low jitter clocks, it is almost always preferable to employ a phase-locked loop (PLL) circuit of some sort. In addition to providing frequency stability, PLL circuits offer great noise reduction capability because the loop filter will act as a tracking band-pass filter. Because in most clocking applications a single frequency is required, parameters

such as acquisition time and tuning range are not of importance. Therefore performance in these areas can be sacrificed to improve the noise performance of the loop. Specifically, a very narrow range VCO can be selected with a center frequency close to the desired clock rate. As the tuning range is reduced, the gain coefficient for the VCO (Kv) is reduced, and the phase noise of the VCO itself is thereby reduced. Also, the loop filter bandwidth is a concern for designers because there is a trade-off between loop bandwidth and acquisition time. Generally speaking, the wider the loop bandwidth, the faster the acquisition and lock time of a loop, but more noise from the reference and phase frequency detector itself is passed through the loop. In the case of a clocking application, this trade-off can be used to achieve narrow loop bandwidths, sacrificing settling time in favor of noise suppression through the loop.

The digital clock requires precise frequency and adjustable phase that can be generated from the direct digital synthesizer (DDS) portion of the device. The DDS on the AD9540 offers 48-bit frequency tuning resolution (1.42 Hz, for the maximum clock rate of 400 MHz) and 14-bit phase adjustment (0.022 degrees). The output of a DDS is a reconstructed sine wave, so two additional external circuits are required. First, a band-pass filter at the desired clock rate must filter the reconstructed sine wave. This will remove most sampling artifacts from the output spectrum as well as remove most broadband noise in the DAC output signal. Second, in order to achieve the required slew rates for most clock circuits, an external comparator needs to be inserted into the clock signal path. An excellent choice, used for this example, is the ADCMP563. A simplified block diagram for the resultant circuit is shown in Figure 7.76. Inputs CLK1/CLK1 are shorted to CLK2/CLK2. The device is programmed such that the CML driver gets its input from the undivided input from CLK1, but the DDS is clocked by the divided output (622 MHz divided by 2 = 311 MHz). The drawing shows the crystal oscillator capability of the REF input of the PLL, demonstrating its use with a 38 MHz crystal. The two output clocks are shown at OUT0 (the low jitter 622 MHz clock) and OUT1 (the phase-programmable auxiliary clock). Edge skew (or time delay) in the auxiliary clock is accomplished by programming a phase offset into the DDS, which will change the relative point in time for the complementary input crossing at the comparator.

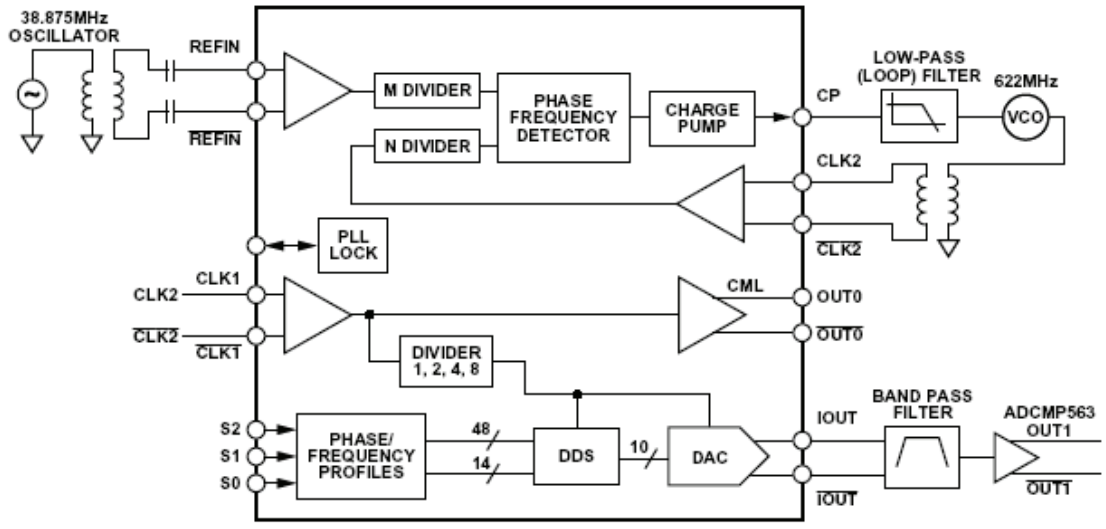


Figure 7.76: *AD9540 Configured for Dual Clock Generation*

PLL CIRCUITRY

The AD9540 includes an RF divider (divide-by-R), a 48-bit DDS core, a 14-bit programmable delay adjustment, a 10-bit DAC, a phase frequency detector, and a programmable current output charge pump. Incorporating these blocks together, users can generate many useful circuits for clock synthesis.

The RF divider accepts differential or single-ended signals up to 2.7 GHz on the CLK1 input pin. The RF divider also supplies the SYSCLK input to the DDS. Because the DDS operates only up to 400 MSPS, the RF divider must be engaged for any CLK1 signal greater than 400 MHz. The RF divider can be programmed to take values of 1, 2, 4, or 8. The ratio for the divider is programmed in the control register. The out-put of the divider can be routed to the input of the on-chip CML driver. For lower frequency input signals, it is possible to use the divider to divide the input signal to the CML driver and to use the undivided input of the divider as the SYSCLK input to the DDS, or vice versa. In all cases, the clock to the DDS should not exceed 400 MSPS.

The on-chip phase frequency detector (PFD) has two differential inputs, REFIN (the reference input) and CLK2 (the feedback or oscillator input). These differential inputs can be driven by single-ended signals. When doing so, tie the unused input through a 100 pF capacitor to the analog supply (AVDD). The maximum speed of the phase frequency detector inputs is 200 MHz. Each of the inputs has a buffer and a divider (÷M on REFIN and ÷N on CLK2) that operates up to 655 MHz. If the signal exceeds 200 MHz, the divider must be used. The dividers are programmed through the control registers and take any integer value between 1 and 16.

The REFIN input also has the option of engaging an in-line oscillator circuit. Engaging this circuit means that the REFIN input can be driven with a crystal in the frequency range of 20 MHz ≤ REFIN ≤ 30 MHz.

The charge pump outputs a current in response to an error signal generated in the phase frequency detector. The output current is programmed through by placing a resistor (CP_RSET) from the CP_RSET pin to ground.

This sets the charge pump's reference output current. Also, a programmable scaler multiplies this base value by any integer from 1 to 8, programmable through the CP current scale bits in the Control Function Register 2.

CML DRIVER

An on-chip current mode logic (CML) driver is also included. This CML driver generates very low jitter clock edges. The outputs of the CML driver are current outputs that drive PECL levels when terminated into a 100 Ω load. The continuous output current of the driver is programmed by attaching a resistor from the DRV_RSET pin to ground (nominally 4.02 kΩ for a continuous current of 7.2 mA). An optional on-chip current programming resistor is enabled by setting a bit in the control register. The rising edge and falling edge slew rates are independently programmable to help control overshoot and ringing by the application of surge current during rising edge and falling edge transitions (see Figure 34). There is a default surge current of 7.6 mA on the rising edge

and of 4.05 mA on the falling edge. Bits in the control register enable additional rising edge and falling edge surge current, and can disable the default surge current. CML driver can be driven by:

- RF divider input (CLK1 directly to the CML driver)
- RF divider output
- CLK2 input

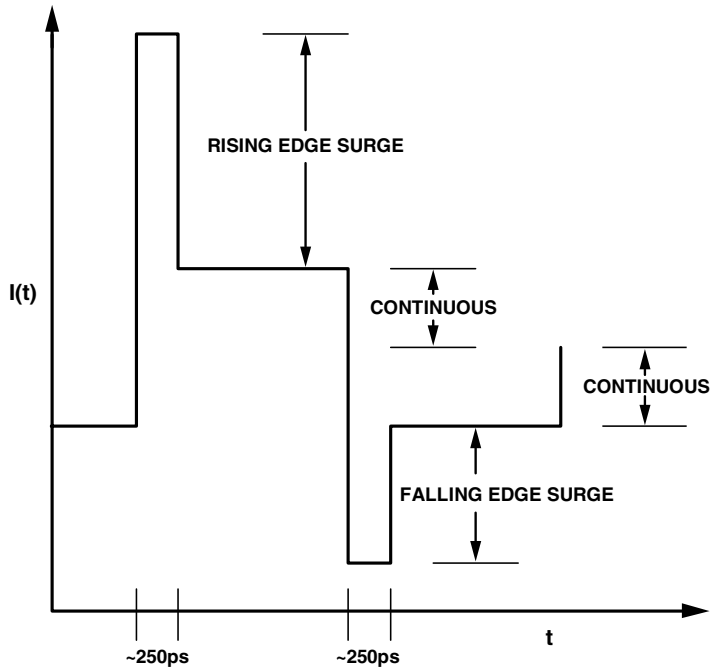


Figure 7.77: *Rising Edge and Falling Edge Surge Current Out of the CML Clock Driver, as Opposed to the Steady State Continuous Current*

DDS AND DAC

The precision frequency division within the device is accomplished using DDS technology. The DDS can control the digital phase relationships by clocking a 48-bit accumulator. The incremental value loaded into the accumulator, known as the frequency tuning word, controls the overflow rate of the accumulator. Similar to a sine wave completing a 2π radian revolution, the overflow of the accumulator is cyclical in nature and generates a fundamental frequency according to:

$$f_0 = \frac{FTW \times (f_s)}{2^{48}} \qquad 0 \le FTW \le 2^{47} \qquad \text{Eq. 7-12}$$

The instantaneous phase of the sine wave is therefore the output of the phase accumulator block. This signal may be phase-offset by programming an additive digital phase that is added to each phase sample coming out of the accumulator. These instantaneous phase values are then passed through a phase-to-amplitude conversion (sometimes called an angle-to-amplitude conversion or AAC) block.

This algorithm follows a cos(x) relationship, where x is the phase coming out of the phase offset block, normalized to 2π. Finally, the amplitude words drive a 10-bit DAC. Because the DAC is a sampled data system, the output is a reconstructed sine wave that needs to be filtered to take high frequency images out of the spectrum. The DAC is a current steering DAC that is AVDD referenced. To get a voltage output, the DAC outputs must be terminated through a load resistor to AVDD, typically 50 Ω. At positive full scale, IOUT sinks no current and the voltage drop across the load resistor is 0.

However, the IOUT output sinks the DAC's programmed full-scale output current, causing the maximum output voltage drop across the load resistor. At negative full-scale, the situation is reversed, and IOUT sinks the full-scale current (and generates the maximum drop across the load resistor), while IOUT sinks no current (and generates no voltage drop). At midscale, the outputs sink equal amounts of current, generating equal voltage drops.

SELECTABLE CLOCK FREQUENCIES AND SELECTABLE EDGE DELAY

Because the precision driver is implemented using a DDS, it is possible to store multiple clock frequency words to enable externally switchable clock frequencies. The phase accumulator runs at a fixed frequency, according to the active profile clock frequency word. Likewise, any delay applied to the rising and falling edges is a static value that comes from the delay shift word of the active profile. The device has eight different phase/frequency profiles, each with its own 48-bit clock frequency word and 14-bit delay shift word. Profiles are selected by applying their digital value on the clock select (S0, S1, and S2) pins. It is not possible to use the phase offset of one profile and the frequency tuning word of another.

SYNCHRONIZATION MODES FOR MULTIPLE DEVICES

In a DDS system, the SYNC_CLK is derived internally from the master system clock, SYSCLK, with a ÷4 divider. Because the divider does not power up to a known state, multiple devices in a system might have staggered clock phase relationships, because each device can potentially generate the SYNC_CLK rising edge from any one of four rising edges of SYSCLK. This ambiguity can be resolved by employing digital synchronization logic to control the phase relationships of the derived clocks among different devices in the system. Note that the synchronization functions included on the AD9540 control only the timing relationships among different digital clocks. They do not compensate for the analog timing delay on the system clock due to mismatched phase relationships on the input clock, CLK1 (see Figure 7.78).

Automatic Synchronization

In automatic synchronization mode, the device is placed in slave mode and automatically aligns the internal SYNC_CLK to a master SYNC_CLK signal, supplied on the SYNC_IN input. When this bit is enabled, the STATUS is not available as an output; however, an out-of-lock condition can be detected by reading Control Function

Register 1 and checking the status of the STATUS_Error bit. The automatic synchronization function is enabled by setting the Control Function Register 1 automatic synchronization bit. To employ this function at higher clock rates (SYNC_CLK > 62.5 MHz, SYSCLK > 250 MHz), the high speed sync enable bit should be set as well.

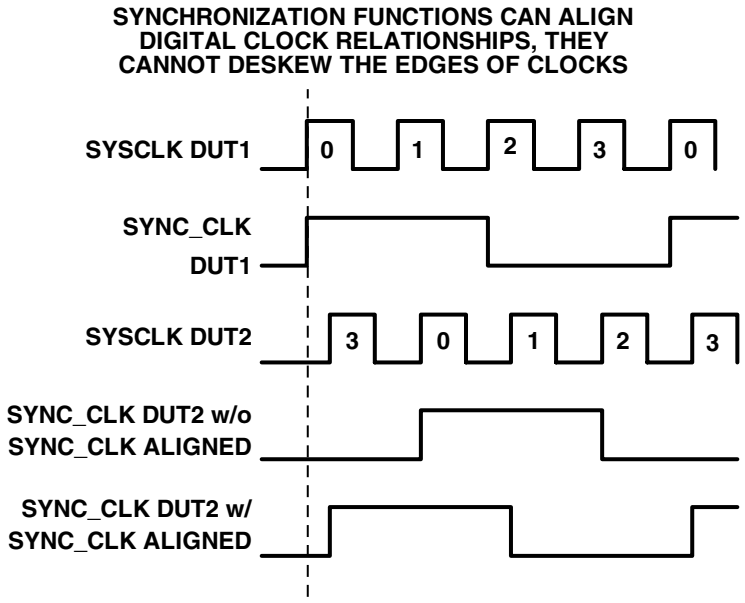


Figure 7.78: *Synchronization Functions: Capabilities and Limitations*

Manual Synchronization, Hardware Controlled

In this mode, the user controls the timing relationship of the SYNC_CLK with respect to SYSCLK. When hardware manual synchronization is enabled, the SYNC_IN/ STATUS pin becomes a digital input. For each rising edge detected on the SYNC_IN input, the device advances the SYNC_IN rising edge by one SYSCLK period. When this bit is enabled, the STATUS is not available as an output; however, an out-of-lock condition can be detected by reading Control Function Register 1 and checking the status of the STATUS_Error bit. This synchronization function is enabled by setting the hardware manual synchronization enable bit.

Manual Synchronization, Software Controlled

In this mode, the user controls the timing relationship between SYNC_CLK and SYSCLK through software programming. When the software manual synchronization bit is set high, the SYNC_CLK is advanced by one SYSCLK cycle. Once this operation is complete, the bit is cleared. The user can set this bit repeatedly to advance the SYNC_CLK rising edge multiple times. Because the operation does not use the SYNC_IN/ STATUS pin as a SYNC_IN input, the STATUS signal can be monitored on the STATUS pin during this operation.

CLOCK DISTRIBUTION CIRCUITS

In addition to the clock generation circuits Analog Devices make clock distribution circuits such as the A9514 and combination circuits such as the AD9510.

The AD9510 provides a multi-output clock distribution function along with an on-chip PLL core. The design emphasizes low jitter and phase noise to maximize data converter performance. Other applications with demanding phase noise and jitter requirements also benefit from this part.

The PLL section consists of a programmable reference divider (R); a low noise phase frequency detector (PFD); a precision charge pump (CP); and a programmable feedback divider (N).

By connecting an external VCXO or VCO to the CLK2/CLK2B pins, frequencies up to 1.6 GHz may be synchronized to the input reference.

There are eight independent clock outputs. Four outputs are LVPECL (1.2 GHz max), and four are selectable as either LVDS (800 MHz max) or CMOS (250 MHz max) levels.

Each output has a programmable divider that may be bypassed or set to divide by any integer up to 32. The phase of one clock output relative to another clock output may be varied by means of a divider phase select function that serves as a coarse timing adjustment. Two of the LVDS/CMOS outputs feature programmable delay elements with full-scale ranges up to 10 ns of delay. This fine tuning delay block has 5-bit resolution, giving 32 possible delays from which to choose for each full-scale setting.

FUNCTIONAL DESCRIPTION

Figure 33 shows a block diagram of the AD9510. The chip combines a programmable PLL core with a configurable clock distribution system. A complete PLL requires the addition of a suitable external VCO (or VCXO) and loop filter. This PLL can lock to a reference input signal and produce an output that is related to the input frequency by the ratio defined by the programmable R and N dividers. The PLL reduces the jitter from the external reference signal, depending on the loop bandwidth and the phase noise performance of the VCO (VCXO).

The output from the VCO (VCXO) can be applied to the clock distribution section of the chip, where it can be divided by any integer value from 1 to 32. The duty cycle and relative phase of the outputs can be selected. There are four LVPECL outputs, (OUT0, OUT1, OUT2, and OUT3) and four outputs that can be either LVDS or CMOS level outputs (OUT4, OUT5, OUT6, and OUT7). Two of these outputs (OUT5 and OUT6) can also make use of a variable delay block.

Alternatively, the clock distribution section can be driven directly by an external clock signal, and the PLL can be powered off. Whenever the clock distribution section is used alone, there is no clock clean-up. The jitter of the input clock signal is passed along directly to the distribution section and may dominate at the clock outputs.

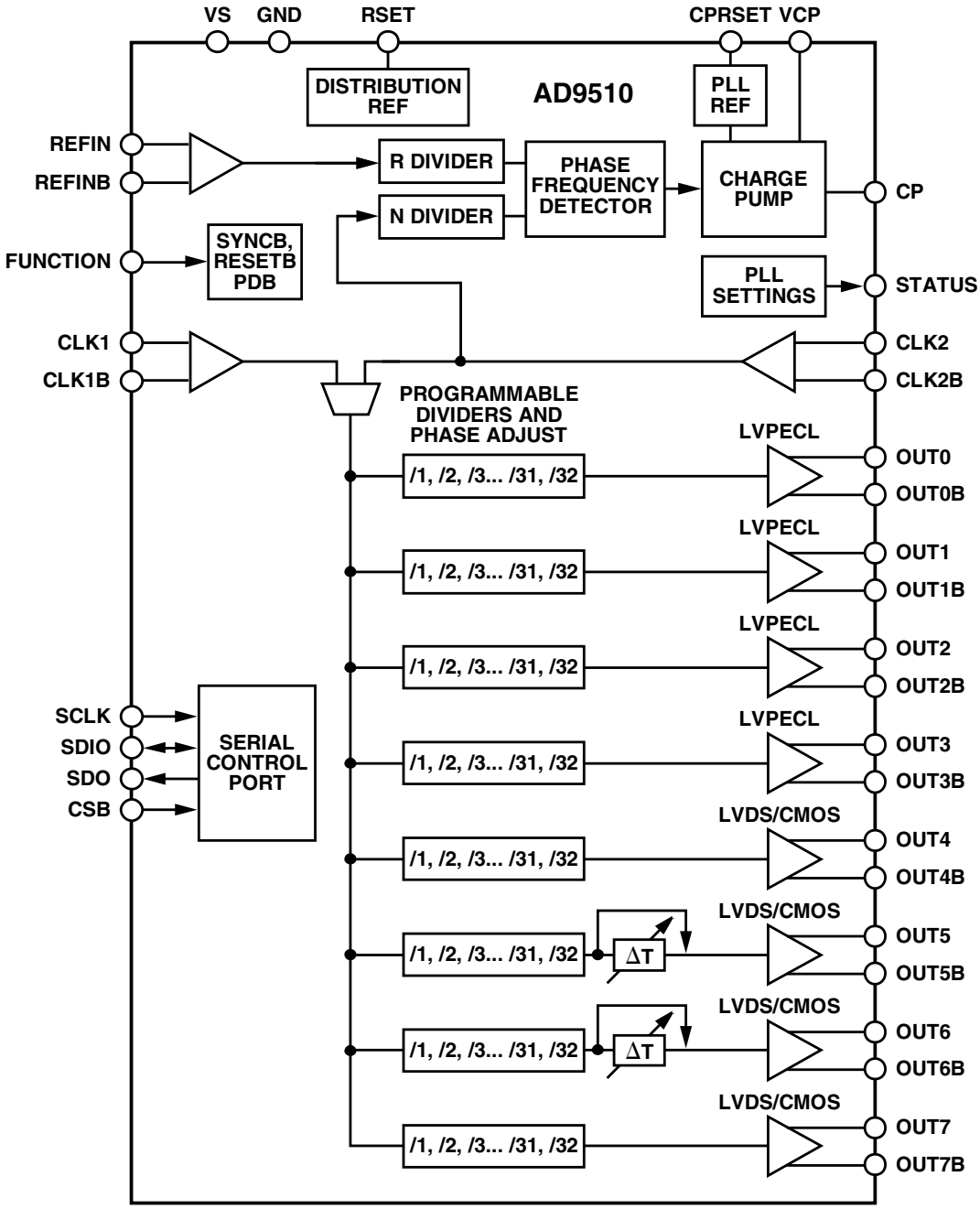


Figure 7.79: *AD9510 Functional Block Diagram*

PLL SECTION

The AD9510 consists of a PLL section and a distribution section. If desired, the PLL section can be used separately from the distribution section.

The AD9510 has a complete PLL core on-chip, requiring only an external loop filter and VCO/VCXO. This PLL is based on the ADF4106, a PLL noted for its superb low phase

noise performance. The operation of the AD9510 PLL is nearly identical to that of the ADF4106, offering an advantage to those with experience with the ADF series of PLLs. Differences include the addition of differential inputs at REFIN and CLK2 and a different control register architecture. Also, the prescaler has been changed to allow N as low as 1. The AD9510 PLL implements the digital lock detect feature somewhat differently than the ADF4106 does, offering improved functionality at higher PFD rates.

PLL Reference Input—REFIN

The REFIN/REFINB pins can be driven by either a differential or a single-ended signal. These pins are internally self-biased so that they can be ac-coupled via capacitors. It is possible to dc-couple to these inputs. If REFIN is driven single-ended, the unused side (REFINB) should be decoupled via a suitable capacitor to a quiet ground. Figure 34 shows the equivalent circuit of REFIN.

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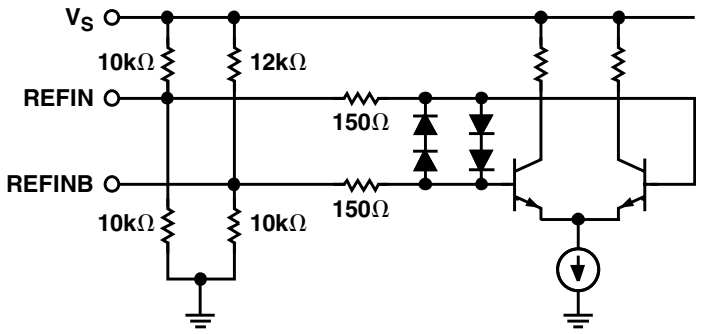

Figure 7.80: *REFIN Equivalent Circuit*

VCO/VCXO Clock Input—CLK2

The CLK2 differential input is used to connect an external VCO or VCXO to the PLL. Only the CLK2 input port has a connection to the PLL N divider. This input can receive up to 1.6 GHz. These inputs are internally self-biased and must be ac-coupled via capacitors.

Alternatively, CLK2 may be used as an input to the distribution section.

The default condition is for CLK1 to feed the distribution section.

PLL Reference Divider—R

The REFIN/REFINB inputs are routed to reference divider, R, which is a 14-bit counter. R may be programmed to any value from 1 to 16383 (a value of 0 results in a divide by 1) via its control register. The output of the R divider goes to one of the phase/frequency detector inputs. The maximum allowable frequency into the phase/frequency detector (PFD) must not be exceeded. This means that the REFIN frequency divided by R must be less than the maximum allowable PFD frequency. See Figure 7.80.

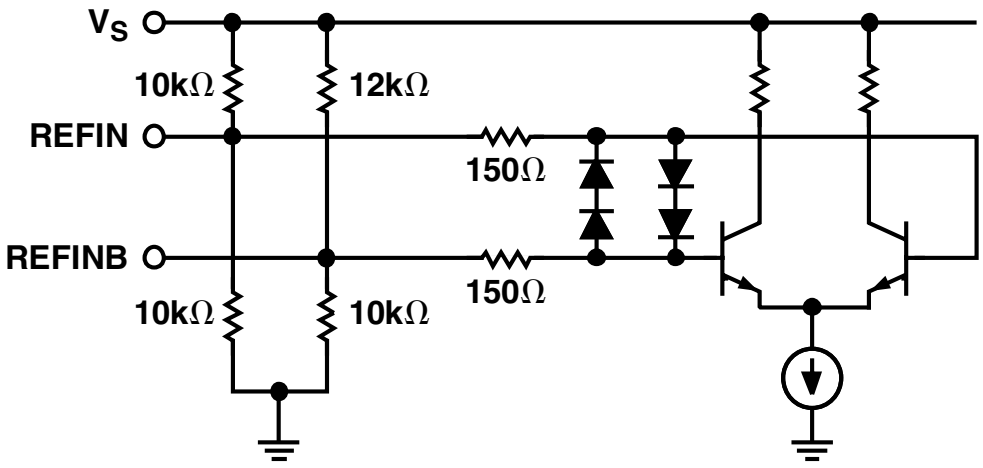

Figure 7.81: *CLK1, CLK2 Equivalent Input Circuit*

VCO/VCXO Feedback Divider—N (P, A, B)

The N divider is a combination of a prescaler, P, (3 bits) and two counters, A (6 bits) and B (13 bits). Although the AD9510's PLL is similar to the ADF4106, the AD9510 has a redesigned prescaler that allows lower values of N. The prescaler has both a dual modulus (DM) and a fixed divide (FD) mode.

When using the prescaler in FD mode, the A counter is not used, and the B counter may need to be bypassed. The DM prescaler modes set some upper limits on the frequency, which can be applied to CLK2.

A and B Counters

The AD9510 B counter has a bypass mode (B = 1), which is not available on the ADF4106. The B counter bypass mode is valid only when using the prescaler in FD mode. The B counter is bypassed by writing 1 to the B counter bypass bit. The valid range of the B counter is 3 to 8191. The default after a reset is 0, which is invalid.

Note that the A counter is not used when the prescaler is in FD mode.

Note also that the A/B counters have their own reset bit, which is primarily intended for testing. The A and B counters can also be reset using the R, A, and B counters' shared reset bit.

Determining Values for P, A, B, and R

When operating the AD9510 in a dual-modulus mode, the input reference frequency, FREF, is related to the VCO output frequency, FVCO:

$$FVCO = (FPRF/R) \times (PB + A) = FREF \times N/R \qquad \text{Eq. 7.13}$$

When operating the prescaler in fixed divide mode, the A counter is not used and the equation simplifies to:

$$FVCO = (FPRF/R) \times (PB) = FREF \times N/R \qquad \text{Eq. 7-14}$$

By using combinations of dual modulus and fixed divide modes, the AD9510 can achieve values of N all the way down to N = 1.

Phase Frequency Detector (PFD) and Charge Pump

The PFD takes inputs from the R counter and the N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 36 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in Register 0Dh control the width of the pulse.

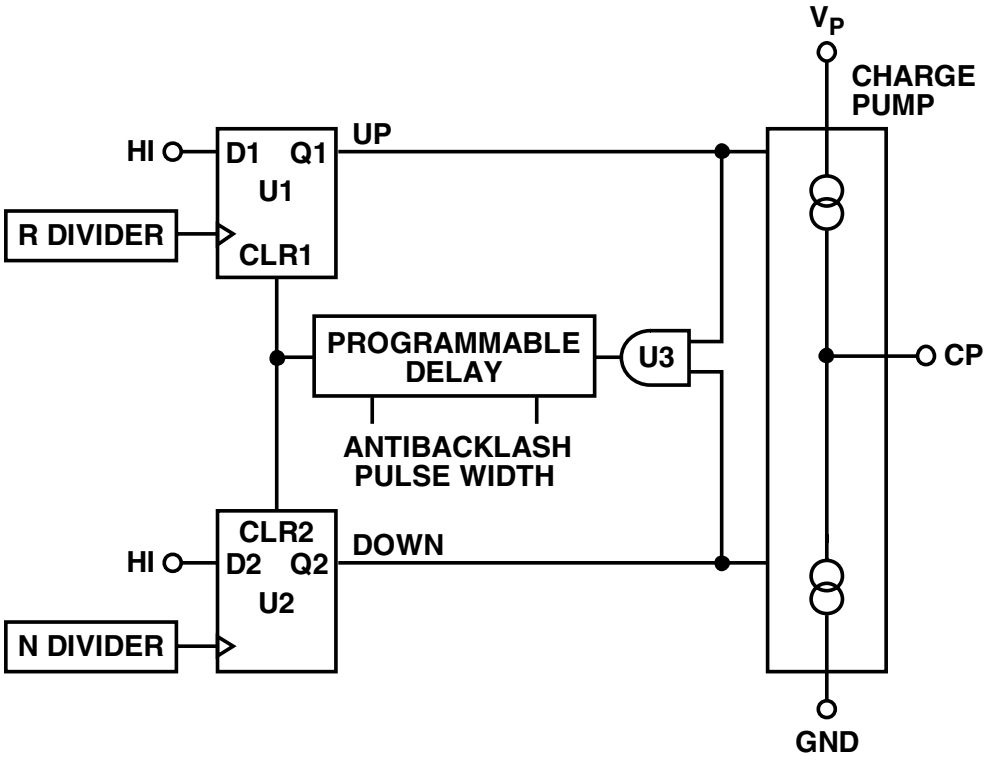

Figure 7.82: *PFD Simplified Schematic and Timing (In Lock)*

Antibacklash Pulse

The PLL features a programmable antibacklash pulse width. The default antibacklash pulse width is 1.3 ns and normally should not need to be changed. The antibacklash pulse eliminates the dead zone around the phase-locked condition and thereby reduces the potential for certain spurs that could be impressed on the VCO signal.

STATUS Pin

The output multiplexer on the AD9510 allows access to various signals and internal points on the chip at the STATUS pin. Figure 37 shows a block diagram of the STATUS pin section. The function of the STATUS pin is controlled by a register.

PLL Digital Lock Detect

The STATUS pin can display two types of PLL lock detect: digital (DLD) and analog (ALD). Whenever digital lock detect is desired, the STATUS pin provides a CMOS level signal, which can be active high or active low.

The digital lock detect has one of two time windows, as selected by a register. The default requires the signal edges on the inputs to the PFD to be coincident within 9.5 ns to set the DLD true, which then must separate by at least 15 ns to give DLD = false.

The other setting makes these coincidence times 3.5 ns for DLD = true and 7 ns for DLD = false. The DLD may be disabled. If the signal at REFIN goes away while DLD is true, the DLD will not necessarily indicate loss-of-lock.

DIVIDERS

Each of the eight clock outputs of the AD9510 has its own divider. The divider can be bypassed to get an output at the same frequency as the input (1×). When a divider is bypassed, it is powered down to save power.

All integer divide ratios from 1 to 32 may be selected. A divide ratio of 1 is selected by bypassing the divider.

Each divider can be configured for divide ratio, phase, and duty cycle. The phase and duty cycle values that can be selected depend on the divide ratio that is chosen.

Divider Phase Offset

The phase of each output may be selected, depending on the divide ratio chosen. This is selected by writing the appropriate values to the registers which set the phase and start high bit/low bit for each output. Each divider has a 4-bit phase offset and a start high bit or low bit.

Following a sync pulse, the phase offset word determines how many fast clock (CLK1 or CLK2) cycles to wait before initiating a clock output edge. The Start H/L bit determines if the divider output starts low or high. By giving each divider a different phase offset, output-to-output delays can be set in increments of the fast clock period, tCLK.

Figure 39 shows four dividers, each set for DIV = 4, 50% duty cycle. By incrementing the phase offset from 0 to 3, each output is offset from the initial edge by a multiple of tCLK.

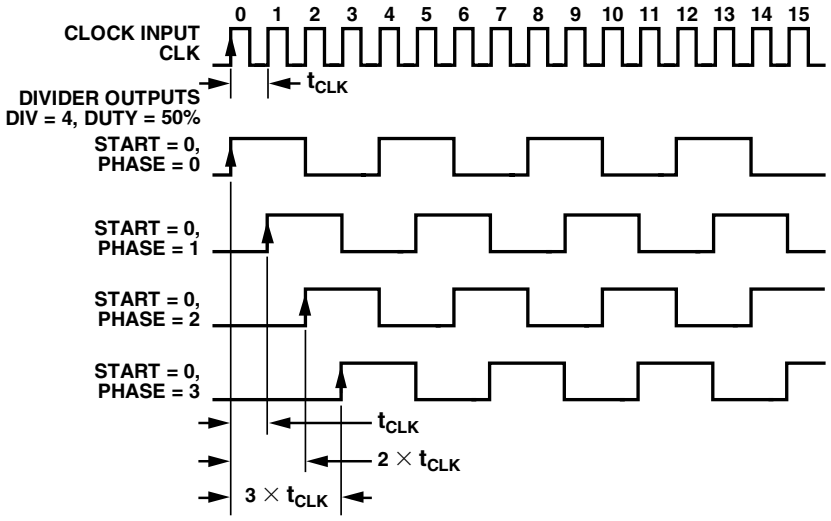

Figure 7.83: *Phase Offset—All Dividers Set for DIV = 4, Phase Set from 0 to 3*

DELAY BLOCK

OUT5 and OUT6 (LVDS/CMOS) include an analog delay element that can be programmed to give variable time delays (Δt) in the clock signal passing through that output.

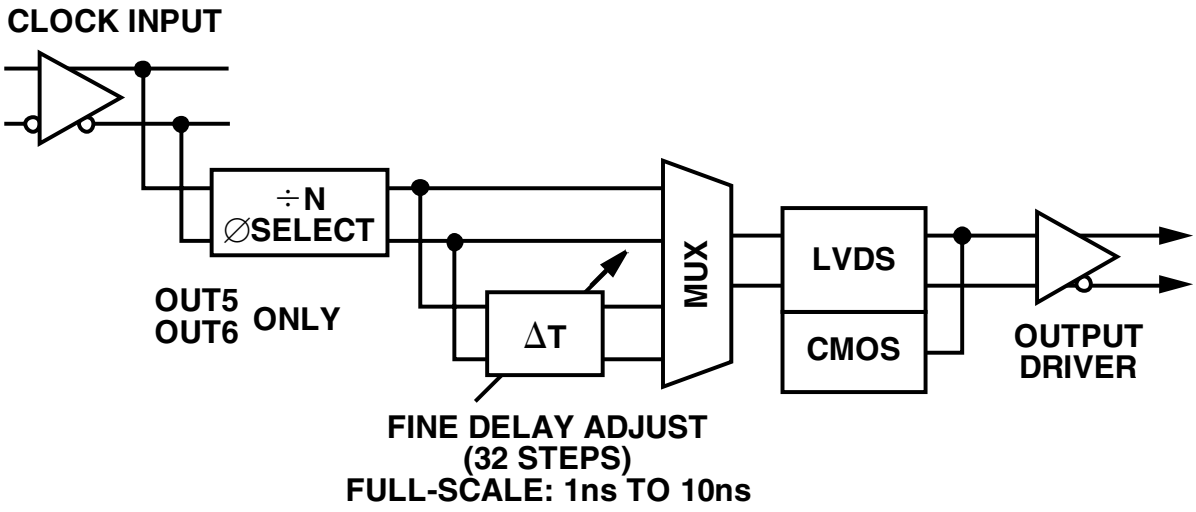

Figure 7.84: *Analog Delay (OUT5 and OUT6)*

The amount of delay that can be used is determined by the frequency of the clock being delayed. The amount of delay can approach one-half cycle of the clock period. For example, for a 10 MHz clock, the delay can extend to the full 10 ns maximum of which the delay element is capable. However, for a 100 MHz clock (with 50% duty cycle), the maximum delay is less than 5 ns (or half of the period).

OUT5 and OUT6 allow a full-scale delay in the range 1 ns to 10 ns. The full-scale delay is selected by choosing a combination of ramp current and the number of capacitor. There are 32 fine delay settings for each full scale.

This path adds some jitter greater than that specified for the nondelay outputs. This means that the delay function should be used primarily for clocking digital chips, such as FPGA, ASIC, DUC, and DDC, rather than for data converters. The jitter is higher for long full scales (~10 ns). This is because the delay block uses a ramp and trip points to create the variable delay. A longer ramp means more noise might be introduced.

The clock distribution circuits feature both LVPECL and LVDS outputs that provide differential clock outputs, which enable clock solutions that maximize converter SNR performance. The input requirements of the ADC (differential or single-ended, logic level, termination) should be considered when selecting the best clocking/converter solution.

Whenever single-ended CMOS clocking is used, some of the following general guidelines should be followed. Point-to-point nets should be designed such that a driver has one receiver only on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

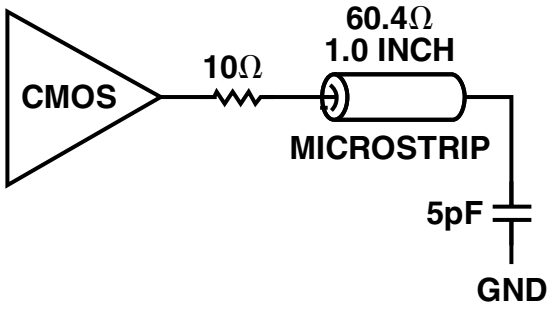

Figure 7.85: *Series Termination of CMOS Outputs*

Termination at the far end of the PCB trace is a second option. The CMOS outputs typically do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 55. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. LVPECL and LVDS outputs are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

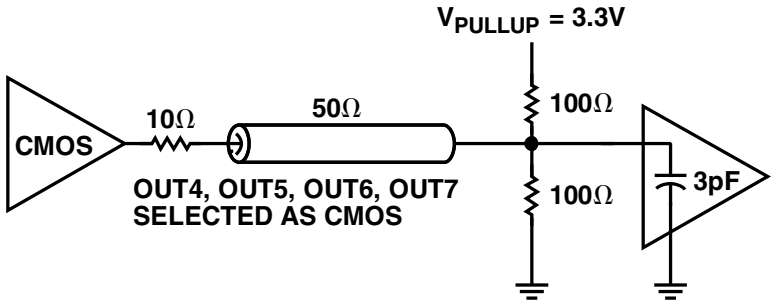

Figure 7.86: *CMOS Output with Far-End Termination*

LVPECL CLOCK DISTRIBUTION

The low voltage, positive emitter-coupled, logic (LVPECL) outputs typically provide the lowest jitter clock signals available from the clock distribution chips. The LVPECL outputs (because they are open emitter) require a dc termination to bias the output transistors. In most applications, a standard LVPECL far-end termination is recommended, as shown in Figure 56. The resistor network is designed to match the transmission line impedance (50 Ω) and the desired switching threshold (1.3 V).

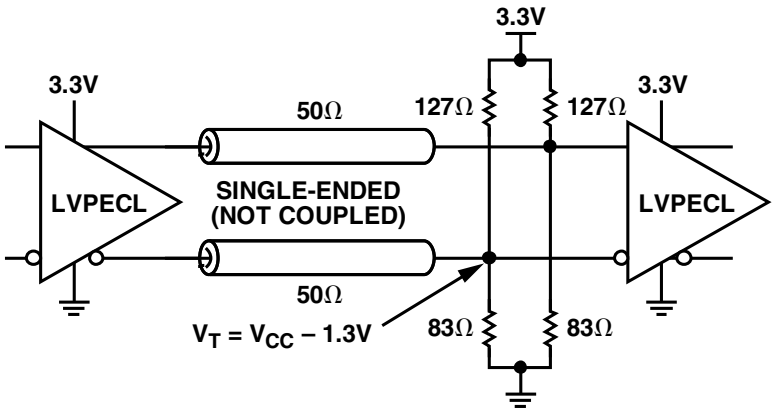

Figure 7.87: *LVPECL Far-End Termination*

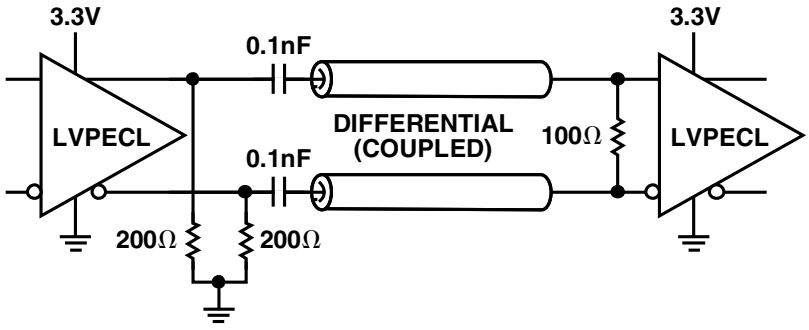

Figure 7.88: *LVPECL with Parallel Transmission Line*

LVDS CLOCK DISTRIBUTION

Low voltage differential signaling *(*LVDS) is a second differential output option. LVDS uses a current mode output stage with several user-selectable current levels. The normal value (default) for this current is 3.5 mA, which yields 350 mV output swing across a 100 Ω resistor. The LVDS outputs of the clock chips meet or exceed all ANSI/TIA/EIA-644 specifications. A recommended termination circuit for the LVDS outputs is shown in Figure 7.89.

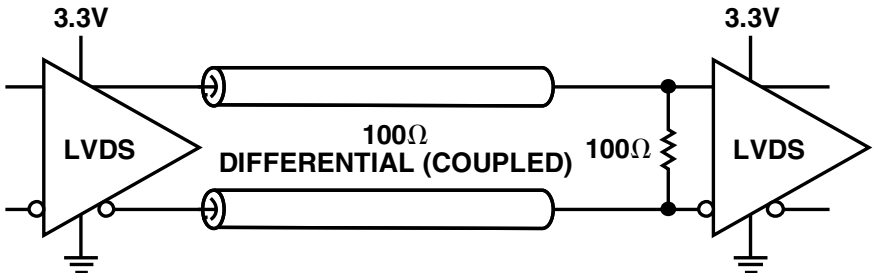

Figure 7.89: *LVDS Output Termination*

POWER MANAGEMENT

The power usage of the AD9510 can be managed to use only the power required for the functions that are being used. Unused features and circuitry can be powered down to save power. The following circuit blocks can be powered down, or are powered down when not selected (see the Register Map and Description section):

- The PLL section can be powered down if not needed.
- Any of the dividers are powered down when bypassed— equivalent to divide-by-one.
- The adjustable delay blocks on OUT5 and OUT6 are powered down when not selected.
- Any output may be powered down. However, LVPECL outputs have both a safe and an off condition. When the LVPECL output is terminated, only the safe shutdown should be used to protect the LVPECL output devices. This still consumes some power.
- The entire distribution section can be powered down when not needed.

Powering down a functional block does not cause the programming information for that block (in the registers) to be lost. This means that blocks can be powered on and off without otherwise having to reprogram the AD9510. However, synchronization is lost. A SYNC must be issued to resynchronize.

APPLICATION TO SYSTEM DEBUGGING

Besides the obvious issues revolving around designing systems to minimize signal degradations, there are several other consequences to these results worth mentioning. These are related to finding the source of mystery spurs and noise.

For instance, if the noise floor rises at the DAC output, it is most likely not caused by clock phase noise. It may be digital coupling into the output circuitry.

If a spur exists in a sampled signal, a good test to see if it comes from the clock is to change the signal amplitude. If it is from the clock it should get proportionally lower.

Analog distortion terms will change at twice (2^{nd}-order distortion) or three times (3rd order distortion) the rate of the signal amplitude change. Spurs due to nonlinearity in the quantizer may not change at all, or if they do change, they will change unpredictably, when the signal amplitude changes. On the other hand, spurs due to the clock will change dB for dB with the signal.

When trying to identify the source of a spur in a sampled data signal, look not only at the explicit spur frequency, which could be caused by a signal directly coupling into the output, but also at the frequency offset from the signal. For example, if a spur is 10 MHz away from the carrier, look to see if there is a 10 MHz oscillator somewhere in the system. If so, this frequency is most likely leaking in through the clock.

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CLOCK GENRERATION AND DISTRIBUTION

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