New Approaches to Data-Acquisition System Design

by T. O. Anderson

Low cost conversion components (such as ADI's μDAC's) make feasible "decentralized" conversion systems—systems wherein each analog input is quantized independently, at the source. These systems exhibit higher overall reliability, higher speeds, and ready ability to compress data and thus increase transmitted intelligence.

With the coming of new components at progressively lower prices, data acquisition system designers should consider new system design approaches. Starting with analog sources, traditional sampled data systems consist of analog transmission lines, a centralized analog time-switching system (viz., multiplexer), a single analog-to-digital converter, and serial computer processing. However, there are many benefits to be obtained by considering a decentralized system design approach wherein each analog input is quantized, preprocessed and buffered *at the source*. The digital data from the source buffers can then be readily transmitted and multiplexed for final central processing. A buffer at each source further suggests self-adaptive multiplexing for efficient bandwidth allocation between sources.

In the paragraphs that follow, we shall first explain the difference between the traditional centralized design approach and the decentralized approach advocated here, then compare the two system-design approaches and finally discuss in some detail the technique of self-adaptive digital output multiplexing.

BASIS FOR COMPARISON

Figure 1 shows a block diagram of a traditional data-acquisition system, and Figure 2 shows such a system of the new design. The sources in both cases are of the same general type (e.g., preamplifier outputs), and the preprocessing, in its simplest form, could be thought of as being some sort of redundancy-reduction data compression.*

*An example of *redundancy-reduction data compression* would be to store in the buffer only those values that change by at least a predetermined amount from the previous value, and to cause the buffer to read out only after it had reached an appropriately full "level-of-content," i.e., number or magnitude of changes stored. Such a process would considerably increase the amount of intelligence transmittable via a data link of given capacity.

In comparing the advantages and disadvantages of the two system configurations, some parameters must be considered fixed and equal for both systems. For the purpose of this discussion, the following parameters are the same for both systems.

1. Cost
2. Number of channels
3. Sampling rate per channel
4. Throughput rate
5. Sample resolution
6. Sample accuracy
7. Channel buffer size

With everything else being equal, the number of channels that can be handled at comparable cost is typically of the order of 20 to 50 at the present time.

OVERALL SYSTEM CONSIDERATIONS

For a given level of cost, the most important advantage of the Figure 2 configuration is the lower probability of catastrophic system failure. In the case of a spacecraft system, this could mean the difference between success and failure; in industrial control, it could be equally important.

Another advantage of the configuration of Figure 2 is that it simplifies system interfaces between the experiments (or sources of data) and the communication system. In a practical system, the interface between the inputs and the communications system can be considered to be the buffer stage. In Figure 2, experiments and preprocessing systems are independent from one another and from the communication system. The signal statistics and processing algorithms of each channel determine the characteristics of the feedback loop between the buffer and the processor for that channel. For example, in a redundancy-reduction data compression scheme, the level-of-content of the buffer may control the significance criteria for the detector. The bandwidth allotment between channels may be

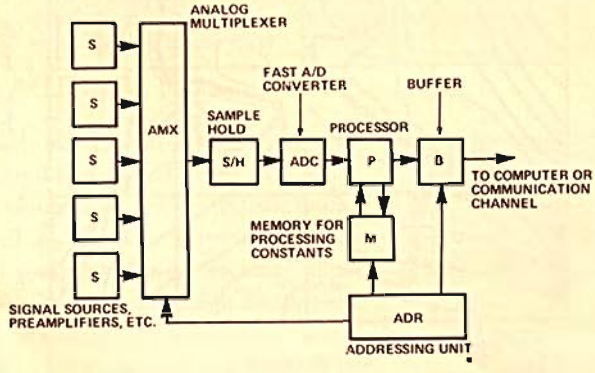

Figure 1. Conventional Centrally-Controlled Data Acquisition System

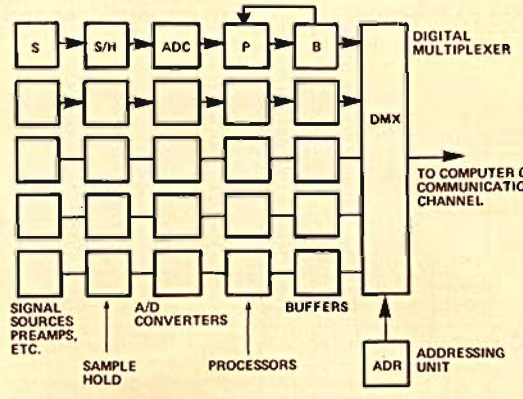

Figure 2. Block Diagram of Decentralized Data Acquisition System

made self-adaptive by making the output multiplexer sample the outputs of those buffers having a higher level of content more often. In an adaptive allotment scheme, prescribed allotments are then also controlled by varying the level-of-content at which a channel buffer is sampled.

On the other hand, the processor in the centralized scheme (Figure 1) could no doubt become quite complex. Not only is a rate buffer required to buffer data for continuous transmission at a fixed rate, but processing constants, which may vary from channel to channel, must also be stored, in a memory. Furthermore, it must be possible conveniently to recall the last accepted sample from a channel.

In the *basic* decentralized system, the implementation of these functions is easily achieved. And when the adaptive output is included, the benefits that are realized occur at only a slight increase of complexity.

In the decentralized scheme, the sampling rate for each channel can be conveniently and independently set, while in that of Figure 1, the sampling rate for each channel is tied to sampling rate of the multiplexer. To achieve variable sampling rates in the centralized system, for example, one must resort to super commutation (one channel connected to more than one multiplexer input) and/or subcommutation (multiple levels of multiplexing).

OTHER DESIGN CONSIDERATIONS

The decentralized scheme lends itself to simple and independent special-purpose preprocessing, at both analog and digital stages. It introduces the possibility of self-adaptive bandwidth allotment. It assures that the experiments do not interact and increases system reliability. A number of detailed technical problems which the designer must cope with in the centralized scheme simply do not exist in the decentralized scheme. For example, in the system of Figure 1, the speed of the converter must be greater than for that of Figure 2 by a factor equal to the number of channels, at least. In the centralized scheme, the sometimes low-level, high-impedance analog voltage must be communicated over long distances, making it susceptible to noise and perhaps requiring costly transmission links. In the decentralized scheme, the transmission of high-level, low-impedance, digital signals normally poses little or no problem. In many instances, they can be transmitted serially over a single wire.

In the scheme of Figure 1, the analog multiplexer can introduce such analog errors as offset voltages and switching noise; in addition, it is bandwidth-limited. The digital multiplexer cannot introduce analog errors and has no significant speed limitations.

MAINTENANCE CONSIDERATIONS

The principal reason the decentralized scheme is cost-competitive is its repetitiveness. A large number of essentially identical, large- or medium-scale, integrated circuits are used, rather than a large number of different circuits having diverse properties, which make up the centralized system. The multiplicity of identical circuits has favorable implications, not only for manufacturing cost, but also for maintenance of the system. Trouble shooting can often be reduced simply to substitution of units, and only a very few kinds of spare units are required.

BUFFER UTILIZATION

In a multi-channel data sample system which includes some form of processing and which then also includes a buffer, a basic decision concerning the buffer utilization is necessary: Should an accepted sample from one channel be allowed to enter the buffer based on the past history of activity of the individual channel, or should it be allowed to enter the buffer based on the past history of activity of all the channels collectively? The system of Figure 1 clearly reflects the "collective" arrangement while that of Figure 2 in its basic configuration clearly is the "individual." However, the addition of the self-adaptive bandwidth feature allows the system of Figure 2 to secure, in addition, the benefits of the collective system.

TIME AND ADDRESS

Considering the same buffer-storage capacity for both systems, and with the buffer organized as one large serial buffer in Figure 1, and as several smaller serial buffers in Figure 2, the time and address integrity is maintained as follows: In the centralized system with the large serial buffer, only the address need accompany a sample. The time* is deduced from its location in the frame.* In the basic form of the decentralized system, the address is deduced from its location in the frame, but time must accompany each sample through the channel buffer. In neither of the basic configurations must *both* time and address accompany the data.

ADAPTIVE BANDWIDTH ALLOCATION

In the system of Figure 2, the processor and its associated buffer are assumed to be equipped with feedback between the buffer level-of-content (see footnote on page 6) and the processor significance detector. This configuration makes it possible also for the *output* of the buffers to be *controlled* by the level-of-content. A simple arrangement may be devised by which nearly empty buffers are sampled less frequently than are buffers that are nearly full.†

The design of such an arrangement is depicted in the logic diagram, Figure 3. A sequencer, whose main purpose it is to control the data flow from a particular buffer onto the output data bus, is normally augmented (i.e., indexed, or advanced) by a word clock. By means of additional control gates, as shown in the diagram, the sequencer can also be augmented by a high speed service clock. This operation is controlled by the level-of-content control terms $b_1, b_2, b_3, \ldots b_n$ from the various buffers as follows: The sequencer will advance at high speed until it reaches the position of a buffer whose control term calls for unloading, and stop. The next advance pulse will be the word clock. If the following position is a buffer with a low level-of-content, the sequencer will again advance at high speed until it finds a buffer term indicating a high level-of-content.

When the self-adaptation bandwidth allocation feature is applied to the system, both time and address *must* accompany a sample. The channel address may be the actual address in

*Time: the instant at which the measurement was taken (e.g., the data was latched into the Sample-Hold). In the case of redundancy-reduction data compression, it is the time at which an item of data accepted into the buffer was obtained. "Location in the frame" means a specific interval in the multiplex cycle.

†Sometimes known as the "squeaky wheel" philosophy.

the frame (mechanized as shown in Figure 4), or in incremental address (number of channels bypassed, Figure 5), or a word that reflects the sampling pattern (Figure 6), transmitted at the end of each frame. In reference to buffer utilization, the addition of the self adaptive bandwidth feature will again allow an accepted sample to enter the buffer based on the past history of activity of all channels collectively rather than on that of an individual channel.

Non-adaptive or prescribed bandwidth allotment between channels is controlled by varying the level-of-content threshold above which the buffer is sampled.

HARDWARE IMPLEMENTATION

Recent advances in the state of the Digital-to-Analog art have made possible complete integrated-circuit Analog-to-Digital converters of physical size small enough to be utilized directly at the signal source. An example of such a device is the Analog Devices, Inc. μDAC, which can be cascaded in 4 bit segments to a maximum resolution of 16 bits. Switching time is 800ns to ±½LSB (10 bits) allowing conversion rates approaching 1MHz at the signal source. The device is monolithic, which enhances its reliability and ability to operate continuously in a deep-space environment. Utilizing the μDAC, and taking advantage of Medium-Scale Integration techniques to provide the logic, a complete 8 bit analog-to-digital converter should be possible in 6 to 8 TO-87 flatpacks.

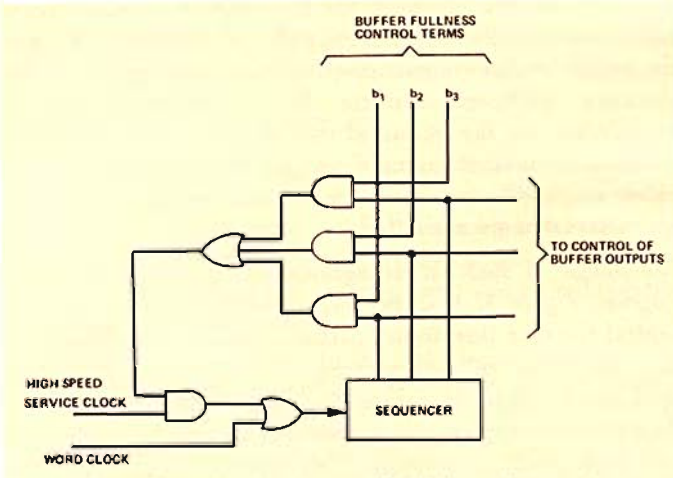

Figure 3. Adaptive Output Multiplexer Control

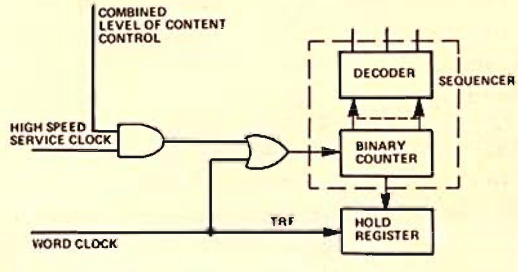

Figure 4. Actual Address Register Logic

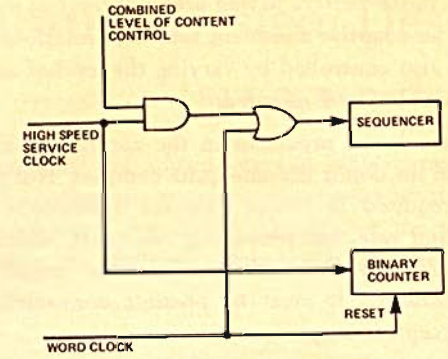

Figure 5. Incremental Address Logic (Counting Number of By-Passed Channels)

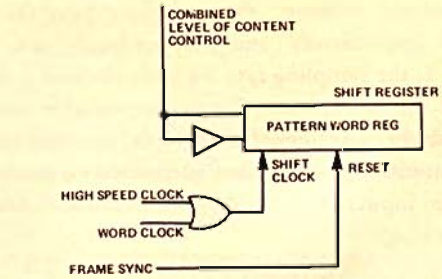

Figure 6. Sampling—Pattern—Word Logic

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Tage O. Anderson was born in Mellerud, Sweden, on August 7, 1926. He received a degree in electrical engineering at the Chalmers Institute of Technology, Gothenberg, Sweden, in 1947.

From 1948 to 1953 he was an Instrumentation Engineer in the Nuclear Chemistry Department, Chalmers Institute of Technology. From 1953 to 1958 he was engaged in design work on digital data processing equipment for a Swedish company, and from 1958 to 1963 he was with Consolidated Systems Corporation (now part of Xerox Data Systems), Pasadena, Calif., where he held a position as Principal Systems Engineer. In 1963 he joined the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, where he is now a member of the Technical Staff in the Telecommunications Division, active in the fields of synchronization, error-control coding, and data compression. He is the holder of several patents in those fields.

Mr. Anderson is a member of Sigma Xi.

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