

Isolating USB

WITH ISOLATION, THE USB FITS A WHOLE NEW CROP OF APPLICATIONS.

Although designers rely on the industry-standard USB (Universal Serial Bus) port to interface computers with hundreds of custom peripherals, isolation issues restrict its use in many applications. Isolation improves common-mode voltage, enhances noise rejection, and permits two circuits to operate at different voltage levels. Two obvious areas that require isolation are the medical field, in which PC-based instruments attach to patients, and the industrial arena, in which large supply-rail offsets can occur. Thanks to its simple, four-wire structure, USB may appear to be a natural interface for electrically isolating a device that connects to a PC.

USB enjoys extensive industry support and has become the standard way to connect peripherals to PCs. The interface oper-

ates at the low speed of 1.5 Mbps, full speed of 12 Mbps, and high speed of 480 Mbps. This article deals with optical isolation for a full-speed USB connection. A 12-Mbps device operates with enough bandwidth for useful data transfers and employs a data rate that inexpensive optocouplers can manage. The USB connector contains four wires. Two, bus voltage and ground, supply power, and two, D+ and D-, move the USB data. The bus-voltage wire provides 5V at as much as 500 mA of current-sourcing ability. The bidirectional D+ and D- signals operate at a 12-Mbps signal rate, or 83 nsec per bit cell. The D+ and D- signaling voltage is 3.3V.

Manufacturers build USB peripherals using a USB transceiver that connects to the D+ and D- lines and either drives or receives under control of an OE (output-enable) control pin (Figure 1). The middle portion, a USB SIE (serial-interface engine), handles translation of the bus signals that the transceiver sends and receives into data bytes and USB signals, respectively, for the application that implements the USB peripheral. The application circuitry might be a microprocessor, an ASIC, or a DSP.

ISOLATION SITES

You could incorporate optical couplers to electrically isolate a USB device from the host computer at the USB itself, the transceiver interface, or the application interface. Optical isolation on the USB wires is impractical, however, because the signaling rate is 12 MHz, which is too high for cost-effective isolators. Also, you must carefully match the D+ and D- signals for propagation delay and skew—a difficult prospect when using optical isolators. In addition, the USB is bidirectional, whereas isolators are unidirectional, complicating the situation. Furthermore, in a peripheral with an integrated transceiver, the OE signal, which indicates direction, is inaccessible.

A USB peripheral that uses an external transceiver exposes the transceiver interface, so you could consider these unidirectional signals for optical isolation. However, this site has the same problem as that for the bus wires: Its data rate is too high. It also has more 12-MHz signals to isolate. Signals VPO (single-ended output for D+), VPI (single-ended input for D+), VMO (single-ended output for D-), VMI (single-ended input for D-), and RCV (single-ended receiver output) all operate at 12 MHz, and you would need to carefully match them for delay and skew. Furthermore, this interface is rarely accessible in modern USB designs that incorporate the SIE and transceiver in the same chip.

The application interface is the most promising place to per-

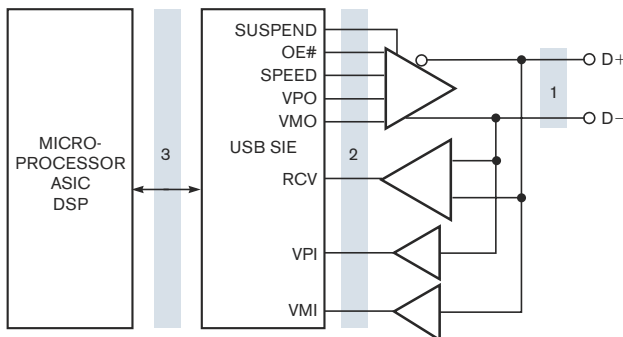


Figure 1 You can isolate a USB peripheral using the USB itself, the transceiver interface, or the application interface. Most current designs integrate the serial-interface engine and the transceiver, making the transceiver interface inaccessible.

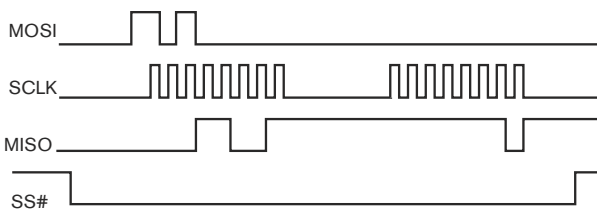


Figure 2 This serial-peripheral-interface example operates in mode (0,0). The same interface can operate in mode (1,1) if you make the SCLK signal active-low and the quiescent state is high. You can easily optically isolate these low-frequency signals.

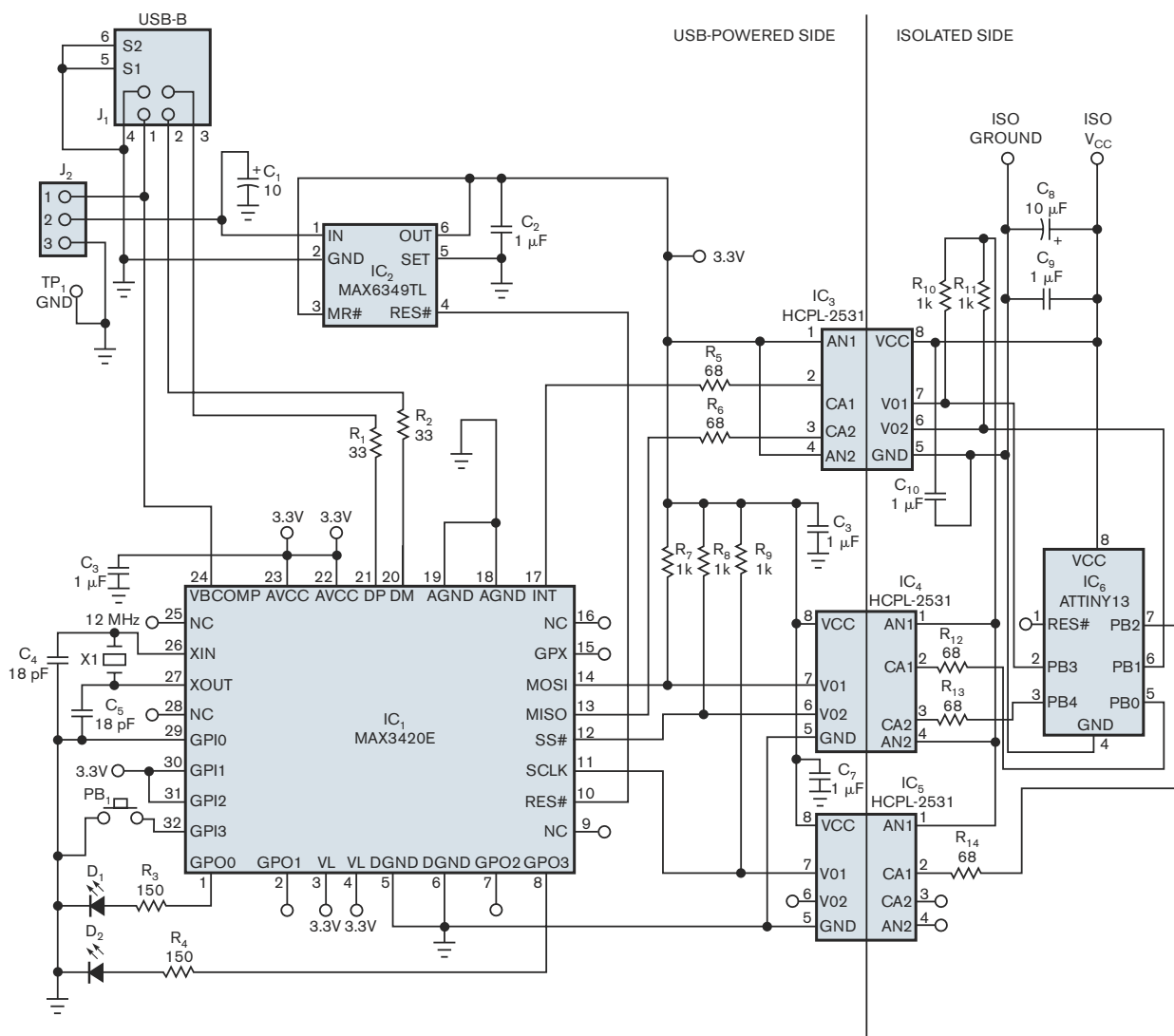


Figure 3 The USB powers the left side of this isolated-USB design, and the right side uses an isolated power supply. Providing the isolation at the SPI makes the design simple and independent of stringent USB timing.

form isolation, because the signals can operate more slowly than the USB data rate and you can build the interface so that it uses only unidirectional signals. An ideal interface would use a few unidirectional signals that operate at a data rate much lower than the USB's 12-MHz signaling rate. The SPI (serial-periph-

eral interface), which Motorola (www.motorola.com) originally defined and which is now widely available in many types of semiconductors, meets these requirements. This popular interface features simplicity and high performance.

With the SPI, a master/slave system, the master initiates and conducts transactions to a single slave. The master provides the SS# (slave-select) signal and the SCLK (serial clock) to synchronize data transfers (**Table 1**). The SPI has four clocking modes, reflecting two CPOL (clock-polarity) mode signals and two CPHA (clock-phase) signals. An SPI data transfer between a microprocessor and an SPI-slave device commonly uses SPI mode (0,0) (**Figure 2**). In mode (0,0), the clock is low in its inactive state, and the SPI master makes the MOSI (master-out/slave-in) data available before the first SCLK positive edge.

TABLE 1 SPI SIGNALS

SPI signal	Description	Comments
SS#	Slave select	Selects the chip for data transmission, which the master supplies
MOSI	Master out/slave in	Unidirectional data pin
MISO	Master in/slave out	Unidirectional data pin
SCLK	Serial clock	Serial clock, which the master supplies

LISTING 1 MAX3420E CODE

```

;-----
; Read a MAX3420E register. Uses MAX_Reg(preserved), Updates MAX_Dat.
;-----
rreg:
    cllT
rr2:  mov     dat,MAX_Reg ; 000rrrrr
      lsl     dat         ; 00rrrrr0
      lsl     dat         ; 0rrrrr00 (R)
      lsl     dat         ; rrrrr000 (write bit is clear--b1)
      bld     dat,0       ; rrrrr00T (T=ACKSTAT bit)
      rcall  send_byte

;
; Now read the MISO data
;
r4:   SCK_LO
      SCK_HI           ; ready the next input bit
      sec              ; speculatively set CY
      sbis     PINB,MISO ; skip if set
      clc
      SCK_LO
      rol     MAX_Dat  ; shift CY into the data byte
      dec     bitcount
      brne   r4
      SS_HI           ; all done
      ret
;

```

For both master and slave devices, SPI data changes on the SCLK falling edge and is sampled on the SCLK rising edge. SPI is easy to implement on any microprocessor, even one that contains no hardware-SPI unit. All it takes is four general-purpose-I/O pins to construct the signals and two subroutines to read and write bytes by directly toggling the I/O pins.

The data rates of the SPI bus and the USB differ dramatically. The isolation approach becomes simple with the SPI signals, which you can tailor to run at any frequency to suit the characteristics of the optical isolators. The system reconciles the wide difference in data rates between the SPI bus that operates the

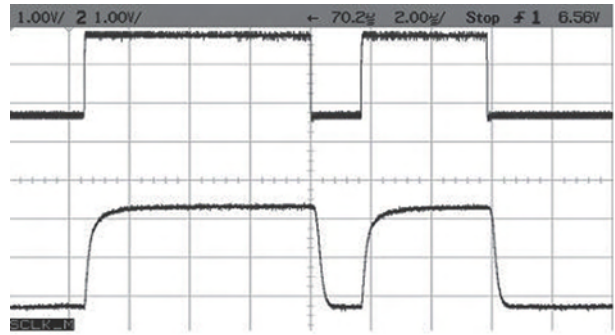


Figure 4 The SPI SCLK signal appears on both sides of the isolated interface. The top trace indicates the isolated supply at Ground 2 of 5V and V_{CC} of 8V.

USB controller and the USB signaling rate using USB's "self-throttling" feature with built-in flow control. It uses an NAK (negative-acknowledge) handshake, whereby a peripheral tells the host asking for data that it is not ready with data, and the host should try again later (see sidebar "USB-flow control"). Thus, a designer can fine-tune the SPI data rate to suit opto-coupler choices for practical and cost-effective designs.

ISOLATED-USB-DESIGN EXAMPLE

Figure 3 shows a circuit based on an inexpensive micro-processor, the Atmel AtTiny13, IC₆; HCPL-2531 optocouplers

USB-FLOW CONTROL

Figure A shows the USB (Universal Serial Bus)-flow-control mechanism in action. Starting with Packet 362, the host issues a "get-descriptor-configuration" request. The 09 in the second-to-last byte of Packet 363 indicates that the host wants 9 bytes of data from the peripheral. The peripheral acknowledges receipt of the request in Packet 364 and then gets busy decoding the request and loading the requested data into its endpoint 0 data FIFO.

A slow peripheral takes some time to answer this request, and the relatively slow SPI (serial-peripheral-interface) bus increases the response time. After Packet 364–988.667 μ sec

later—the host starts asking for the requested data in Packet 366. The peripheral doesn't yet have the data, so the USB hardware automatically responds with the NAK (negative-acknowledge) handshake, indicating "I'm busy; try again later." The host tries again in Packet 368 and gets the same NAK answer from the peripheral.

This process continues until Packet 419, when the peripheral at last has the requested data and arms its endpoint 0 for the data transfer. Now, instead of NAK, it responds with the 9-byte data packet in Packet 420, which the host acknowledges in Packet 421. The NAK pairs (dotted rectangle in Figure A) can

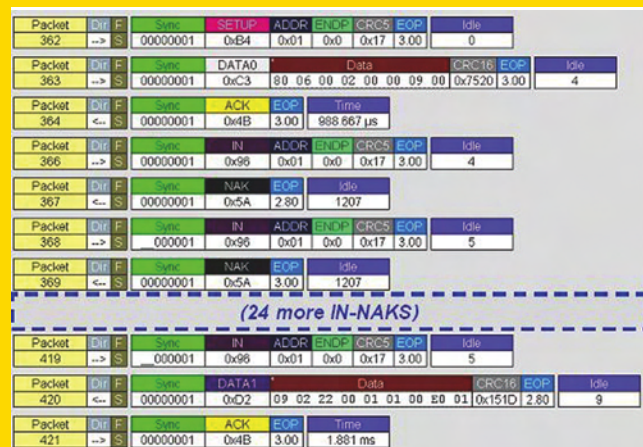


Figure A A USB trace shows a slow peripheral responding to a host's request for data. The host requests the data in packets 362 through 364. The peripheral is ready with the data in Packet 420. The intervening NAK packets demonstrate USB-flow control. The peripheral responds with NAKs until it is ready with data.

occur any number of times, which means there is no lower limit on the rate at which the SPI can operate.

IC₃, IC₄, and IC₅; and the MAX3420E, IC₁, a USB peripheral controller with an SPI to its register set. Even though IC₆ contains no hardware-SPI unit, “bit-banging” some general-purpose-I/O pins easily manages the SPI. IC₁ provides four general-purpose input pins and four general-purpose output pins to replace and add to the pins the microprocessor uses to implement the SPI. This design uses two output pins to drive LED indicators D₁ and D₂ and one input pin to connect the pushbutton switch S₁. Because IC₁ contains I/O pins of its own that SPI controls, they are inherently isolated from IC₆ and require no individual isolation.

Scope traces of the SCLK signal on both sides of the isolated interface demonstrate the optocoupler performance (Figure 4). The optocouplers have a throughput delay of approximately 0.5 μsec with the resistor values for this design. The short SCLK pulse in the center is the result of a portion of IC₆'s code that drives the SCLK I/O pin (Listing 1). Just before the “r4” label, the SCLK signal is driven low and then immediately high again. Assembler macros SCK_LO and SCK_HI ease the assignment of I/O pins for pc-board layouts without changing the code. By inserting a few NOP (no-operation) instructions between these two statements, you can lengthen the narrow pulse in Figure

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4, opening the possibility for using lower cost optocouplers. This example shows the flexibility that the SPI offers for optically isolated systems.

Electrically isolating the USB has been a challenge due to the high-speed, bidirectional nature and stringent matching requirements of the USB-data signals. The

situation becomes simpler if you isolate the interface between the USB controller and the application processor, because this interface can run at any rate. The lower signaling rate suits USB for low-cost optocoupler systems. As with any isolation design, the fewer lines that require isolation, the more cost savings you accrue. The SPI is an ideal candidate for isolation because it uses only four low-speed, unidirectional signals. **EDN**

AUTHOR'S BIOGRAPHY



Lane Hauck works in San Diego, CA, as a senior scientist at Maxim Integrated Products (Sunnyvale, CA), where he has worked since 2002. He received a bachelor's degree in physics from the University of California—Los Angeles and a master's degree in computer science from California State University—Los Angeles. His personal interests include music and digital photography.

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