Inverting level-shift circuit has negative potential

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Digital-system designs require you to consider many core voltages. Memory operates at 1.8V, I²C and FPGA devices operate at 3.3V, microcontrollers operate at 5V, and charge-coupled-device image sensors operate at –9 to 8V. Clocks for each device must suit their operating voltages.

You can use the level-shift circuit in **Figure 1** to adjust an input clock signal to the proper logic-high and logic-low voltage levels, including negative voltages. This property is handy for devices that need a negative voltage, such as a charge-coupled-device sensor. Although the circuit's output clock is 180°-inverted relative to the input clock, that inversion does not affect the function of the device.

The level-shift circuit comprises fast-switching transistors Q_1 and Q_2. The user chooses level-shift high and level-shift low, which are dc-bias voltages and which connect to the transistor emitters, to match the desired output high- and low-logic levels. C_1, R_1, D_1, C_2, R_2, and D_2 keep the base voltages of Q_1 and Q_2 close to that of their emitters.

Because memory and charge-coupled-device sensors usually have high-frequency clocks, you can choose C_1 and C_2 to prevent low-frequency-noise pass-through. The circuit in **Figure 1** uses a 20-MHz signal for measurements (**Table 1**) and thus uses a value of 100 pF for C_1 and C_2. When the input voltage's clock is low, Q_1 turns on and Q_2 turns off, driving the output voltage's clock to the level shift's high potential. When the input voltage's clock is high, Q_1 turns off and Q_2 turns on, driving the output voltage's clock to the level shift's low potential, even when that potential is negative relative to ground.

Because of the circuit's high switching speeds, keep component leads as short as possible to minimize inductance. This caveat is especially true for C_3 through C_6's leads to their respective transistor emitters and to the ground plane or the output ground return. EDN

TABLE 1 INPUT AND OUTPUT CLOCKS

High/low level shift (V)	Input clock (V)	Output clock (V)
3.3/0	0/5	3.3/0
20/10	0/5	20/10
–5/–10	0/5	–5/–10
2/–4	0/5	2/–4

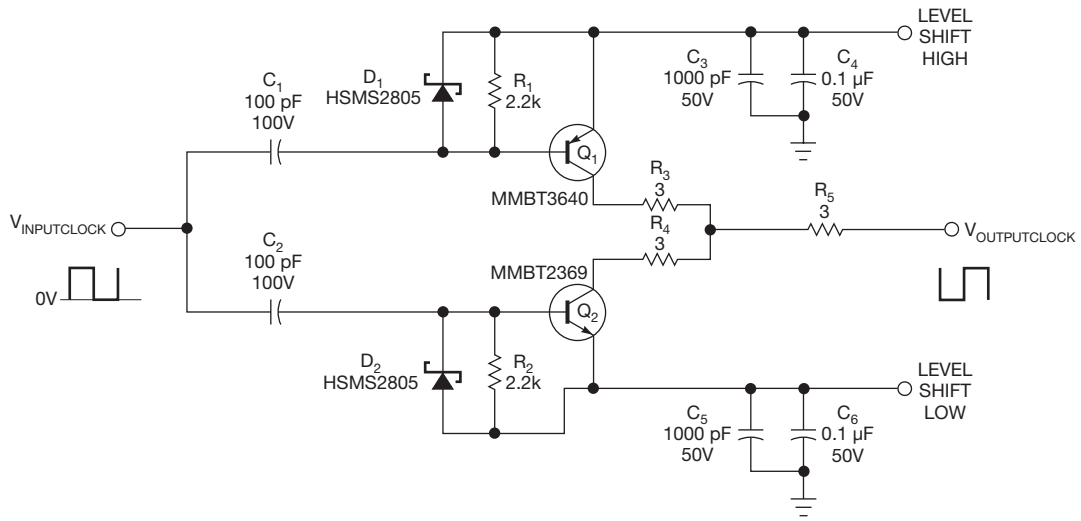

Figure 1 This simple and fast level-shift circuit can adjust an input clock to both positive and negative voltage levels.