ELECTRONICS —it's easy! PART 32

Concluding Digital-to-Analogue and introducing Analogue-to-Digital conversion.

INTEGRATED CIRCUIT CURRENT SOURCES — As the DAC principle finds a variety of uses, manufacturers offer an integrated current, the magnitude of which is controlled by a four bit, binary-code input. The IC, as shown in Fig. 1, has enough precision to be used in 12-bit D/A and A/D conversion. Figure 2 illustrates how two of these ICs are combined to produce an 8-bit DAC.

Digitally controlled sources — The DAC's described above are usually concerned with signal processing as opposed to analogue power control. If larger output powers are needed digitally-controlled power supplies can be used — also referred to as digitally programmed supplies. They are available with digital control of current or voltage outputs. Instruments in the Hewlett-Packard range, for example, can provide up to 125 watt maximum demand whilst the output is controlled by binary or BCD inputs with a programming time of around 350μs.

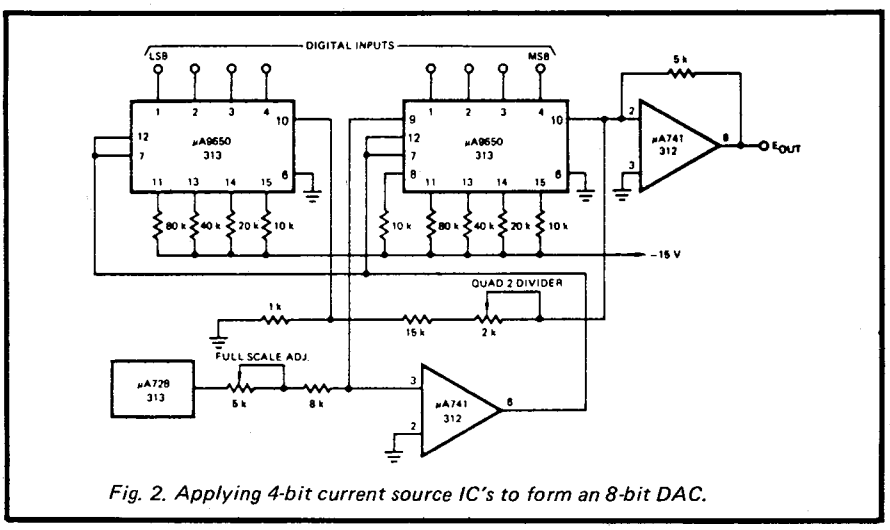


Fig. 2. Applying 4-bit current source IC's to form an 8-bit DAC.

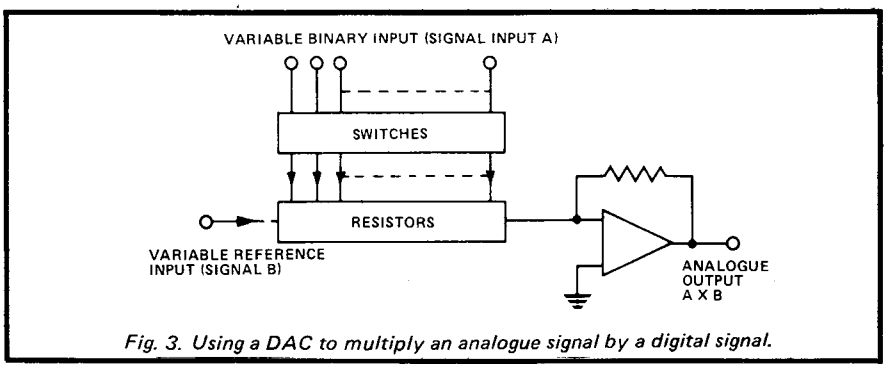


Fig. 3. Using a DAC to multiply an analogue signal by a digital signal.

ARITHMETIC OPERATIONS WITH DAC's

Multiplication — The resistor network of a DAC has two inputs — the reference supply (which is fixed in normal D/A conversion) and the switch inputs representing digital numbers. If the reference is allowed to vary as an input variable, see Fig. 3, the output of the DAC is the multiplicand of the two signal inputs. The reference may also be an ac signal and division and attenuation are also possible. The advantages of this method are the high precision and speed available.

Addition — If the difference or sum of two digital signals is needed as an analogue output, two DAC's may be combined, as sum or difference, into the output op-amp, as shown in Fig. 4.

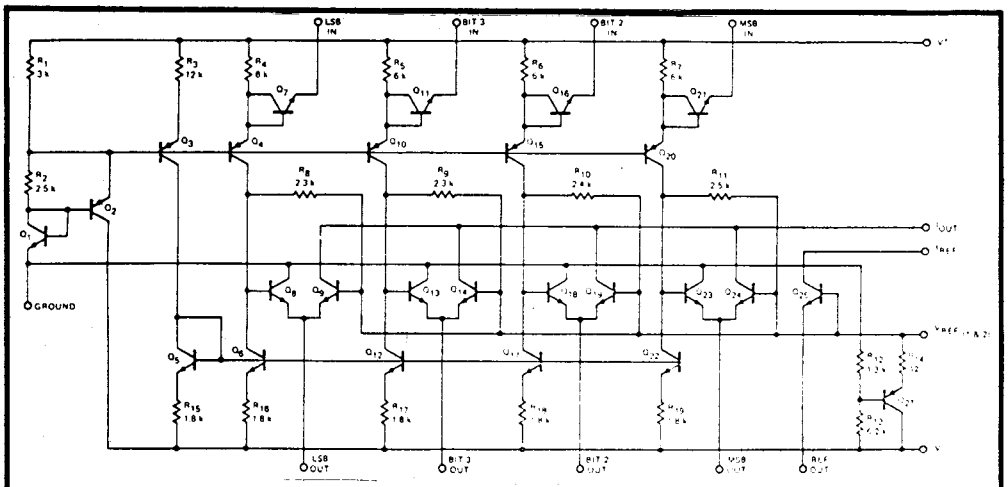


Fig. 1. Schematic of dual- in-line 4-bit current source (Fairchild μA9650).

ANALOGUE TO DIGITAL CONVERSION

Conversion from analogue to digital code can be obtained by many alternative techniques, each alternative having many variations. Basically, methods group into open-loop and feedback-loop systems. In each group some four to eight ways are in common usage. Here we look at a few of the most popular techniques, beginning with open-loop methods.

Analogue-to-frequency — The analogue voltage is converted, on a continuous basis, into a signal of proportional frequency by the use of an appropriately accurate V-to-F converter. (Voltage controlled oscillators are used — they must be adequately linear). This signal, see Fig. 5, is gated into a digital counter using fixed times of gate aperture. The counter accumulates a digital number equal to the average analogue level over the gate period. The counter output is released upon demand when gate periods expire. This method suffices for low accuracy analogue

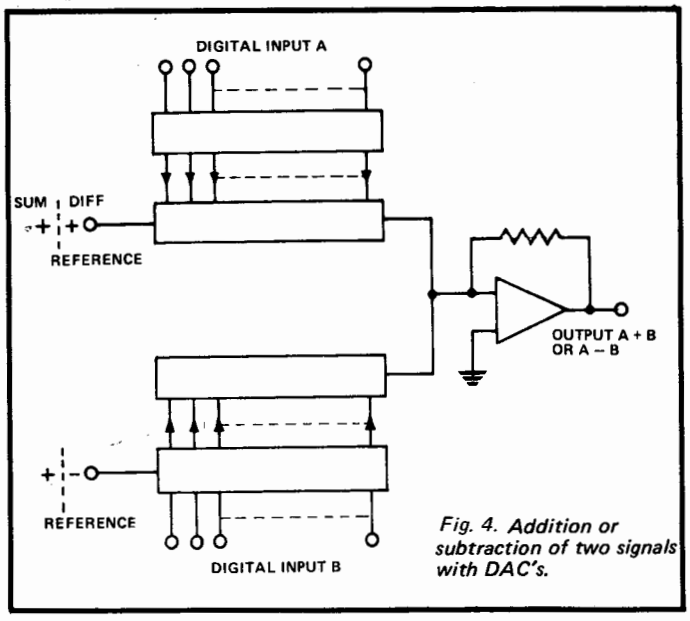


Fig. 4. Addition or subtraction of two signals with DAC's.

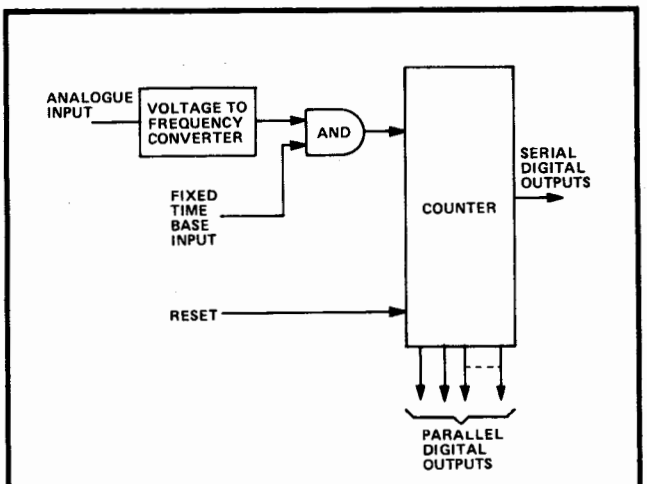


Fig. 5. Voltage-to-frequency method of A/D conversion.

inputs but becomes expensive when precision, wide dynamic range is required.

A variation of this is to reverse the philosophy and vary the pulse width of accurately generated pulses of constant frequency. The variable pulse width is then converted to a digital count proportional to the pulse width.

Simultaneous, parallel or flash conversion – The input analogue signal is presented to a stack of comparators (Schmidtt trigger action) each set to trigger at increasing binary-weighted signal levels. The set of comparator outputs are then decoded to provide the required binary output form. Decoding is needed because at any instant all comparators set to below the signal level are in the one state, all above in the other. The method is given in Fig. 6. Although extremely fast – quantization time is the speed of a single comparator – the method has the serious disadvantage that large bit ranges require many comparators and numerous decoding gates.

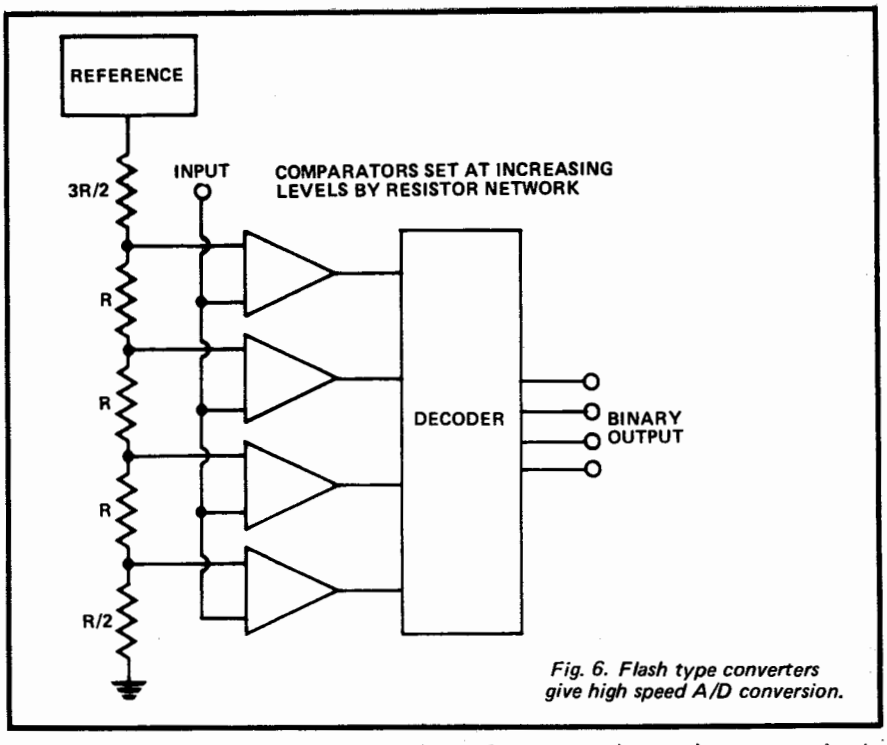


Fig. 6. Flash type converters give high speed A/D conversion.

Closed-loop methods – are more popular and there are about six main alternatives The methods known as integrating, successive approximation and servo-DAC are most generally applied.

Dual-ramp integration – The analogue voltage is first converted to a time period which in turn is converted into a binary number by a timer/counting system. Referring to Fig. 7a, conversion begins when the switch connects the analogue-signal input to the integrator which commences to ramp up. At the same time the counter begins, from zero, to count the clock pulses. When a predetermined number of pulses (1000 is convenient) appear in the counter the integrator is electronically switched over to the reference. At this point the capacitor has then charged linearly from the input, rising as a ramp to a voltage level decided by the average input-signal value as shown in Fig. 7b.

As the switch changes to the reference position the counter is reset to zero and begins counting again. The reference, chosen to be of opposite polarity to the input signal, now causes the charged capacitor of the integrator to ramp back downward at a constant slope. When the integrator output reaches the zero threshold the counter is stopped and its contents displayed. The count displayed is the ratio of downward ramp counts to upward ramp counts which, when a 1000 upward limit is used, gives a direct reading of input voltage if the reference voltage is appropriately chosen.

A simpler form, using only one ramp, is also used but it lacks the features of the dual-ramp method in which the absolute value of the capacitor and the clock frequency are of no significance provided they are stable for the duration of the conversion period. The dual ramp method does, however, require a relatively long conversion period but this is an advantage in one respect – the value measured is more accurate. This is due to the fact that when noise is integrated over an extended time period it tends to zero.

A more sophisticated triple-ramp method provides increased speed and accuracy for a moderate increase in cost and complexity. In essence two reference signals are provided, one

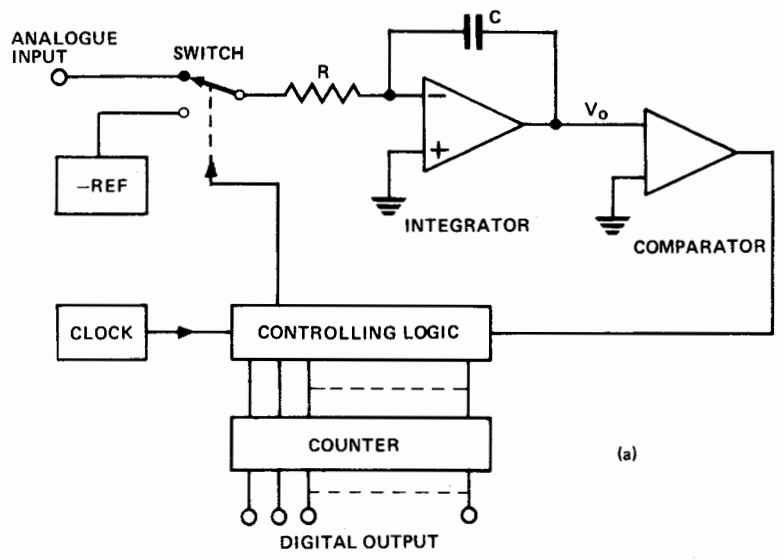


Fig. 7. A/D conversion using dual-ramp integration. (a) schematic (b) timing diagram.

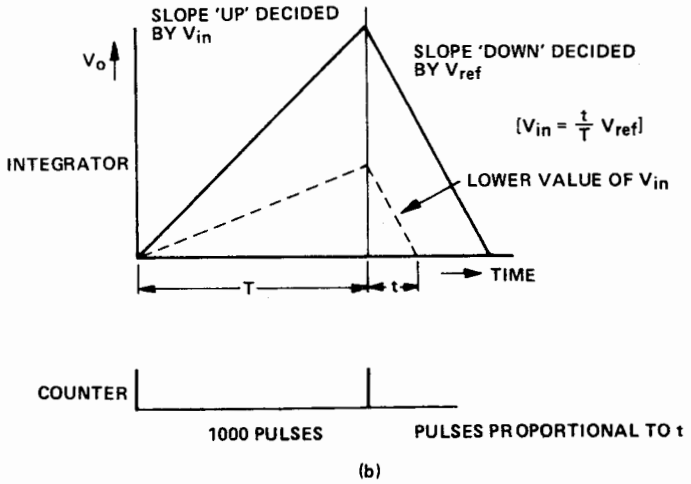
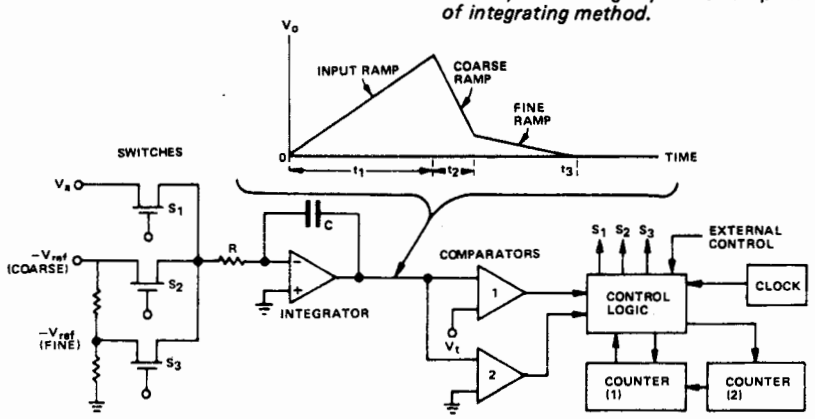


Fig. 8. Triple-ramp A/D converters offer faster speed for slightly more complexity of integrating method.



acting as a 'coarse', the other as a 'fine' ramping control. The 'coarse' ramp rapidly converts the bulk of the input signal level leaving the 'fine' ramp to add the extra resolution. Figure 8 shows the schematic and timing diagram of a triple-ramp A/D converter.

Successive approximation – Due to its high resolution and fast conversion speed successive approximation is the most widely used method. A schematic diagram is given in Fig. 9. Conversion progresses step-wise with the precisely generated DAC output being compared against the unknown analogue input. The first comparison is made with the most significant digit of the DAC, which gives 1/2 full scale, being compared against the unknown. If it is smaller, the bit is retained as a '0', if larger it is set to '1', thus the MSD value of the programmer is found. The next digit, working towards the least significant end one digit at a time, is then tested for the same criteria being set accordingly. The process is repeated until all programmer digits are set to '0' or '1'. The value in the programmer is then transferred to the register for outputing in parallel or serial form. Conversion time is not decided by the value of input as in ramp methods, duration of conversion being the number of bits times a fixed digit test interval, which can be as fast as 100ns. By comparison, from one maker's options, successive approximation instruments offer conversion times which range from 1-60μs compared with 2.5-6.0ms for integrating converters. Accuracy clearly depends upon that of the DAC which forms part of the comparison system.

Serve DAC method – Fig. 10 shows this system. When conversion begins, a counter is gated and commences to count upward. Its digital output is converted back to analogue form by a DAC. The output of the DAC is compared against the unknown input voltage. When the two analogue voltages are equal, the comparator inhibits the counter. At that time the value in the counter is a digital representation of the input – with 1:1 correspondence; or other ratios depending upon the summing resistances used. It is a simple low-cost method providing reasonable accuracy but operates at a slower speed than offered by successive approximation designs.

Non-linear conversion – Each bit of the above methods represents an equal quantum error. Thus one quantum error in full-scale is considerably less inaccuracy than in say a tenth or hundredth of full-scale. The smaller the reading, the greater the relative error of quantisation. When range-changing is not practicable a non-linear digital method can be used to compress the large scale in order to reduce the percentage of reading error The method is explained in Motorola Application Note AN-471.

SAMPLE-AND-HOLD UNITS

A digital signal provided by an A/D converter represents some measure of the analogue level seen in a certain gating period – the so-called aperture time. Aperture time, bit resolution and maximum signal frequency are strictly

interrelated. Figure 11 is a chart enabling this characteristic to be found. For example, we may need to digitize a 10 kHz sinusoid (as the highest frequency to be preserved in a complex waveform) to a resolution of 12 bits. The chart shows we must have an aperture time of no greater than 42 ns. Thus we see extremely fast converters are needed for direct conversion of moderately high-frequency signals at high resolution.

A sample-and-hold circuit circumvents this difficulty by taking a rapid narrow-aperture sample of a signal and holding it in a simple analogue store long enough for the converter to act with a much wider aperture time. Figure 14 shows such a system. To preserve the highest signal frequency of a complex signal we only need to sample at twice (or higher) the signal frequency (Shannon's sampling theorem). This is a considerably slower rate than needed for direct A/D conversion. If sampled too slowly, not only will higher frequency information be lost but an effect, called aliasing, will occur by which a lower frequency is generated that may not exist in the original signal.

As mentioned above sample-and-hold circuits are also used in DAC's to remove glitches.

Basically a sample-and-hold comprises a capacitor with which to store an analogue voltage level, and a switch to charge the capacitor to that value in a way that can be rapidly and effectively isolated from the source. In practice low leakage FET switches are used in conjunction with IC op-amp integrators. It is also important to buffer the output of the sample-and-hold to reduce the loading which would otherwise decay the stored level.

Many circuit variations exist, the one shown in Fig. 12 – a closed loop configuration – gives good linearity and accuracy. When extremely long storage times, or negligible decay with time is needed, the voltage on the capacitor can be transferred via an A/D converter into a digital storage register and back again into analogue form via a DAC as shown schematically in Fig. 13. This naturally increases the cost considerably. More detailed information is available in "Analog-digital conversion handbook" TH6, by Analog Devices.

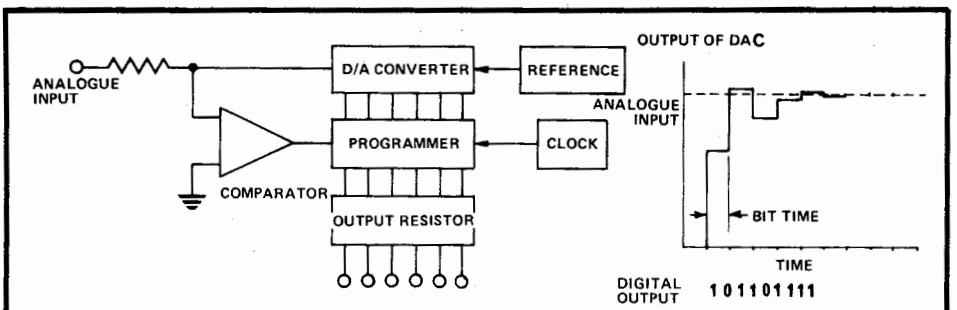


Fig. 9. In the successive approximation A/D converters a DAC is used to convert the incremented digital stage output back to analogue form for comparision with the input.

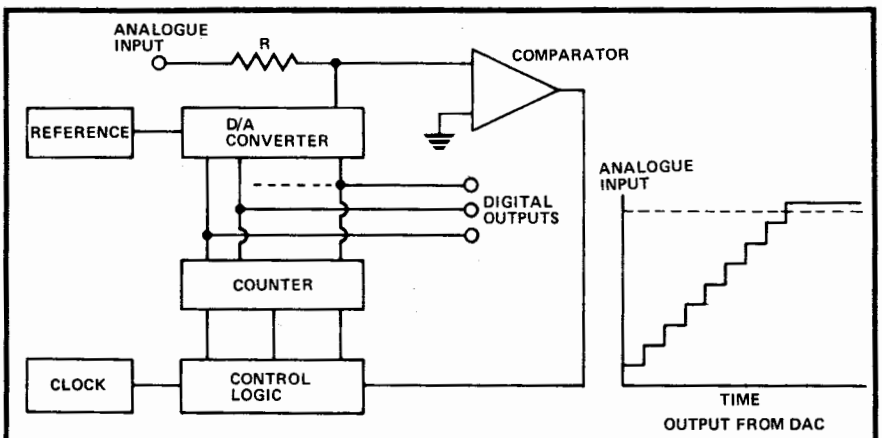


Fig. 10. Schematic of servo A/D converter system.

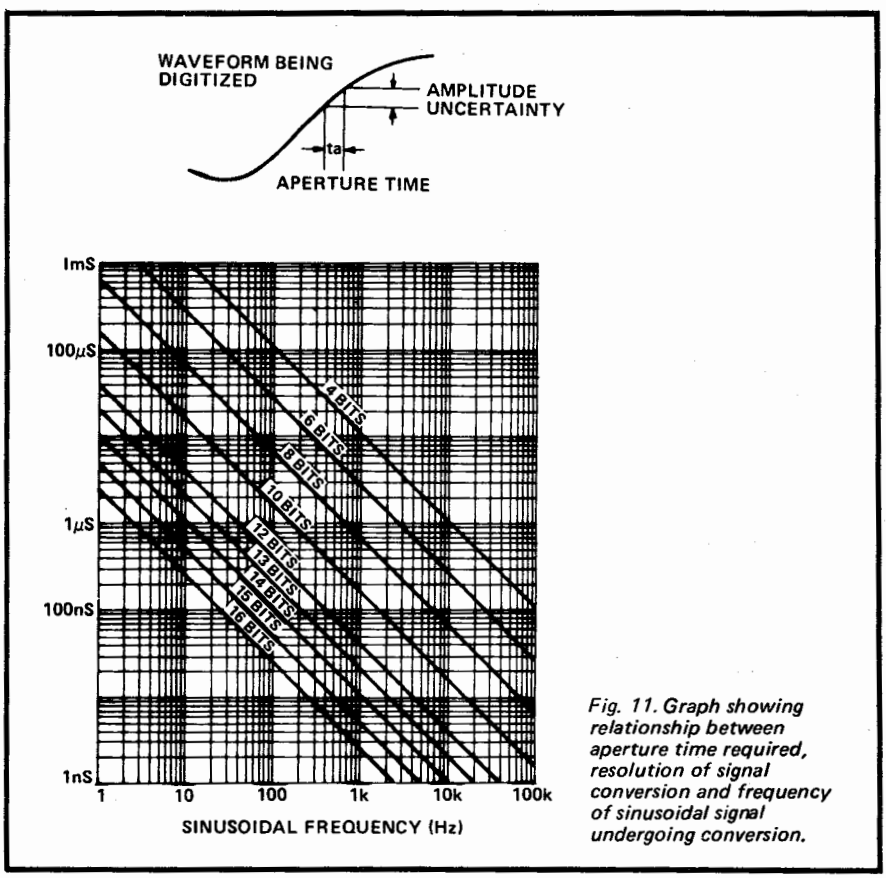


Fig. 11. Graph showing relationship between aperture time required, resolution of signal conversion and frequency of sinusoidal signal undergoing conversion.

MULTIPLEXERS

The task of the multiplexer, shown in Fig. 14, is to sequentially connect a multiplicity of compatible inputs to a single output line. In the case given in Fig. 14 it feeds a sample-and-hold, which stores the signal for A/D conversion.

A multiplexer consists, therefore, of as many switches as there are input channels to be combined. In practice these must possess adequate speed and very low on-to-off switch resistance ratio. Solid-state multiplexers mostly use MOSFET switching devices feeding a buffer stage (a voltage follower configuration which has extremely high, 10^9 ohms, input impedance).

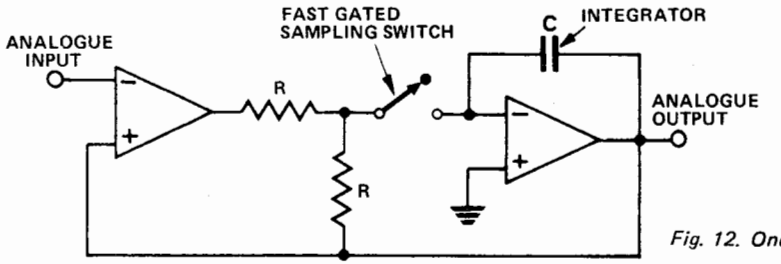


Fig. 12. One form of stable and accurate sample-and-hold circuit.

FURTHER READING

A comprehensive discussion of the topics, and a long bibliography, of this part is to be found in "Analog-digital conversion handbook", D.H. Sheingold, Analog Devices, U.S.A. 1972. Less extensive but nevertheless very useful articles are – "Engineering product handbook", Datel Systems, CAT-T99405, 1974, U.S.A.

"Analog-to-digital conversion techniques", E. Renschler, Motorola Semiconductor Products Inc., AN-471, 1969, U.S.A. "Product Guide", Analog Devices, 1975, U.S.A. ●

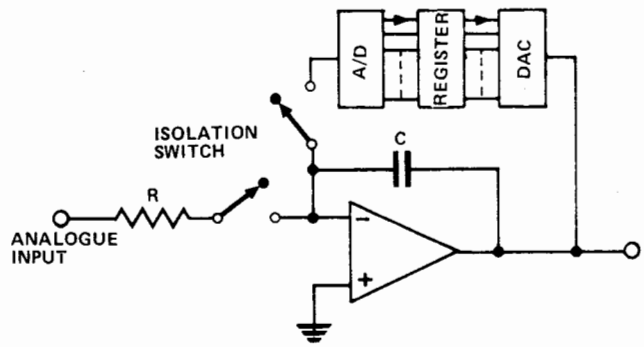


Fig. 13. Infinite hold is obtained by transferring the integrated value into a digital store using A/D and D/A conversion.