C-MOS counter sets divider's modulus

by Arie Shavit
Kiriat Tivon, Israel

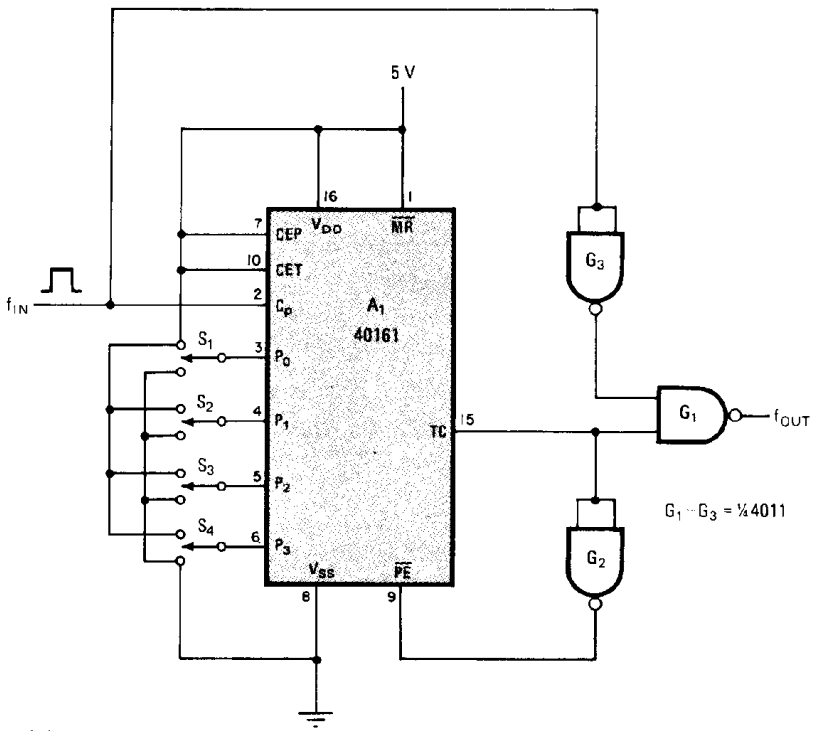
The cost and power consumption of Albing's C-MOS variable-modulo divider[1] can be reduced even further with this circuit, which uses logic gates and four low-cost binary switches to replace one counter and the multiple-pole selector, respectively. Although the counter's modulus is set with the binary elements, thereby sacrificing the convenience of ordering up values in the familiar decimal form, the ease of interfacing the counter to microprocessor-based control systems is immensely enhanced. Divider ratios of from 1 to 16 can be selected.

The 40161 synchronous binary counter, A_1, which has parallel-load capability, is stepped by input frequency f_{in}, as shown in (a). Switches S_1–S_4 set the binary representation of $16-n$ at the parallel-load inputs P_0–P_3, where n is the desired divider ratio, as shown in (b).

Output pin TC of A_1 moves high after n cycles of f_{in}. Thus the output signal from gate G_1 is a pulse of short duration having a frequency of $f_{out} = f_{in}/n$. TC is then inverted by gate G_2 and used to reset the counter.

Gate G_3 comes into play if a modulus of 1 is set. Under these conditions, TC remains high and f_{in} serves to gate itself to the output. □

References
1. Bradley Albing, "C-MOS counter-decoder pair sets divider's modulus," Aug. 30, 1979, p. 140.



Binary code				Divider ratio n
S_4	S_3	S_2	S_1	
1	1	1	1	1
1	1	1	0	2
1	1	0	1	3
1	1	0	0	4
1	0	1	1	5
1	0	1	0	6
1	0	0	1	7
1	0	0	0	8
0	1	1	1	9
0	1	1	0	10
0	1	0	1	11
0	1	0	0	12
0	0	1	1	13
0	0	1	0	14
0	0	0	1	15
0	0	0	0	16

(b)

Binary breakup. Single counter and three gates simplify design of variable-modulo divider (a). Binary switches S_1–S_4 set counter to $16-n$, where n is desired divider ratio (b). Output of gate G_1 is a pulse with a frequency equal to $f_{out} = f_{in}/n$, for $1 \leq n \leq 16$.