Counter inverts period to measure low frequency

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Measuring the frequency of a low-frequency signal directly is a slow process, since enough signal cycles must be counted to give the needed resolution. Measuring the signal's period instead can give the needed information in only one period, but computation or circuitry to convert period to frequency is necessary. The circuit described here finds the reciprocal of the measured period by means of standard binary and binary-coded-decimal counters.

The concept underlying the technique is illustrated in Fig. 1. Four counters are required. Counter A measures the period of the unknown signal by counting the number of clock pulses, N, during a cycle. The number N programs counter B, which is a programable divide-by-N unit. Counter C creates a burst with a fixed number of pulses K.

This burst is applied to counter B, which computes a number K/N, thus taking the reciprocal of the period, N, and producing a number of pulses proportional to the unknown signal frequency. Finally, counter D accumulates these pulses to display the frequency.

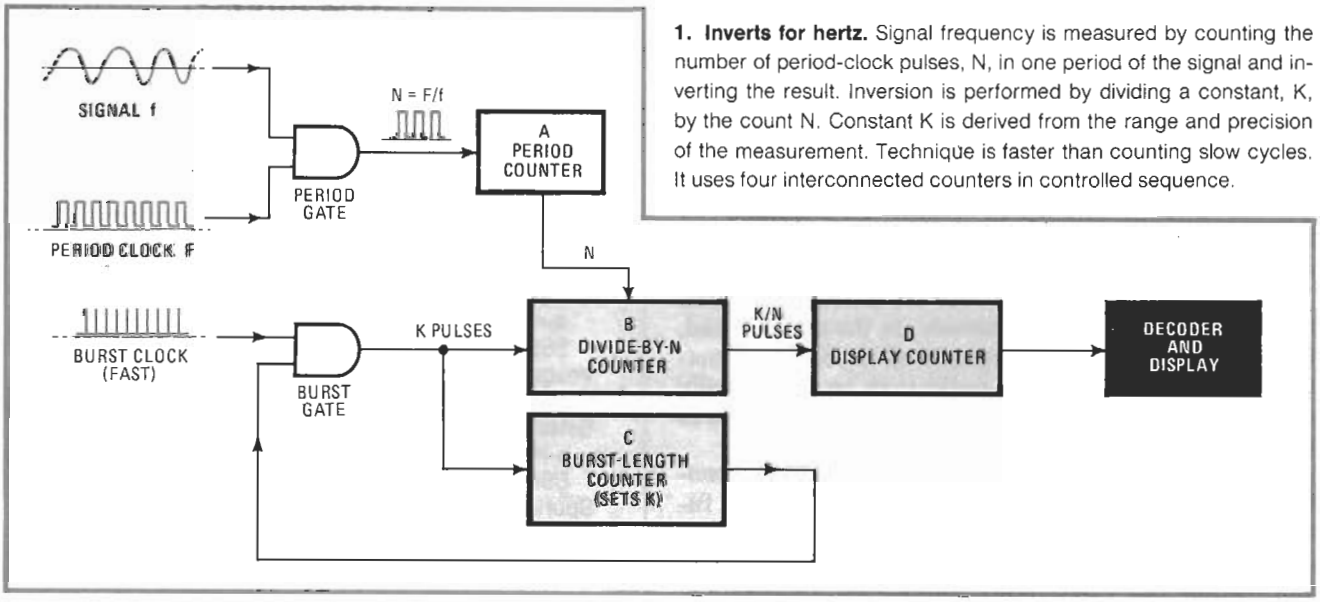
The application determines the clock frequency and the counter lengths.

1. Clock frequency is defined by the highest frequency to be measured, and the resolution with which it must be measured. For example, if 1 kilohertz must be measured to 1% accuracy, 100 clock pulses must occur in 1 millisecond (one signal period). This defines a clock frequency of 100 kHz.
2. The lowest frequency to be measured has the longest period, which defines the lengths of counters A and B. In this example, a low-frequency limit of 10 hertz would require a counter capable of counting 0.1 second (period of 10 Hz) × 100 kHz, or 10^4 clock pulses. Fourteen bits would suffice.
3. The size of counter C depends on the length of the pulse burst. The period of a 10-Hz signal results in a count of 10^4 in counter A. If K/N is to be 10, then K, the number of pulses in the burst, must be 10^5. A 17-bit counter is required. The actual frequency of the burst does not enter into the end result; to speed calculation, the burst frequency should be as high as is convenient.
4. Finally, counter D must count to the highest frequency measured, 1,000. This requires 10 bits, or 3 BCD decades if the frequency is to be displayed.

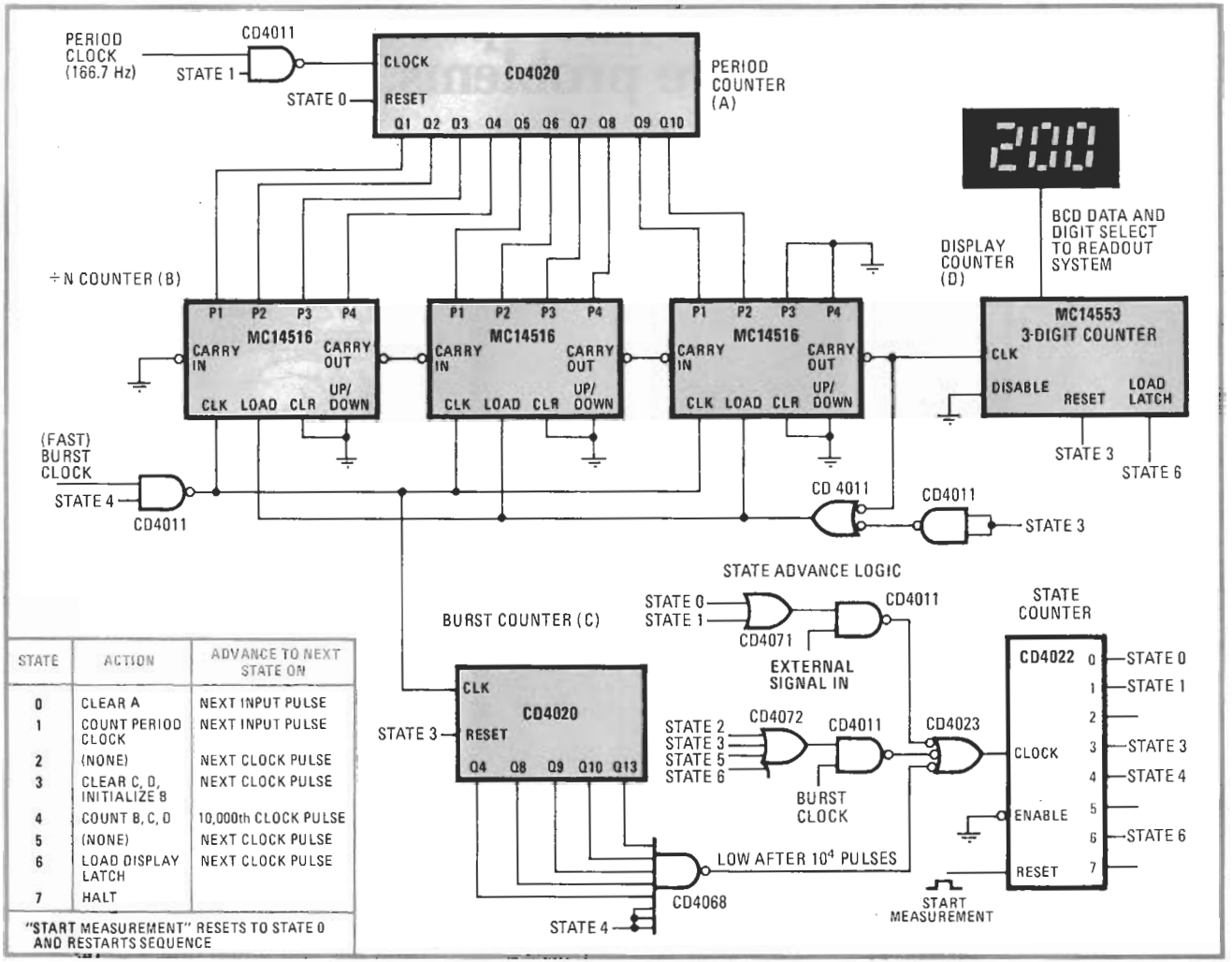
Control logic, to implement the sequencing required, must of course be provided.

Figure 2 shows how the technique may be used in a tachometer capable of measuring shaft speed from 10 to 200 revolutions per minute, with 2% resolution at 200 rpm. The four steps above give the circuit parameters.

1. At 200 revolutions per minute, the signal period is 0.3 second. To measure the speed to 2%, 50 clock pulses must be counted in this time, so the clock frequency must be 166.7 Hz.
2. At 10 rpm, the signal period is 6 seconds. Counting clock pulses for this time results in 6 × 166.7 = 1,000 counts, so counters A and B are each 10 bits.
3. The pulse burst must give a quotient of 10 with 1,000 counts, so it must be 10,000 counts long. Therefore K is 10^4, and counter C thus requires 14 bits.
4. Counter D, the display register, must count up to the



1. Inverts for hertz. Signal frequency is measured by counting the number of period-clock pulses, N, in one period of the signal and inverting the result. Inversion is performed by dividing a constant, K, by the count N. Constant K is derived from the range and precision of the measurement. Technique is faster than counting slow cycles. It uses four interconnected counters in controlled sequence.



STATE	ACTION	ADVANCE TO NEXT STATE ON
0	CLEAR A	NEXT INPUT PULSE
1	COUNT PERIOD CLOCK	NEXT INPUT PULSE
2	(NONE)	NEXT CLOCK PULSE
3	CLEAR C, D, INITIALIZE B	NEXT CLOCK PULSE
4	COUNT B, C, D	10,000th CLOCK PULSE
5	(NONE)	NEXT CLOCK PULSE
6	LOAD DISPLAY LATCH	NEXT CLOCK PULSE
7	HALT	

"START MEASUREMENT" RESETS TO STATE 0 AND RESTARTS SEQUENCE

2. Measuring frequency. Implementation of arrangement in Fig. 1 uses C-MOS devices. A fifth counter, the CD4022 divide-by-8, sequences the steps of the procedure, as shown in the table. This measurement system is fast because it counts clock pulses for only one period of the signal frequency, instead of counting many cycles of signal. Precision of measurement is high because clock rate is high.

maximum of 200. Three BCD decades will suffice. For the low frequencies involved, complementary-MOS devices are adequate. The control logic consists of a CD4022 divide-by-8 counter with individually decoded outputs. Each output corresponds to a step in the control sequence as follows:

- Clear period counter A.
- On next signal transition, start counting clock pulses in counter A.
- On next signal transition, stop counting A.
- Clear counters C and D.
- Enable counters B, C, D to compute frequency.
- After 10,000 pulses, stop counting.
- Load output latch to update BCD display.

A network of gates selects the proper signals to advance the sequencer from state to state.

For easier implementation, the length of the pulse burst may be chosen to be an exact power of 2. This simplifies the logic around counter C.

The final display is equal to K/FT, where K is the length of the burst, F is the period-clock frequency, and T is the signal period. Scaling either K or F changes the displayed result accordingly and provides an easy way to change the units of the displayed answer. □