Counter delivers data in signed or complemented form

by N. Bhaskara Rao
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Adding one chip to the basic digital-averaging circuit proposed by Frazier [*Electronics*, Nov. 9, 1978, p. 114] forms a data counter whose outputs express a negative number not only by its magnitude and sign, but by its 2's complement as well. Expressing numbers in the latter form enhances the circuit's usefulness by allowing direct interfacing with computer circuits.

The circuit shown works differently from Frazier's, which generates a sign bit and reverses the direction of the count when the counter is about to move down through zero. Instead, the 74193 is allowed to go below zero, where its R output becomes 15 and the state of its borrow output changes, thereby clocking the 7470 flip-flop. The 7470's Q output, which is the sign bit, S, then moves high.

The sign bit and the R bits are applied to the 7483 4-bit full adder (not part of the original circuit) through the 7486 exclusive-OR gates. The 7483 and 7486 together form an add-or-subtract unit. As a result, the output of the adder, M, will be equal to R if the 74193 indicates it holds a positive count (S = 0), and will be equal to 16 − R if the 74193 has gone negative (S = 1).

If S = 0, the R bits, as seen at the output of the 74193, will represent the binary equivalent of the number. Any negative number will be represented by its 2's complement value and an enabled borrow bit. □

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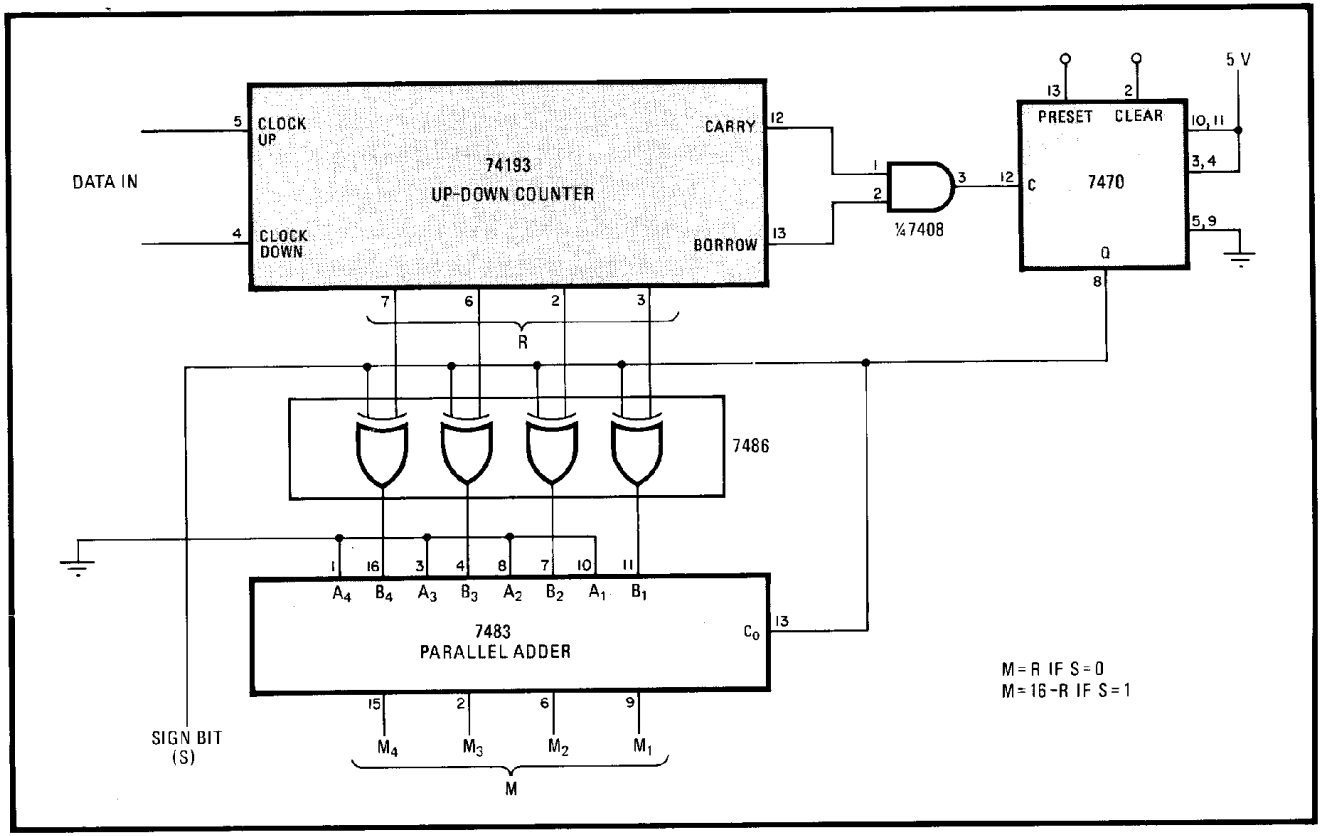


Number forms. Availability of any number in both binary equivalent or magnitude-sign forms enhance circuit's interfacing capability. Data generated by 74193, expressed as binary number (R bits), is converted into magnitude-sign form by add-or-subtract unit 7483–7486. R represents the 2's complement of any negative number when counter steps down through zero.

Industrial counter handles widely varying intervals

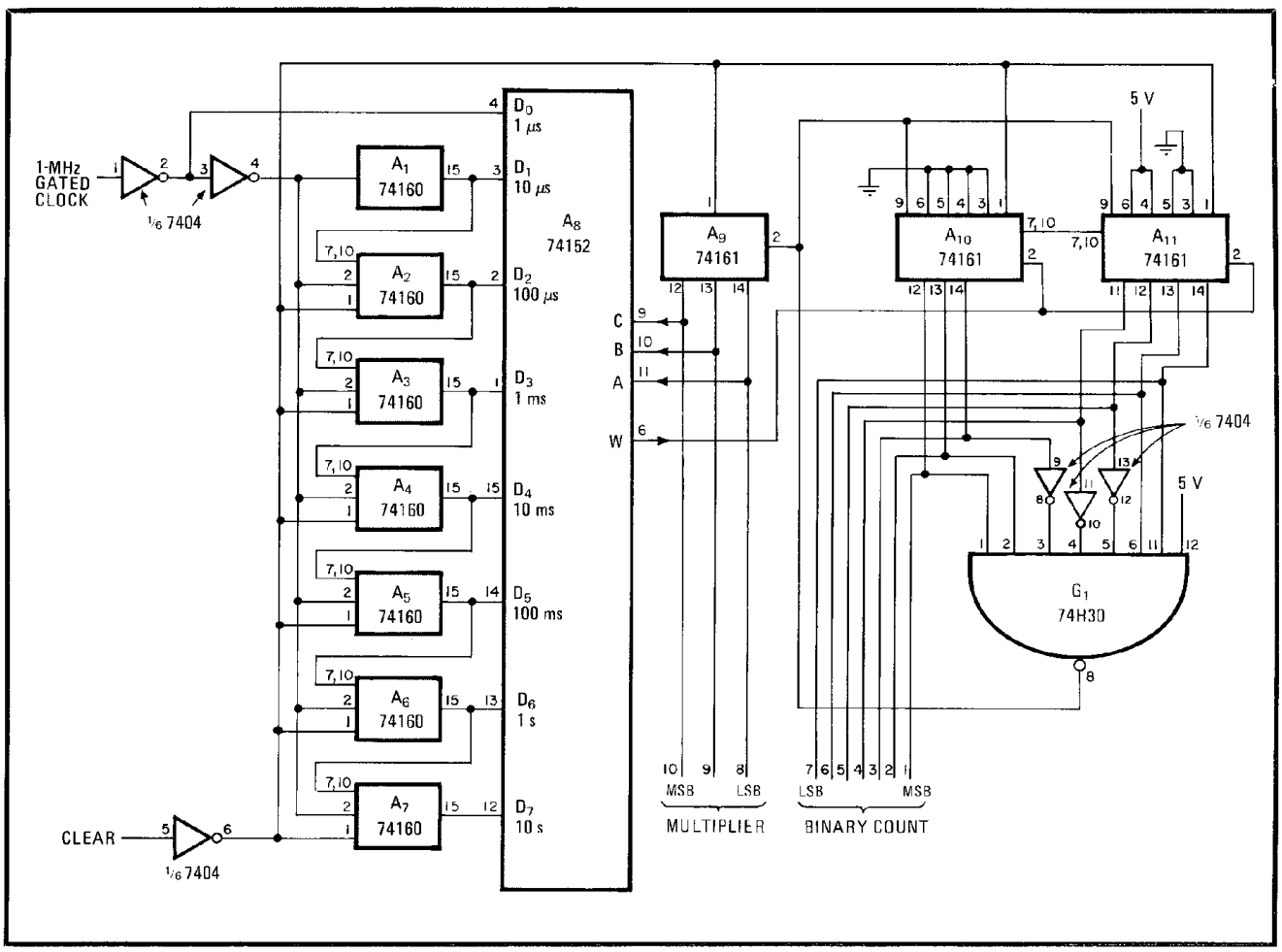
by Rudolf E. Six
The Detroit News, Electronics Department, Detroit, Mich.

The time intervals between consecutive events in industrial processes can often vary over several decades, creating a problem if their values are to be stored in a microprocessor-based system. Normally, a great many input/output ports would be needed to handle, say, the 24 significant bits needed to represent a 10-second interval measured with a 1-megahertz clock. But this counter requires only 10 output lines to represent intervals ranging from 1 microsecond to 10 seconds, making it easy for a 16-bit data system to process a 24-bit binary number.

Wiring a set of 4-bit counters, A_1–A_7, as a one-decade divider is what makes it possible for fewer lines to be used. At the start of a measurement, a string of 74160 counters immediately begin to divide down a gated 1-MHz clock signal into seven decades of time ranging from 1 microsecond to 10 seconds in duration, as shown. The outputs of A_1–A_7 are then presented to A_8, the 74152 eight-to-one multiplexer.

A_{10} and A_{11}, two 74161 binary counters, are incremented once each microsecond until their combined count reaches 99. G_1 moves low at this time. On count 100, G_1 moves high and presets A_{10}–A_{11} to a count of 10, and steps the multiplier counter A_9. A_9 enables A_8 to advance to the next decade position (D_i to D_{i+1}). A_{10}–A_{11} now counts at one tenth of the rate it did before A_8 was stepped to D_{i+1}.

The process continues until such time that the measurement interval is terminated. On the seven binary-count lines will be a binary-equivalent number that is



Line reduction. Counter that measures time interval between two events over a range of 1 microsecond to 10 seconds needs only 10 output lines to display the results and store them in a microprocessor-based system. System resolution is adequate for most applications but may be increased if an extra 74161 is cascaded with the A_{10}–A_{11} counter, at a cost of three more output lines.

related to the number of pulses in the gated clock signal. The actual (decimal-point) magnitude in microseconds, milliseconds, etc., is determined by the remaining three multiplier output lines, which indicate the decade value (D_0–D_7) as a three-bit binary number.

For example, an output of 01010001 on the binary lines combined with an output of 001 on the multiplier lines indicates a time interval of 810 μs between two events. After the computer has stored the information, a clear signal resets all the counters.

The resolution of the system (1 μs at the low edge, 10 s at the high end) is adequate for most applications, but it may be improved if an additional 74161 counter is cascaded to the A_{10}–A_{11} circuit. This extension will increase system accuracy by 1 bit, but then three additional output lines will be required. □

Eight-port counter handles coinciding input pulses

by Gary Steinbaugh
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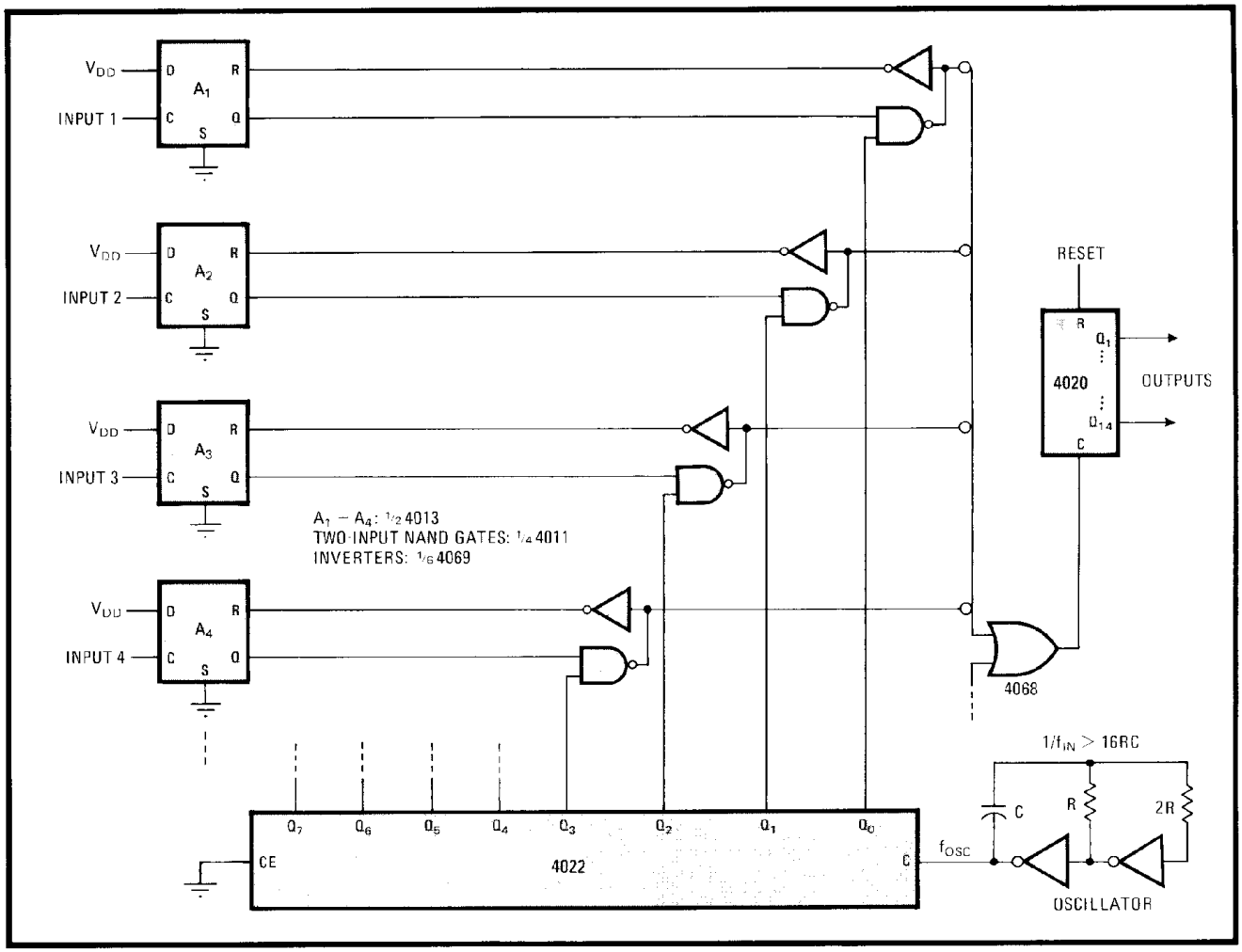
In applications where an asynchronous counter is driven by more than one input source, there is always the possibility that pulses will arrive simultaneously, causing an incorrect count. This circuit overcomes the problem by latching all input pulses as they occur and multiplexing the latch outputs so that the pulses may be applied to the counter one at a time.

As shown in the figure, four 4013 dual latches and their associated gates, in conjunction with a clocked 4022 Johnson counter, drive the 4020 ripple-carry binary device that is used to accumulate a count. (In the interests of space, the identical circuitry of A_5–A_8 and their gates is not shown.) One eight-input NAND gate, the 4068, is used to clock the 4020.

A_1–A_4 will latch on the rising edge of any pulse that appears at their respective inputs. The 4022, driven by an oscillator, scans the contents of each flip-flop; if the output of the flip-flop scanned is at logic 1, a pulse appears at the output of the 4068 and the 4020 is advanced. At the same time, the flip-flop is reset.

The counter may be configured for any number of inputs. Note that the frequency of the oscillator driving the Johnson counter must be high enough to permit each flip-flop to be reset before it is set by a following input pulse; otherwise, the event will not be recorded. For an n-input counter, $f_{in} < nf_{osc}$, where f_{in} is the highest input frequency expected (the reciprocal of the time between any two pulses at a given input) and f_{osc} is the frequency of the oscillator. □



Serial stepping. This multiplexer circuit avoids the difficulties associated with multi-input counters that are called upon to handle simultaneously occurring pulses. The clocked 4022 Johnson counter, driven by a simple RC oscillator, scans each flip-flop so that input pulses previously latched are applied one by one to 4020 accumulator. The counter can be easily configured for any number of inputs.

Up-down counter measures cumulative frequency error

by A. M. Downing
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Determining the cumulative error, in cycles, between the frequency of a test signal and that of a secondary standard, this simple circuit is particularly useful in monitoring the short-term stability of a power-line generator versus a quartz-crystal reference. The sign of the error (plus if greater than the reference frequency, minus if less) is also displayed.

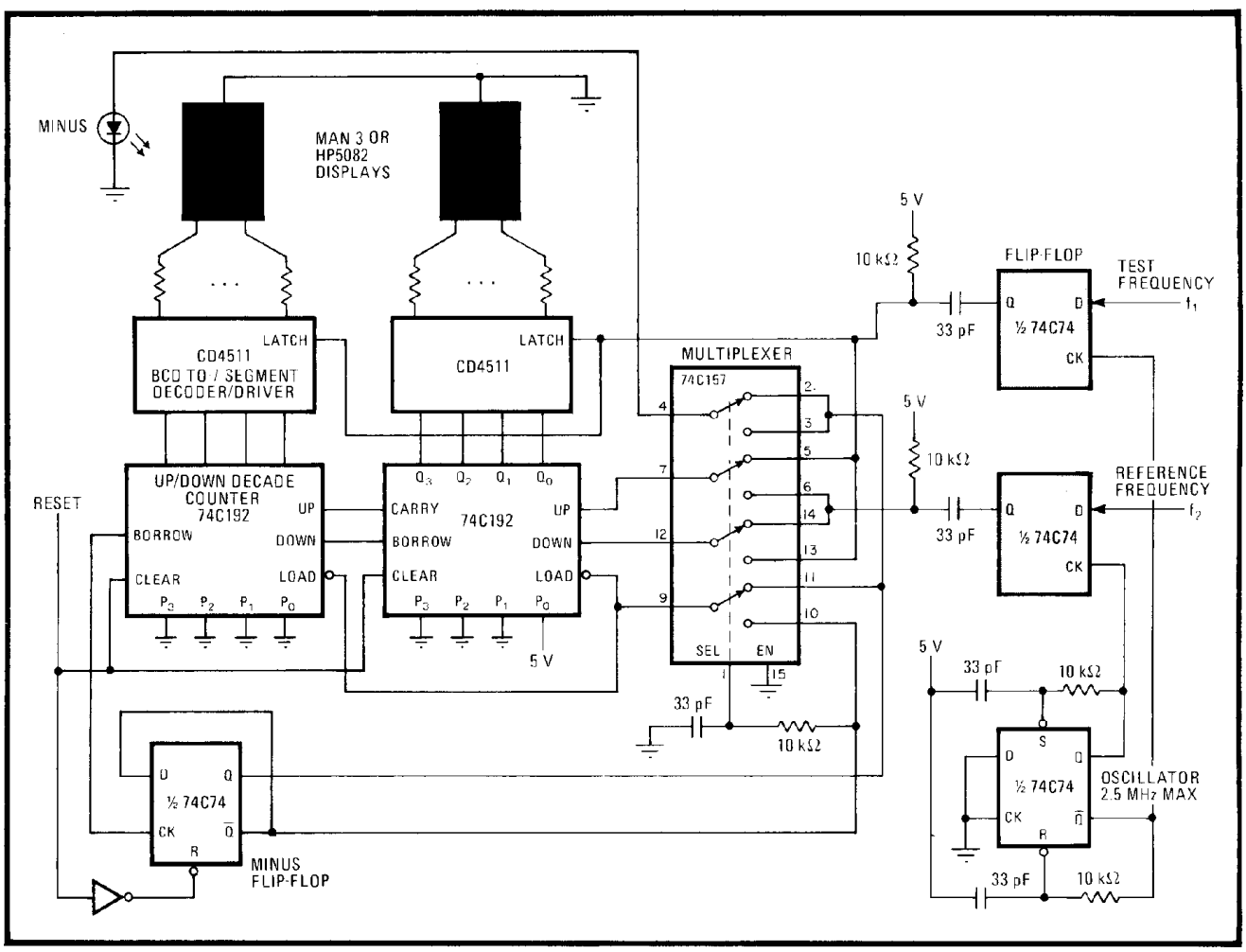
Two counter chains are usually required to compare the corresponding frequencies, and often a third chain is needed to accumulate the error count. Here a single up-down counter provides both functions, simplifying the circuit and cutting cost.

Signals f_1 and f_2 are initially synchronized by the 74C74 flip-flops at the input, which are clocked out of phase by a high-speed oscillator. The output of each signal-path flip-flop is therefore always separated by at least one half cycle of the oscillator frequency, depending on the actual frequencies of f_1 and f_2.

The Q output of the flip-flop associated with f_1 drives the up port of the two-stage 74C192 up-down counter via a two-channel multiplexer. Similarly, the f_2 flip-flop drives the down input of the 74C192. Thus, if $f_1 = f_2$, the 74C192 alternately counts up from zero to some value in a given sampling period, then decrements back to zero. Therefore the display—which is latched at the beginning of the next sampling period so that a correct value is rendered without flicker—indicates a zero count.

If f_1 is greater than f_2, the counter does not return to zero and the display will indicate a positive value. In the opposite case, that is, for f_1 less than f_2, the counter generates a borrow signal as it attempts to go below zero and thence to 99. In that event, the minus flip-flop is toggled so that the multiplexer is switched to its remaining channel. Thereafter, the f_1 flip-flop drives the counter's down port and the f_2 flip-flop drives the up input. Simultaneously, a counter-load pulse is generated, and the counter proceeds to count up from one, but with the minus light-emitting diode activated.

Should the count go below zero in a subsequent cycle, a borrow pulse is again generated and the multiplexer switched back to its initial channel. The LED is thus turned off, indicating a positive count. □



Accumulation. Single-chain counter finds the cumulative error, in cycles, between the test and reference frequencies. Signals f_1 and f_2 increment or decrement the counter, respectively, over a given sampling period; the result in the counter at that time represents the magnitude of the error. The light-emitting diode indicates the polarity of the differential count with respect to the reference.

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Designer's casebook

TTL decade counter divides pulse train by any integer

by T. Durgavich and D. Abrams
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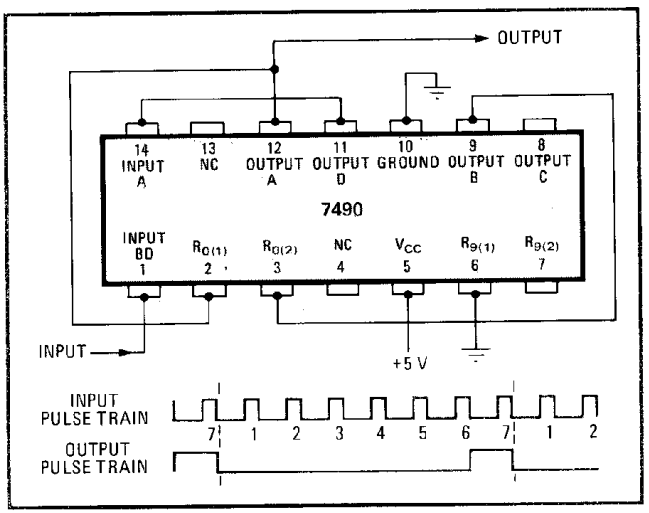
In many applications a pulse train must be divided by a fixed integer. For example, digital clocks often divide the line frequency by 60 to obtain a 1-hertz output, and time-base generators divide a crystal oscillator frequency down to several stable low-frequency outputs. If the integer is 10 or less, just one 7490 TTL decade-counter can handle the division.

Usually frequency division in TTL circuits is accomplished by using binary counters and logic gates. To divide by N—i.e., to get one output pulse for every N input pulses—the logic gates are connected so that the counter is reset when the N^{th} pulse is counted. The most significant bit is used as the output, because it makes the high-to-low clocking transition only once for every N input pulses. If it is necessary to have an output pulse of a specific length, then a monostable may be triggered when the N^{th} pulse is detected.

The disadvantage of this division technique is that, even for divisors less than 10, two ICs are required—a binary counter and a gate. But a pulse train can be divided by any integer between 2 and 10 by use of just one 7490 TTL decade-counter IC, owing partly to its divide-by-2 and divide-by-5 stages and partly to its internal ANDed reset, which lets it reset only when both pin 2 and pin 3 are high.

The counter can be made to reset on any count from 2 to 10 by appropriate connections of the pins. The necessary interconnections for each value of N are shown in the table.

For example, if division by 7 is desired, the 7490 is wired as shown in the figure. The input and output pulse trains for this configuration are also shown. If a larger division is required, it's only necessary to cascade several stages together, provided the divisor has factors that are all less than 10. □



Divide-by-7 circuit. A 7490 TTL decade-counter integrated circuit, when connected as shown here, produces one output pulse for every seven input pulses. Because the divide-by-2 stage follows the divide-by-5 stage, the seventh count is a non-BCD code and can be detected by the internal two-input NAND gate to reset the counter. Other connections permit division by any other integer up to 10.

OPERATION OF 7490 IC AS A DIVIDE-BY-N COUNTER

DIVISOR N	INPUT PIN NO.	OUTPUT PIN NO.	EXTERNAL CONNECTIONS
2	14	12	PIN 2 OR 3 LOW
3	1	8	PIN 8 TO PIN 2 PIN 9 TO PIN 3
4	1	8	PIN 11 TO PINS 2 AND 3
5	1	11	PIN 2 OR 3 LOW
6	14	8	PIN 12 TO PIN 1 PIN 9 TO PIN 2 PIN 8 TO PIN 3
7	1	12	PIN 11 TO PIN 14 PIN 12 TO PIN 2 PIN 9 TO PIN 3
8	14	8	PIN 12 TO PIN 1 PIN 11 TO PINS 2 AND 3
9	14	11	PIN 12 TO PINS 1 AND 2 PIN 11 TO PIN 3
10	14	11	PIN 12 TO PIN 1 PIN 2 OR 3 LOW