DOWN-COUNTER COOKBOOK

Presettable down-counters do more than you think.

RAY MARSTON

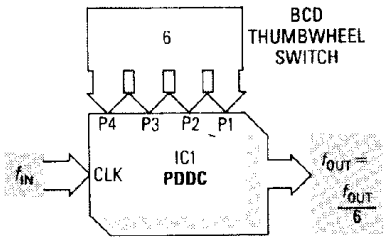


FIG. 1—A PROGRAMMABLE DECADE down-counter (PDDC) can count/divide by any BCD number fed into its PRESET pins.

LET'S EXAMINE PRESETTABLE DOWN-counters; how to design frequency dividers, frequency synthesizers, and alpha-numeric displays.

Jam inputs

By feeding a binary number into their PRESET pins—often called JAM pins—those counter IC's can be externally programmed to divide-by any binary number: either *B*inary *C*oded *D*ecimal (BCD), or straight binary form. For example, Fig. 1 shows a *P*rogrammable *D*ecade *D*own *C*ounter (PDDC) having a BCD code fed into its PRESET inputs via a thumbwheel switch.

The unique feature of the PDDC is known as *programmable cascadability*. As shown in Fig. 2, the *hundreds* counter is set to divide-by-2, the *tens* counter is set to divide-by-6, and the *units* counter is set to divide-by-3, which has an overall division ratio of 200 + 60 + 3, or 263. On the other hand, Fig. 3 shows that when conventional counters are cascaded with the same division ratios they would, of course, have a resultant of 200 × 60 × 3, or 36,000. We see that the presettable-types output the sum of the division ratios, while the conventional-types output the product of the division ratios.

Practical PDDC's can be programmed by a variety of methods. The two most common are electromechanical programming via thumbwheel switches, and there's electronic programming via microprocessor control.

Preset truth table

Figure 4-*a* shows a PDDC 4-stage synchronous down-counter, which shifts down one count for each positive transition of the CLOCK signal. Note however, as shown in Fig. 4-*b*, that when the down count reaches BCD 0 (ØØØØ), the next arriving clock pulse causes the counter to jump to BCD 9 (1ØØ1).

Other features of the PDDC include the following: The CLOCK signal can be disabled by a high level on the INHIBIT control. A decoded ZERO OUTPUT goes high only when the Q4-Q1 outputs are in the ØØØØ state. Also, by applying a high level to the LOAD pin, the counters are forced to take up the BCD states of the PRESET inputs.

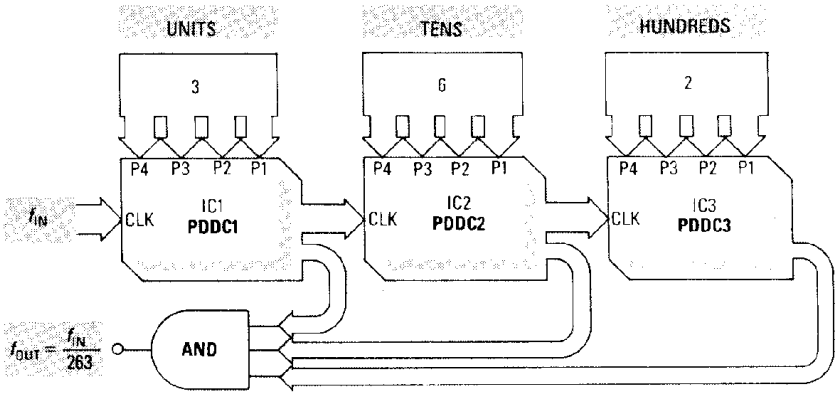


FIG. 2—PDDC's HAVE *PROGRAMMABLE CASCADABILITY*; the output is equal to the sum of the individual division ratios.

Programmable down-counter

Figure 5 shows a PDDC hookup that will count down from a BCD number loaded into the PRESET pins, by depressing the *start* button. For example, suppose the BCD number 6 (Ø11Ø) is loaded via the *start* button. On the arrival of each CLOCK pulse, the IC counts down one step, going through the numbers 5, 4, 3, 2, 1 and, finally, on the arrival of the 6th pulse, to 0, at which point the ZERO OUTPUT pin goes high. That logical high is fed back to the INHIBIT pin, causing all further CLOCK pulses to be ignored. The count sequence is now completed, but can be restarted only by depressing the *start* button once again.

Figure 6 shows how two PDDC's can be cascaded to make a down-counter having a count of 26. Notice that the ZERO OUTPUTS of both IC's are inputs to a logical AND gate that triggers the INHIBIT control of PDDC1. Also, the CLOCK signal of PDDC2 comes from the Q4 output of PDDC1. When the *start* button is depressed, counting action of the circuit is as follows: The BCD number 2 (ØØ1Ø) is loaded into the *tens* counter; the BCD number 6 (Ø11Ø) is loaded into the *units* counter; after which, the CLOCK input signal is initiated. PDDC1 counts down from 6 to 0 through the first six clock pulses. But then, because both IC's ZERO OUTPUTS are not high, PDDC1 is not inhibited. Instead, it starts acting as a divide-by-10

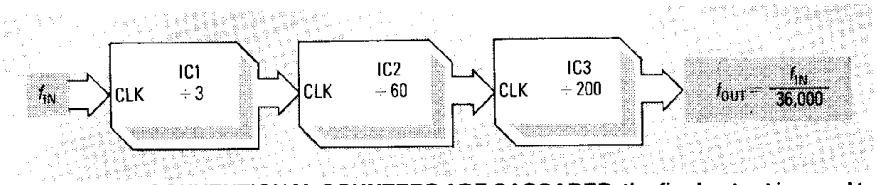
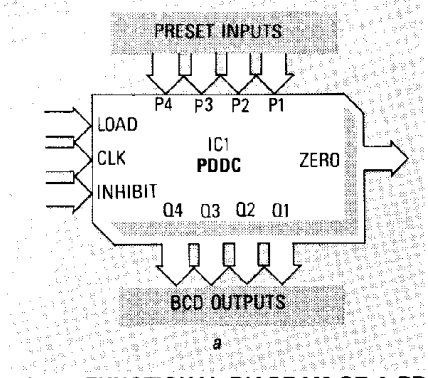


FIG. 3—WHEN CONVENTIONAL COUNTERS ARE CASCADED, the final output is equal to the product of the individual division ratios.



COUNT SEQUENCE	Q4	Q3	Q2	Q1	BCD NUMBER
▶n+1	1	0	0	1	9
n+2	1	0	0	0	8
n+3	0	1	1	1	7
n+4	0	1	1	0	6
n+5	0	1	0	1	5
n+6	0	1	0	0	4
n+7	0	0	1	1	3
n+8	0	0	1	0	2
n+9	0	0	0	1	1
n	0	0	0	0	0

b

FIG. 4—FUNCTIONAL DIAGRAM OF A PDDC. A 4-stage synchronous down counter is shown in (*a*), together with its truth table shown in (*b*).

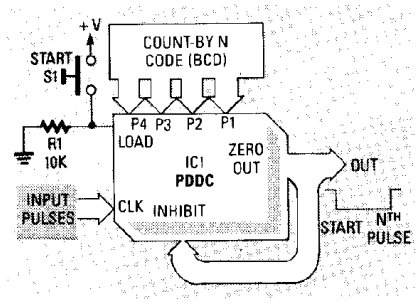


FIG. 5—PDDC CONNECTED AS a programmable down-counter.

counter, and counts down from BCD number 9 (code 1ØØ1) on the arrival of the 7th pulse, simultaneously sending a single CLOCK pulse to PDDC2 as Q4 output switches high. Ten pulses later (on the 17th pulse), PDDC1 sends another CLOCK pulse to PDDC2, causing its ZERO OUTPUT to go high. Nine pulses later (on the 26th pulse), the ZERO OUTPUT of PDDC1 also goes high, at which time the output of the AND gate goes high, inhibiting further counting action.

Figure 7 shows how to connect a single PDDC as a programmable timer. The output goes high as soon as the *start* button is depressed, but goes low again after a programmed amount of time. The circuit is the same as Fig. 5, except that the final output is inverted, and the CLOCK signal is taken from a fixed time-reference source (1 pulse/second). Looking back, Fig. 6 can also be made to act as a programmable timer by similarly inverting its final output, and taking the CLOCK signal from a fixed time-reference source.

Frequency division

Figure 8 shows how to connect a PDDC as a programmable frequency-divider. The divide-by-N code is fed to the PRESET pins. The output of the counter is taken from the ZERO OUTPUT pin, and is coupled back to the LOAD pin. Suppose the starting BCD number 4 (Ø1ØØ) has been loaded into the counter. On the arrival of the 1st CLOCK pulse, the counter decrements to 3, on the 2nd pulse to 2, on the 3rd pulse to 1, and on the 4th pulse to 0. At which point, the ZERO OUTPUT goes high, and that loads the BCD number 4 (Ø1ØØ) back into the counters. Now the whole sequence starts over again, and the ZERO OUTPUT switches back low. Thus, the counter repeatedly counts by the number set on the PRESET inputs, and the output (from the ZERO OUTPUT pin) takes the form of a narrow pulse only a few hundred nanoseconds wide.

Figure 9 shows a PDDC connected as a simple divide-by-10 counter/divider. The LOAD pin is grounded, so the PRESET codes have no effect and the counter repeatedly cycles through its basic BCD count from 9 to 0, and then back to 9 again, and so on. The output is taken from the ZERO OUTPUT

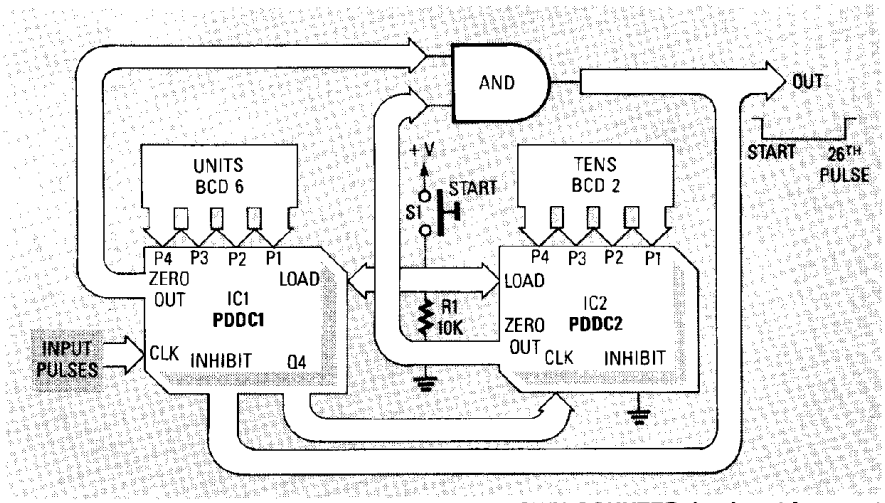


FIG. 6—TWO-IC (CASCADED) PROGRAMMABLE DOWN-COUNTER that is set for count 26 operation.

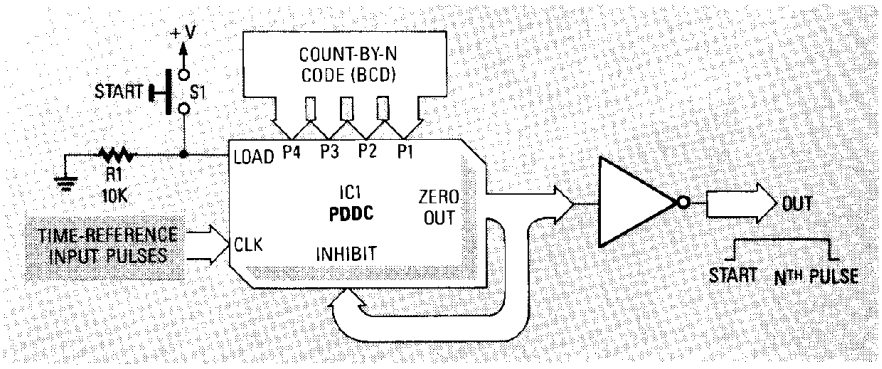


FIG. 7—PDDC CONNECTED AS A programmable timer.

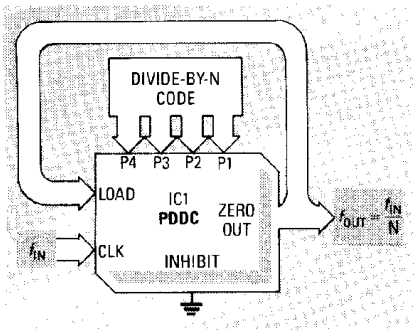


FIG. 8—PDDC CONNECTED AS A PROgrammable frequency-divider. The PDDC counts down to 0000 from the PRESET inputs—the ZERO OUTPUT pin is a narrow pulse of a few nanoseconds.

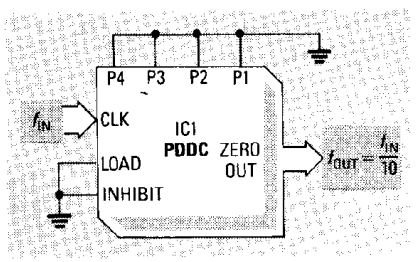


FIG. 9—PDDC CONNECTED AS A decade frequency-divider. The LOAD pin is grounded, so the PRESET pins have no effect on the circuit, consequently, the counter cycles through its basic decade count, from 9 to 0.

pin, which remains low until the all-zero count, when it pulses high for a few nanoseconds.

Figure 10 shows how to cascade two PDDC's to make a programmable frequency-divider. The ZERO OUTPUTS of the two counters are inputted to an AND gate to provide the LOAD action, and the CLOCK signal of PDDC2 is derived from the Q4 output of PDDC1. For example, assume that at the start of the count cycle the BCD number 24 (0010,0100) is loaded into the counters. For the first few counts, PDDC1 counts down from 4 to 0, and then the ZERO OUTPUT goes high. However, because PDDC2's ZERO OUTPUT is low, the AND gate's output does not go high; that would reload the counters. But instead, PDDC1 reverts to the normal divide-by-10 mode, jumping to the 9 state, simultaneously feeding a clock pulse to PDDC2 as Q4 output switches high. That action continues until the arrival of the 24th pulse, when the ZERO OUTPUTS of both IC's go high together. At that time, the output of the logical AND gate goes high (for a few nanoseconds), and reloads the BCD number 24 back into the counters. The whole sequence then starts over again.

Frequency synthesis

The main application of programmable frequency-dividers, as shown in Fig. 11, is in frequency synthesizers when used in conjunction with a (PLL) *P*hase *L*ocked *L*oop. Notice that the output of a *V*oltage *C*ontrolled *O*scillator (VCO) is fed, via the programmable divide-by-N counter, to one input of a phase detector. The other phase-detector input is taken from a (fixed frequency) crystal-controlled reference generator. The phase detector produces an output voltage proportional to the difference between the two input frequencies. That voltage is filtered into a DC voltage, and fed to the VCO's control input that automatically adjusts the VCO's frequency. When the output of the divide-by-counter is the same as the reference generator, the PLL is said to be locked.

Notice that in Fig. 11, the output frequency of the VCO is N-times the value of the frequency reaching the input of the phase detector. Consequently, when the PLL is locked, the output frequency of the VCO is equal to N-times the reference frequency; for example, if N = 236, and the reference frequency = 1 kHz, then the VCO frequency output equals 236 kHz, and also has crystal accuracy.

4522B/4526B down counters

The best-known family of CMOS programmable (cascadable) down-counters is shown in Fig. 12; it is composed of the 4522B (decimal) and the 4526B (binary) 4-bit IC's, which both have the same pinout. Those IC's are almost identical to Fig. 4, except that the counters can be synchronously set to the zero state by forcing the MR (master reset) pin high. The AND gate is built into the ZERO OUTPUT line, so the ZERO OUTPUT can only go high if the CF (cascade feedback) pin is also high; that enables cascading without external gates.

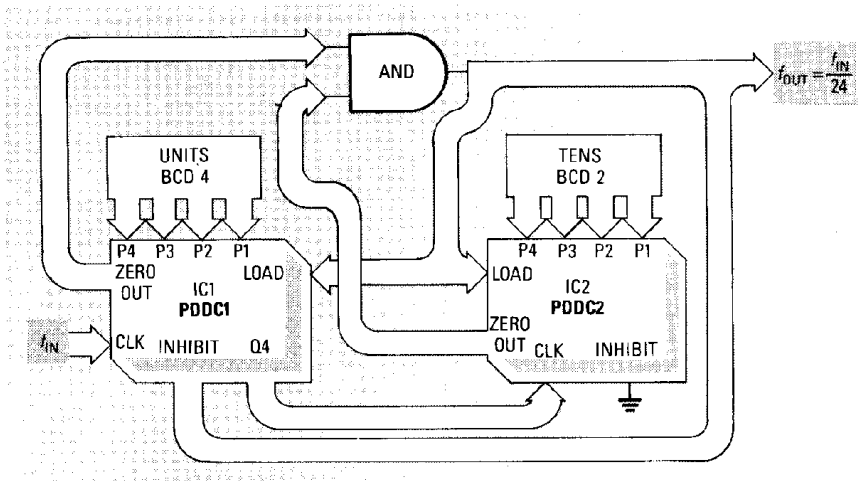


FIG. 10—TWO-IC (CASCADED) PROGRAMMABLE FREQUENCY-DIVIDER, set for divide-by-24 operation.

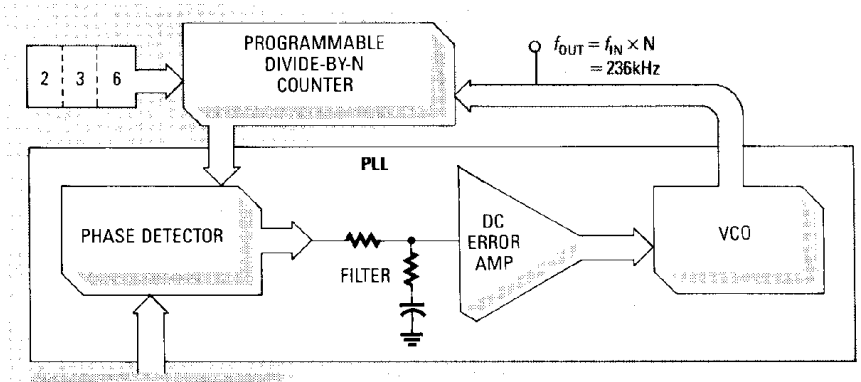


FIG. 11—A PROGRAMMABLE FREQUENCY-SYNTHESIZER can be constructed using a divide-by-N counter in conjunction with a PLL.

The 4522B and 4526B can be used in the same ways as the counters shown in Figs. 5 to 11, except that the MR pin is normally grounded, and the AND gate is built into the IC. When those IC's are used alone, the CF pin must be tied high to enable the ZERO OUTPUT. When cascading two or more IC's, tie the ZERO OUTPUT of the *M*ost *S*ignificant *D*igit (MSD) IC to the CF pin of the IC that is used for the next most significant digit, repeating the process until the *L*east *S*ignificant *D*igit (LSD) IC is reached. Figure 13 shows the hookup for making a 2-stage programmable down-counter, and Fig. 14 shows the connections for a 2-stage programmable frequency-divider.

When using those IC's, notice that all unused inputs, including PRESETS, must be tied high or low, as appropriate. Also, the outputs of all internal counter stages are available through the Q output pins, enabling the counter states to be decoded by using external circuitry.

40102B/40103B down counters

Each IC in the 40102B and 40103B family of devices (see Fig. 15-*a*) effectively act as a pair of presettable 4-bit down counters, cascaded in a single package. The ZERO OUTPUT that goes low under the zero-count condition is the only externally available counting signal. That's in contrast to the Q outputs typically available on other counter IC's. The truth table in Fig. 15-*b* is common to both IC's. The 40102B is a 2-decade BCD down-counter, while the 40103B IC is an 8-bit (or two 4-bit words) binary counter. Both types of counters clock down on the positive transition of the CLOCK signal.

Codes that are applied to the eight

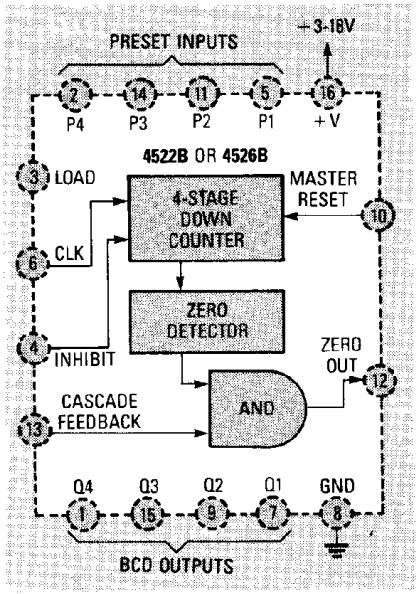


FIG. 12—THE 4522B (DECADE), AND 4526B (BINARY) programmable down-counters. Those are the same as the PDDC counters except that the AND gate that's used when cascading IC's is integrated into the IC.

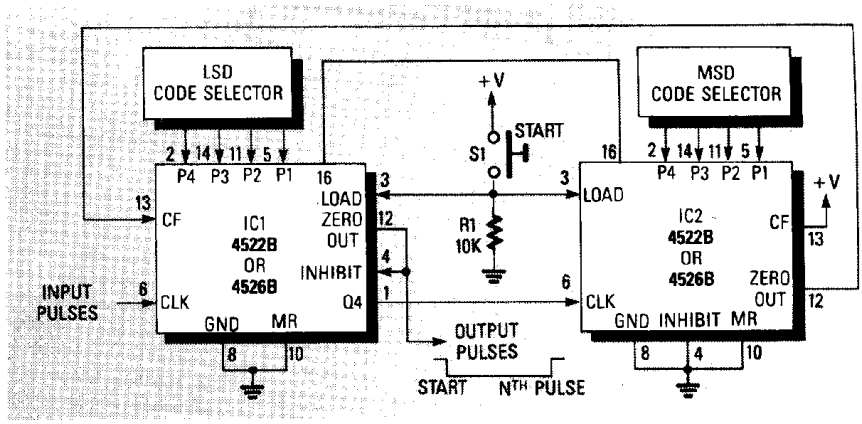


FIG. 13—TWO-IC (CASCADED) PROGRAMMABLE DOWN-COUNTER using the 4522B or 4526B.

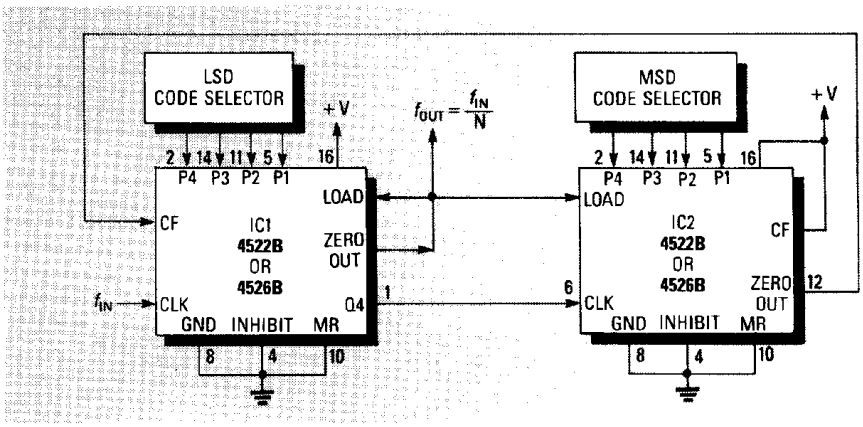
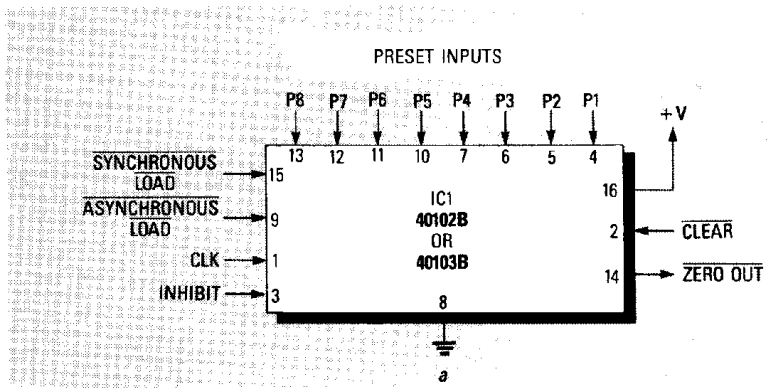


FIG. 14—TWO-IC (CASCADED) PROGRAMMABLE FREQUENCY-DIVIDER using the 4522B or 4526B.



CONTROL INPUTS				LOAD MODE	ACTION
CLR	AL	SL	INH		
1	1	1	1	SYNC	INHIBITS COUNTER
1	1	1	0	SYNC	COUNT DOWN
1	1	0	X	SYNC	LOAD ON NEXT CLK PULSE
1	0	X	X	ASYNC	LOAD ASYNCHRONOUSLY
0	X	X	X	ASYNC	CLEAR TO MAXIMUM COUNT

b

FIG. 15—FUNCTIONAL DIAGRAM *(a)* AND TRUTH TABLE *(b)* of the 40102B dual-decade and 40103B 8-bit binary down-counters.

PRESET pins of those IC's can be loaded asynchronously by pulling the $\overline{AL}$ pin low, or synchronously on the arrival of the next CLOCK pulse by pulling the $\overline{SL}$ pin low. When the $\overline{CLR}$ input is pulled low, the counter asynchronously clears to its maximum count. When the INH control is pulled high, it inhibits both the CLOCK counting action, and the ZERO OUTPUT action. The INH control thereby acts as a CARRY-IN pin for cascading counter IC applications.

Figures 16 to 19 show four ways of using that family of presettable down-counters. Figure 16 shows the connection for making a programmable 8-bit, or 2-word timer, or down-counter. Figure 17 shows the circuit of a programmable frequency-divider that has divide-by-(N + 1) operation. Its ZERO OUTPUT going low for one full clock cycle under the zero-count condition. True divide-by-N operation can be obtained by tying $\overline{SL}$ high and connecting ZERO OUTPUT to $\overline{AL}$; the output pulses will have widths of only a few hundred nanoseconds.

Finally, Figs. 18 and 19 show the basic connections that are used to cascade 40102B or 40103B stages in large-word programmable applications. Figure 18 shows the counter hookup for the fully synchronous clocking that's needed when used for high-speed applications.

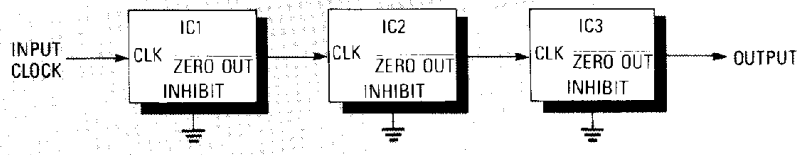


FIG. 18—METHOD OF RIPPLE CASCADING 40102B or 40103B counters.

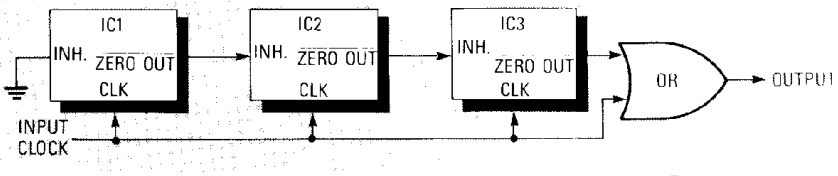


FIG. 19—METHOD OF SYNCHRONOUS CASCADING 40102B or 40103B counters.

Decoders

Most of the counter/dividers that we've looked at have 4-bit coded outputs, which take the standard code forms shown in Fig. 20-*a*. Thus, when the counters are in the BCD-5 state, they have an output code of Ø1Ø1. When in the BCD-7 state, they have an output code of Ø111 (read with Q4 to the left). Individual output states of the counters can easily be decoded and used for driving external display units or control lines, by using the basic logic technique shown in Figs. 20-*b* and 20-*c*. The decoder outputs that are high (logic-1) in the desired code state are fed directly to the inputs of a 4-input AND gate, and those that are low are fed through an inverter. If BCD numbers are to be decoded, and the numbers fall between 2 and 7 inclusive, the Q4 code can be ignored, and a 3-input AND gate can be used.

If more than three code states are to be decoded, it's economical to use dedicated CMOS decoder IC's, such as the 4028B, 4514B or 4515B. The 4028B in Fig. 21 is a 4-bit BCD-to-Decimal decoder that has direct decoding of the ten possible input BCD numbers 0 to 9 inclusive. Only one of the ten decoded outputs will go high with the remaining outputs low. The 4514B and 4515B in Fig. 22 are full 4-bit binary decoders having an individual output for each of the sixteen possible code numbers. The 4514 has *active high* outputs; that means that all outputs are low except the decoded line, which is high. The 4515B has *active low* outputs. Those IC's are considerably more sophisticated than the 4028B type, and they have their FOLLOW/$\overline{\text{LATCH}}$ control on pin-1, and they have a DECODE INHIBIT control on pin-23.

When the DECODE INHIBIT pin is brought high, all decoding functions are disabled; it drives all outputs low in the 4514B, or all outputs high in the 4515B, irrespective of the states of all other pins. When the FOLLOW/$\overline{\text{LATCH}}$ pin is high, the IC's act as straight decoders; but when the pin is pulled low, it latches the prevailing input code into memory and retains it, irrespective of the subsequent states of the input code.

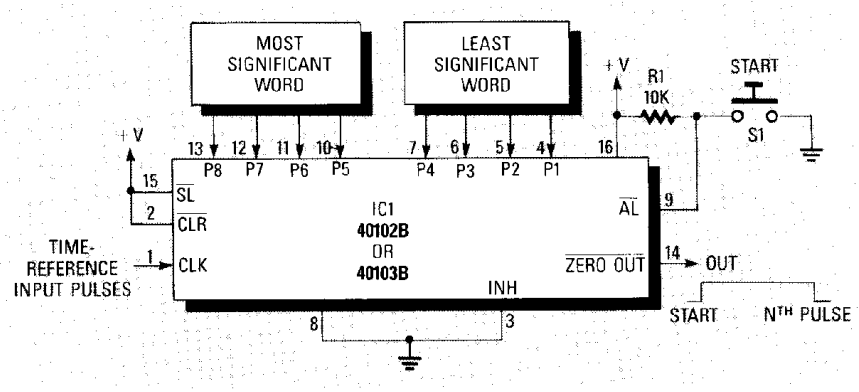


FIG. 16—PROGRAMMABLE TIMER using a 40102B or 40103B.

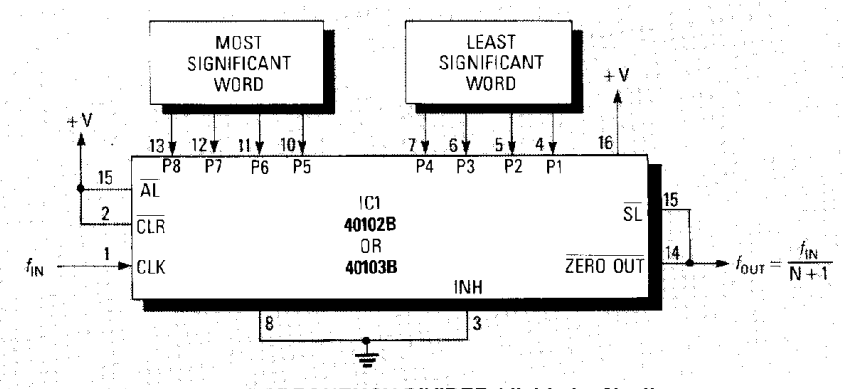


FIG. 17—PROGRAMMABLE FREQUENCY DIVIDER (divide-by-N + 1).

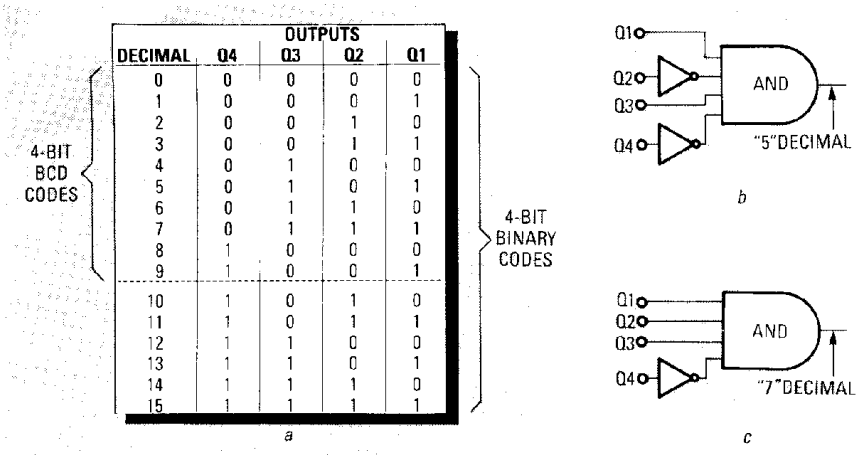


FIG. 20—THE CODED Q4-Q1 OUTPUTS of a 4-bit counter are shown in *(a)*, while *(b)* and *(c)* show how to decode the numbers 5 and 7, respectively.

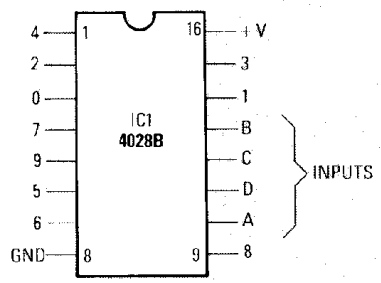


FIG. 21—PINOUT OF THE 4028B bcd-to-decimal (1-of-10) decoder.

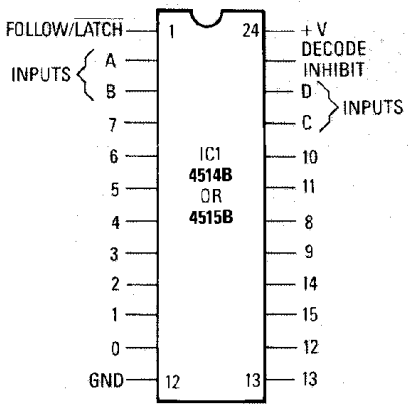
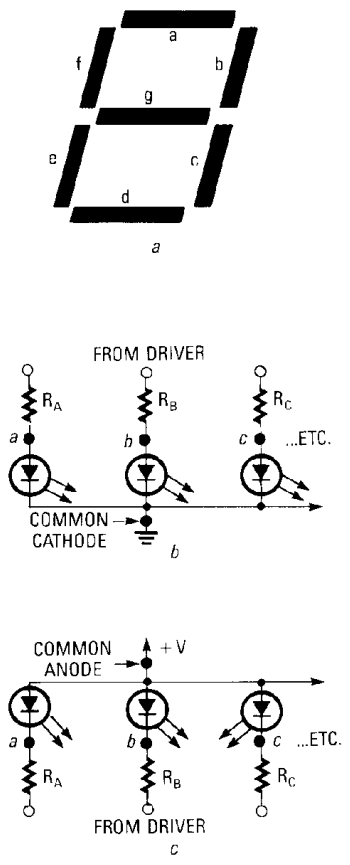


FIG. 22—PINOUT OF THE 4-BIT BINARY (1-of-16) decoders, the 4514B (active-high output) and the 4515B (active-low output).

BCD-to-7-segment decoder

The BCD outputs of decade counters can easily be decoded and used to drive 7-segment (*l*ight *E*mitting *D*iodes) LED's, or (*L*iquid *C*rystal *D*isplays) LCD's, by using suitable decoder/driver IC's. The 7-segment displays have the standard format and pin notations shown in Fig. 23-*a*, with each LED segment having its own individual pin. LED 7-segment displays are available in either common-cathode form shown in Fig. 23-*b*, or common-anode form shown in Fig. 23-*c*. Common-cathode types must be driven by IC's that can source significant current, while common-anode types must be activated by devices that can sink a significant amount of current. Notice that a current-limiting resistor must be wired in series with each LED segment.



IG. 23—THE 7-SEGMENT LED (OR LCD) DISPLAYS have the standard segment format shown in *(a)*. The LED types are available as either common-cathode *(b)*, or commom-anode *(c)* types.

The most popular CMOS IC for driving 7-segment LED displays is the 4511B BCD-to-7-segment decoder/LED-driver, shown in Fig. 24. That IC is ideally suited for driving common-cathode displays because its outputs can each source up to 25 milliamperes of current.

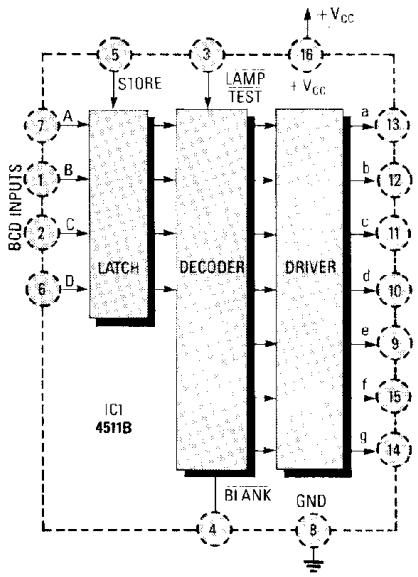


FIG. 24—THE 4511B BCD-TO-7-SEGMENT Latch/Decoder/LED-Driver. This single IC has the combined capability of a 4-bit data latch, a BCD-to-7-segment decoder, and a transistor-driver output for LED displays.

The 5411B is an easy IC to use. It has 4 pins as a BCD input, an output driving pin for each of the seven LED segments, and only three input control pins. The $\overline{\text{LAMP TEST}}$ input pin is normally tied high; when pulled low, it turns on all seven segments of the display, irrespective of the input code. The $\overline{\text{BLANK}}$ input pin is also normally tied high; when pulled low, it turns off all display segments, irrespective of the input code. The STORE control enables the IC to have either transparent or latched decoder operation. When STORE is low, the IC has transparent decoding of the BCD inputs. When STORE is switched high, the BCD input that is present at the moment of switching is latched into an internal memory and then decoded. That BCD number is held as long as STORE remains high.

7-segment LCD drivers

The 7-segment LCD's (*L*iquid *C*rystal *D*isplays) have the same format as LED types, except that their common pin is known as the *back-*

plane (BP). LCD's must be driven by AC signals that have virtually no DC components. In practice, the AC signal takes the form of a square wave with a frequency in the 30-Hz to 200-Hz range.

Old-style LCD drivers relied on the use of dual power supplies to provide the AC drive. Modern types, however, use the bridge-supply technique, shown in Fig. 25-*a*, to provide the necessary AC drive. When a segment is turned on using the bridge supply, the segment and backplane are driven by antiphase square waves. The resulting voltage across the LCD is AC as far as the display is concerned; it's the value of segment voltage relative to the backplane voltage that is important. Lets examine how that works. In Fig. 25-*b*, part **A** of the waveform shows the segment to be 10-volts positive to the backplane; in part **B**, it is 10-volts negative to the backplane. Therefore, the LCD is effectively driven by an AC signal with a peak-to-peak value of 20 volts, and with no DC component. In that LCD driving system, when a segment is turned off, it is simply shorted to the backplane of the display.

The most popular CMOS IC for driving 7-segment LCD's is the 4543B BCD to 7-segment decoder/LCD-driver, which uses the bridge power-supply technique. Figure 26 shows the 4543B. That device has to have its PHASE pin connected to the backplane of the display, and must be driven form a symmetrical external square wave. The BLANK pin is normally grounded; that pin blanks the entire display when pulled high. The $\overline{\text{STORE}}$ control causes transparent decoding when pulled high, or causes latched decoding when pulled low.

In conclusion, all of the devices that we have discussed in this article are intended for use in fairly simple applications such as the ones shown. For dedicated applications such as frequency meters, or digital clocks, you should consider the potential applications for the special VLSI IC's. **R-E**

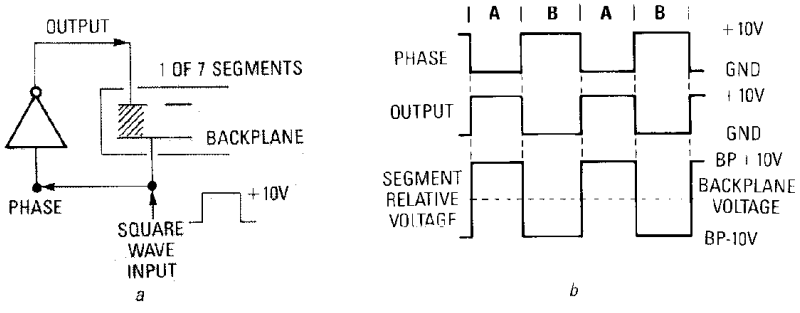


FIG. 25—VOLTAGE-DOUBLING BRIDGE METHOD of driving *L*iquid *C*rystal *D*isplays (LCD). A square wave is inputted to the phase inverter and backplane (BP) shown in *(a)*. That creates an AC voltage across the backplane shown in *(b)*.

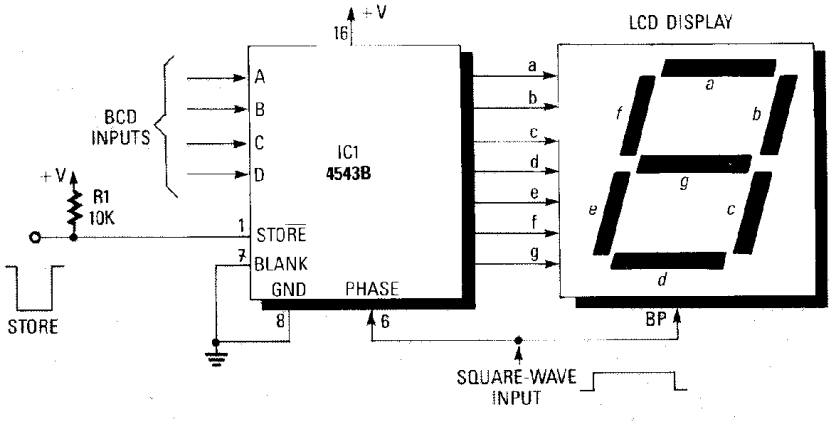


FIG. 26—THE 4543B BCD-TO-7-SEGMENT Latch/Decoder/LCD-Driver. The decoder outputs (*a-g*) are connected directly to the LCD display.