Weigh-counting technique is faster than binary

by Patrick F. Howden
Sydney University, Sydney, Australia

A system of counting that is more condensed and much faster than binary can easily be implemented with tri-state integrated circuits. It is based on the fact that all rational numbers can be represented through a series such as . . . 243, 81, 27, 9, 3, 1, $1/3$, $1/9$, $1/27$, . . . , assuming any of these "weights" can be put on either "pan" of a "scale." This weigh-counting scheme is not related to tertiary counting, though it uses the same number of digits as does tertiary with a sign bit.

A weight digit is designated by a plus sign in a circle if it is in the pan opposite the number to be measured, and by a minus sign in a circle if it is in the same pan. Then the integers 1 through 15 can be represented as shown in the table.

As can be seen, n digits of weigh-counting reach

WEIGH-DIGIT FORMAT AND COUNTING RULES

	27	9	3	1
1				⊕
2			⊕	⊖
3			⊕	○
4			⊕	⊕
5		⊕	⊖	⊖
6		⊕	⊖	○
7		⊕	⊖	⊕
8		⊕	○	⊖
9		⊕	○	○
10		⊕	○	⊕
11		⊕	⊕	⊖
12		⊕	⊕	○
13		⊕	⊕	⊕
14	⊕	⊖	⊖	⊖
15	⊕	⊖	⊖	○

ADDITION

RULES

○ + ○ = ○
⊖ + ○ = ⊖
⊕ + ○ = ⊕
⊕ + ⊖ = ○
⊖ + ⊖ = ⊕ AND CARRY ⊖
⊕ + ⊕ = ⊖ AND CARRY ⊕

EXAMPLE

⊕ ⊖ ⊖ = 5
+ ⊕ ⊖ ○ = + 6
⊕ ⊕ ⊖ = 11

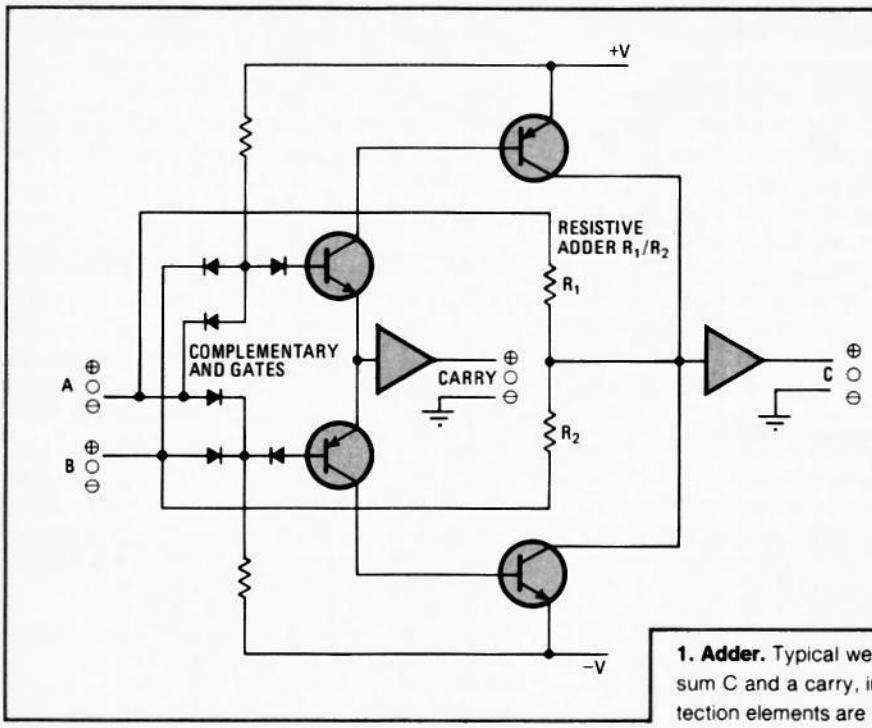
MULTIPLICATION

RULES

○ × ○ = ○
⊖ × ○ = ○
⊕ × ○ = ○
⊕ × ⊖ = ⊖
⊖ × ⊖ = ⊕
⊕ × ⊕ = ⊕

EXAMPLE

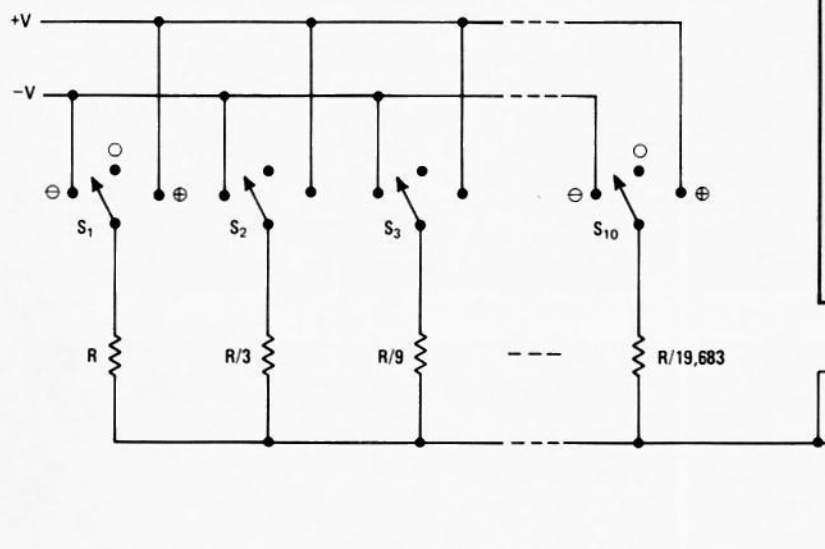
⊕ ⊖ ⊖ = 5
× ⊕ ⊖ ○ = × 6
○ ○ ○
⊖ ⊕ ⊕
⊕ ⊖ ⊖
○ ⊕ ○ ⊕ ○ = 30



ADDER TRUTH TABLE			
A	B	C	CARRY
○	○	○	○
⊕	○	⊕	○
○	⊕	⊕	○
⊖	○	⊖	○
○	⊖	⊖	○
⊕	⊖	○	○
⊖	⊕	○	○
⊕	⊕	⊖	⊕
⊖	⊖	⊕	⊖

⊕ = POSITIVE VOLTAGE
⊖ = NEGATIVE VOLTAGE
○ = ZERO VOLTAGE

1. Adder. Typical weigh-logic circuit adds digits A and B to produce sum C and a carry, in accordance with truth table. Biasing and protection elements are not included in this schematic.



2. D-a converter. Weigh-system converter uses 10 resistors with 3-position switches to sink or source any combination of 10 different currents to summing amplifier. Each switch can be set for positive, negative, or zero positions. Thus, for a fixed magnitude of voltage V, 29,524 positive and negative current outputs are possible—a total of $3^{10}-1$ levels. A binary converter with this many levels requires 16 bits.

½(3^n−1), whereas an n-bit binary system counts only to 2^n−1. Therefore seven weights are approximately equivalent to 10 bits, and 10 weights are equivalent to 15 bits (or 16 bits with sign). This allows a dramatic compression of registers, counters, and wiring. Power consumption is also reduced, and speed is increased, especially if three-state devices are used.

The rules for addition in weigh-digit format are shown in the table. Subtraction is simple. All weighted symbols are reversed in the number to be subtracted, and the result is then added. Long columns of addition and subtraction can therefore be performed simultaneously; the "carries" do not tend to accumulate (as they do in binary or other addition), but rather cancel because two oppositely weighted symbols equal zero.

Parallel multiplication is also simple. As shown in the table, a negative-weight digit in the multiplier reverses all the digits in the multiplicand, and multiplication by successively more significant digits (1,3,9, . . .) merely shifts the multiplicand to the left by 0,1,2, . . . places.

Fast low-power digital-logic packages to perform these arithmetic functions are easy to assemble. Figure 1 shows a typical basic one-digit adder.

Another example is the 10-bit digital-to-analog converter shown in Fig. 2. Only 10 resistors are required to span 59,048 levels, which is almost 16 bits in binary operation. Resistors R and r set the scale factors, and S_{10} is the most-significant-resistor switch.

Engineer's Notebook is a regular feature in Electronics. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $50 for each item published.