Rate multiplier controls noninteger frequency divider

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Frequency dividers capable of dividing by integer and noninteger values can be built inexpensively from very few parts now that synchronous binary rate multipliers are available on single chips. To increase the resolution of the noninteger value, the rate multipliers are simply cascaded.

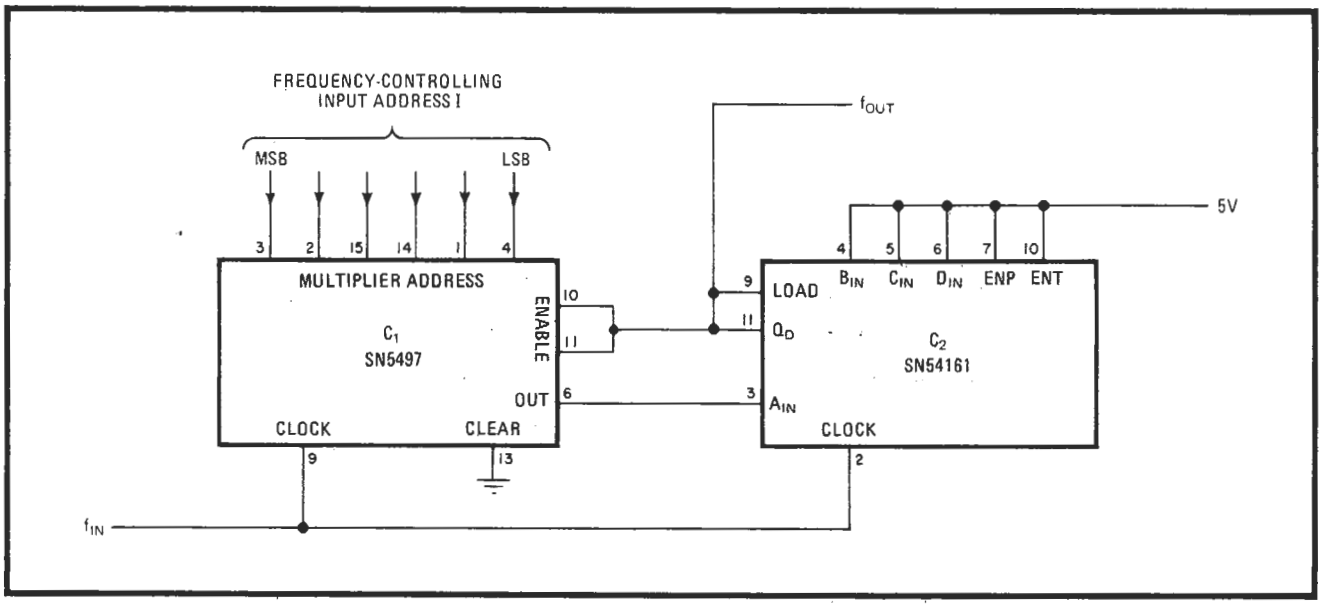
The ratio at which division is performed is set in an indirect manner by the 5497 rate multiplier. This number lies between two values preset in the 54161 synchronous counter, n and $n-1$. The circuit divides the input frequency by a ratio directly proportional to the time the counter spends in the n mode versus the time it spends in the $n-1$ mode.

The number of input pulses rate multiplier C_1 passes to synchronous counter C_2 is proportional to input address I. In this instance the counter is preloaded at either 14 or 15 by inputs A_{in} through D_{in}. C_1's output (pin 6) is connected to the counter's input A_{in}. Address I consequently controls the percentage of time the counter spends at divide values $n = 2$ and $n = 3$.

The rate multiplier's pulse-train output frequency is $f = f_{in}(I/M)$, where M is the size of the rate multiplier (in this case $2^6 = 64$). This particular circuit configuration results in $f_{out} = M(f_{in})/(nM-I)$. The actual divide ratio is $n' = n-(I/M)$.

The value of M determines the size of the available frequency step. The circuit as shown has been used to set f_{out} from 4 to 6 megahertz in steps of about 30 kilohertz; adding one more six-line rate multiplier would bring the step size down to about 400 hertz. Frequency steps in hundredths of a hertz can be easily obtained by cascading more multipliers.

This divider circuit will generate the exact number of clock pulses per second desired, but there will be some phase jitter, with $\Delta\phi = 360/n$. □



Continuous division. Synchronous frequency counter uses rate multiplier in two-chip circuit to program circuit's divide ratio at any value. Output frequency is proportional to the time spent between two preset divide values, n and $n-1$. Multipliers can be cascaded for step-size resolution all the way down to hundredths of a hertz. The amount of phase jitter at the output, in degrees, equals 360/n.