Converter changes 7-segment output to decimal or BCD

by Prentice L. Orswell
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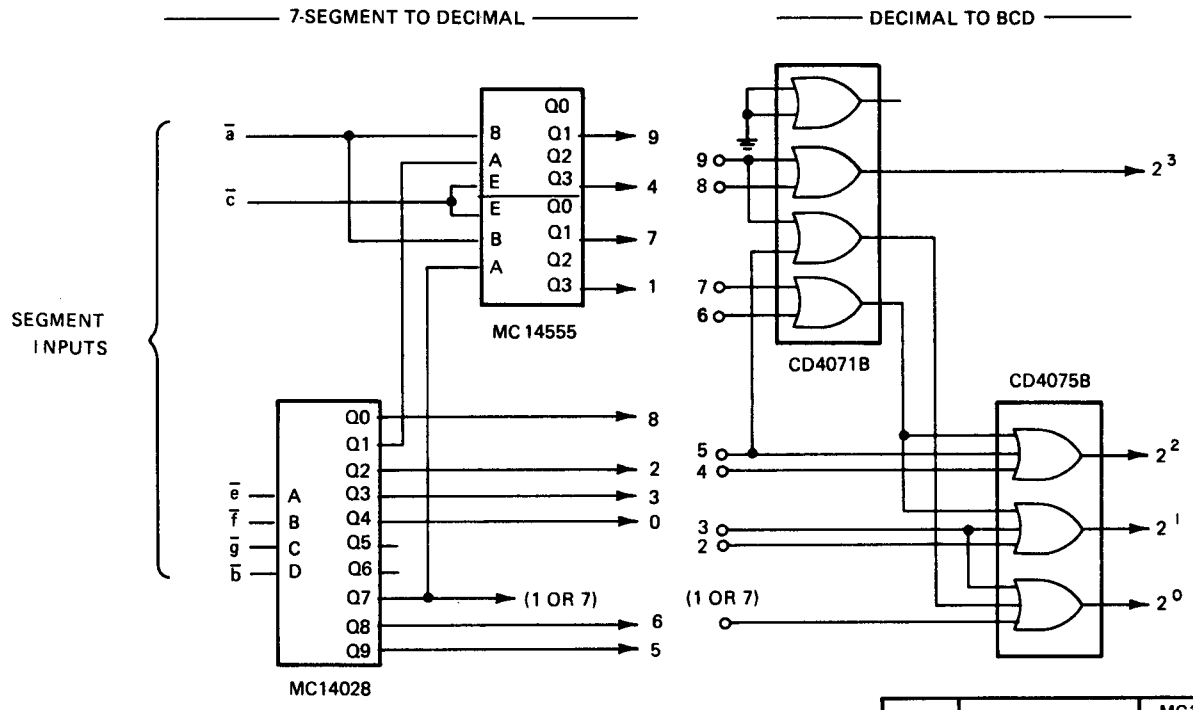
Calculator chips and other LSI circuits with outputs coded to drive seven-segment displays can have more varied applications if the seven-segment outputs are converted to decimal or binary-coded decimal. The converter described here accepts seven-segment MOS signals directly at voltages up to +15 volts and provides decimal and/or BCD outputs with blanking. It uses only four packages, at a component cost of less than $5. (For a seven-segment-to-decimal converter that used discrete transistors, gates, and an expensive demultiplexer, see *Electronics*, August 8, 1974, p. 105.)

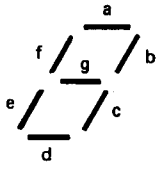
Only six of the segment outputs are required for this circuit. Four of them—b, e, f, and g—are applied to the input terminals of an MC14028 IC; a and c are applied to an MC14555, along with two signals from the MC14028. These two packages have a combined total of 10 output terminals, one of which goes high to represent a numeral (0 through 9) when the complements of the numeral's seven-segment voltages are applied at the input; most LSI circuits provide complementary outputs. The 10 terminals are the decimal outputs. (Another output, corresponding to either 1 or 7, is discussed below.)

If BCD outputs are desired, the decimal outputs are connected to the input terminals of a CD4071B and a CD4075B. These units provide a total of four output terminals, which go high to represent the four BCD bits.

In the seven-segment-to-decimal portion of the circuit, the MC14028 (which is a BCD-to-decimal decoder) uniquely determines six of the decimal outputs. The complements of b, e, f, and g segment voltages for both 1 and 7 decode to output Q7, and digits 4 and 9 both decode to Q1. To separate these in the MC14555 (which is a dual binary-to-1-of-4 decoder), the complement of a is used as an additional input. Full blanking is assured by applying the complement of c at the enable inputs.

Conversion to BCD from the decimal code could be accomplished in several ways. An ideal one-package so-





7-SEG. DIGIT	SEGMENT a c d	SEGMENT b g f e	MC14028 OUTPUT SELECTED
0	000	0100	Q4
1	101	0111	Q7
2	010	0010	Q2
3	000	0011	Q3
4	101	0001	Q1
5	000	1001	Q9
6	000	1000	Q8
7	001	0111	Q7
8	000	0000	Q0
9	000	0001	Q1
BLANK	111	1111	ALL LOW

Converter. Complements of seven-segment voltages, fed into inputs of this circuit, produce high level on one of the decimal-output lines and (if the conversion is carried over to the BCD) on one or more of the BCD output lines. Thus for segment voltages that could display a seven-segment 5, inputs for the b and e segments are high, producing a voltage on decimal output line marked 5; and if BCD-to-decimal stage is connected, lines marked 2^0 and 2^2 go high.

Two of 16 LEDs display 8-bit binary word

by Dennis Saputelli
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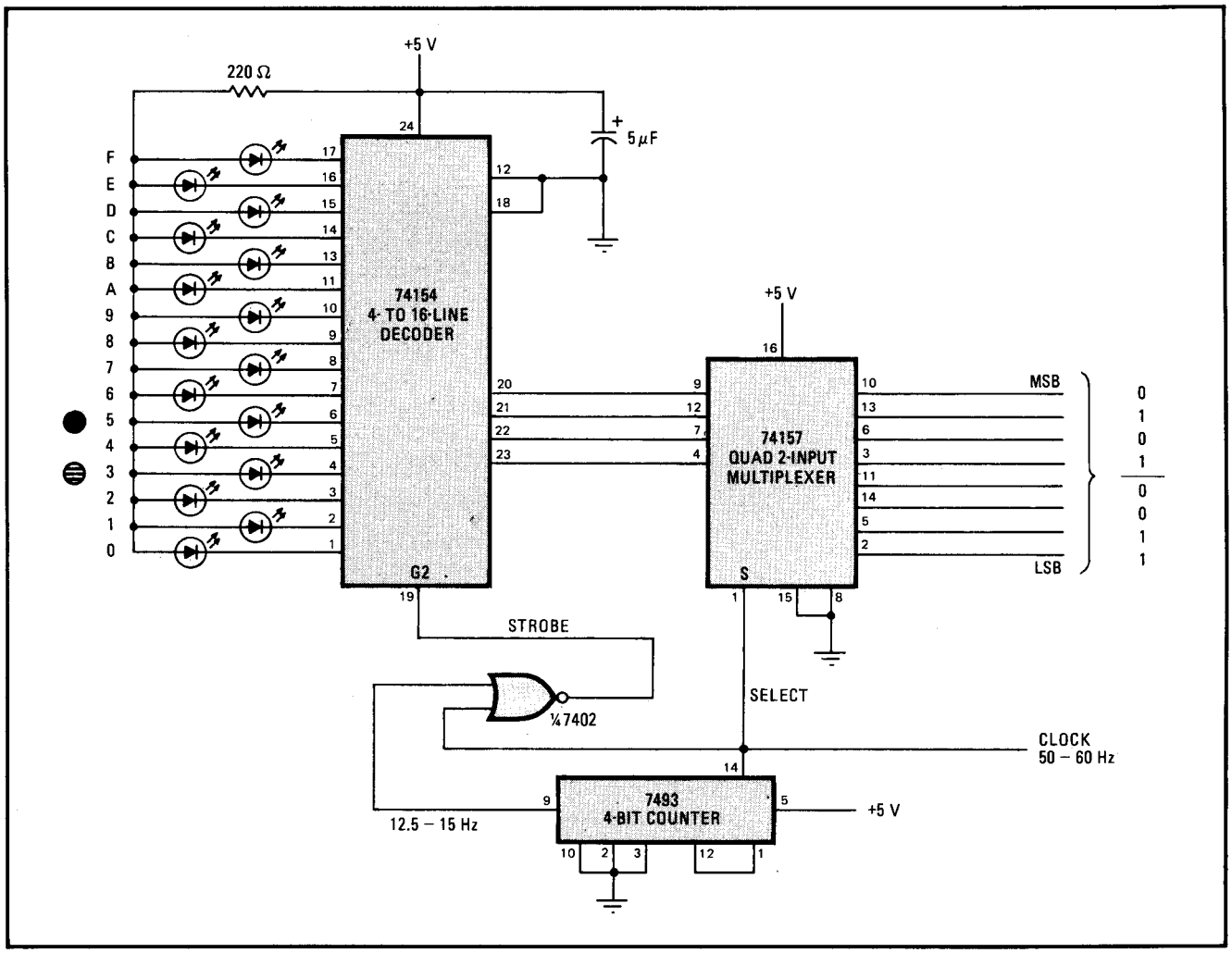
As a low-cost alternative to a numerical display, this binary-to-hexadecimal converter employs light-emitting diodes in an unusual manner. Only 2 LEDs out of a total of 16 light up at any one time to provide a unique indication of 1 out of a possible 256 states. The magnitude of the number may therefore be more quickly recognized from them than from a straight binary display, making it easier to spot trends in changing data.

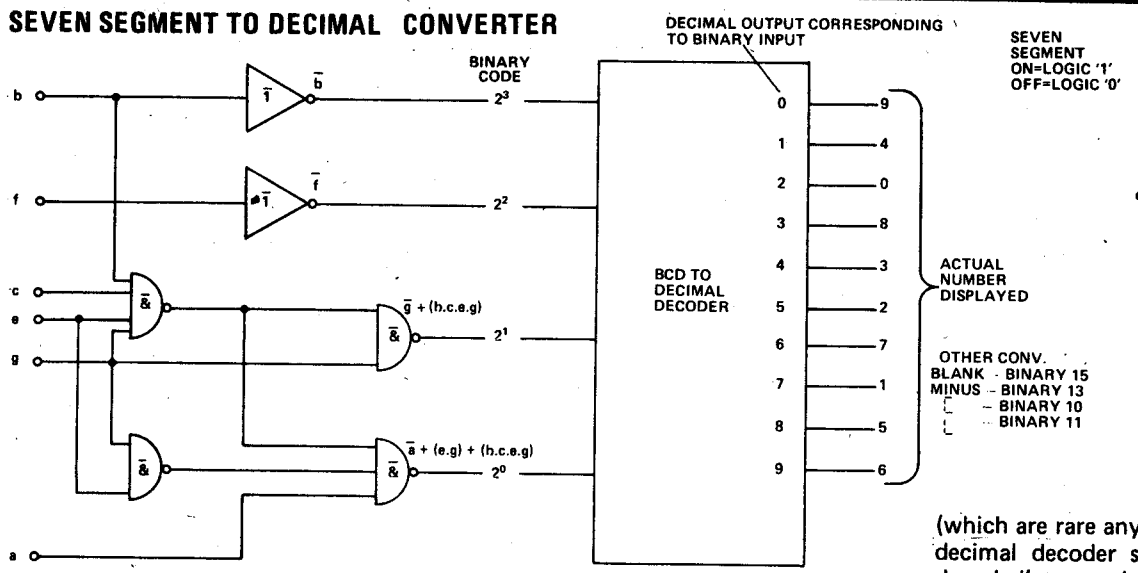
The converter's operation is quite simple. An incoming 8-bit binary number is partitioned into two 4-bit words and presented to the input of the 74157 quad two-input multiplexer, as shown in the figure. A 50-to-60-hertz input clock moves high so that the 4 most significant bits of the number are selected. The strobe signal generated at the 7402 NOR gate moves low at this time, enabling the output lines of the 74154 4-to-16-line decoder, so that the hexadecimal equivalent of these bits is displayed. The clock then moves low, enabling selection and display of the 4 least significant bits.

Each LED must be distinguished from all the others so that the user is aware of its weight factor (16^0 or 16^1) in the hexadecimal system. All 8 bits of the word are sampled 60 times per second or so, which is fast enough to provide the appearance of a continuous glow in the most significant LED. Although the most significant bits are displayed at this rate, the least significant bits are displayed at only one quarter of this rate because of the

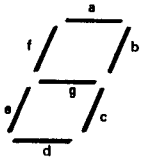


Binary conversion. Eight-bit binary-to-hexadecimal converter uses standard ICs and very simple LED display. LED associated with most significant bit of word glows continuously, while flashing LED indicates value of least significant bit.

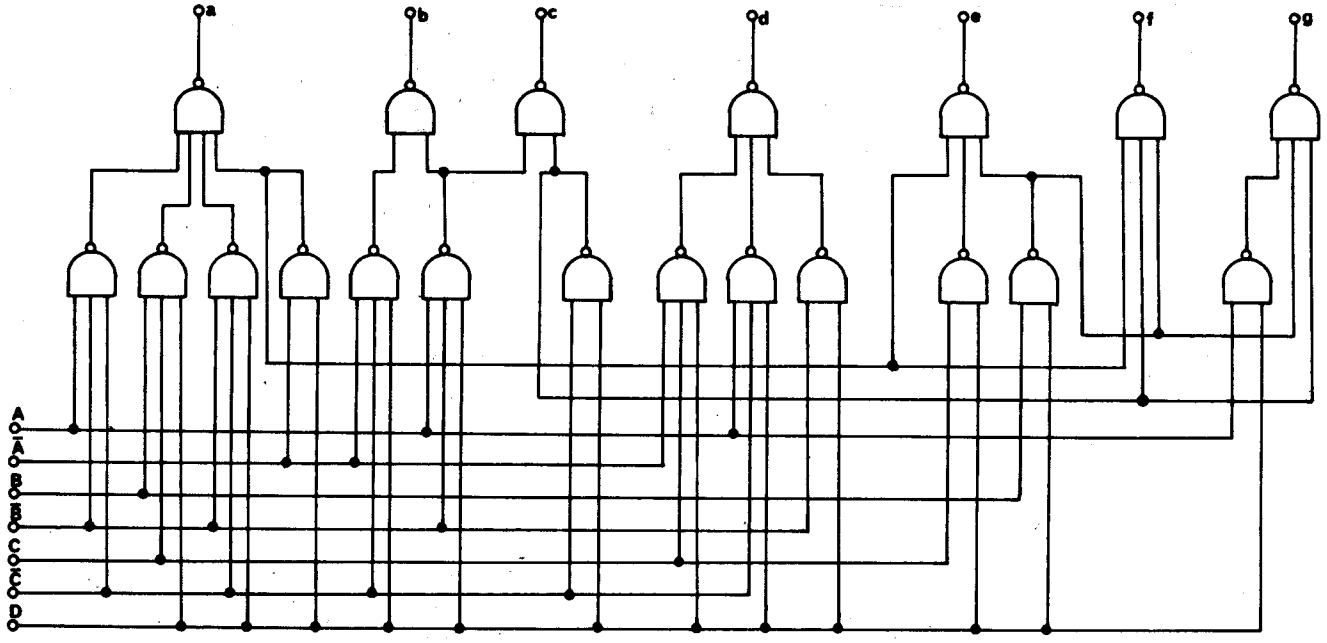
SEVEN SEGMENT TO DECIMAL CONVERTER



SEVEN SEGMENT
ON=LOGIC '1'
OFF=LOGIC '0'



Note that the output from the gates is not 'straight' BCD so the outputs from the BCD to decimal decoder are transposed. It will convert 6's and 9's with or without the top and bottom bars respectively but not 'hooked' 7's (which are rare anyway). The BCD to decimal decoder should be the 'fully decoded' type with blanking for BCD inputs over 9 since a blank is encoded as binary 15, hence a 74141 instead of 7441. Some other conversions which result from this circuit are shown.



HEXADECIMAL TO 7-SEGMENT DECODER.

The circuit described below provides an extension to the 7448 BCD to seven-segment decoder, converting it into a hexadecimal to seven-segment decoder which will give the numerals 0-9 and the characters A,B,C,D,E, and F as output for a four bit binary input.

(Inputs of A,$\overline{A}$,B,$\overline{B}$,C,$\overline{C}$,$\overline{D}$ are needed with an inverting buffer - fan out 30 - on the $\overline{D}$ input.)

The 7448 is disabled by bringing the blanking input low when the input is greater than 0111_2 (i.e. $\overline{D}$ is connected to B1/RBØ on the 7448.) Outputs from the 7448 and the add-on decoder are OR-ed together creating a single seven-segment output.

D	C	B	A	a	b	c	d	e	f	g
Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	Ø	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	1	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø
Ø	1	1	1	Ø	Ø	Ø	Ø	Ø	Ø	Ø
1	Ø	Ø	Ø	1	1	1	1	1	1	1
1	Ø	Ø	1	1	1	1	1	Ø	1	1
1	Ø	1	Ø	1	1	1	Ø	1	1	1
1	Ø	1	1	Ø	Ø	1	1	1	1	1
1	1	Ø	Ø	1	Ø	Ø	1	1	1	Ø
1	1	Ø	1	Ø	1	1	1	1	Ø	1
1	1	1	Ø	1	Ø	Ø	1	1	1	1
1	1	1	1	1	Ø	Ø	Ø	1	1	1

TRUTH TABLE for the 'add-on' decoder. Note that when the input is $Ø110_2$ (6_{10}) a logical one is inserted in the 'a' column to provide the resulting seven-segment '6' with a cap, thus differentiating it from a 'B'.

Decoders convert binary code for hexadecimal display

by Robert F. Starr
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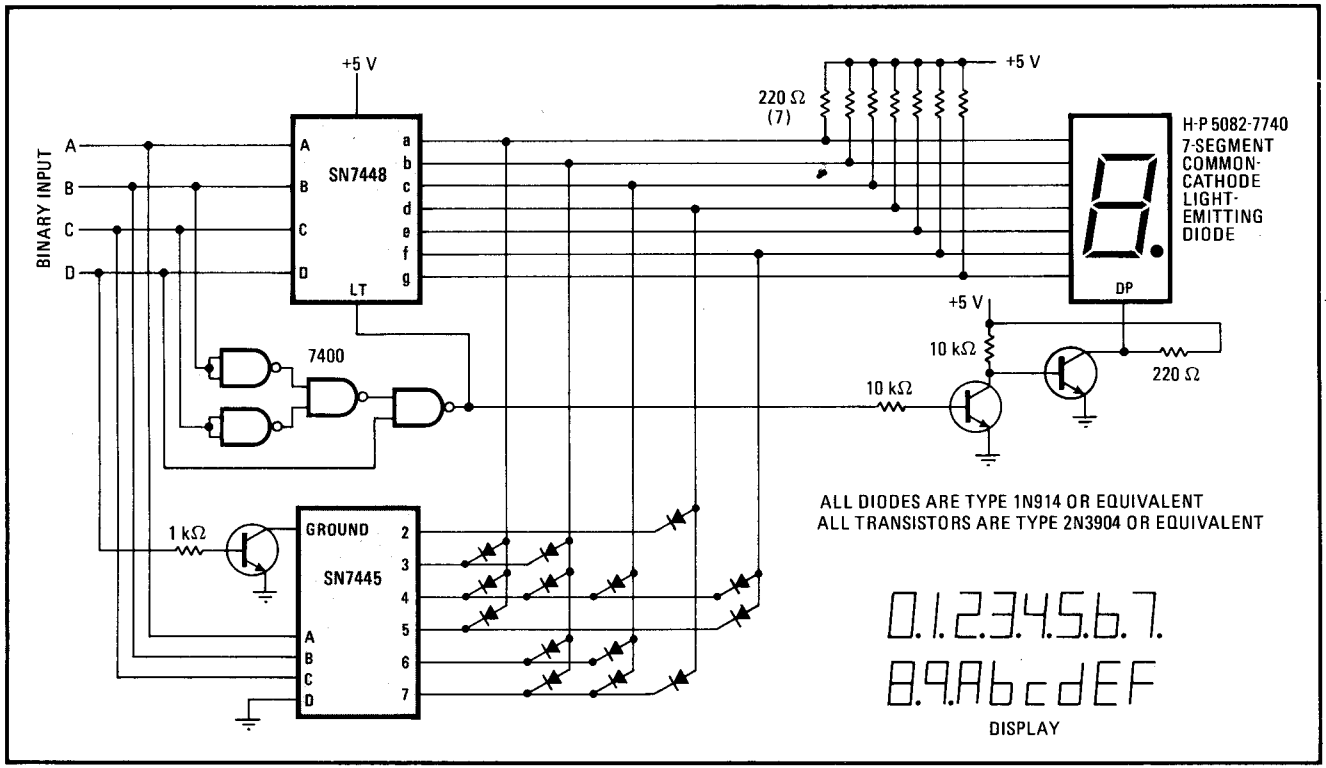
Hexadecimal code symbols can be shown cheaply and easily on a regular seven-segment display by two decoder/drivers and some logic circuitry. To keep the hex digits A through F completely recognizable, the circuit described here generates both upper-case and lower-case letters. The 7448 seven-segment decoder/driver displays a symbol for "6" that is identical to a "b". Therefore, the decimal point of the display is activated for the numbers 0 through 9, and extinguished for the letters A through F.

The circuit operation is quite straightforward. For binary inputs to the 7448 from 0000 to 1001 (0 to 9), the 7448 functions normally, displaying the appropriate digit on the light-emitting-diode display. As soon as the binary input exceeds 1001, the LT (Lamp test) input on the 7448 is brought low, lighting all segments, and extinguishing the decimal point (DP) on the LED. In addition, as soon as the D input (most significant bit) on the 7448 goes high, the 7445 binary-coded-decimal-to-decimal decoder/driver turns on.

With the D input of the 7445 grounded, the device sees only the three least significant bits of the input. When the binary input is 1011, for example, the 7445 sees a 011 (3) and brings the 3 output low. This output is decoded by the diode matrix, which turns off segments a and b of the LED display, forming a "b" on the display. The process is similar for all other binary inputs from 1010 to 1111 (A, c, d, E, and F).

An H-P 5082-7740 LED display is shown here, but other types can be used. For most of the larger displays, it may be necessary to pull the seven-segment lines to ±5 volts through 220-ohm resistors to achieve the desired brightness. □



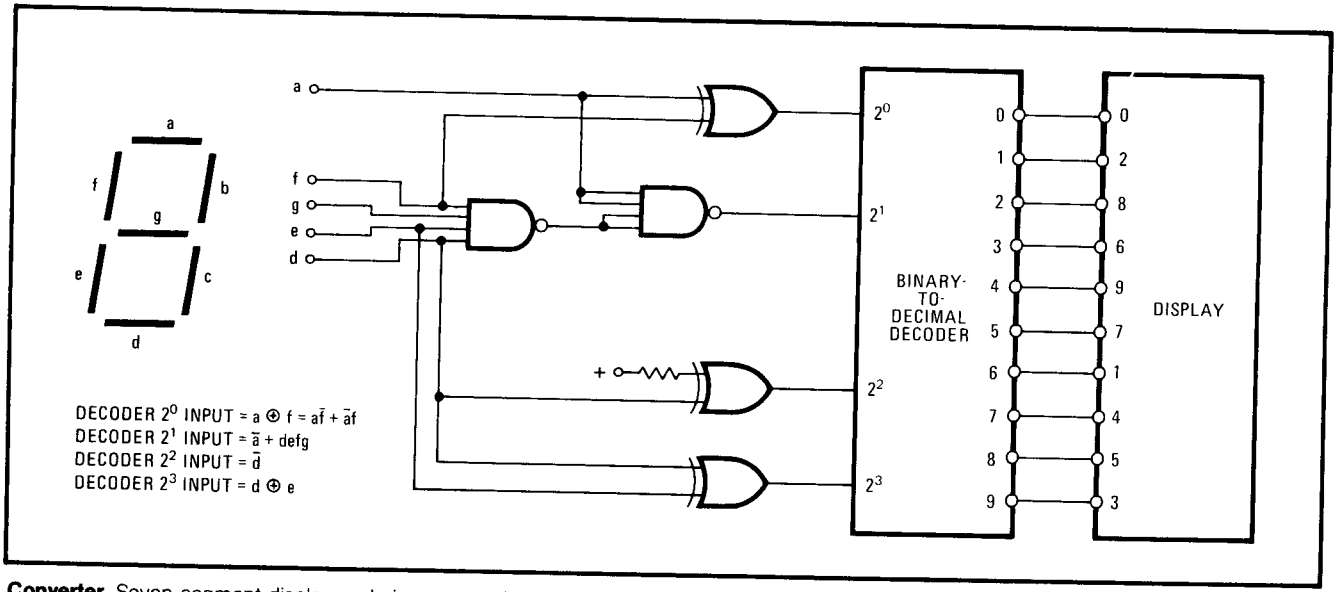
Hex signs. Binary inputs produce hexadecimal code on a standard seven-segment display with this circuit. To emphasize distinctions between numerals and letters, a decimal point is activated for numbers 0 through 9, as shown. Cost of parts (not including LED display) is less than $5. For more than one digit, the inputs can be multiplexed. Pull-up resistors may not be required for small displays.

IC trio converts 7-segment code to decimal

by James Southway
McDonnell Douglas Astronautics Co., St. Louis, Mo.

A device that converts a seven-segment display code into decimal code and is less expensive than the demultiplexer described in a previous article [*Electronics*, Aug. 8, p. 105], uses only three integrated circuits. The only other requirement is front-end buffering, and only if its TTL circuitry is to be used with a MOS system. Like the demultiplexer, this device enables a seven-segment display code to directly drive any kind of cold-cathode gas discharge indicator tubes.

The small number of ICs is made possible, in part, by combining the logic of the binary-to-decimal decoder with a few external logic gates, and by cross-wiring the decoder outputs to the display inputs. In other words, output 1 of the decoder drives the display input for 2; output 4 drives the input 9, and so on. (The only uncrossed output is 0, as shown in the diagram.) The decoder is a 74141 or equivalent; the external logic is one dual four-input NAND, 7420, and one quad exclusive-OR, 7486. Another saving is made by using one of the four exclusive-OR gates in the 7486 as an inverter, and one of the two four-input NANDs in the 7420 as a two-input NAND. □



Converter. Seven-segment display code is converted into a 1-out-of-10 code for driving such things as indicator tubes, and uses only three integrated circuits. Decoder, external logic, and cross-wired outputs keep the IC count low.

Cascaded C-MOS blocks form binary-to-BCD converters

by Haim Bitner
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Low-power complementary-metal-oxide-semiconductor adders and comparators are easily combined to form this 4-bit binary-to-BCD converter. When the basic adder-comparator blocks are cascaded, the converter can be expanded to turn n binary input bits into a binary-coded-decimal output. The circuit is simpler than one using counters, and read-only memories are eliminated.

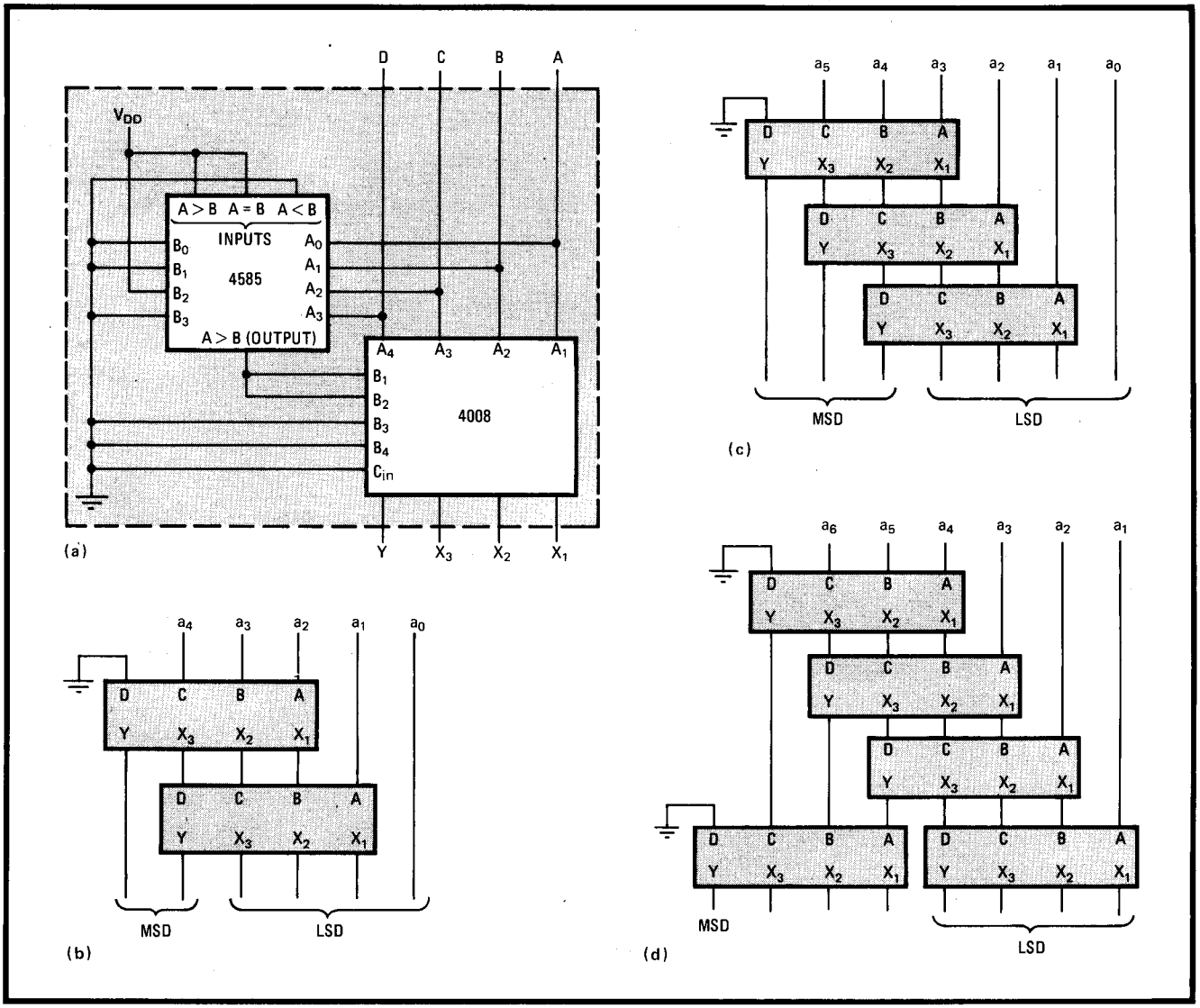
Comprising the basic 4-bit converter block (a) are the 4008 full adder and the 4585 comparator. The binary inputs are introduced at A–C, with A being the next to least significant bit, and D grounded. The BCD output appears at X_1–X_3 and Y of the 4008. The LSB input bypasses the unit and becomes the LSB output.

The 4585 compares the input bits to a binary number (0100) which is hard-wired to pins B_0–B_3. Thus the output of the 4585 is low if the number at A–D is less or equal to 4. The X_1–X_3 outputs of the 4008 are then identical to the input bits.

If the input number becomes greater than 4 (that is, greater than 0100), the 4585's output moves high, and so binary number 0011 is placed on the B_1 and B_2 inputs of the 4008 adder. Thus, 3 is added to the input number and the Y output of the 4008 goes high, indicating the most significant digit is active.

By cascading units, 5-bit (b), 6-bit (c) and 7-bit (d) converters can be built. The method can be used to extend indefinitely the number of bits processed. Note that the value of the least significant input bit (a_0) is numerically equal to its BCD-equivalent and so passes straight from input to output in all cases. □

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



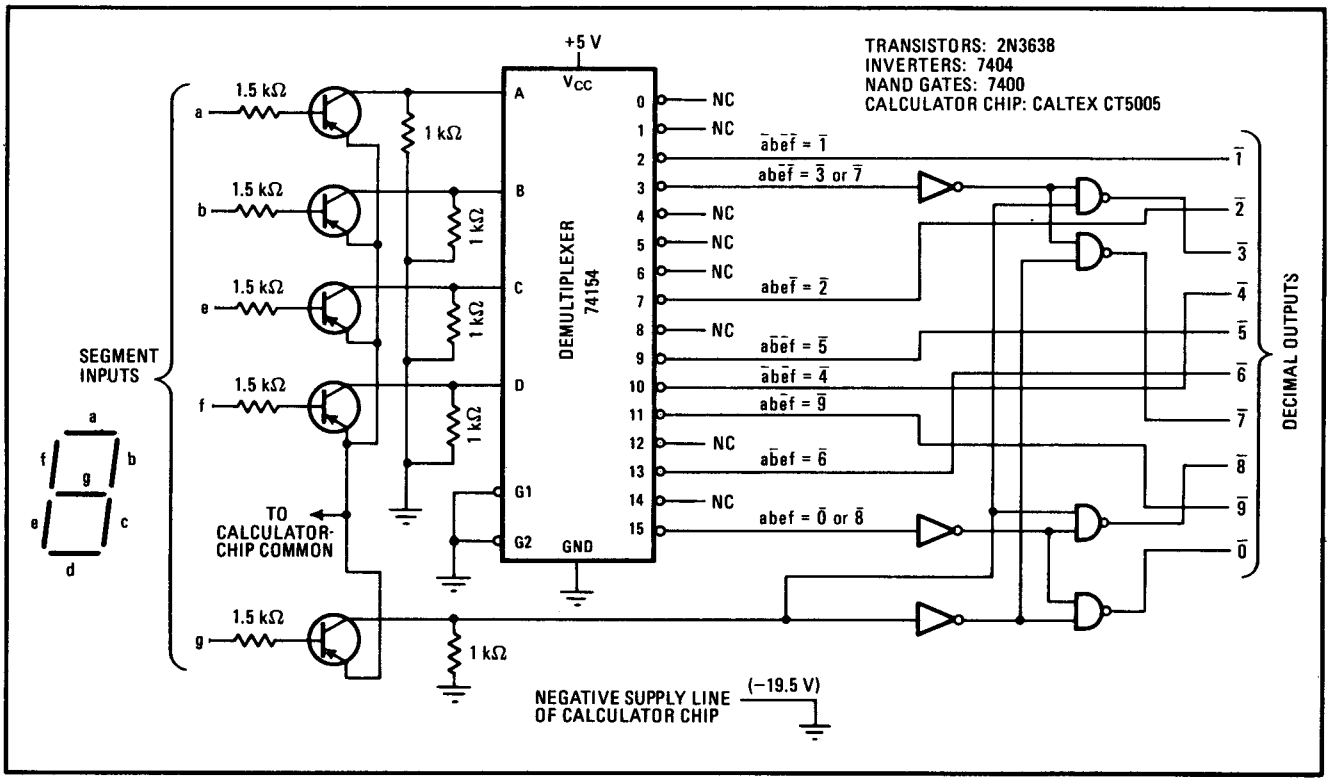
Add infinitum. Low-power binary-to-BCD converter (a) requires only C-MOS adder and comparator for processing 4 bits. Unit is so configured that basic building blocks can be easily combined to form 5-bit (b), 6-bit (c), and 7-bit (d) converters.

Providing a decimal output for a calculator chip

by Jack Lambert
Lambert Associates, Lexington, Mass.

Calculator chips, which are becoming readily available, can be used to advantage in applications other than pocket calculators. However, these chips usually have an output that drives a multiplexed seven-segment display. This is not really convenient for performing subsequent operations or even for interfacing with Nixie-type readouts.

With the circuit shown here, the output of a calculator chip can be converted to the more convenient decimal form. If desired, this decimal output can also be converted, for example, to a binary-coded-decimal form. A calculator chip having a decimal output can be used as an input to another calculator, to operate a



More applications. Decoder circuit converts the seven-segment-display outputs of a calculator chip to decimal form, greatly increasing the application versatility of the chip. All 10 of the decimal outputs can be derived from only five of the segment inputs. The same power supply is used for both the chip and the decoder's TTL circuitry. The chip's negative supply line acts as ground for the TTL supply.

large dot-matrix display, to feed a printer, or to drive a digital controller or computer.

Although the conversion circuit is not necessarily the simplest logic scheme, it is easy to set up and to wire. Only three TTL IC packages are required—they are a four-line-to-16-line demultiplexer, a hex inverter, and a quad two-input NAND gate.

The lower-case letters in the diagram correspond to the display segments used to set up the logic for the conversion circuit. Only five of the seven possible segment inputs are needed to develop all of the decimal outputs; the other two segments are redundant. The seven-segment logic inputs are high, while the decimal outputs are low. The gate inputs (G1 and G2) to the demultiplexer may be used if desired, otherwise they should be tied low, as shown.

This particular conversion circuit is intended for the Caltex type CT5005 calculator chip. A separate 5-volt supply is used for the TTL ICs, but the negative line (−19.5 V) of the chip supply is made the ground line of the TTL supply. This allows a single supply, one having the proper dropping resistors and regulation, to be used for both the chip and the conversion circuit.

The discrete transistors serve as a simple interface between the chip and TTL devices. This means that the display outputs of the chip can directly drive the conversion circuit. Of course, a chip other than the type CT5005 device may require other interfacing.

The use of the type 74154 demultiplexer results in a certain amount of redundancy in the circuit's decoding process. However, the demultiplexer does keep the wiring simple, and it also conserves board space without increasing parts cost significantly. The entire circuit costs about $3.50 to build. □

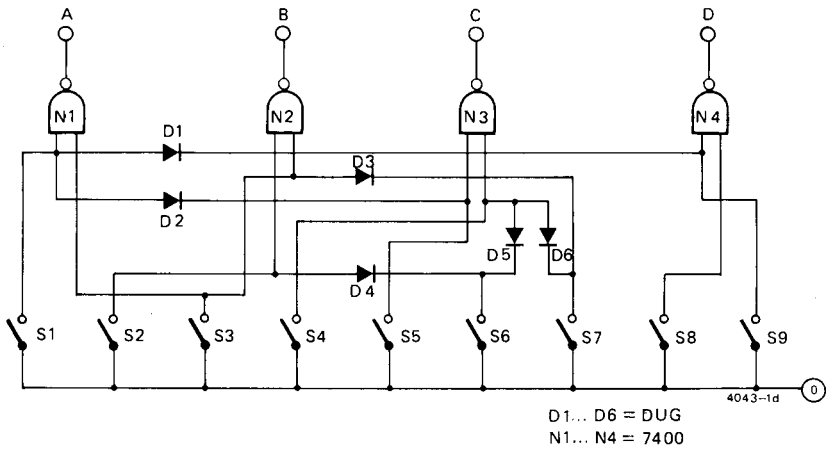
decimal to bcd converter

This converter can be used as a manual encoder which will convert decimal coded signals into BCD codes and drive digital circuits. Furthermore, the converter can be used as a teaching aid for explaining the BCD code.

One IC and six germanium diodes are sufficient for converting a decimal number into a BCD number. A switch for zero is not provided because the converter automatically indicates zero when all switches are open. The reverse resistance of the diodes must be as high as possible (if necessary, check with an ohmmeter) and the gate inputs can be provided with a pull-up resistor connected to the positive supply voltage.

If the circuit is to be used to explain the BCD code, the BCD-output conditions can be indicated by means of LED's. The circuit for the required buffer stage is shown in figure 2.

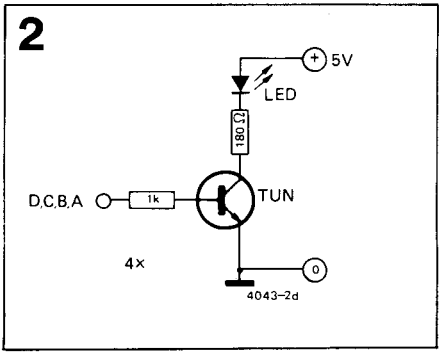
1



Table

D	C	B	A	Decimal
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

2



1

P. Höfs

Table 1.

	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1

Cold-cathode numicator tubes are gradually passing out of use and are being replaced by various types of seven-segment displays. As the life of these tubes is about 10 years there are still many serviceable pieces of digital equipment around which, although in good working order, have tubes that are beginning to fail. Some readers may have DVM's or digital clocks, which they would like to convert for a seven-segment display.

This article describes two simple decoders, which will convert the decimal output of the numicator decoder to a seven-segment code. The circuits are also useful for demonstrating seven-segment displays using a ten position single-pole switch to programme the numbers.

To work out the simplest decoding circuit it is first necessary to draw up a truth table for the seven-segment display (table 1). A '1' in a column indicates that the particular segment is illuminated. A '0' indicates that it is extinguished.

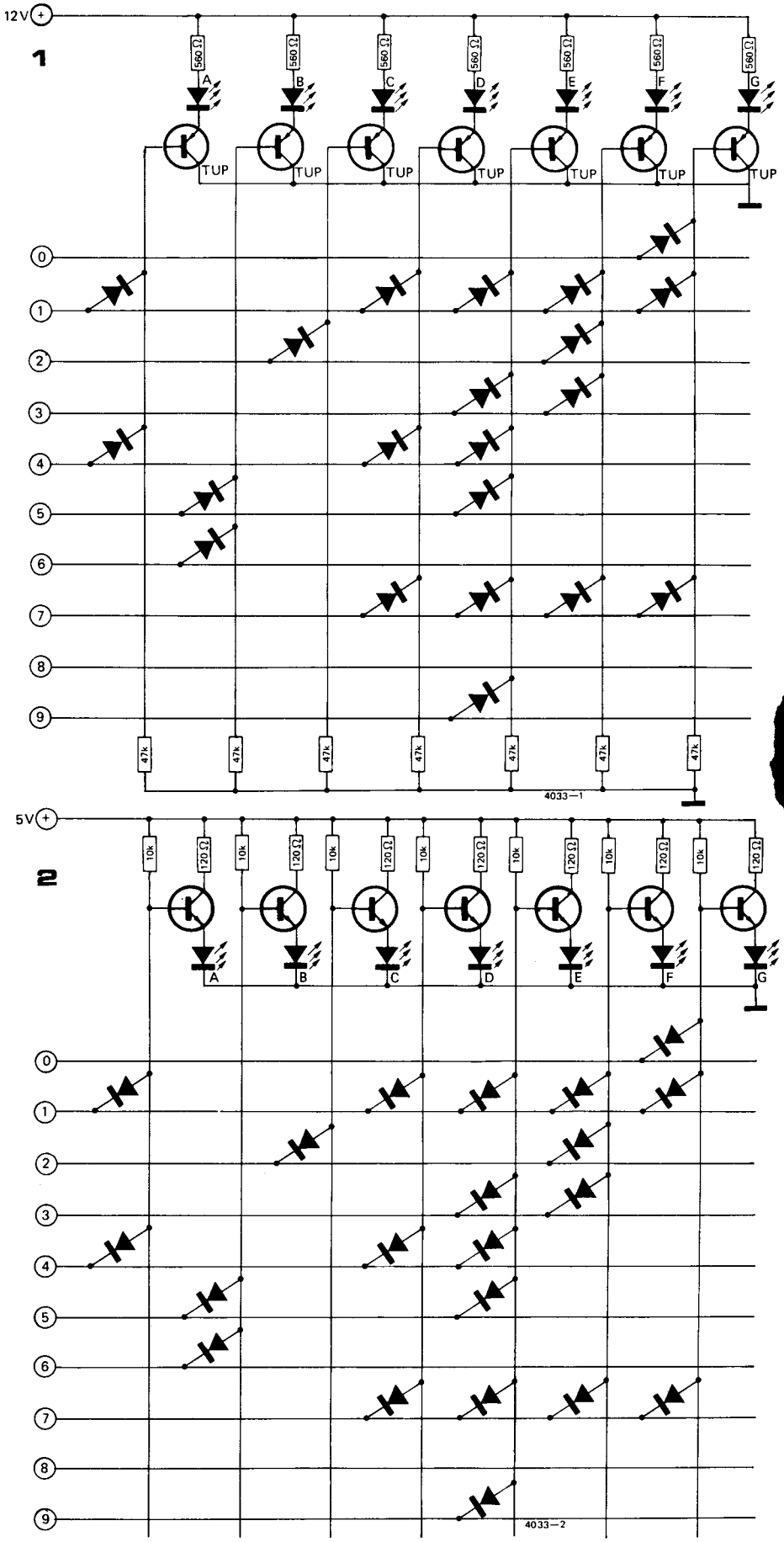
It is apparent that there are a great deal more 'ones' in the truth table than there are 'noughts', 49 as against 21. It is therefore evident that the simplest conversion will be achieved via the 'noughts'. i.e. all segments are normally illuminated and the ones not required for a particular digit are suppressed.

The decoder consists basically of a diode matrix. The rows of the matrix are the decimal inputs, whilst the columns are the outputs to the seven segment display. Where a digit requires that particular segments are suppressed, diodes are connected from the appropriate row to the appropriate columns.

Two versions of the decoder are shown in figures 1 and 2. Figure one is intended for positive logic inputs, i.e. when a particular digit is enabled, that row input is 'high' and all the others are low. The TUP's are all normally turned on, but when a particular digit input goes 'high' then the diodes connected to that row hold the bases of the transistors connected to them to about +11.4 V, thus turning off the transistors and extinguishing the appropriate display segments.

The version of the decoder shown in figure 2 is intended for negative logic inputs such as numicator tube decoder outputs. The transistors are all normally turned on, but when any row input goes 'low' it will ground the bases of the transistors connected to it by diodes, thus turning them off.

The two versions of the decoder are shown for different supply voltages, but either may be used with the other supply voltage by substituting the resistor values from the other circuit.



decimal to seven segment converter using 21 diodes

tech - tips

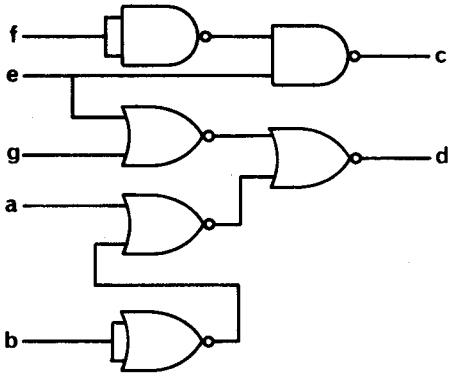
Seven Segment Decoder

Yap Sue-Ken

As not all of the possible seven segment codes are used, only 5 lines are required to define the ten numerals without ambiguity. The logic circuitry required to recover the other two segments are as shown in the figure.

In the case of microprocessor controll-ed displays this can save two valuable I/o pins.

	INPUT SEGMENTS					OUTPUT SEGMENTS	
DECIMAL DIGIT	a	b	e	f	g	c	d
0	1	1	1	1	0	1	1
1	0	1	0	0	0	1	0
2	1	1	1	0	1	0	1
3	1	1	0	0	1	1	1
4	0	1	0	1	1	1	0
5	1	0	0	1	1	1	1
6	1	0	1	1	1	1	1
7	1	1	0	0	0	1	0
8	1	1	1	1	1	1	1
9	1	1	0	1	1	1	1



NOR GATE = CD4001 OR SN7402
NAND GATE = CD4011 OR SN7400
POSITIVE LOGIC: '1' = ON

$c = \overline{e.f.}$

$d = \overline{(g+e)} + \overline{(a+b)}$