C-MOS flip-flop can do more than logic tasks

The high impedance and threshold properties of the complementary-MOS flip-flop enable it to handle several unconventional jobs, such as pulse generation, duty-cycle modulation, and limit detection

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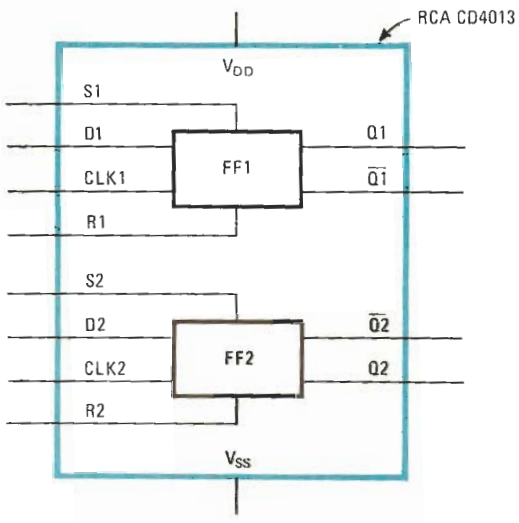
☐ The advantages of complementary-MOS logic—like high noise immunity, low power dissipation, and wide operating range—are well known by now. What may not be as well known is the versatility of the C-MOS flip-flop. Because of its high threshold voltage and high input impedance, it can be made to perform tasks other than the logic applications for which it normally is intended. Its input impedance, which is on the order of 10^{12} ohms, means that source loading is never a problem, and its logic-high threshold level, which is typically about 45% of the supply voltage, permits very large time constants to be realized.

For example, the model 4013, a dual data-type flip-flop with set/reset capability, can operate as a one-shot with an output-pulse width that can be adjusted over a 10,000:1 range. The device can also be wired for use as a limit detector for sensing pulse rates, as a temperature-level alarm, or as a go/no-go diode-leakage tester. Other possible applications include use as a duty-cycle modulator or as a pulse generator having an output-duty cycle adjustable over a wide range. If a second 4013-type flip-flop is used, the result can be a simple pulse-rate discriminator or even a logic-controlled duty-cycle modulator.

This sort of flexibility is not limited to the 4013-type flip-flop—other C-MOS flip-flops can also be used in a similar variety of circuits. A closer look at the applications just mentioned for the 4013-type device will help to illustrate how it's done.

As shown in Fig. 1, the 4013-type integrated circuit consists of two identical D-type flip-flops, each having independent data, clock, set, and reset inputs, as well as complementary outputs. It is intended for use as an R-S flip-flop, a toggle flip-flop, or a D-type flip-flop, as well as in shift-register or counter applications. As indicated by the unit's truth table (Fig. 1), the logic level present at either D input is transferred to the corresponding Q output during the positive-going transition of a clock pulse. Either flip-flop can be set or reset independently of the clock pulse by placing a logic high on either the set or reset line.

To wire this C-MOS IC as a one-shot, an RC network is connected to the Q1 output with a feedback path to the R1 input, as shown in Fig. 2. When a trigger pulse is ap-



TRUTH TABLE

CLK	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	X	0	0	NO CHANGE	NO CHANGE
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

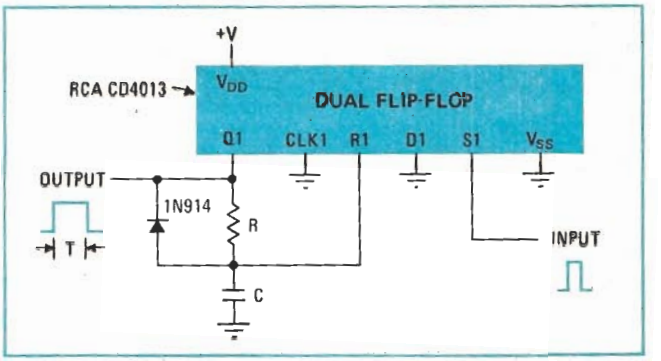
X = DON'T CARE

1. The basic device. The 4013-type C-MOS integrated circuit is a dual data-type flip-flop offering set/reset capability. Each of its two flip-flops has independent data (D), clock (CLK), set (S), and reset (R) lines, plus independent complementary outputs (Q and $\overline{Q}$). As the truth table shows, a logic signal is transferred from the D input to the Q output during a positive-going clock transition.

plied to the S1 input, the output will be a pulse having a width (T) of approximately 0.66RC second. Because of the flip-flop's high input impedance, the maximum value of resistor R can be as high as 10 megohms. The resistor's minimum value, on the other hand, is limited by the flip-flop's maximum output current capability. Typically, resistor R can be as low as 20 kilohms. Just by varying the value of resistor R, then, the output pulse width of this one-shot can be adjusted over at least a 500:1 range.

The lower limit of capacitor C is determined by the flip-flop's minimum reset pulse width, which is about 125 nanoseconds. When the capacitor is discharged, its voltage should remain higher than the flip-flop's reset threshold voltage for a very short time. This duration is the minimum reset pulse width. A typical value of capacitor C is 0.033 microfarad. When the triggering frequency is low, capacitor C can be quite large, provided that its discharge current does not exceed the flip-flop's maximum output drive current. The diode in the circuit ensures that the capacitor discharges quickly.

If the values of both resistor R and capacitor C are varied, the output pulse width of the one-shot can generally be adjusted over about a 10,000:1 range. When the triggering pulse to the S1 input is longer than 0.66RC, the output voltage will stay high as long as the trigger voltage remains high. The one-shot can be reset by applying a voltage to the flip-flop's CLK1 input, instead of returning this pin to ground as shown in the diagram.



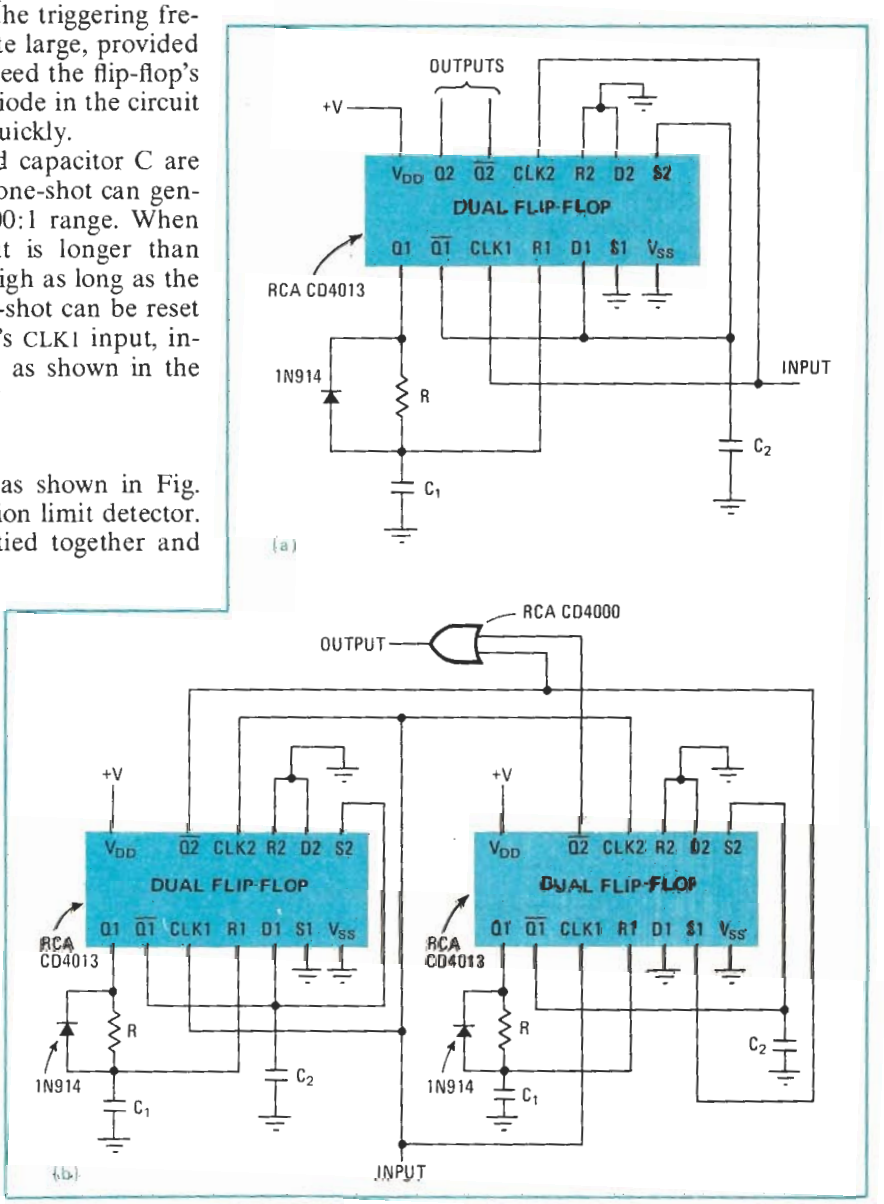
2. One-shot hookup. Only one of the flip-flops in the 4013 type is needed to realize a monostable multivibrator. Because both resistor R and capacitor C can have a wide range of values, the output-pulse width of this one-shot can be varied over a 10,000:1 range.

Building detector circuits

If the 4013-type flip-flop is wired as shown in Fig. 3(a), the device becomes a multifunction limit detector. Here, input D1 and output Q1 are tied together and then run to the S2 input. The clock inputs, CLK1 and CLK2, are triggered simultaneously by the same train of narrow pulses. Part of the flip-flop remains wired for one-shot operation, as illustrated in Fig. 2.

The circuit can be used as a pulse-rate limit detector. When the period between input pulses (T_0) becomes equal to or less than the one-shot's timing period (T_1), outputs Q2 and $\overline{Q2}$ will change state, producing an output pulse for every other input pulse. As long as this input off-time period is greater than the one-shot's period, output Q2 will remain high, and output $\overline{Q2}$ will remain low. The period of the one-shot is approximately equal to $0.66RC_1$.

Capacitor C_2 delays the pulse to the S2 input so that the pulses to the CLK2 terminal are not overridden. Increasing the value of this capacitor, which is typically 0.0068 μF, not only widens the circuit's output pulses, but also introduces a small amount of hysteresis around the cir-



3. As a detector. The 4013-type flip-flop can also operate as a limit detector. In (a), output pulses are produced at Q2 and $\overline{Q2}$ when the input pulse off-time is less than the one-shot's period ($T_1 = RC_1$). If resistance R is a thermistor or a photocell, the circuit will perform as an ambient-level alarm. Adding a second 4013 type, as in (b), creates a simple pulse-rate discriminator whose output is synchronized with the input and has the same period.

cuit's detection point. (Depending on the application, this hysteresis may or may not be desirable.)

In addition to being used as a pulse-rate detector, the circuit can be adapted for other applications. Since resistance R can have a wide range of values, a resistive element, such as a thermistor or a photocell, can be substituted for a resistor. If the input pulse rate is kept constant and resistance R varies instead, the circuit can function as an ambient-level alarm for sensing temperature or light. When the preset ambient level is exceeded, an output-pulse train will be produced.

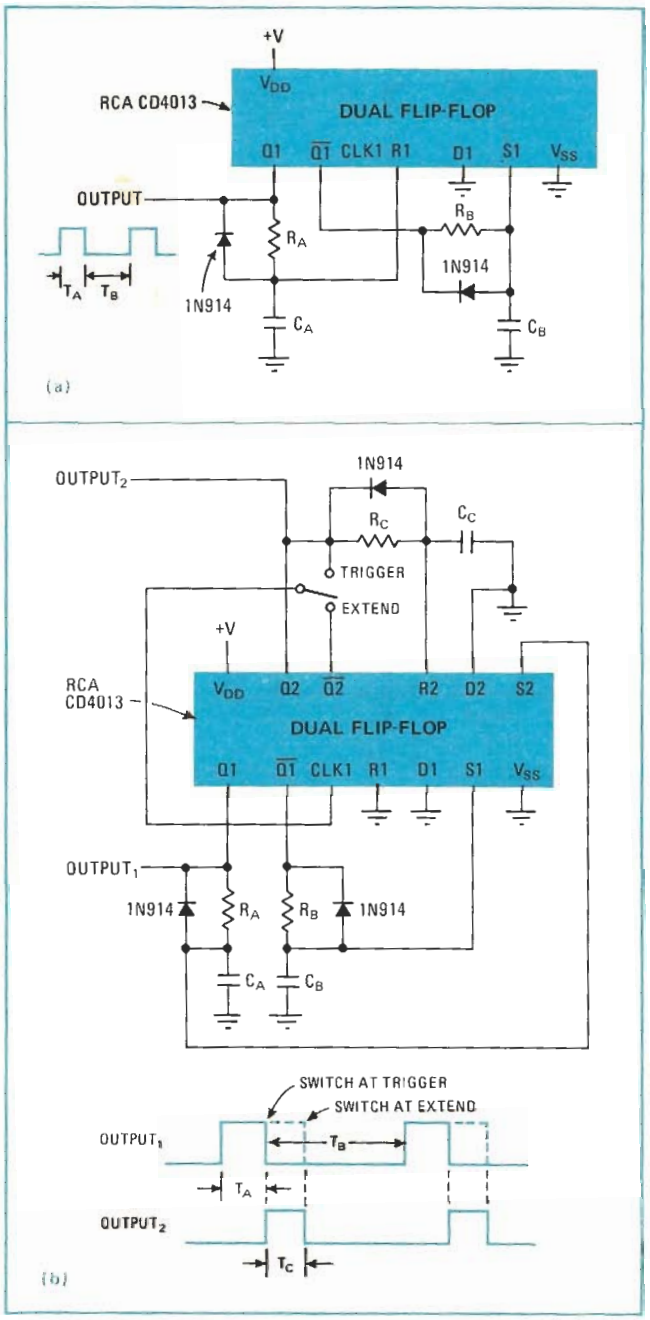
The circuit can also be part of an automatic control system. Suppose, for example, that the input-pulse rate corresponds to motor speed. Suppose also that resistance R is a temperature-sensitive element. In this arrangement the circuit can be used to lower the limit of a motor overspeed alarm on a hot summer day.

Resistance R in the one-shot's timing network can be eliminated altogether, leaving only the diode and capacitor C_1. Here the output-pulse width is determined by the diode's leakage current, which is an exponential function of the ambient temperature. At a controlled temperature, the circuit can be used as a go/no-go tester for diode leakage. It can also operate as a temperature-level alarm. And if a photodiode is substituted for the junction diode, the circuit can become a light-level alarm or a dark-current tester for photodiodes.

There are also medical applications for this detector circuit. For instance, with appropriate modification, it can be operated as a tachycardia detector for monitoring heart beat.

By adding a second flip-flop to the circuit of Fig. 3(a), as in Fig. 3(b), a pulse-rate discriminator is realized. When the input period is less than the one-shot period, the $\overline{Q2}$ output of the left-hand flip-flop generates pulses at every other input pulse, while the $\overline{Q2}$ output of the right-hand flip-flop produces pulses for those inputs missed by the left-hand flip-flop.

The OR gate at the output of the circuit remains inhibited until the input-threshold frequency is reached. Once this happens, the gate will produce a pulse train that has the same period as the input signal and that is synchronized with the input. Because the discriminator circuit operates in real time, its response has an unusually sharp cutoff, but practically no delay.



4. **Generating pulses.** Half of the 4013-type flip-flop can be wired as a pulse generator (a) having an output duty cycle that can be adjusted over a wide range. By using both halves of the flip-flop, it can be made to produce a delayed trigger pulse, as in (b).

Generating pulses and modulating duty cycle

Another application for the 4013 flip-flop is as a pulse generator, as in Fig. 4(a). Different time constants are introduced into the device's set and reset lines. Resistor R_A and capacitor C_A control the delay from the Q1 output to the R1 input, while resistor R_B and capacitor C_B determine the delay between the $\overline{Q1}$ output and the S1 input.

The circuit's output will be a square wave having an on-time (T_A) of approximately $0.66R_AC_A$ and an off-time (T_B) of about $0.66R_BC_B$. The output pulse frequency is simply $1/(T_A+T_B)$. Since T_A and T_B can be adjusted separately, the circuit's output duty cycle can be varied over nearly a full 100% range. The values of the timing resistors and capacitors have the same limitations as those for the one-shot circuit of Fig. 2. Again, the diodes assure fast capacitor discharge.

This simple pulse generator can be made to produce delayed trigger pulses by utilizing the other half of the 4013-type flip-flop, as shown in Fig. 4(b). Additionally, the on-time of the pulse generator can be extended.

With the switch in the TRIGGER position, the Q1 output will remain high for a period (T_A) of approximately $0.66R_AC_A$ seconds. This signal activates the S2 line so that Q2 goes high and resets Q1. The Q2 output stays high for a period (T_C) of about $0.66R_CC_C$ second, and the Q1 output stays low for a period (T_B) of around

$0.66R_BC_B$ second. The cycle repeats after the T_B period is complete.

With the switch in the EXTEND position, the Q1 output remains high for a period of $T_A + T_C$ before it is reset. The Q2 output again goes high at the end of the T_A period until T_C seconds have passed. Then the off-time period of T_B begins. The position of the switch, therefore, determines whether the delayed pulse at Q2 is within the on-time frame of the Q1 pulse or occurs immediately after the Q1 pulse.

A variation of this delayed trigger-pulse circuit enables a single 4013-type flip-flop to perform as a duty-cycle modulator, as in Fig. 5(a). When D1 is low, the circuit behaves exactly like the one of Fig. 4(b) with the switch in the TRIGGER position—namely, the output at Q1 will be high for T_A seconds and low for T_B seconds. However, if T_B is greater than T_C and D1 is high, the on-time of the Q1 output will still be T_A, but the Q1 off-time will be T_C because of the feedback path between $\overline{Q2}$ and CLK1.

The circuit, therefore, can be used to modulate the duty cycle of the control signal at D1. The off-time of the output will be alternated between T_B and T_C, and the ratio of T_B to T_C can be very large. Capacitor C_1, which is typically 150 picofarads, is needed to delay the pulse to CLK1 so that the reset signal does not override the clock signal.

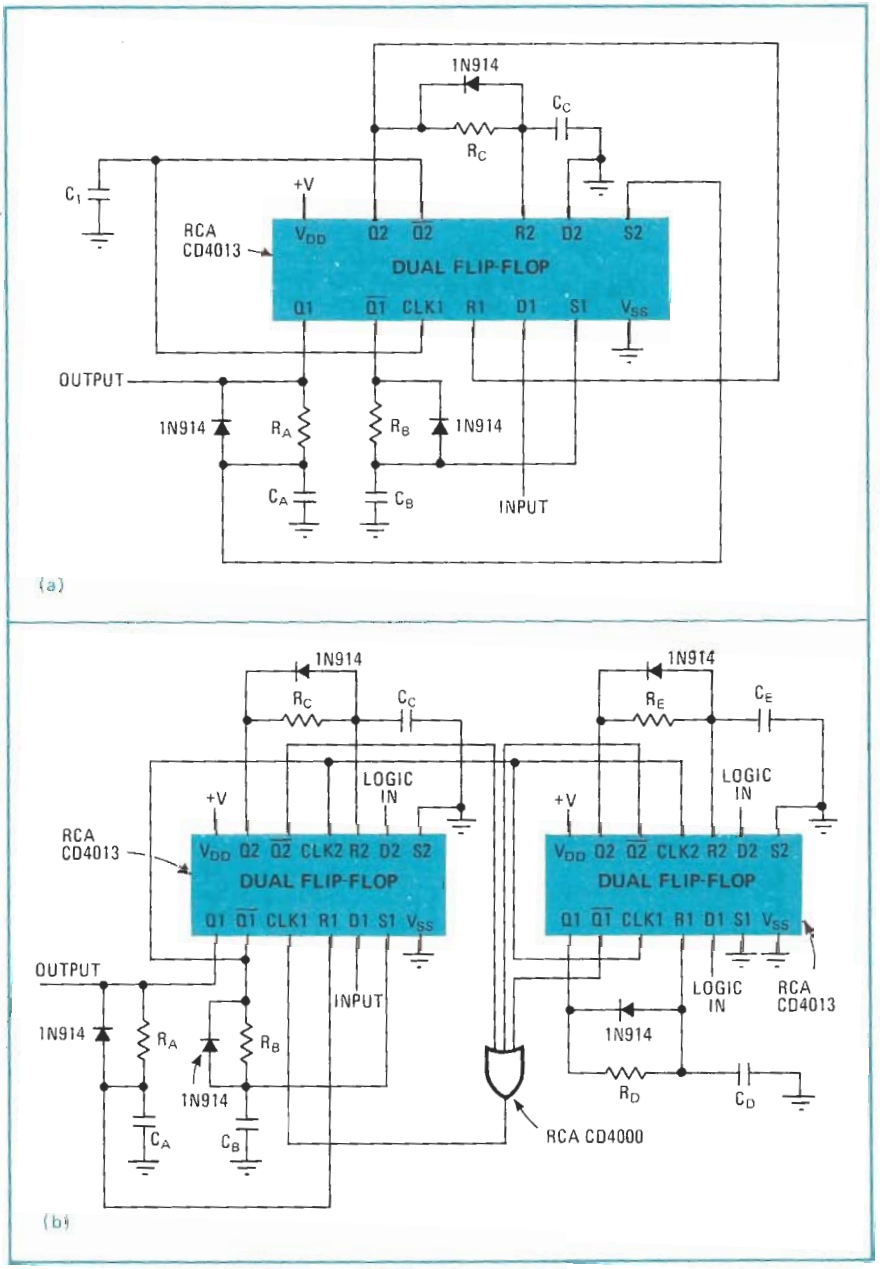
With a second flip-flop package, a more complex duty-cycle modulator can be built. In the circuit of Fig. 5(b), the control signal is applied to the D1 terminal of the left-hand flip-flop. The on-time of the output waveform remains unchanged at T_A seconds, but the off-time depends on the voltage level present at the LOGIC IN data terminals of the flip-flops when the Q1 output is reset.

If the D2 data input of the left-hand flip-flop and both data inputs of the right-hand flip-flop are all grounded, the off-time will be T_B seconds. Placing a logic high on the D2 input of the left-hand flip-flop produces an off-time of T_C seconds. Similarly, a logic high on either the D1 or D2 input of the right-hand flip-flop gives an off-time, respectively, of either T_D or T_E seconds. The circuit, therefore, performs as a logic-controlled duty-cycle modulator.

Other C-MOS flip-flops

As this article has demonstrated, the 4013-type C-MOS flip-flop can be used to implement low-power pulse circuits with relative simplicity. The device's four input terminals—data, clock, set, and reset—in addition to its high input impedance and threshold voltage levels, permit its inputs and outputs to be connected in a variety of ways.

The 4027-type C-MOS flip-flop, a dual J-K device having set/reset capability, offers even greater flexibility than the 4013 type because its J and K logic inputs are additional controls over the clock input. Another versatile C-MOS flip-flop is the 4043-type quad R-S unit. With this, it is possible to build a low-power wide-range four-stage ring counter, in which all four timing periods can be adjusted individually over a broad range by simply varying resistor and capacitor values. □



5. Modulating duty cycle. A single 4013-type flip-flop can be wired as a duty-cycle modulator (a). With two flip-flops, a logic-controlled modulator (b) can be built. Here, the off-time of the output depends on the logic level present at the three LOGIC IN ports. The output on-time is the same for both of these circuits.