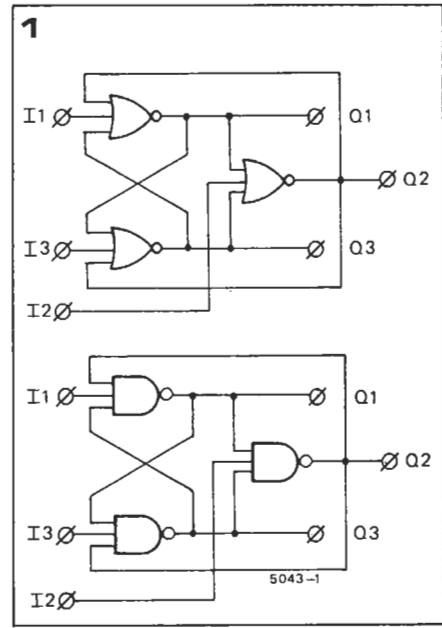
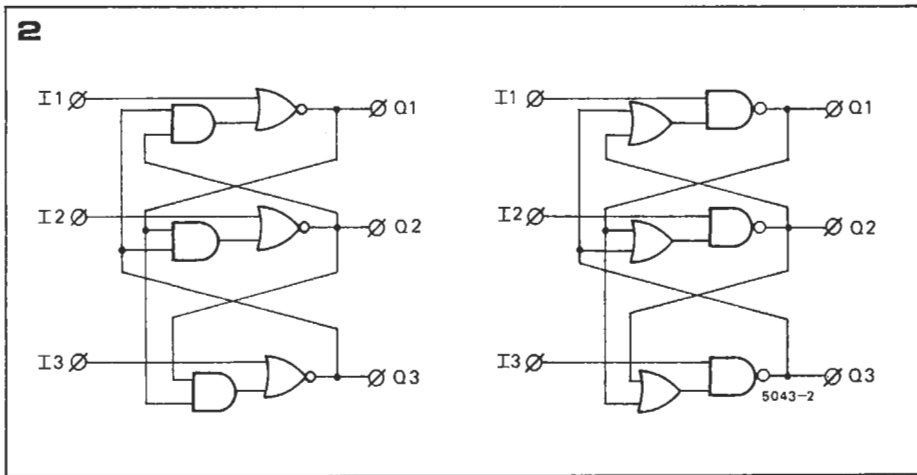


# tri-stable



It is possible to use two NAND or NOR gates to make up a flipflop - a circuit with two stable conditions. The process can be extended to obtain circuits with three or even more stable states.



The arrangements shown in figure 1 both have 3 stable states. The state taken up by the outputs will depend on the input conditions applied. These circuits have the objection that correct operation is only guaranteed when drive is applied to two of the inputs at once (see table 1).

It is however possible to modify the circuits so that a single input drive will produce the desired output state. The circuit as a whole becomes more extensive; but it becomes easier to use. Figure 2 shows the modified arrangement. The operation of this circuit can be followed from table 2.

Figure 3 shows a master-slave shift register. If C is at logic '1', then the OR-gate outputs will also be '1', so that the state of Q<sub>1</sub>-Q<sub>2</sub>-Q<sub>3</sub> does not change. If C becomes '0', the AND-gate outputs will also be '0', so that the state of Q<sub>4</sub>-Q<sub>5</sub>-Q<sub>6</sub> is held.

Suppose for example that C is logic '0', with I<sub>1</sub> = '0', I<sub>2</sub> = '0' and I<sub>3</sub> = '1'. We find that Q<sub>1</sub> = '1', Q<sub>2</sub> = '1' and Q<sub>3</sub> = '0'. Since C is '0' the state of Q<sub>4</sub>-Q<sub>5</sub>-Q<sub>6</sub> is maintained. If C now goes to '1', the outputs Q<sub>1</sub>, Q<sub>2</sub> and Q<sub>3</sub> will not change. This state is also the state at the inputs I<sub>4</sub>, I<sub>5</sub> and I<sub>6</sub>. Q<sub>4</sub> therefore becomes '0', Q<sub>5</sub> also '0' and Q<sub>6</sub> '1'. This shows that the input information '0'-'0'-'1' appears, after one clock pulse, at the output. ◀

NOR gates						
I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
0	0	0	x	x	x	
1	1	0	0	0	1	
1	0	1	0	1	0	
0	1	1	1	0	0	
1	1	1	0	0	0	

NAND gates						
I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
0	0	0	1	1	1	
0	0	1	1	1	0	
0	1	0	1	0	1	
1	0	0	0	1	1	
1	1	1	x	x	x	

Table 1

NOR gates						
I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
0	0	0	x	x	x	
1	0	0	0	1	1	
0	1	0	1	0	1	
0	0	1	1	1	0	
1	1	1	0	0	0	

NAND gates						
I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	
0	0	0	1	1	1	
0	1	1	1	0	0	
1	0	1	0	1	0	
1	1	0	0	0	1	
1	1	1	x	x	x	

Table 2

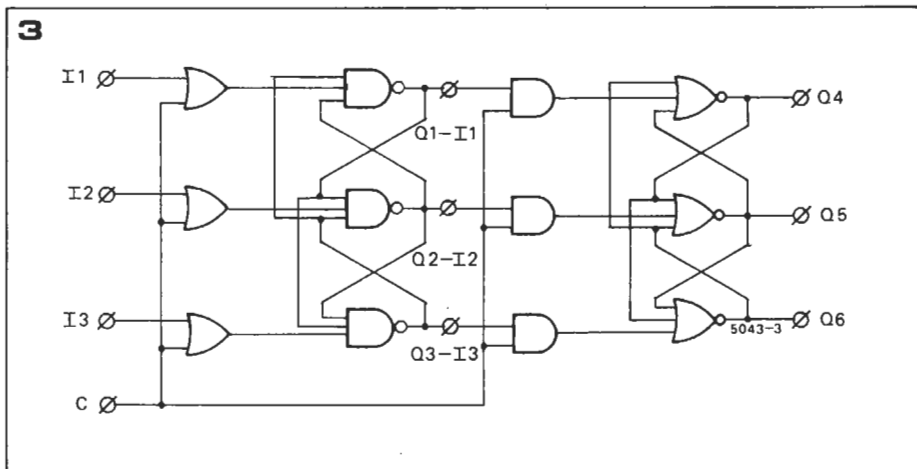


Table 3