Operating a logic gate as a flip-flop

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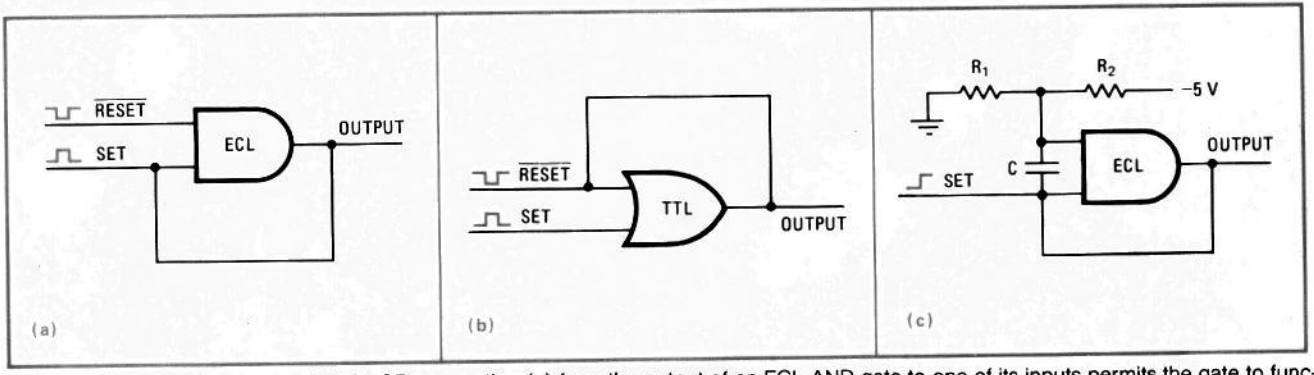
Did you ever need just a single flip-flop, and find that all you have left on your circuit board is one unused gate? Or, perhaps space is your problem—you have room for one more gate, but can't fit a flip-flop.

Here's a way to make that unused gate behave as though it were a flip-flop. The technique relies on the wired-AND capability of a TTL gate, and the wired-OR capability of an ECL gate.

If the outputs of two or more TTL gates are tied together, then the resulting wired-AND connection will go high only when the outputs of all the gates are high. Similarly, if the outputs of two or more ECL gates are joined together, the resulting wired-OR junction will become high when any one of the gate outputs go high.

An ECL AND gate (a), then, that has its output tied back to one of its inputs will act like a flip-flop. The gate's $\overline{\text{RESET}}$ input is normally high, and a negative-going pulse on this $\overline{\text{RESET}}$ input causes the gate's output to go low. On the other hand, a positive-going pulse at the



Getting a bistable from a gate. Wired-OR connection (a) from the output of an ECL AND gate to one of its inputs permits the gate to function as a flip-flop. For a positive SET pulse, the output is high; for a negative $\overline{\text{RESET}}$ pulse, the output is low. Similarly, a TTL OR gate (b) with a wired-AND connection to one of its inputs also acts as a flip-flop. A simple RC network (c) can be added to produce a one-shot.

SET input will make the output go high. The wired-OR connection at the output will keep the SET line high, thus latching the gate until the next RESET pulse comes along. (Note that the SET input is forced high, a condition that may be unacceptable for some circuits.)

A TTL OR gate (b) that has an open-collector output can be made to operate similarly. In this case, the gate's output is tied to its RESET input line. For the single-gate TTL flip-flop, a negative-going RESET input pulse causes the output to go low, and a positive-going SET input pulse produces a high output.

With a slight modification, the flip-flops can be operated as one-shots. The circuit of (c) shows what this easy-to-add modification looks like for the ECL AND gate.

The one-shot is triggered by a positive-going edge at its SET input. This keeps both inputs high until the capacitor has discharged through resistor R_1. The two resistors, R_1 and R_2, form a voltage divider that is connected between ground and -5 volts to bias the gate's input lines to a logic low. (For the TTL one-shot, resistor R_2 can be eliminated.)

Both flip-flops and the one-shot have an interesting and rather unusual feature—there is no gate delay between one of the inputs and the output. Either flip-flop does have one important limitation, however—one of its input lines is forced to follow the output. □