Simple gating circuit marks both pulse edges

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A bidirectional edge detector can be built from only two integrated-circuit packages—or with only one package if exclusive-OR gates are used. Applications for the circuit include triggering for event counters and frequency doubling for digital data communications.

The configuration for the standard edge detector is drawn in black in (a). If NAND gates are used, as indicated here, the circuit responds to positive-going edges. If NOR gates are used, it detects negative-going edges.

When the input signal is low, the output of gate G_4 will be high. And when the input becomes high, G_4's output goes low one gate propagation delay later. Meanwhile, the input signal ripples through gates G_1, G_2, and G_3, causing G_3's output to go low after three gate delays. The output of G_4 then become high again one gate delay later. This means that G_4's output is a negative pulse that is three gate delays wide. The four gates, therefore, mark the positive-going edges of the input.

Adding three NOR gates to this standard circuit, as shown in color in (a), enables the circuit to mark both positive and negative edges. Gate G_5, together with gates G_1, G_2, and G_3, form a negative-edge detector. Gate G_6 simply inverts the output from gate G_4, while gate G_7 simply sums and inverts the detected edges.

The same dual edge detection can be obtained from a single quad exclusive-OR gate package when the gates are connected as indicated in (b). Or, an equivalent circuit can be constructed by hooking up three inverters and four NAND gates, as in (c).

The timing diagram shows the key waveforms for all the circuits. □

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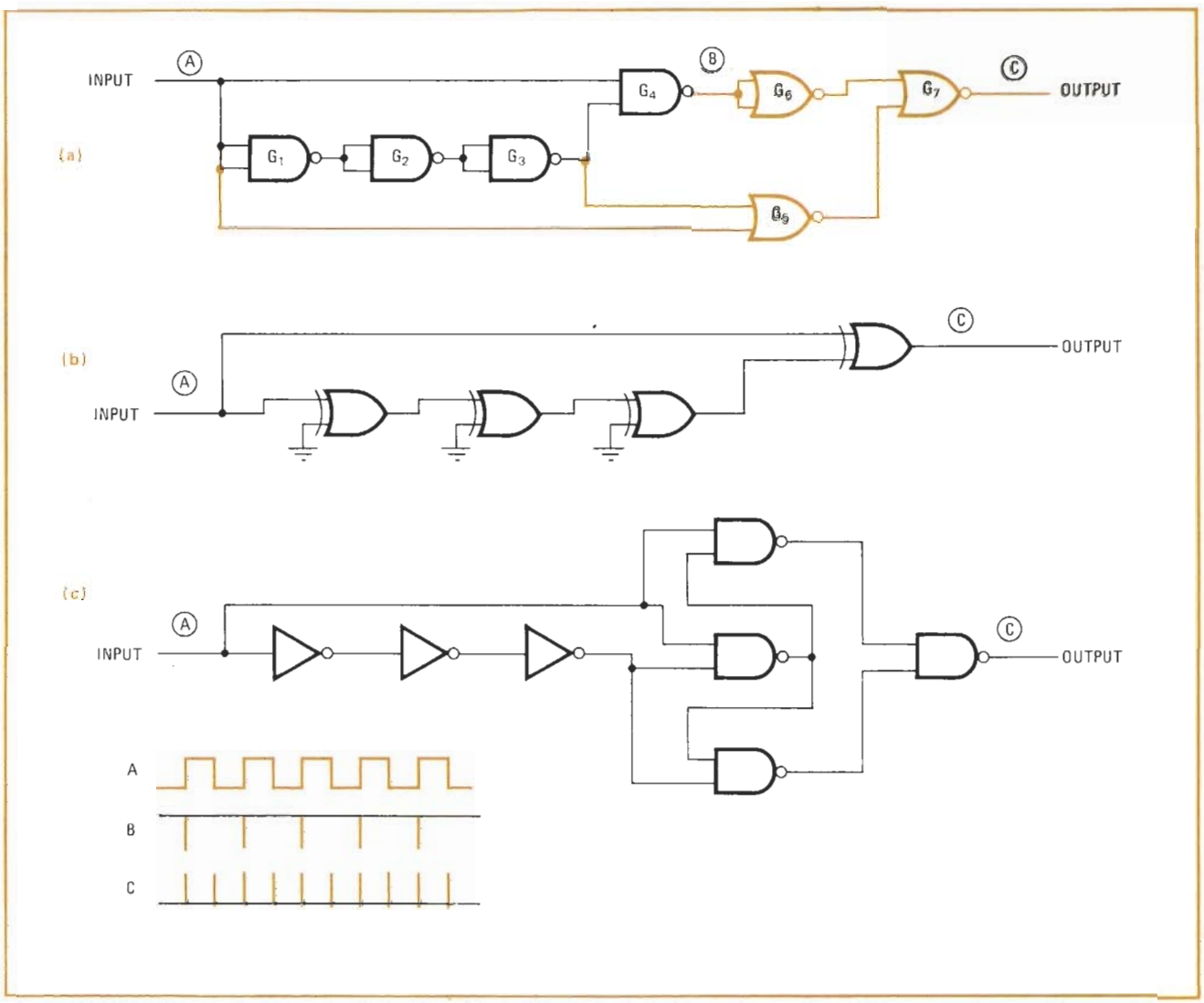

Noting each pulse-edge direction. Both positive and negative pulse edges can be detected with the same circuit by adding the three gates drawn in color in (a) to a standard unidirectional edge detector (drawn in black). If exclusive-OR gates are used, as in (b), the bidirectional edge detector requires only one IC package. Inverters and NAND gates, as in (c), can also provide the same circuit function.

ing bias tracks the forward blocking voltage of diode D_1 as the temperature changes.

Because of this temperature-compensating arming bias, it is possible to realize constant detection efficiency over a wide temperature range, in addition to a constant rf threshold detection level. For a constant rf input of 55 mV, the detection voltage developed by the circuit varies only 1.8 mV between −20°C and +90°C. Rf peak voltages as large as 80 mV can be detected quite efficiently.

The operational amplifier at the output of the circuit senses the detection voltage and translates it to a 12-volt level. This output voltage varies only 2.1% from −20°C to +90°C for a constant rf input drive. Here, the op amp's gain is 40 dB, a figure that can be safely increased to 50 dB without adversely affecting the output stability of the circuit.

The circuit's performance will be further enhanced if the detector is made insensitive to variations in supply voltage. This can be done by adding a current source (shown in color in the diagram). The current source keeps the rf threshold voltage constant, despite supply variations of ±0.5 V. In connecting this source, resistor R_1 must be omitted. □