Exclusive-OR gate and flip-flops make half-integer divider

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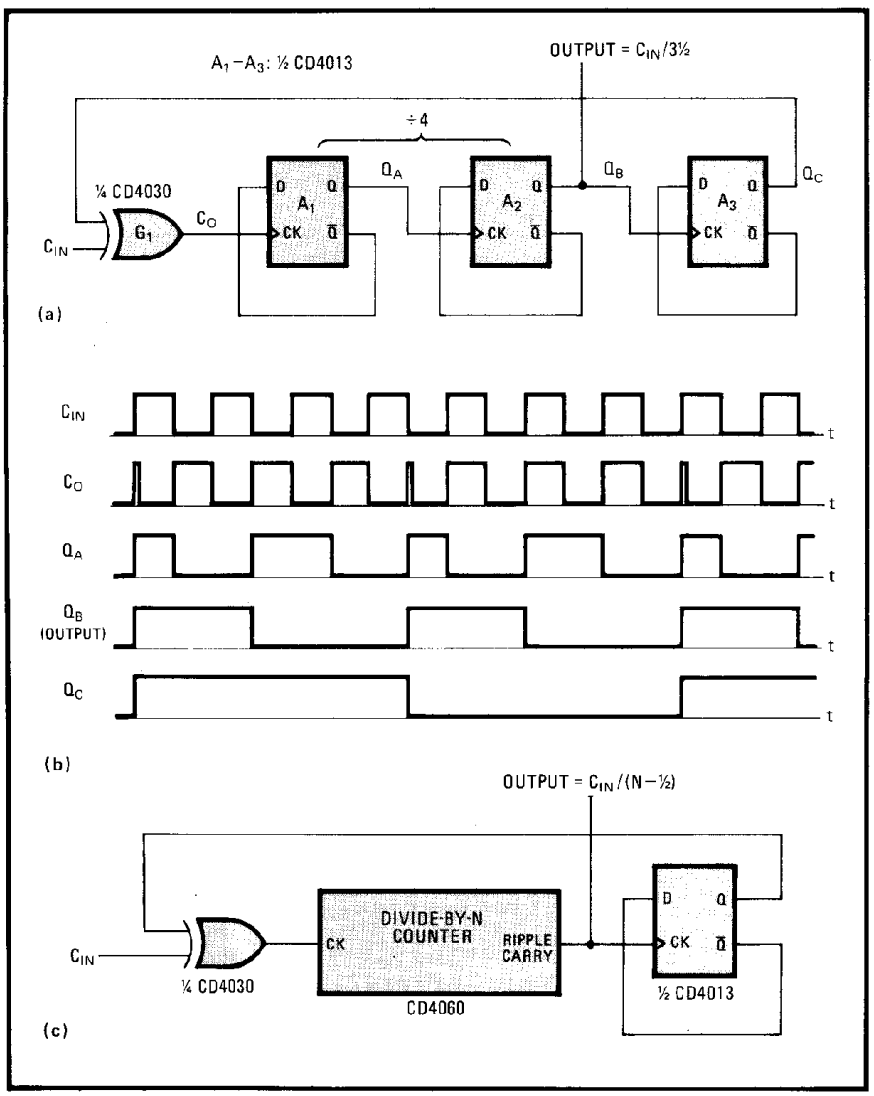
A simple and inexpensive divide-by-(N − ½) counter can be built with D flip-flops and an exclusive-OR gate. The circuit uses very few parts, largely because, unlike many such dividers, it does not rely on a collection of monostable multivibrators. Nor are there difficult timing considerations, which would also complicate the circuit and act to increase its parts count.

Various logic circuits need to be driven by what may be termed a half-integer clock signal that is derived from a master clock. For instance, the MM-57100 video-game integrated circuit is driven by a 1.0227-megahertz signal, which the chip's manufacturer (National Semiconductor Corp.) recommends be derived from the television set's 3.579545-MHz color-burst crystal oscillator. This application requires a divide-by-3½ counter, which may be built by modifying a divide-by-4 circuit as shown in Fig. 1a.

Flip-flops A_1 and A_2 form the divide-by-4 counter. The master clock, C_{IN}, drives A_1 through the exclusive-OR gate, G_1. However, the output state of G_1 is additionally controlled by A_3.

As a result, A_3 converts the divider to a divide-by-3½ counter. A_3 is situated in the feedback loop such that it enables generation of a short pulse at C_O for every 3½ counts of C_{IN}. The pulse is generated if C_{IN} either falls to logic 0 or rises to logic 1, which depends on the state of Q_C. Its shortness is due to the delay between the initial



Half-integer divider. Divide-by-3½ counter is divide-by-4 circuit modified by flip-flop A_3 and exclusive-OR gate G_1 (a). Timing diagram details operation (b). Method may be extended to form a divide-by-(N − ½) counter by replacing flip-flops A_1 and A_2 by ripple-carry, divide-by-N counter (c).

0-to-1 transition of C_O (caused by C_{IN}) and the change of state of Q_C—as Q_C changes state, it disables gate G_1, causing C_O to fall almost immediately after it has reached logic 1. The timing diagram given in Fig. 1b details circuit operation.

This method may be extended to the general case of the divide-by-(N − ½) counter, as shown in Fig. 1c, simply by substituting a single synchronous or asynchronous counter for the flip-flops A_i that would otherwise be required. □