CMOS

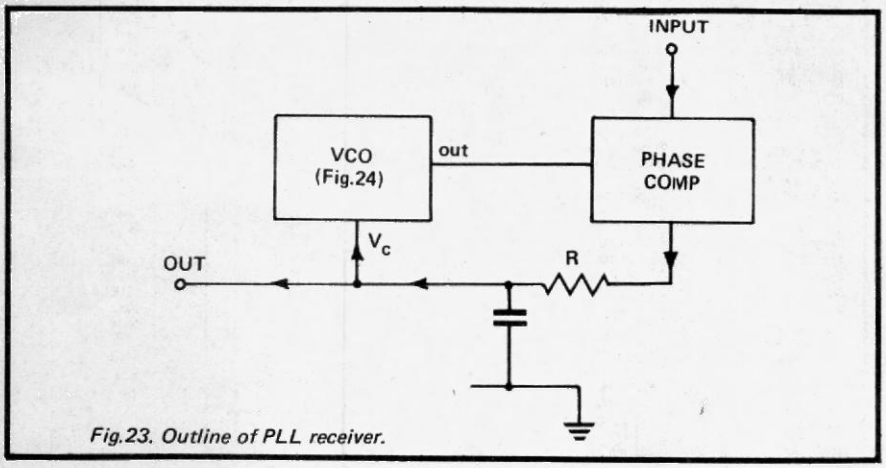


Fig.23. Outline of PLL receiver.

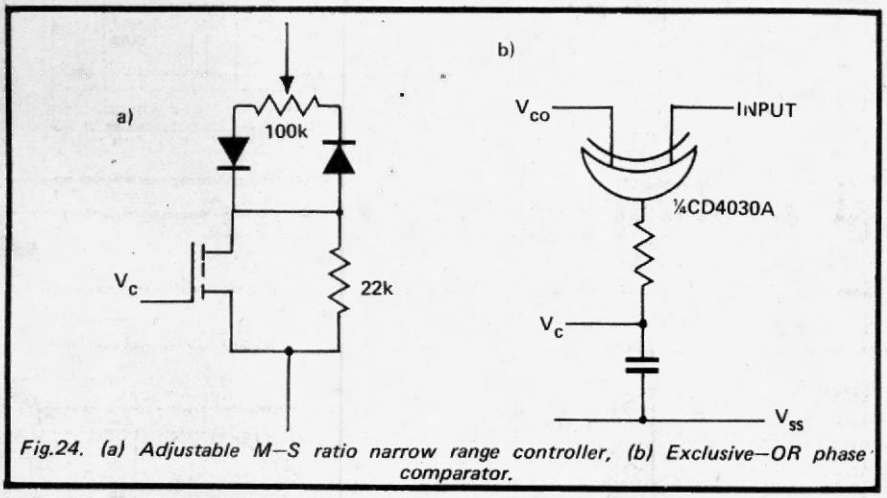
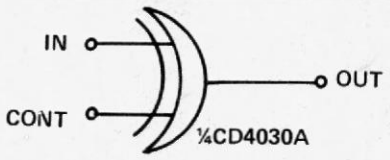


Fig.24. (a) Adjustable M–S ratio narrow range controller, (b) Exclusive–OR phase comparator.

Fig.25. Exclusive–OR gate used as a conditional inverter together with the device's truth table.

IN-1	IN-2	OUT
0	0	0
0	1	1
1	0	1
1	1	0



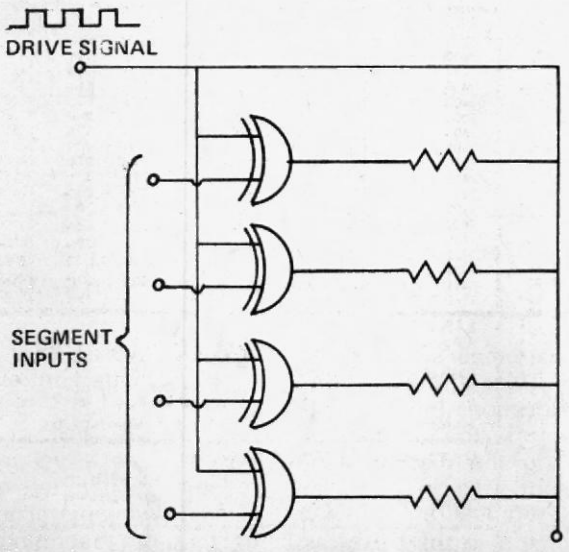


Fig.26. Exclusive–OR gates driving liquid crystal segments, represented by resistors.

the FET. As V_c varies between V_{DD} and V_{SS} so the resistance of the FET varies between about 1k and 1000MΩ. If the upper value is limited to 10MΩ by making R_T that value, then the circuit will sweep over a 10000 : 1 range in frequency. There would seem to be scope here for experimenting with a pulse frequency modulation communications system. One might produce an analogue system although distortion would probably be high due to mismatching. The transmitter could be the circuit in fig. 22 and the receiver a phase locked loop along similar lines (fig. 23) using some sort of phase comparator and a low-pass R-C filter.

EXCLUSIVE-OR GATES

Exclusive-or gates, for example the 4030 (see fig. 2) will function as phase comparators but they require a unity mark-space ratio to be effective. Perhaps a voltage controlled oscillator might be designed with a narrower range along the lines of fig. 24 for both transmitter and receiver, together with a phase comparator and low pass filter as shown in fig. 24. While we are on the subject of the exclusive-or function we shall consider two more uses of these devices. Fig. 25 shows the exclusive-or truth table and its use as a conditional inverter. This configuration causes the input signal to be inverted when the control input is high but not when it is low.

Liquid crystal displays are undoubtedly the readout devices of the future but they last longer in general if an a.c. drive is used. If then a square wave is applied to one end of a liquid crystal segment and also to the other connection via a conditional inverter (see fig. 26) then the control input will decide whether or not there is a net voltage across the segment.

CMOS and liquid crystal make an ideal combination for ultra-low power logic and display systems and so manufacturers have produced BCD to seven segment decoders and drivers specifically for this application. Their type numbers are 4054/5/6, the variations being due to the addition of latches and other refinements. These devices have too limited an appeal to justify a full description here and it is suggested that if it is intended to experiment with this technology, data sheets should be obtained from a manufacturer* or large distributor.

*e.g. RCA, Sunbury-on-Thames, Middlesex, for the "CD4054/5/6A" range. *Continued next month...*

"high" the bottom FET is turned on and the top one off. Thus the output voltage is held very low. When the input is low the FETs reverse roles and the output is high. Now look at fig. 16 which shows the internal circuitry of the 4007. You should be able to see how joining a few pins together will allow three separate inverters to be produced. Reference to fig. 17 will reveal how several other gates may be produced and their mode of operation should be relatively easy to discern.

TRANSMISSION GATES

There is another way of connecting two FETS which produces a result unique to CMOS. This is the transmission gate (fig. 18). Here, due to the inverter, both FETS are either on or off simultaneously. When they are on, the path between input and output (they are interchangeable) may be regarded as a resistor of about 500-1kΩ whereas when they are off the equivalent value is about 1000MΩ.

Thus the device behaves as a switch capable of passing analogue signals with very little distortion provided that the load resistance is fairly high (≈100kΩ). We shall have more to say about these "bilateral switches" later but while we are dealing with the 4007 fig. 19 shows how to connect one as a single pole-double throw switch which will pass analogue signals in both directions.

Any of the three or less inverter circuits we have mentioned to date may be realised with a 4007, as may several more interesting designs. Fig. 22 shows a linear frequency to voltage converter which works by charging a capacitor up once for every input cycle, the charge to do so being passed by a MOSFET into a summing amplifier. The component values given are based on an approximate five volt output for the given frequency. The resistor R1 should be made a 100kΩ preset if it is required to set a range exactly. The capacitor C2 "smooths" the output and need not be changed from 10μF if fast response on the upper ranges is not needed. The linearity achieved on the top range will depend on the particular "741" used and if reliable operation is required a higher speed op-amp should be used.

Fig. 21 shows an alternative monostable multivibrator. We have already given a number of multivibrator circuits and so we shall say nothing more about this one except

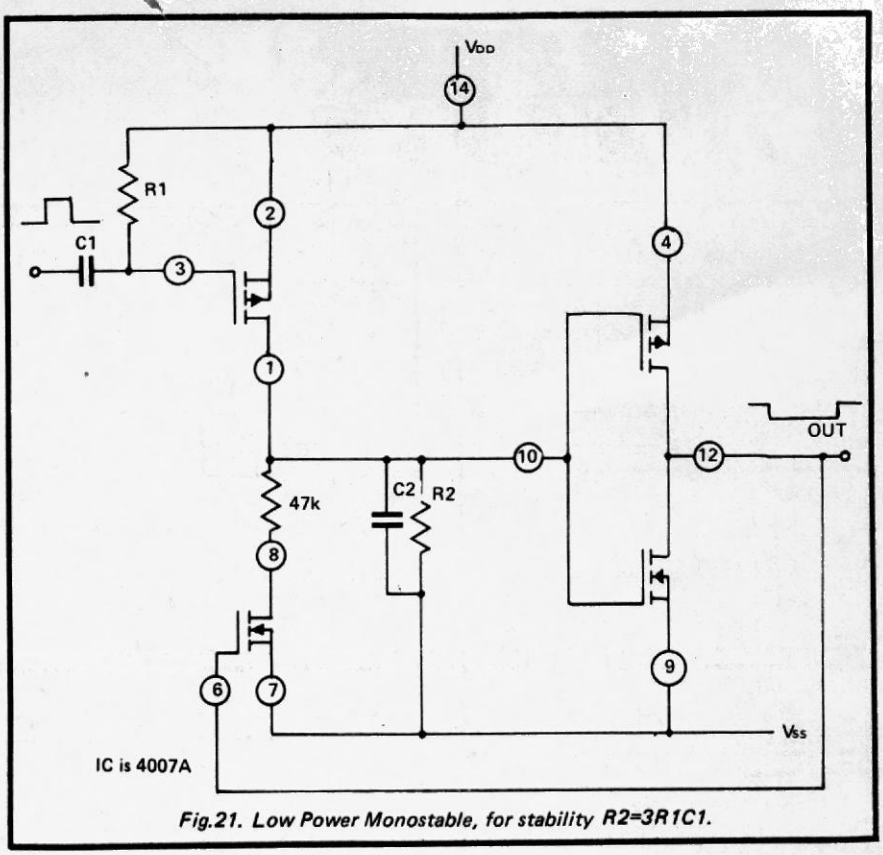


Fig.21. Low Power Monostable, for stability R2=3R1C1.

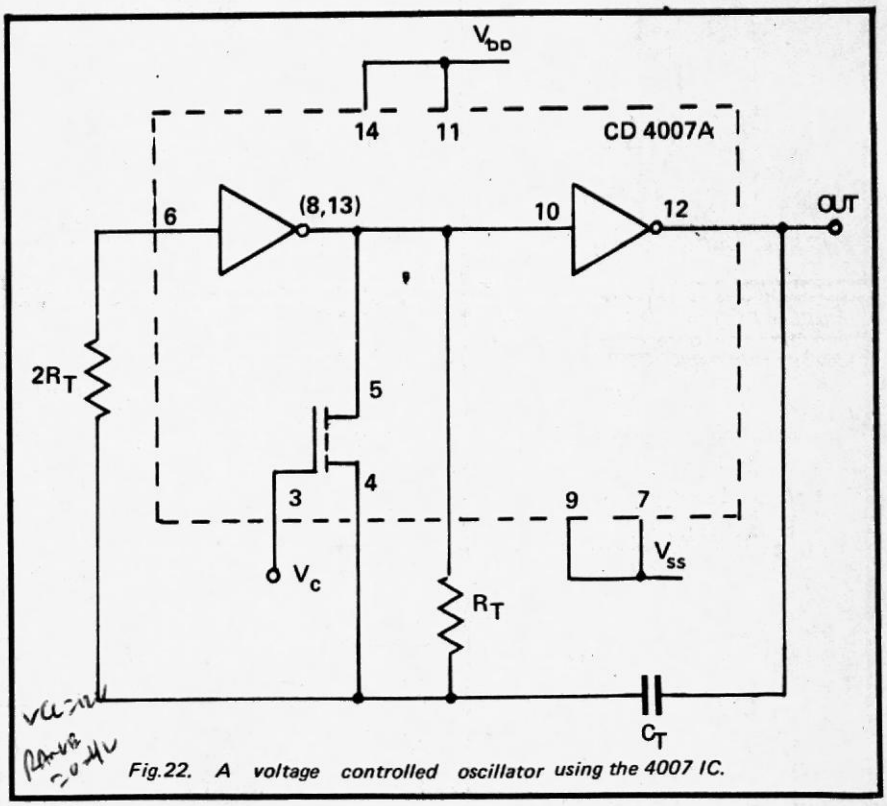


Fig.22. A voltage controlled oscillator using the 4007 IC.

that it has an extremely small power consumption. This is due to the feedback connection (pins 12-6) which turns off the n-channel MOSFET during the discharge of the time constant. This circuit is also an interesting demonstration of the use of components in the 4007 as discrete transistors.

A WIDE RANGE VCO

The voltage controlled oscillator depicted in fig. 24 uses two inverters as well as a separate transistor as a voltage controlled resistor. The inverters function as an astable multivibrator in the manner of Fig. 4 but the timing resistance is the parallel combination of R_T and