Cross-coupled gates prevent push-pull-driver overlap

Richard Rice, Oconomowoc, WI

Overlap—the short period during which a push-pull drive's two transistors are both simultaneously on—is a common problem with these drives in a center-tapped transformer's primary. Overlap causes a large current spike and increased switching losses. The fact that saturated transistors turn off more slowly than they turn on causes the problem. One method of preventing overlap is to provide a time delay after turning off one transistor and before turning on the other one. This method requires several extra components and must include enough delay for a worst-case scenario. This Design Idea uses cross-coupled gates to prevent one transistor from turning

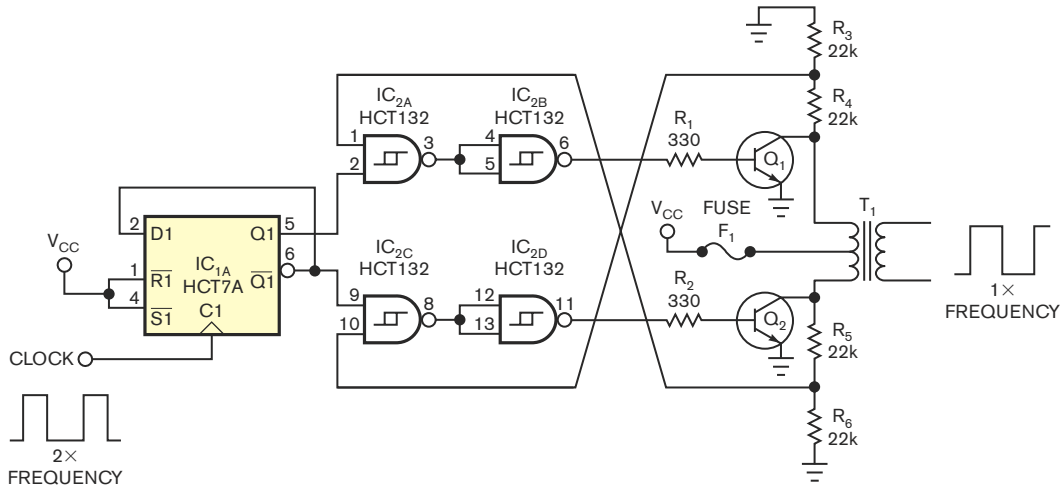

Figure 1 Cross-coupled gates prevent one transistor from turning on before the other turns off. Fuse F_1 protects against catastrophic failures.

on before the other turns off (**Figure 1**). For simplicity, the **figure** omits the depiction of bypass capacitors, snubber networks, and other components unnecessary for illustrating the method.

Gate IC_{2A} prevents Q_1 from turning on until Q_2 turns off. Likewise, gate IC_{2C} prevents Q_2 from turning on until Q_1 turns off. Gates IC_{2B} and IC_{2D} function as inverters to provide the correct polarity to drive the switching transistors. Monitoring the transistors' collector voltages senses the turn-off of each transistor using the voltage dividers R_3/R_4 and R_5/R_6. Because the collector voltage swings to twice the supply voltage, the voltage dividers halve the voltage. The impedance of the voltage dividers also limits the gates' input current to a safe level during overshoot.

The switching frequency is one-half the input-clock frequency. D-type flip-flop IC_{1A} divides the input-clock frequency by two and provides complementary outputs with a 50% duty cycle. The complementary outputs drive the switching transistors in an alternating sequence. The secondary of transformer T_1 provides an isolated square-wave output. EDN