Cascaded flip-flops set periodic-sequence generator

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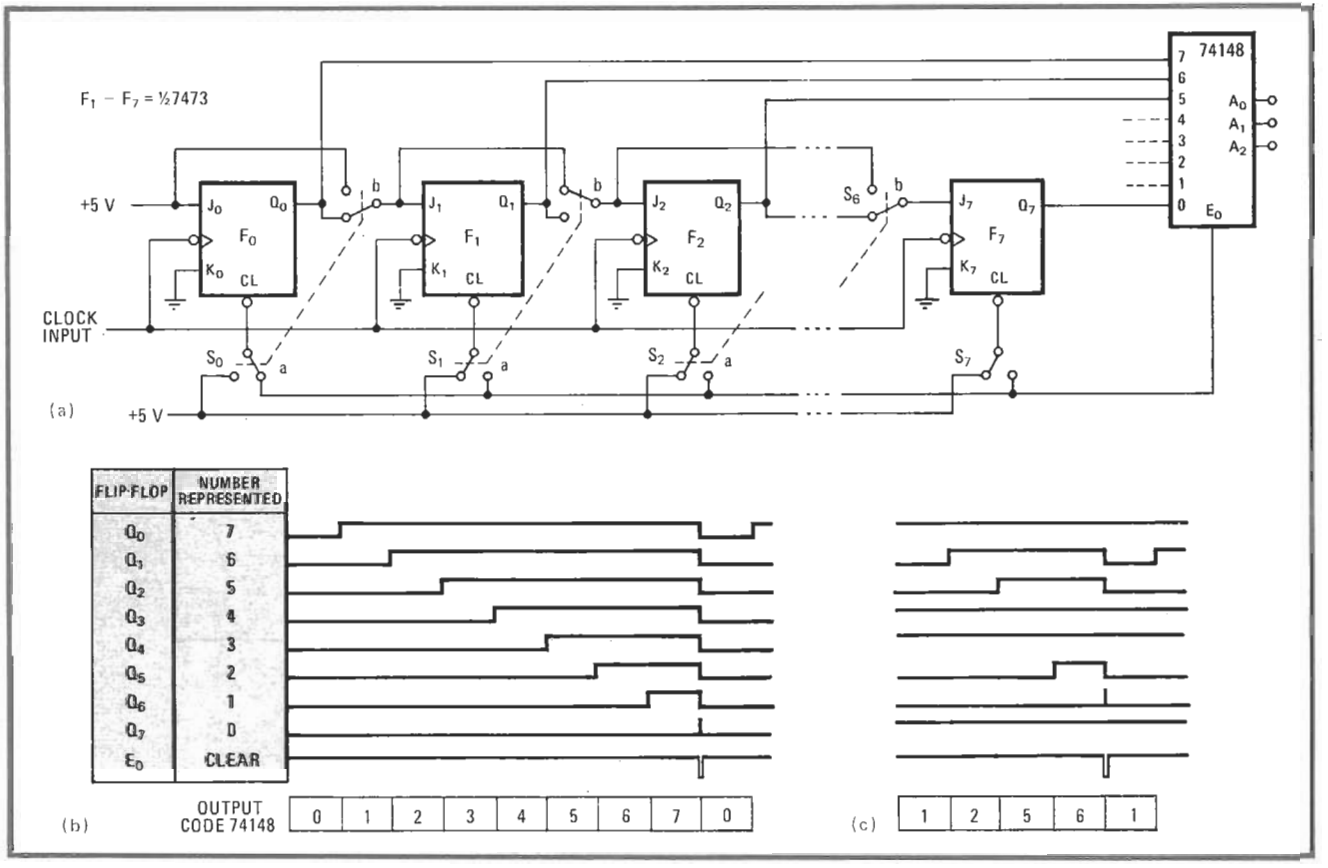
This circuit, which generates a periodic sequence of nonconsecutive binary numbers, will serve well as an address generator in multiplexed data-communications systems. Using several J-K flip-flops whose outputs drive a priority encoder, the circuit produces a selectable, monotonically increasing output code having zero dead time (no lag) between numbers. Implementing this circuit is far simpler than modifying a standard binary-counter circuit, which is more useful in applications where the numbers to be generated are consecutive.

As shown in (a), a double-pole, double-throw switch is required for all but the last flip-flop desired, which requires a single-pole, double-throw switch. In this case, seven flip-flops are used—thus the numbers 0 through 7 can be generated.

When each flip-flop is active (Q disconnected from the J port of its succeeding 7473 flip-flop and its clear port connected to E_0 of the 74148), the sequence generator will advance in order from 0 through 7, as shown in (b). At the end of the sequence, when all inputs to the 74148 are high, E_0 moves high, clearing all flip-flops and



Chosen order. Periodic-sequence generator (a) produces selectable, monotonically increasing binary output code (b) having zero dead time. Any number can be omitted from the sequence (c) by using double-pole, double-throw switches to disconnect Q output of the flip-flop corresponding to that number from succeeding flip-flop and bringing its clear port to 5 V.