USING CMOS SWITCHES FOR.....

by Jerry Whitmore

LOW-COST SAMPLE-HOLD

The sample-hold circuit shown in Figure 1 uses an AD7510K quad analog CMOS switch, two IC op amps (AD301A and AD741K), and a handful of miscellaneous components.* The circuit consists of a capacitor-to-ground, unloaded by a unity-gain follower (A2), in a feedback loop. During *sample*, the output of the follower is fed back to the negative input of op amp A1, while the signal is applied to the + input. The output of A1 must do whatever it can to force the voltage on C2 (hence the output) to track the input. During *hold*, the loop is opened, and the charge remains on the capacitor (except for leakage).

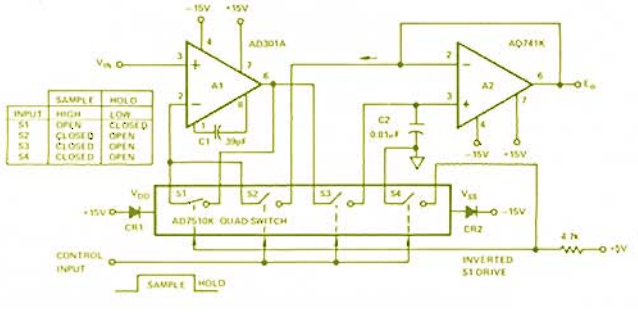

Figure 1. Schematic diagram of sample-hold circuit. Parts cost (purchased in 100's) is less than $16.

Switching is performed by an AD7510 quad switch. S4 inverts the logic applied to S1; it is closed when S2 & S3 are open (*hold*), and open when they are closed (*sample*). In *hold*, S1 connects A1 as a follower, S2 disconnects A1's –input from the output of A2, and S3 disconnects A1's output from the capacitor. In *sample*, S1 opens the local loop around A1, S2 connects the output of A2 to the –input of A1, and S3 connects the output of A1 to C2 (+ input of A2).

In *hold*, the leakage rate, $dV/dt = I_{LKG}/C$, is dominated by the op amp's bias current, 75nA, and is about 7.5mV/ms. This means that for 8-bit accuracy (½LSB = 0.2%FS ≅ 20mV), a signal could be held for more than 2.5ms without excessive degradation. For conversion rates of 5-10kHz, the total signal degradation due to this droop would only be about 0.02%FS.

Dynamic error (*sample* to *hold*) is determined by the switch *aperture time* (~700ns) and the maximum rate-of-change of the signal (Figure 2). For sine waves with full 20Vp-p amplitude, aperture errors are less than ½LSB of 8 bits for frequencies up to 300Hz, and proportionally less for lower-level inputs (slower changes).

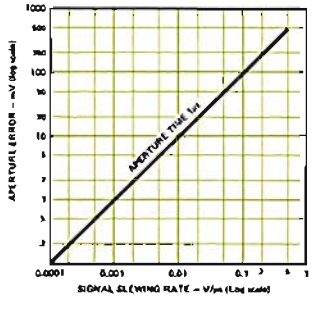

Figure 2. Aperture error as a function of input-signal slewing rate (within response capability of the system).

*For information on the quad switch and op amps, request **L15**. For information on complete sample-holds manufactured by Analog Devices, request **L20**.

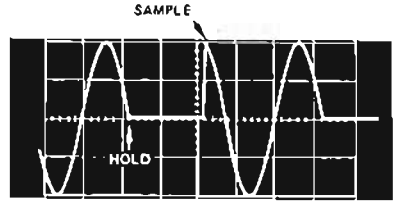

Figure 3. Typical waveforms of sample-hold circuit. Sinewave input is 20Vp-p, 2kHz. Vertical scale is 5V/division; horizontal scale is 200µs/division. Hold-to-sample is slew-rate limited.

During *sample*, small-signal bandwidth (–3dB) is 130kHz, limited principally by C_2 and the R_{on} of S3. Full-power response is about 6kHz, limited by the slewing rates of the amplifiers, which also reduces 20V settling time to about 50µs (Figure 3). CR1 and CR2 protect the quad switches from failure if the input/output voltages exceed the power-supply. C1 provides phase compensation for stability when the loop is closed in *sample*.

DIGITALLY-CONTROLLED TIMING USING THE AD7501 MULTIPLEXER†

The circuit of Figure 4 provides digital control for variable time-delay generation. The 3 digital inputs, A_0 through A_2, select a resistor, R_1 – R_8, to provide time delays of 1-8 seconds in 1s increments. A negative transition at the 555 timer's trigger input starts the timing sequence. Additional intervals can be generated by stacking multiplexers and using their *enable* lines to select the appropriate AD7501. ▶▶▶

CODE	DELAY
000	1s
001	2s
010	3s
011	4s
100	5s
101	6s
110	7s
111	8s

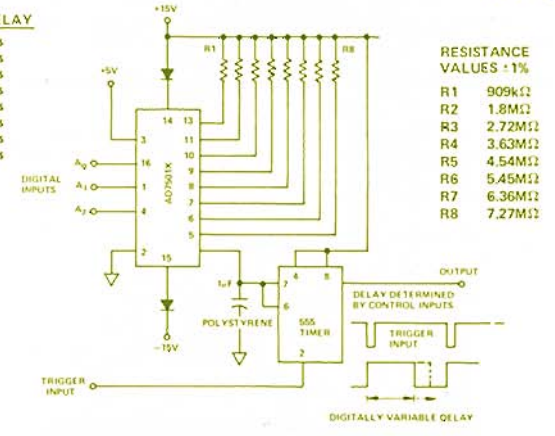

Figure 4. 8-Step digitally-controlled timer: circuit and timing diagram.

†For information on the AD7501 Multiplexer, request **L16**.