PROJECT

16K EXPANSION

NOW THAT a single chip 16384 bit memories are readily available, even if still a little (I almost wrote bit) expensive, the possibility of using only eight chips to produce a 16k byte memory would seem to be a possibility. Even at the current price of $150 for eight devices this price compares favourably with the 128 devices required if IK static memories were used. Further price reductions are certain, as shown by the 4K memories which were similar price less than a year ago and are now available for around $8 each. Dynamic memories also have the advantage of power savings, and equivalent static memory array (128 x 2102's) would consume nearly six amps at five volts compared with the mere three tenths of an amp of the dynamic array. A dynamic memory can often be added without uprating the power supplies, this would obviously not be the case if IK static devices were used.

Advantages And Disadvantages

If dynamic memories have these obvious advantages why are they not used more widely. The answer is that there are disadvantages as well. To understand how these disadvantages arise the way in which dynamic memories function requires some explanation. In a modern device each storage cell consists of a single MOS transistor and a capacitor (Figure 1), whether the capacitor is charged or discharged indicates whether the bit is a '1' or a '0'. The charge on the capacitor gradually leaks away and must be topped up or refreshed at regular intervals. Additional circuitry must therefore be used to ensure that each storage cell is refreshed at least every 2 mS, this may be effected either by a normal read or write cycle or a special refresh cycle which does not enable the chip. Also, until recently, dynamic memories required special high voltage (12V) circuitry to drive the clock inputs (chip enable).

Overall the added complexity of the refresh circuitry means that unless large memory arrays are being built it is far easier to use static devices. The 16K bit dynamic RAM now makes this effort well worth while. These devices are only available in a 16 pin package and all inputs and outputs are compatible with TTL levels so that standard TTL chips can be used throughout the refresh circuitry.

Squeezing A Quart Into A Pint Pot

Fourteen address lines are required to access 16384 bits, four pins are required for power supplies, two pins to get data in and out and one to indicate whether data is to be read from or written to the device. This makes a total of 21 lines,so how are they squeezed into a 16 pin package? The ingenious answer is to split the 14 address lines into two sets which then require only seven pins. The first seven bits, known as the row address, are stored internally by a signal on the row address strobe (RAS). The remaining seven bits can then be applied to the same pins and again stored by the column address strobe (CAS). This switching or multiplexing of the address lines adds further complication to the circuitry but not as much as might be expected because the refresh addresses also have to be multiplexed onto the same pins. (See Fig.2.).

One advantage of this arrangement is that similar pin configurations can be used for the 4K, 16K and even the much publicised 64K memories.. The last of these only used a single voltage power supply and therefore has two spare pins for the extra address bits. Motorola's version even has provision for automatic refreshing which would eliminate this major disadvantage.

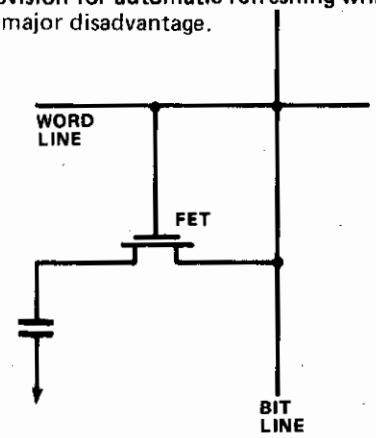


Fig 1. A typical memory cell circuit.

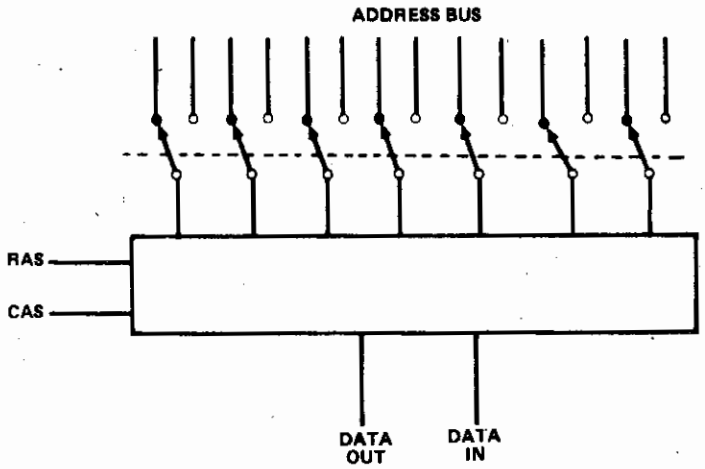


Fig 2. How the chip multiplexes 14 address lines onto 7 pins. The switches are incorporated in the IC itself.

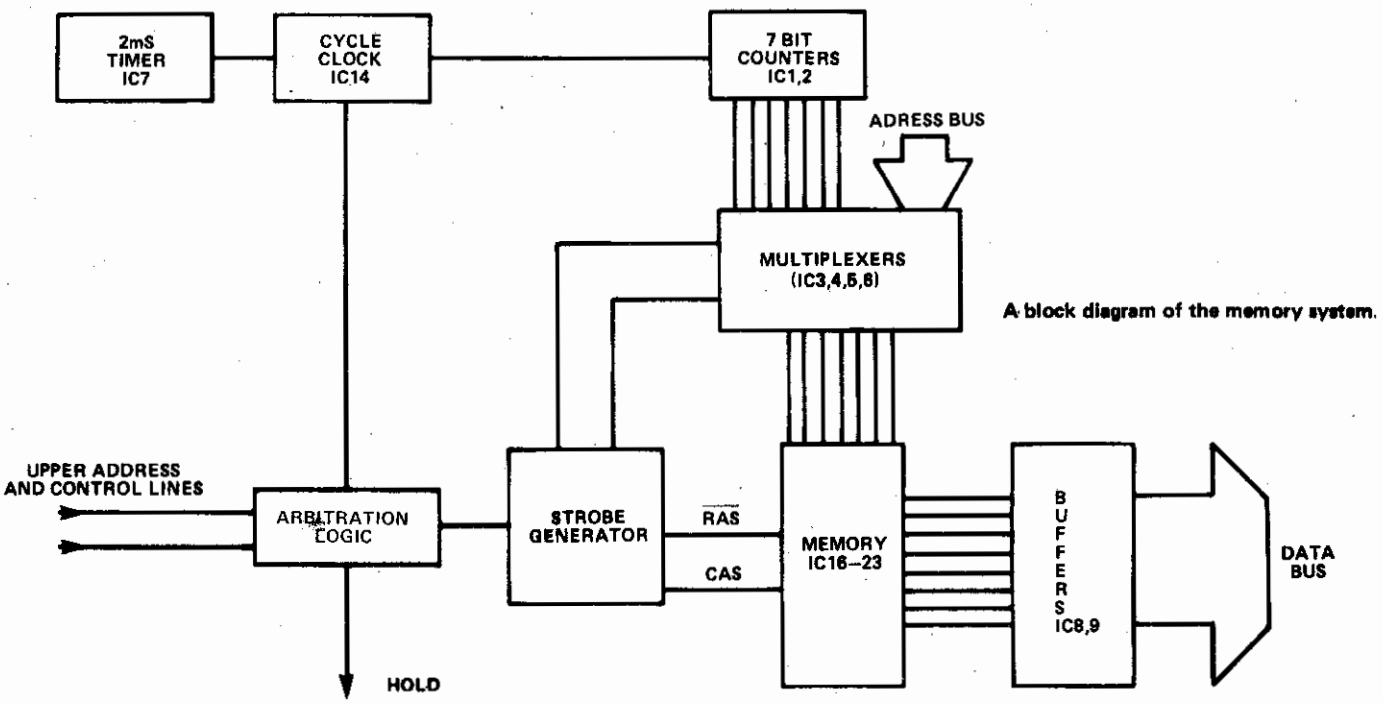
Refreshing

The refresh sequence can be carried out in one of three modes. The first is the burst mode in which normal read or write operation is prevented while all of the 128 combinations of the row address are accessed. The second method is to periodically steal a single cycle from the microprocessor's normal operation to refresh a single row. The third method does not affect normal operation of the microprocessor as the refreshing takes place when the memory is not being used, and is said to be transparent.

Once a refresh, read or write cycle has been started it must not be terminated prematurely. That is another cycle cannot start until the current one has finished otherwise a whole row of data will be lost. This means that either the refresh cycles must be synchronised with the microprocessor clock or logic must be provided to decide whether sufficient time has elapsed since the previous cycle.

Construction

The layout of dynamic memory boards can be critical as nearly all the power is consumed when the CAS and RAS



A block diagram of the memory system.

inputs change state. Efficient decoupling is a must to prevent the transients produced from causing some interesting and unexpected errors. Each chip should be decoupled by at least one ceramic capacitor and the power supply lines especially ground should be as thick as possible. Other signal lines should be kept short. If these precautions are taken veroboard can be used to produce prototype boards but a double sided printed circuit board is highly recommended, and a prototype PCB is shown in Fig.4.

Memory Operation

Outside the burst refresh period the output of the most significant bit of counter IC2 remains high and inhibits the oscillator formed by IC 14 c,d by forcing the output of IC 14c high. When a valid read or write signal occurs the output of IC 12c also goes high. This pulse appears in its inverted form at the output of 14a which in turn enables either the input buffer IC8 or the output buffer IC9 and, after the delay imposed by the RC network and IC 11e, produces a negative going pulse (RAS). This latches the row address supplied by the multiplexers IC3-6. After a short delay produced by IC 13b and IC 10b the multiplexer is switched to the upper seven address bits (column address). The column address is latched into the RAM by the slightly later pulse delayed by IC 13c and IC 10a. The relative timing of these pulses is shown in the figure. At the end of the access period the data is written to or read from the data bus via the buffers IC 8/9. Every 2 mS this process is interrupted by the 10 uS pulse produced by the astable multivibrator formed around IC7. This resets the counters ICI and 2 unless a read or write cycle is in progress in which case the counters are reset only when the cycle is completed. As a result the most significant bit output of IC2 goes low which in turn inhibits the production of the CAS pulses (IC 10a/b), starts the oscillator (IC14 c/d) and produces a hold signal to halt the microprocessor only if it attempts to access the memory during the refresh period (IC 12b, 11f). It also switches the multiplexer from the address bus to the output of the counters ICI/2. The oscillator output provides the clock for the counters and is also delayed by IC 11b, 13a, 14b, 11c to provide the RAS pulse for refreshing the memory. Thus each

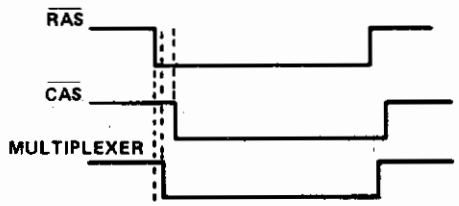


Fig 3. Typical waveforms of the row and column address strobes.

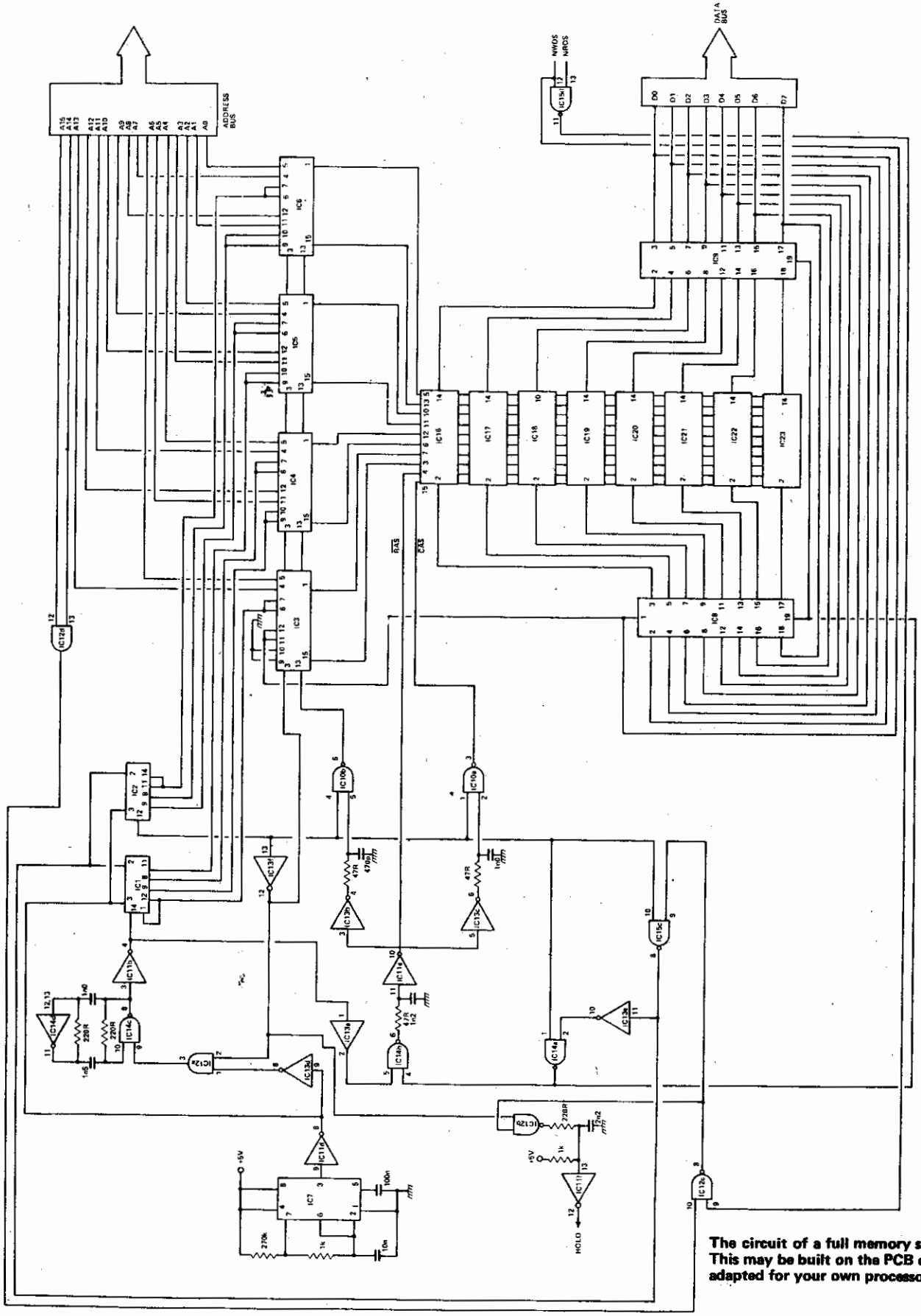
of the 128 row addresses are refreshed by the RAS only method (CAS is inhibited) before the most significant bit of goes high. The circuit then reverts to normal read or write operation.

If the microprocessor attempts to access the memory during refresh it is halted and the read or write cycle is resumed as soon as the burst refresh finishes. The Hold signal remains low until this cycle is complete.

The other gates in the system arbitrate in the case of a request for read or write arriving at the same time as the timer requests a refresh.

Prototyping Board For Dynamic Memories

Ideally a double sided printed circuit board should be used for the construction of reliable memories. One way to overcome this problem is to use the board shown in Fig. 4. This has two thirds of its area devoted to housing 32 memory chips that is, the board could contain 64K bytes of memory if the 16384 bit chips are used or 16K bytes if the cheaper 4096 bit ones are preferred. The remaining portion of the board is laid out to accept a wide range of 0.3" and 0.6"



The circuit of a full memory system. This may be built on the PCB or adapted for your own processor.

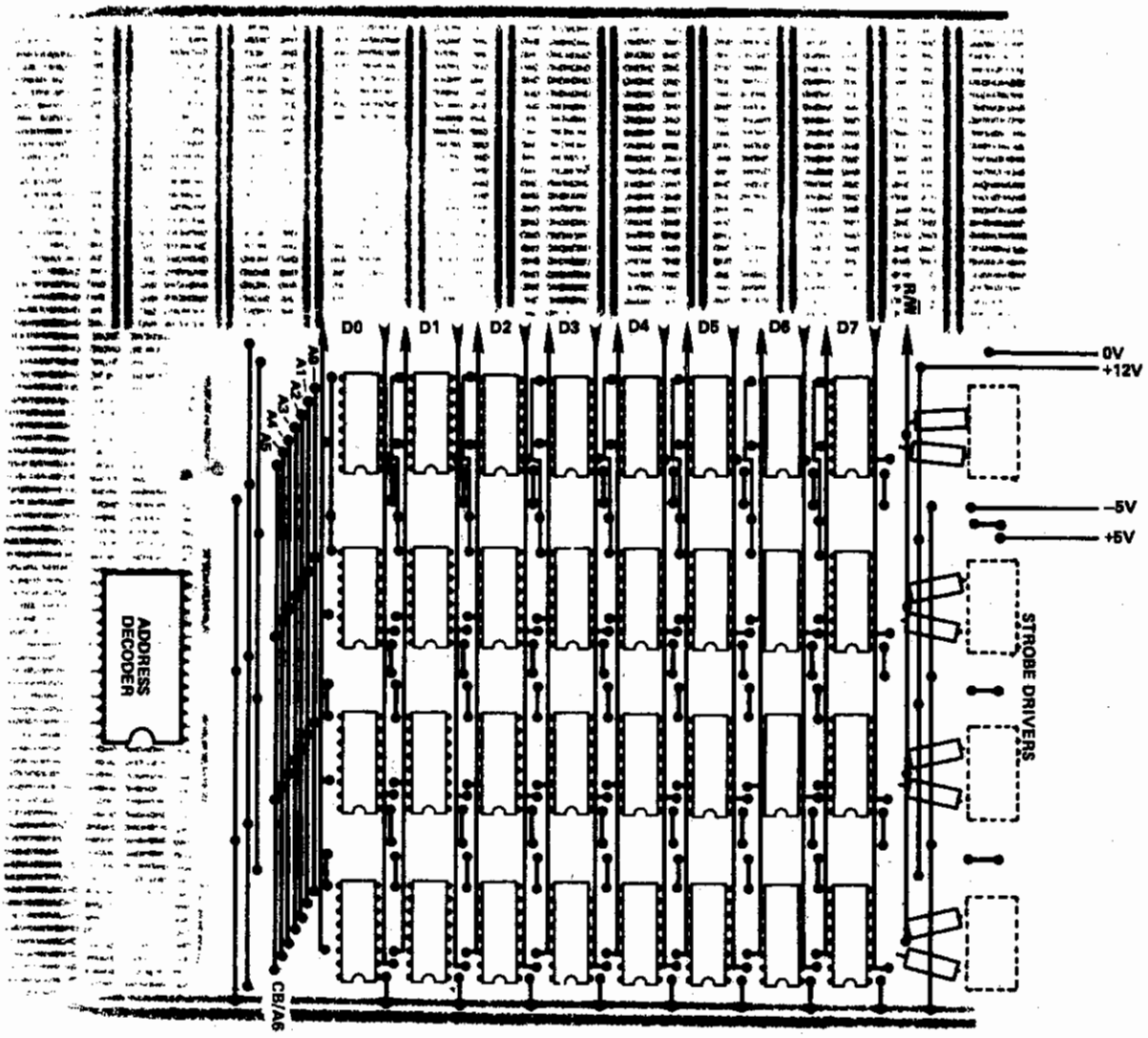


Fig 4. The overlay for the prototyping board.

Please note, Spectrum Electronics will not be supplying the breadboard pcb. For a list of other suppliers, see table of contents.

PARTS LIST

		+5 V	0 V
IC 1,2	7493	pin 5	pin 10
IC 3,4,5,6	9309	pin 16	pin 7
IC 7	555	pin 8	pin 1
IC 8,9	81LS95	pin 20	pin 10
IC 10	74132	pin 14	pin 7
IC 11	7414	pin 14	pin 7
IC 12	7408	pin 14	pin 7
IC 13	7404	pin 14	pin 7
IC 14,15	7400	pin 14	pin 7
IC 16 – 23	F16K	pin 9	pin 16
		(-5 V pin 1, +12 V pin 8)	

devices. As the two memories differ only in the function of pin 13 it is possible to build a 16K board initially which can then be upgraded to 64K as the price of the larger device falls. Obviously address decoding would have to be altered to take account of the different memory size but apart from this pin 13 can be tied to the column address strobe for chip selection (4K chips) but must obviously be used for the most significant address bit in the 16K devices.

Layout is not critical for most of the ancilliary circuitry except for the drivers for address and strobe lines. These drivers should be located at the ends of the arrays as shown in Fig. 5. If the multiplexer/refresh counter (3242) is used this is capable of driving the high capacitance load provided by thirty two devices, otherwise each row of eight should have its own TTL driver. In view of the ease with which it is possible to interchange the 4K and 16K devices it is recommended that the 16K multiplexer/refresh counter (Intel 3242) is used rather than the 4K version (3232) especially as the difference in cost is minimal. In high performance applications where the required cycle time is very short 22

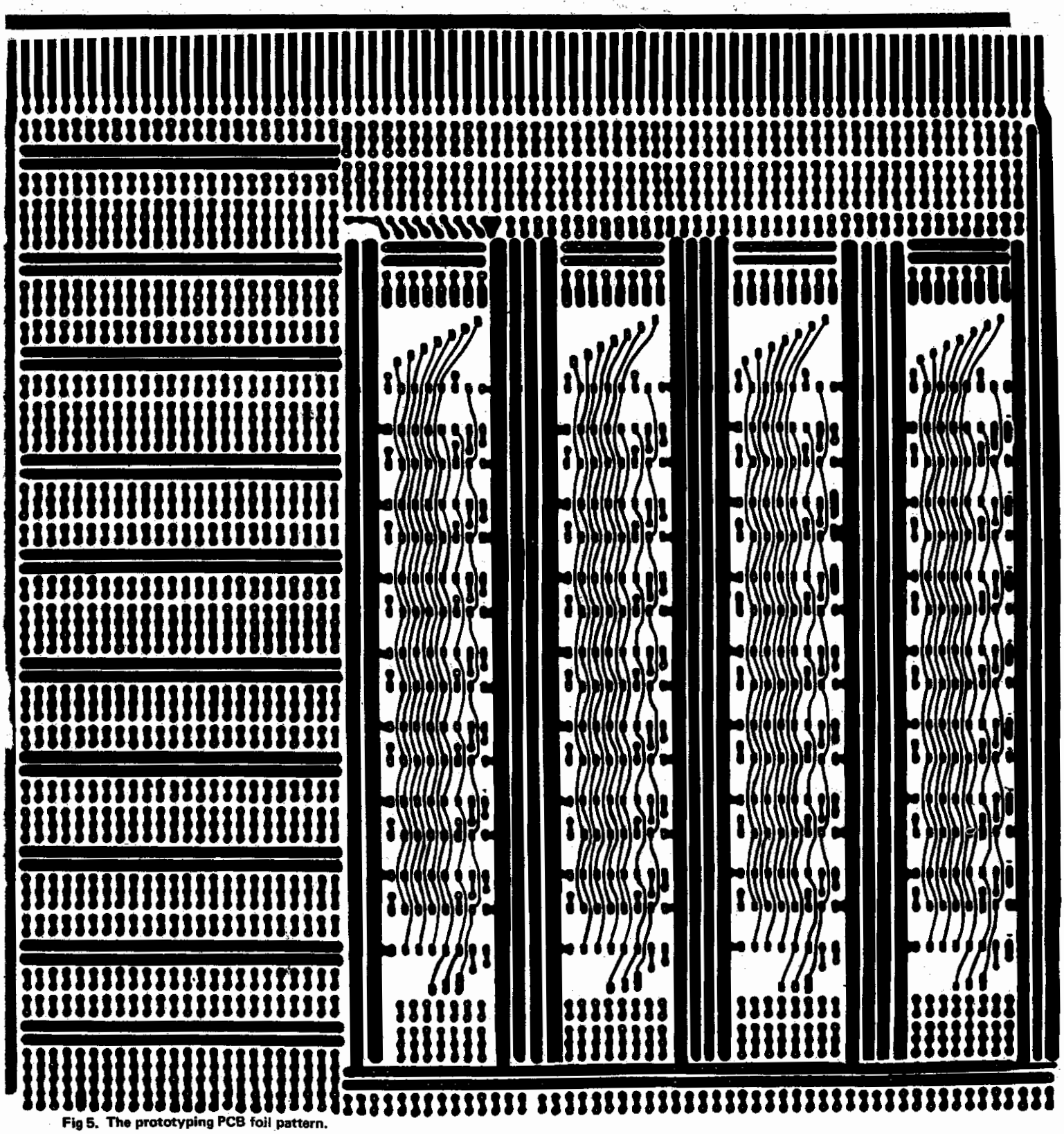


Fig 5. The prototyping PCB foil pattern.

ohm resistors should be put in series with the output of the strobe drivers to reduce transients in these lines (as shown in Fig. 5.).

Care should be taken with decoupling and with the layout of the power supply lines. It is easy to add 0.1 uF ceramic capacitors to decouple the +12 V and −5 V to ground every other device, as close as possible to the pins of the devices. The +5 V supply should be decoupled every eight devices and electrolytic capacitors (4.7 uF) should be used on all three power lines at similar intervals. In addition +12, −5 and O V lines should be strapped by connections not only at each end of the array but at least twice inbetween using 0.6mm wire although 0.25mm wire is adequate for the rest of the wiring.●