Measuring the access time of bipolar read-only memories

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The access time of a semiconductor memory, particularly that of a bipolar read-only memory, can be difficult and time-consuming to measure. But here's a tester that makes this measurement quickly and does not require the data pattern stored in the ROM to be known. There is one condition, however. The ROM must be tested first for its dc parameters.

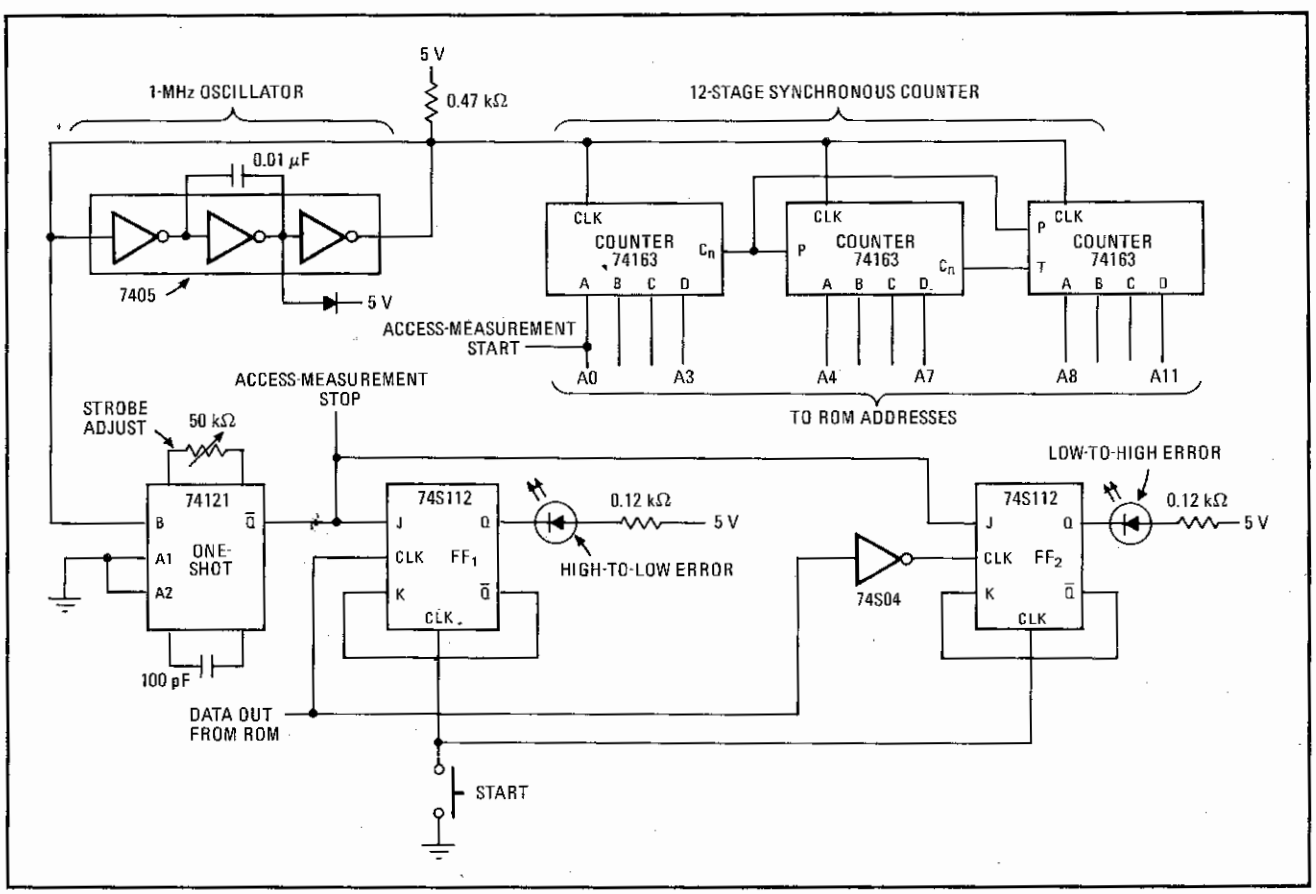
Memory access time is considered to be the maximum address-to-output delay from any address to any output. For bipolar ROMs, access time typically ranges from 30 to 150 nanoseconds, and storage capacities can be as large as 8,192 bits. Conventional testing techniques require a single-shot time-interval measurement for each bit, since each address and output of the ROM generally has a different delay time. The maximum delay measured in this way is recorded as the access time.

Single-shot time-interval measurements, however, have two major drawbacks. Each reading requires about a millisecond, which can add up if the memory is a large one. And the Schmitt-trigger discriminators, which are used to establish the start and stop times, rely on a specific transition direction (either high to low or low to high) through a voltage threshold to implement the start or stop.

This last condition is a problem because the transition direction cannot be predicted for a ROM, unless the data pattern in the ROM is stored in a random-access memory. The problem then becomes one of finding a RAM that is as large and as fast as the ROM being tested to tell the measurement system what to expect. Even if such a RAM can be found, spikes can appear prior to the access time and can trigger the discriminators.

Another measurement technique is to compare the ROM with a RAM that is loaded with ROM data. But again, there is the problem of finding a RAM as fast as the ROM to be tested.

The tester in the figure uses a totally different ap-



Time-saving tester. This circuit checks out the access time of a bipolar read-only memory by regarding any transition occurring at the memory output after the allowable access time as an error. The counter string changes all of the ROM's addresses at the same time. The one-shot acts as a strobe whose timing cycle is set to the allowable access time. A pair of Schottky-TTL flip-flops monitors each ROM output line. If a high-to-low transition error occurs, FF_1 lights its LED; if a low-to-high transition error occurs, FF_2 lights its LED.

proach. It looks for transitions after the expected access time, and defines any transition from this access time until the next address change as an error. This method takes advantage of the fact that the memory reaches a steady-state value before the access time, and the data outputs should not change again until the address is changed. Although the data pattern stored in the ROM does not have to be known, the unit must first be checked for dc parameters, since a package without a chip inside will pass the test.

In the test circuit, 4-bit totally synchronous counters are used to count through all the addresses of the ROM, guaranteeing that all the addresses change at the same time. These address transitions define the start of the access measurement. The counters are driven by a 1-megahertz oscillator, which is constructed with logic inverters. Two Schottky-TTL J-K flip-flops are employed to look for transitions after the access time—FF_1 looks for high-to-low transitions, while FF_2 looks for low-to-high transitions.

The one-shot stops the flip-flops from watching for transitions prior to the access time by holding each one's J input low until the access time is reached. This prevents the flip-flops from changing state. They remain in their initially cleared condition, with their Q outputs low and their $\bar{Q}$ outputs high.

After the one-shot completes it timing cycle, the J input of each flip-flop goes high. If a high-to-low transition now occurs on the memory output line, flip-flop FF_1 changes state—its $\bar{Q}$ output goes low, and its Q output goes high, turning on the error-indicating light-emitting diode. The flip-flop, and therefore the error, remain latched because the unit's $\bar{Q}$ output is tied to its K input. (Depressing the START button will clear the error.)

Flip-flop FF^2 operates identically, but turns on its error-indicating LED for a high-to-low transition on the memory output line. This scheme can be expanded to monitor n memory outputs by adding 2n flip-flops to the test circuit. (A pair of flip-flops is required for each memory output.)

The tester can be calibrated by attaching a pulse generator or delay line of known duration between the access-measurement start and stop inputs to the circuit. This simulates the memory access time, so that the one-shot strobe can be adjusted until a failure just occurs for a set GO/NO-GO limit. The tester can accurately measure an access time to within an accuracy of ±4 ns. □